

GENERAL DESCRIPTION

This document describes the specifications for the IDTF1100 Zero-Distortion™ RF to IF Downconverting Mixer. This device is part of a series of downconverting mixers covering all UTRA bands. See the Part# Matrix for the details of all devices in the series.

The F1100 dual channel device operates with a single 5V supply. It is optimized for operation in a Multi-carrier BaseStation Receiver for RF bands from 698 to 915 MHz with High Side Injection. IF frequencies from 150 to 450 MHz are supported. Nominally, the device offers +41 dBm Output IP3 with 350 mA of I_{CC} .

COMPETITIVE ADVANTAGE

In typical basestation receivers the mixer limits the linearity performance for the entire receive system. The F1100 with Zero-Distortion technology dramatically improves the maximum IM_3 interference that the BTS can withstand at a desired Signal to Noise Ratio (SNR.)

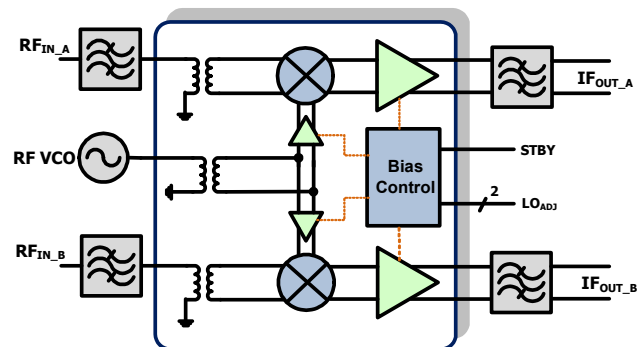
- ✓ $IP3_O$: \uparrow 7 dB
- ✓ Allows for higher RF gain improving **Sensitivity**



FEATURES

- Dual Path for Diversity Systems
- Ideal for Multi-Carrier Systems
- MIMO friendly: -6 dBm min LO drive
- 9 dB Gain
- Ultra linear: +41 dBm $IP3_O$ (350 MHz IF)
- Low NF \sim 10 dB
- 200 Ω output impedance
- Ultra high +13 dBm $P1dB_I$
- Pin Compatible w/Existing solutions
- 6x6 36 pin package
- Power Down mode
- Standard Mode: $I_{CC} = 350$ mA

DEVICE BLOCK DIAGRAM

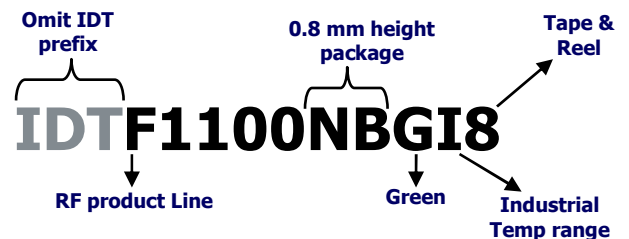


PART# MATRIX

Part#	RF freq range	UTRA bands	IF freq range	Typ. Gain	Injection
F1100	698 - 915	5,6,8,12,13,14,17,19,20	150 - 450	9	High Side
F1102	400 - 1000	5,6,8,12,13,14,17,19,20	50 - 300	9.0	Both
F1150	1700 - 2200	1,2,3,4,9,10,33,34,35,36,37,39	50 - 450	8.5	High Side
F1152	1400 - 2200	1,2,3,4,9,10,21 ¹ ,24 ¹ ,33,34,35,36,37,39	50 - 350	8.5	Low Side
F1162	2300 - 2700	7,38,40,41	50 - 500	8.8	Both

1 - with High side injection

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

VCC to GND	-0.3V to +5.5V
STBY	-0.3V to (VCC_ + 0.3V)
IF_A+, IF_B+, IF_A-, IF_B-, LO1_ADJ, LO2_ADJ	-0.3V to (VCC_ + 0.3V)
LO_IN, LO_IN_ALT, RF_A, RF_B	-0.3V to +0.3V
IF_BiasA, IF_BiasB to GND	-0.3V to +0.3V
RF Input Power (RF_A, RF_B)	+20dBm
Continuous Power Dissipation	2.2W
θ_{JA} (Junction – Ambient)	+35°C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	+2.5°C/W
Operating Temperature Range (Case Temperature)	$T_C = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s) .	+260°C

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

IDTF1100 SPECIFICATION (698 – 915 MHz MIXER W/HIGH SIDE INJECTION)

Specifications apply at $V_{CC} = +5.0V$, $F_{RF} = 850 \text{ MHz}$, $F_{IF} = 350\text{MHz}$, Hi-Side Inj., $P_{LO} = 0 \text{ dBm}$, $T_{CASE} = +25^{\circ}\text{C}$, $STBY = GND$, Trace and Transformer Losses de-embedded unless otherwise noted.

Parameter	Comment	Symbol	min	typ	max	units
Logic Input High	For Standby Pin	V_{IH}	2			V
Logic Input Low	For Standby Pin	V_{IL}			0.8	V
Logic Current	For Standby Pin	I_{IH}, I_{IL}	-5		+5	μA
Supply Voltage(s)	All V_{CC} pins	V_{CC}		4.75 to 5.25		V
Operating Temperature	Case Temperature	T_{CASE}		-40 to +100		degC
Supply Current	Total V_{CC} Both Channels	I_{STD}		350	395	mA
Supply Current	Standby Mode <ul style="list-style-type: none"> ▪ $STBY = V_{IH}$ ▪ Total Both Channels 	I_{STBY}		28	35	mA
RF Freq Range	Operating Range	F_{RF}		698 to 915		MHz
IF Freq Range	Operating Range	F_{IF}		150 to 450		MHz
LO Freq Range	Operating Range	F_{LO}		848 to 1365		MHz
LO Power	Operating Range	P_{LO}		-6 to +6		dBm
RF Input Impedance	Single Ended <i>Return Loss > 15 dB</i>	Z_{RF}		50		Ω
IF Output Impedance	Differential <i>Return Loss > 15 dB</i>	Z_{IF}		200		Ω
LO port Impedance	Single Ended <i>Return Loss > 15 dB</i>	Z_{LO}		50		Ω
Gain (low freq)	Conversion Gain <ul style="list-style-type: none"> • $F_{RF} = 698 \text{ MHz}$ • $F_{IF} = 450 \text{ MHz}$ • EVB trace and transformer loss = 0.9 dB 	G_1	7.8	8.9	10	dB
Gain (high freq)	Conversion Gain <ul style="list-style-type: none"> • $F_{RF} = 915 \text{ MHz}$ • $F_{IF} = 350 \text{ MHz}$ • EVB trace and transformer loss = 0.8 dB 	G_2	8.0	9.0	10	dB

IDTF1100 SPECIFICATION (CONTINUED)

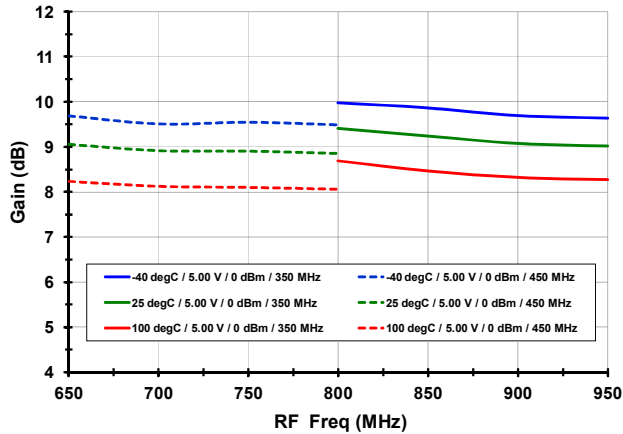
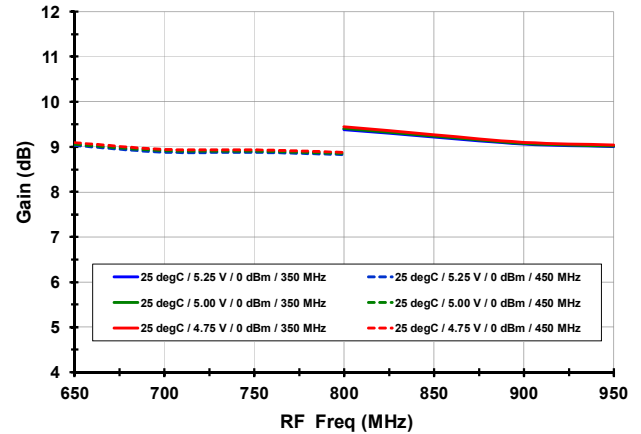
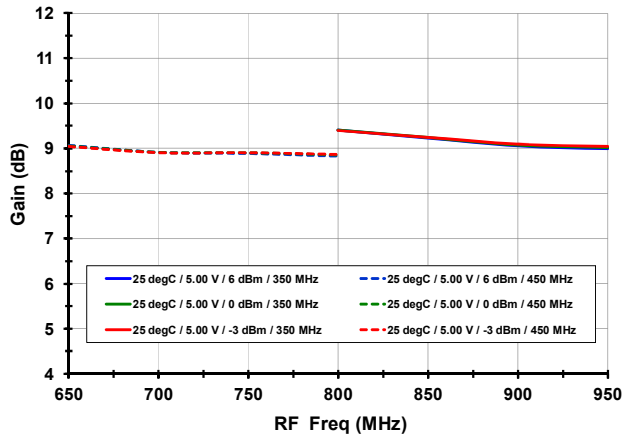
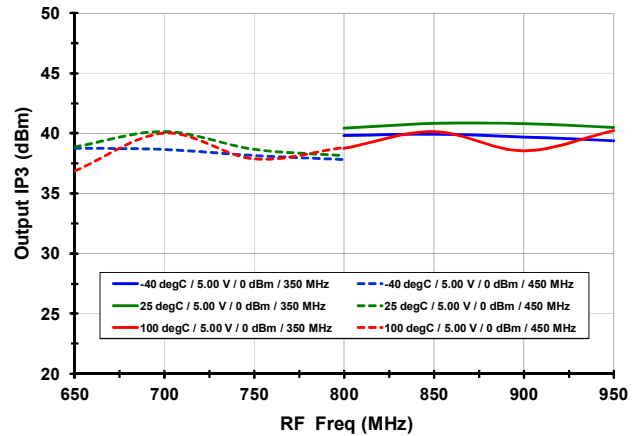
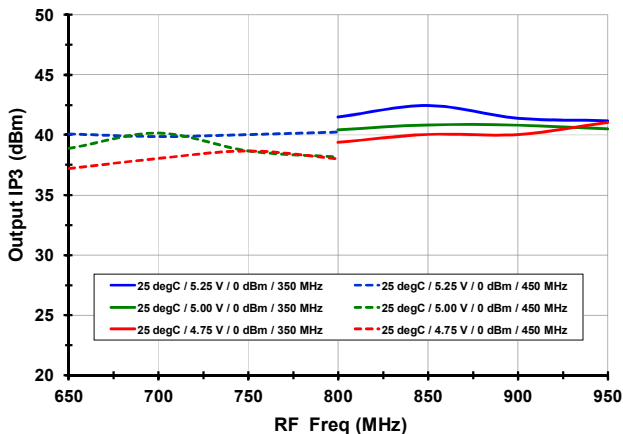
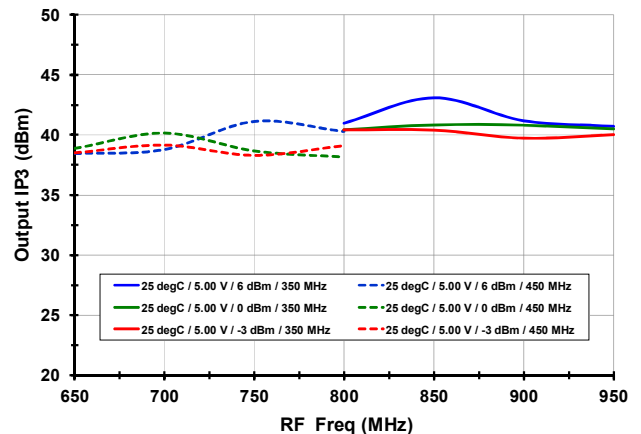
Parameter	Comment	Symbol	min	typ	max	units
Noise Figure	<ul style="list-style-type: none"> $F_{RF} = 850$ MHz $F_{IF} = 350$ MHz 	NF_{STD}		10		dB
NF w/Blocker	<ul style="list-style-type: none"> 50 MHz offset blocker $P_{IN} = +10$ dBm $F_{IF} = 350$ MHz $F_{RF} = 900$ MHz 	NF_{BLK}		20.3		dB
Output IP3 – Narrowband	<ul style="list-style-type: none"> $P_{IN} = -10$ dBm per tone 800 KHz Tone Separation $F_{IF} = 350$ MHz $F_{RF} = 850$ MHz 	$IP3_{O1}$	38	41		dBm
Output IP3 – Wideband	<ul style="list-style-type: none"> $P_{IN} = -10$ dBm per tone 15 MHz Tone Separation $F_{IF} = 350$ MHz 	$IP3_{O2}$		41		dBm
2RF X 2LO rejection	<ul style="list-style-type: none"> $P_{RF} = -10$ dBm $F_{IF} = 350$ MHz $F_{LO} = 1200$ MHz $F_{SPUR} = F_{LO} - \frac{1}{2} F_{IF}$ 	2x2		-80		dBc
3RF X 3LO rejection	<ul style="list-style-type: none"> $P_{RF} = -10$ dBm $F_{IF} = 350$ MHz $F_{LO} = 1200$ MHz $F_{SPUR} = F_{LO} - \frac{1}{3} F_{IF}$ 	3x3		-82		dBc
1 dB Compression	<ul style="list-style-type: none"> Input referred $F_{IF} = 350$ MHz 	$P1dB_I$	12.4	13.1		dBm
Channel Isolation	IF_B Pout vs. IF_A w/ RF_A input	ISO_C		60		dB
LO to IF leakage		ISO_{LI}		-19	-13	dBm
RF to IF leakage	$P_{in} = -10$ dBm	ISO_{RI}		-39	-33	dBm
LO to RF leakage		ISO_{LR}		-40		dBm

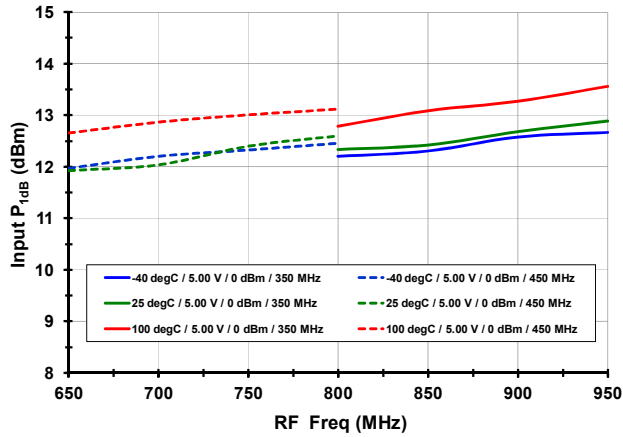
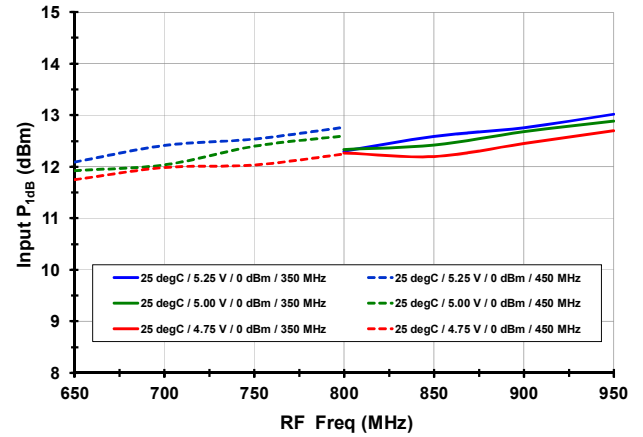
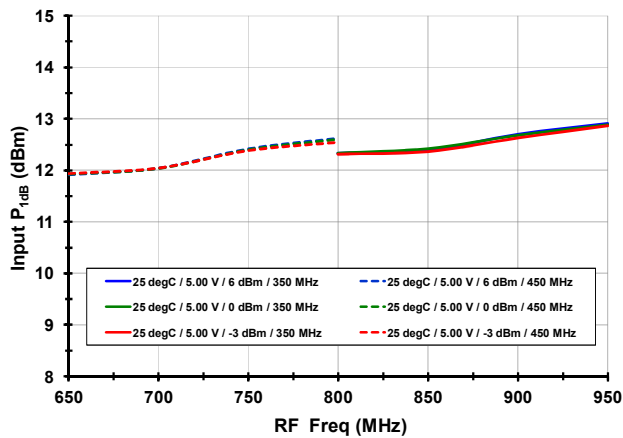
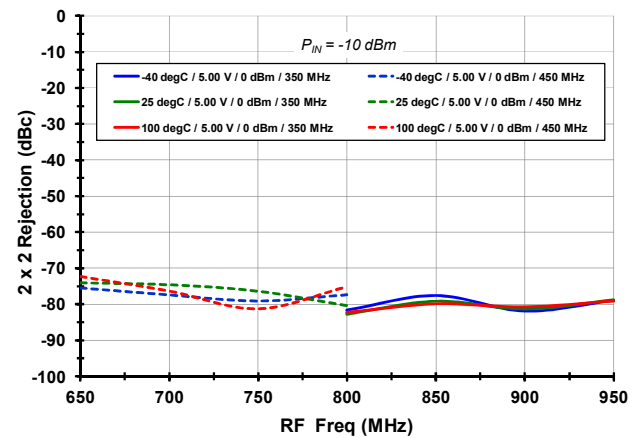
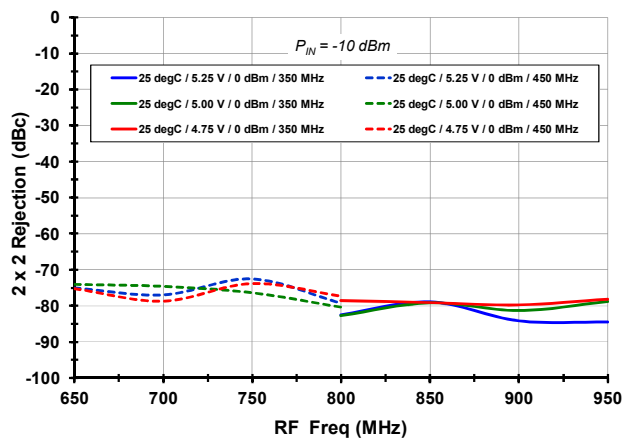
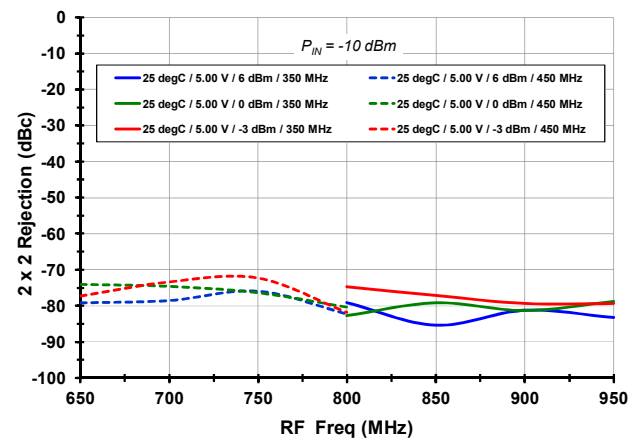
1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test

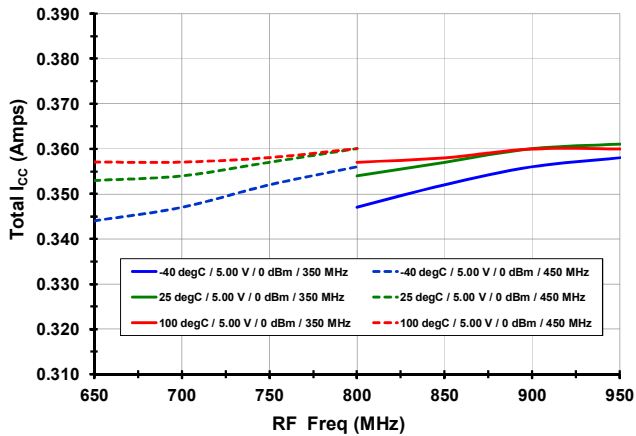
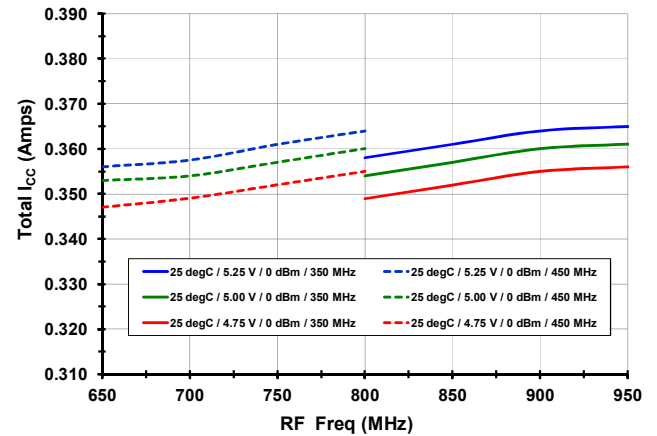
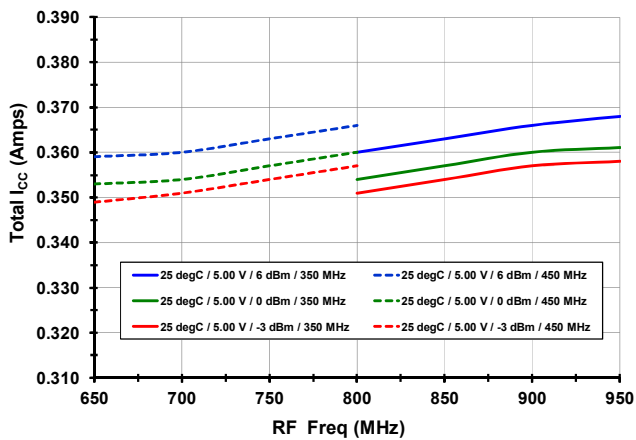
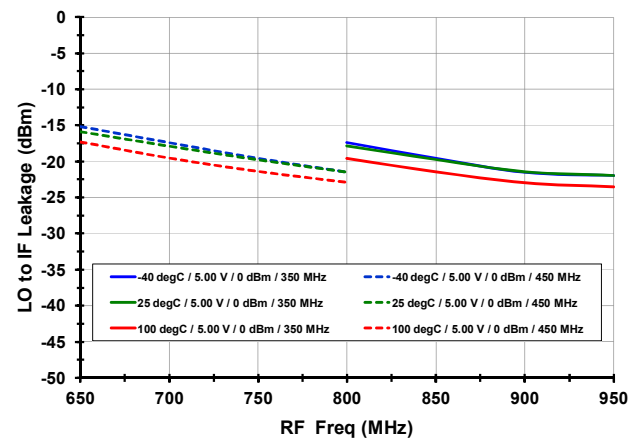
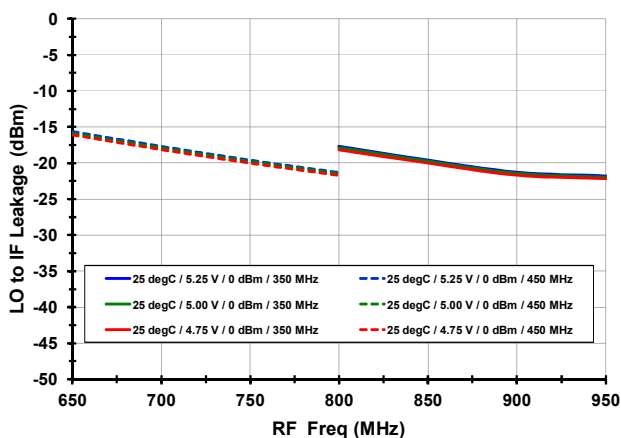
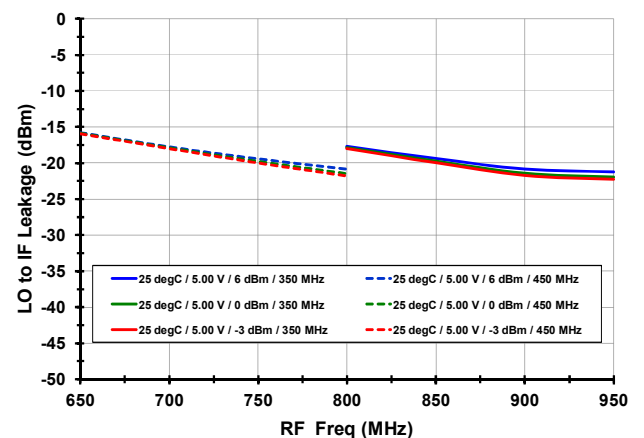
2 – All other Items in min/max columns are Guaranteed by Design Centering

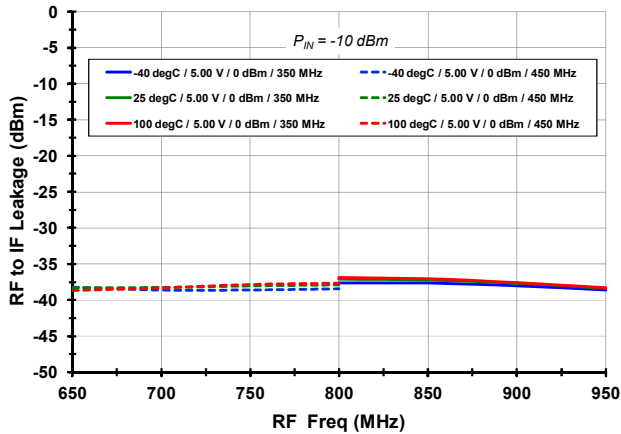
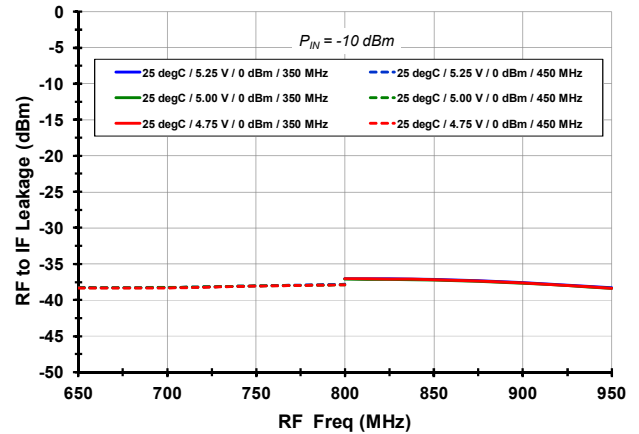
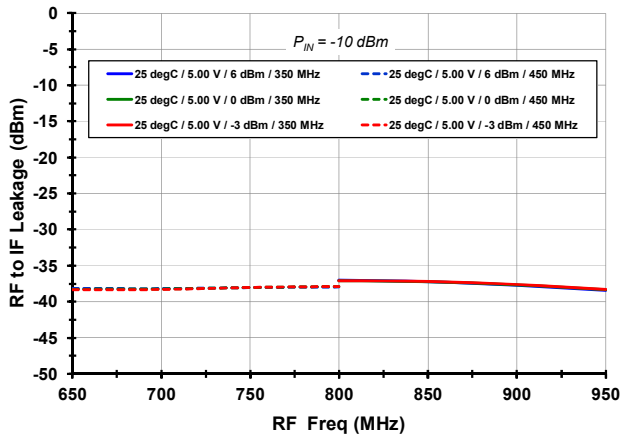
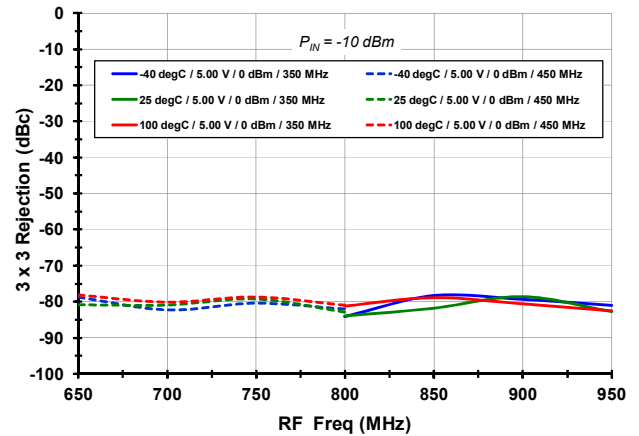
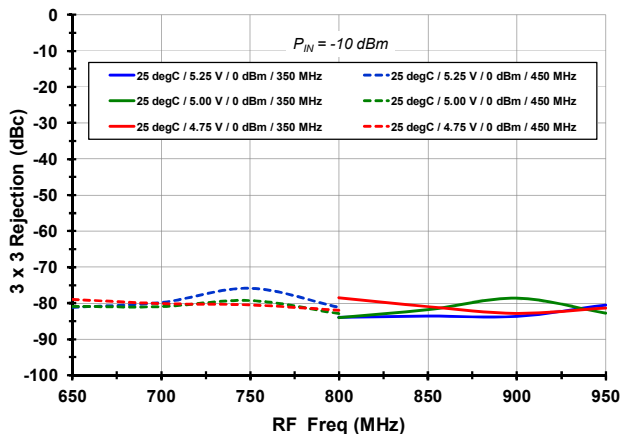
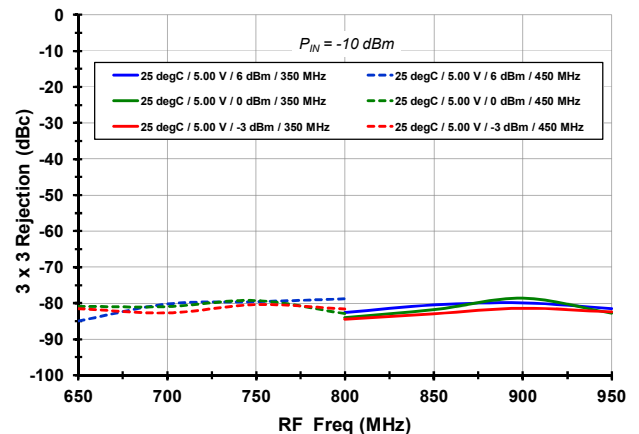
TYPICAL OPERATING CONDITIONS
Unless Otherwise Noted:

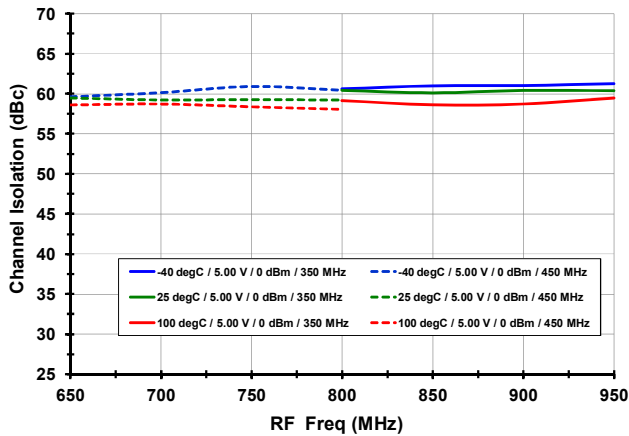
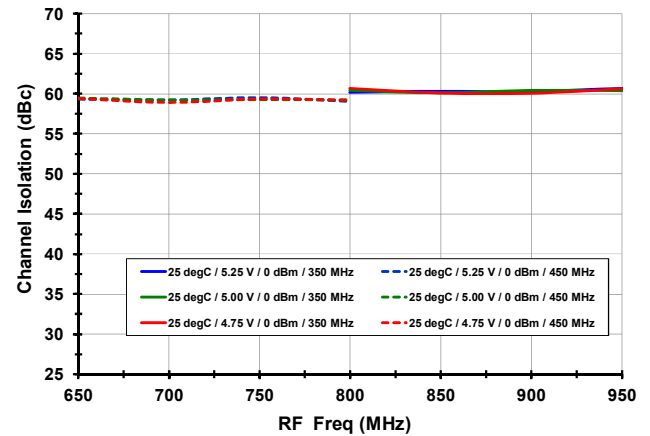
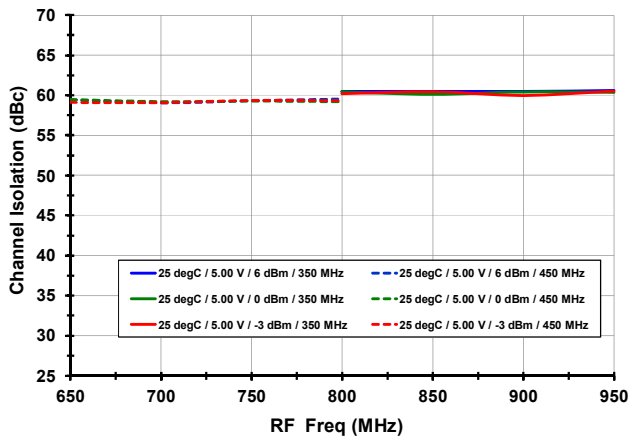
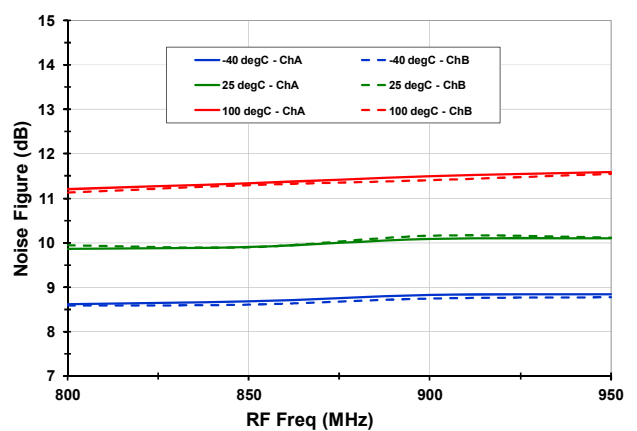
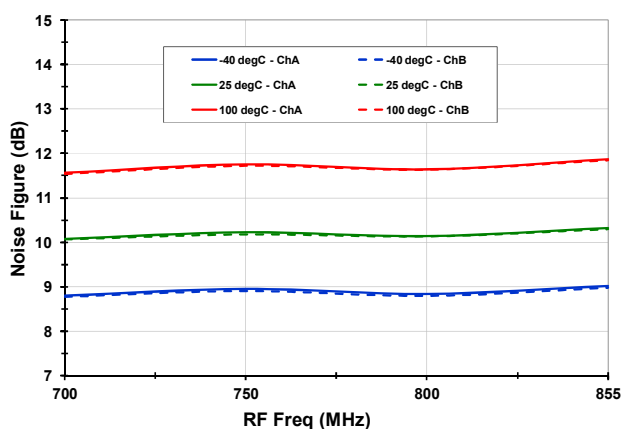
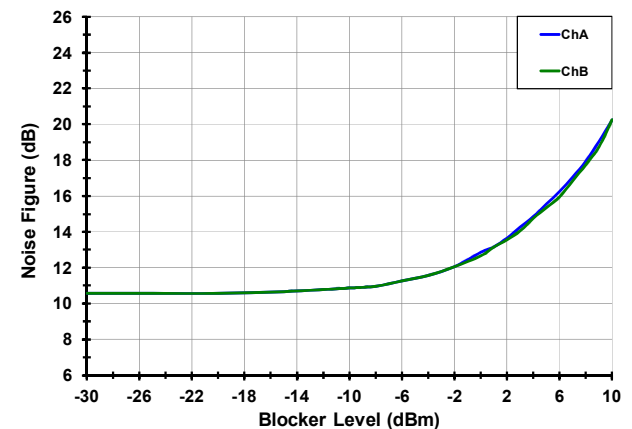
- Dotted Lines: 450 MHz IF / Solid Lines: 350 MHz IF
- High Side Injection
- 800 KHz Channel Spacing
- Average of ChA, ChB
- $P_{in} = -10$ dBm
- Trace & Transformer Losses de-embedded

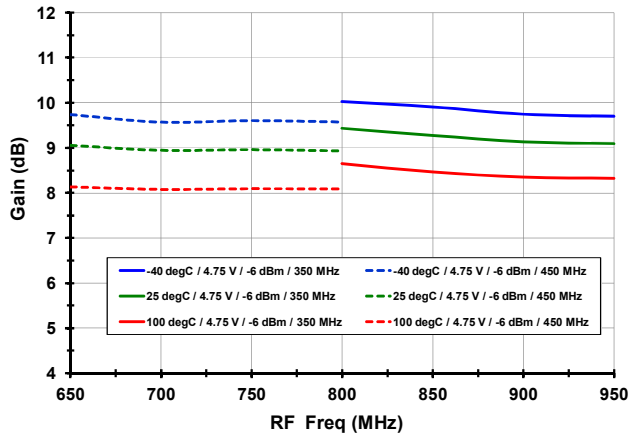
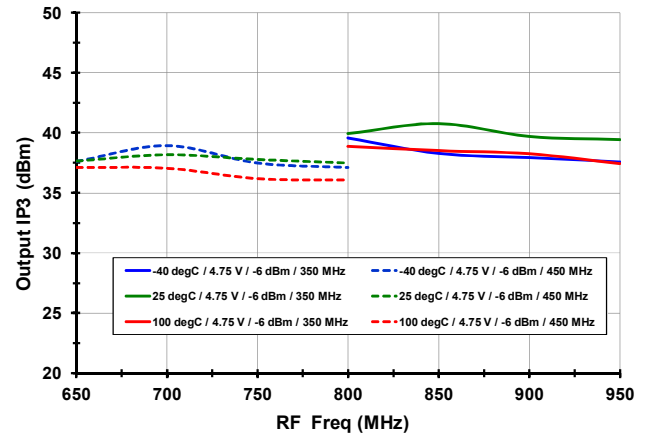
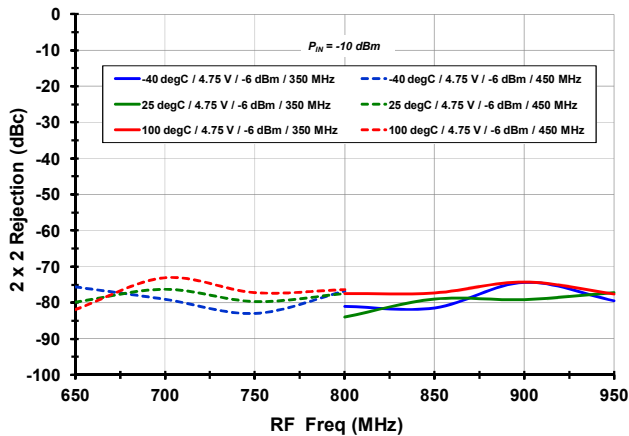
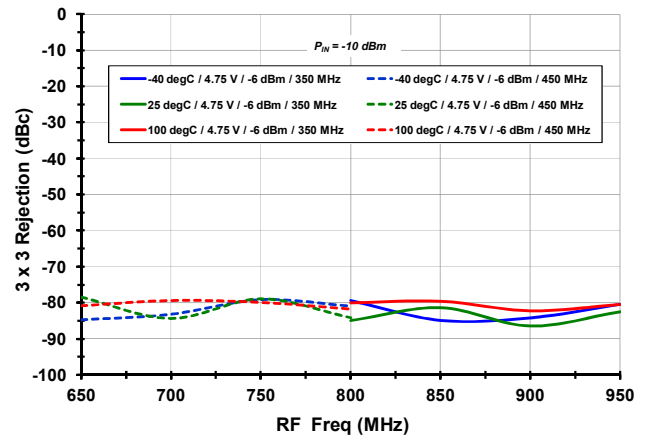
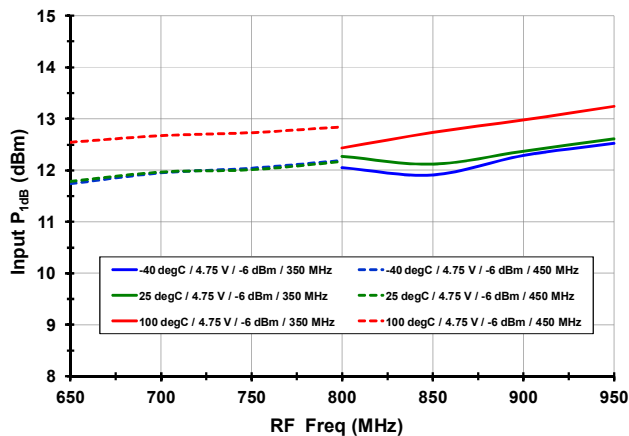
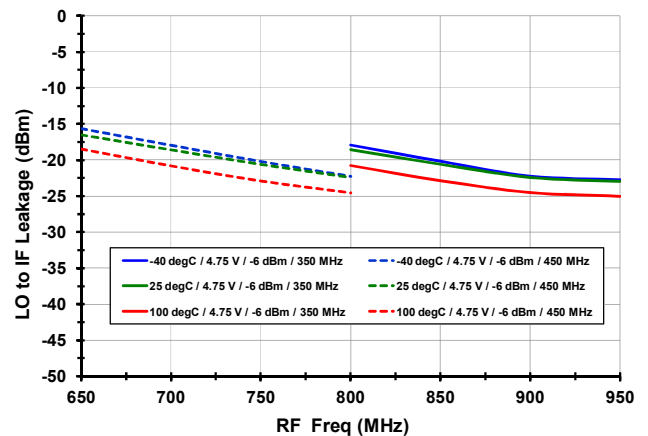
TYPICAL OPERATING CONDITIONS (-1-)
Gain vs. T_{CASE}

Gain vs. V_{CC}

Gain vs. LO Level

Output IP3 vs. T_{CASE}

Output IP3 vs. V_{CC}

Output IP3 vs. LO Level


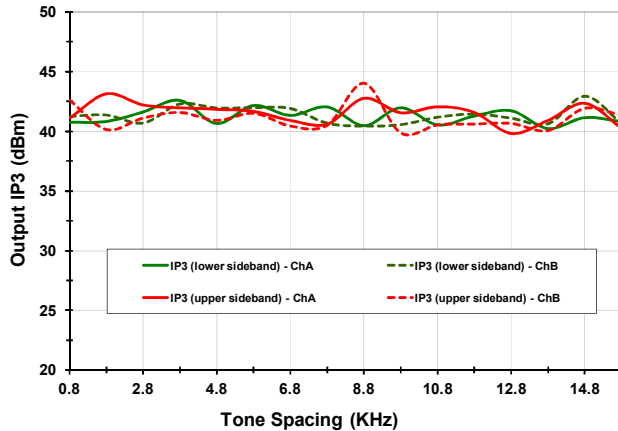
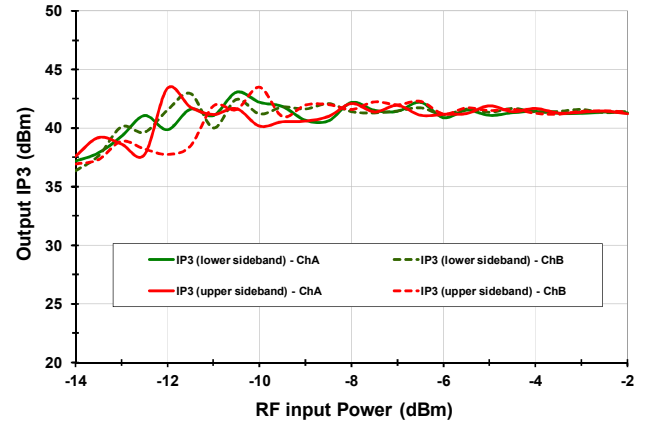
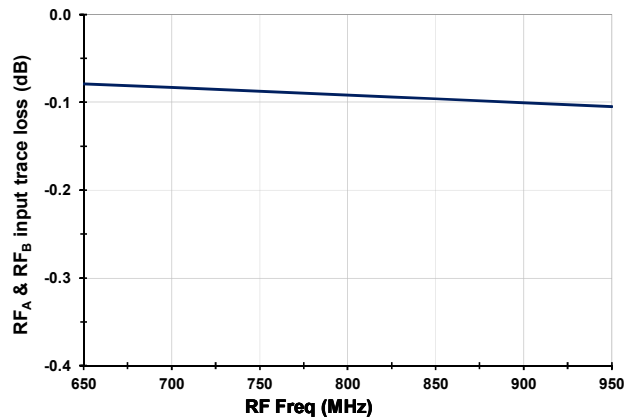
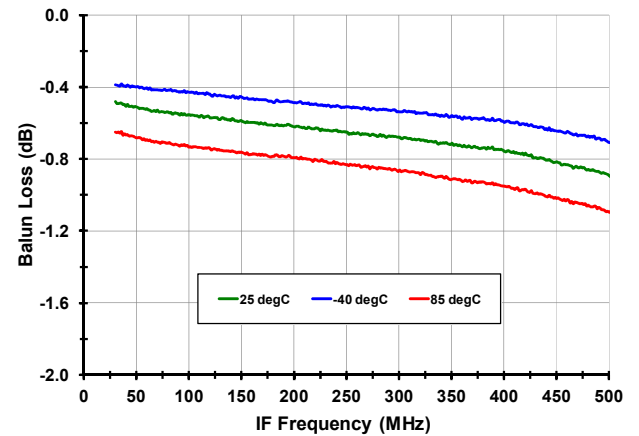
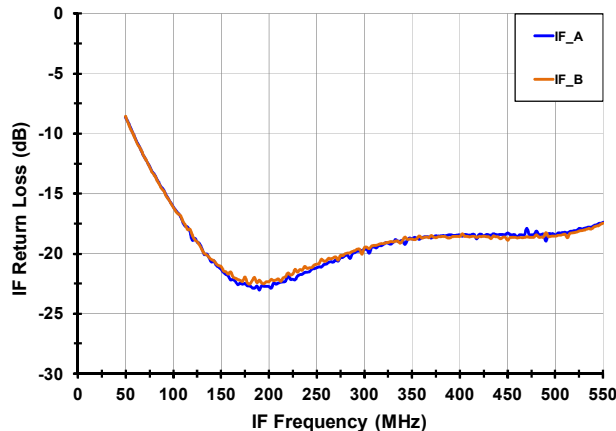
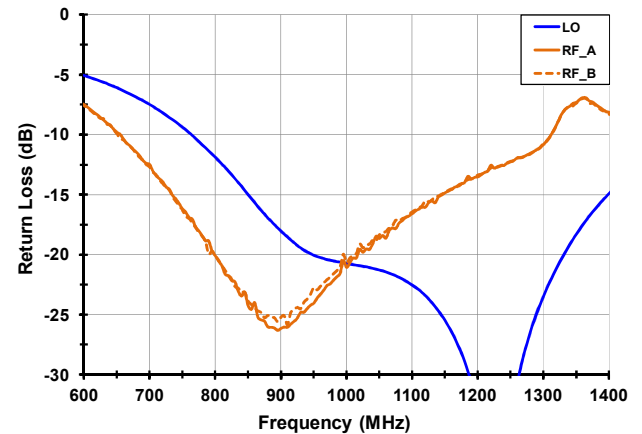
TYPICAL OPERATING CONDITIONS (-2-)
P1dB vs. T_{CASE}

P1dB vs. V_{CC}

P1dB vs. LO Level

2RF x 2LO rejection vs. T_{CASE}

2RF x 2LO Rejection vs. V_{CC}

2RF x 2LO Rejection vs. LO Level


TYPICAL OPERATING CONDITIONS (-3-)
I_{CC} vs. T_{CASE}

I_{CC} vs. V_{CC}

I_{CC} vs. LO Level

LO-IF Leakage vs. T_{CASE}

LO-IF Leakage vs. V_{CC}

LO-IF Leakage vs. LO Level


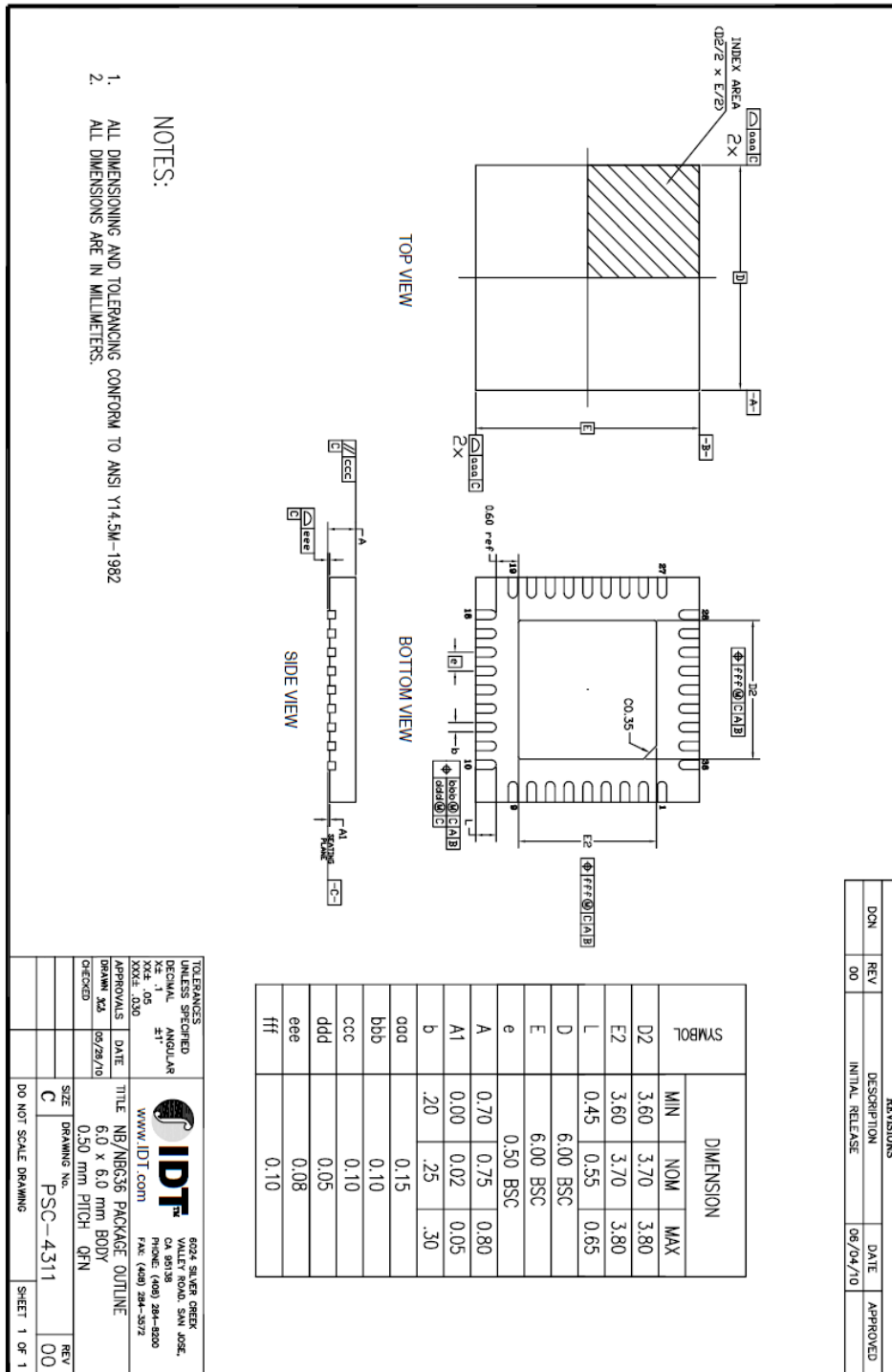
TYPICAL OPERATING CONDITIONS (-4-)
RF-IF Leakage vs. T_{CASE}

RF-IF Leakage vs. V_{CC}

RF-IF Leakage vs. LO Level

3RF X 3LO Rejection vs. T_{CASE}

3RF X 3LO Rejection vs. V_{CC}

3RF X 3LO Rejection vs. LO Level


TYPICAL OPERATING CONDITIONS (-5-)
Channel Isolation vs. T_{CASE}

Channel Isolation vs. V_{CC}

Channel Isolation vs. LO Level

Noise Figure vs. T_{CASE} (350 MHz IF, RF trace de-embedded)

Noise Figure vs. T_{CASE} (450 MHz IF, RF trace de-embedded)

NF vs. Blocker (RF = 900 MHz, IF = 350 MHz, T_A = 25C)


RF to IF Dual Downconverting Mixer
698 - 915 MHz F1100NBGI
TYPICAL OPERATING CONDITIONS [*Extreme Conditions: low Supply, low LO level -6 dBm*] **(-6-)**
Gain

Output IP3

2x2 Rejection

3x3 Rejection

Input P1dB

LO to IF Leakage


TYPICAL OPERATING CONDITIONS [General] (-7-)
IP_{3O} vs. Δf ($T_A = 25C$, Freq = 850 MHz, IF = 350 MHz)

IP_{3O} vs. P_{IN} ($T_A = 25C$, Freq = 850 MHz, IF = 350 MHz)

EVkit Input RF Trace Loss ($T_A = 25C$)

TC4-6T Transformer Loss

EVkit IF Port Match ($T_A = 25C$)

EVkit RF & LO Port Match ($T_A = 25C$)


PACKAGE DRAWING (6X6 QFN)



REVISIONS			
DCN	REV	DESCRIPTION	DATE
00		INITIAL RELEASE	08/04/10

TOLERANCES UNLESS SPECIFIED		6024 SILVER GREEK	
DECIMAL	ANGULAR	WALLET ROAD, SUITE 409E, COSTA MESA, CA 92626	
XXX .050	±1°	WWW.IDT.COM FAX: (408) 284-5972	
APPROVALS	DATE	TITLE	
DRAWN XA	05/28/10	NB/NBGS6 PACKAGE OUTLINE	
CHECKED		6.0 x 6.0 mm BODY 0.50 mm PITCH OPEN	
SIZE	DRAWING NO.	REV	
C	PSC-4311	00	
DO NOT SCALE DRAWING			SHEET 1 OF 1

PINOUTS

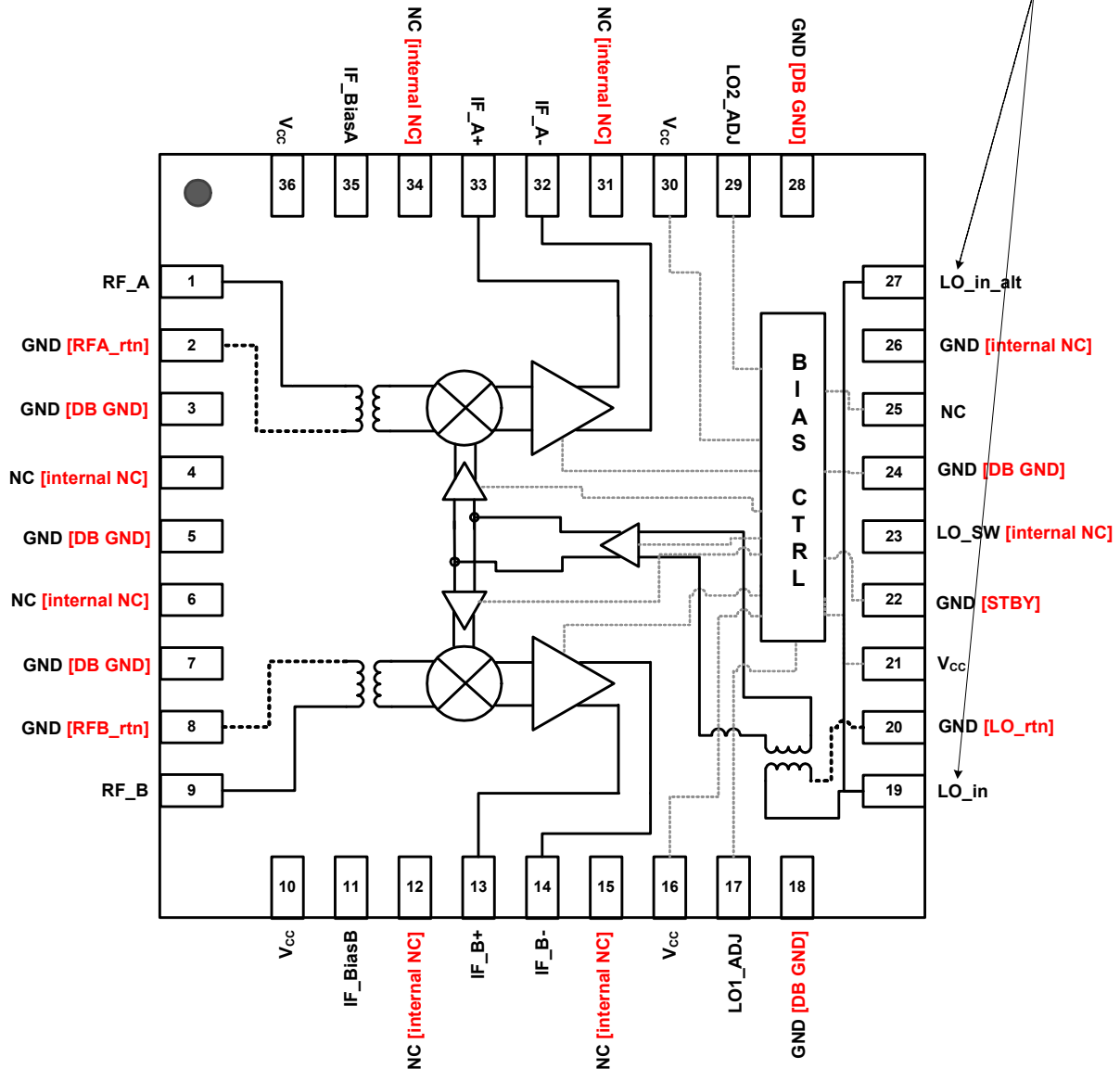
Black Text denotes recommended external connection

Red Text denotes internal Function or Connection

- DB GND = Downbonded to Paddle
- Internal NC = Pin not connected

Please Note!

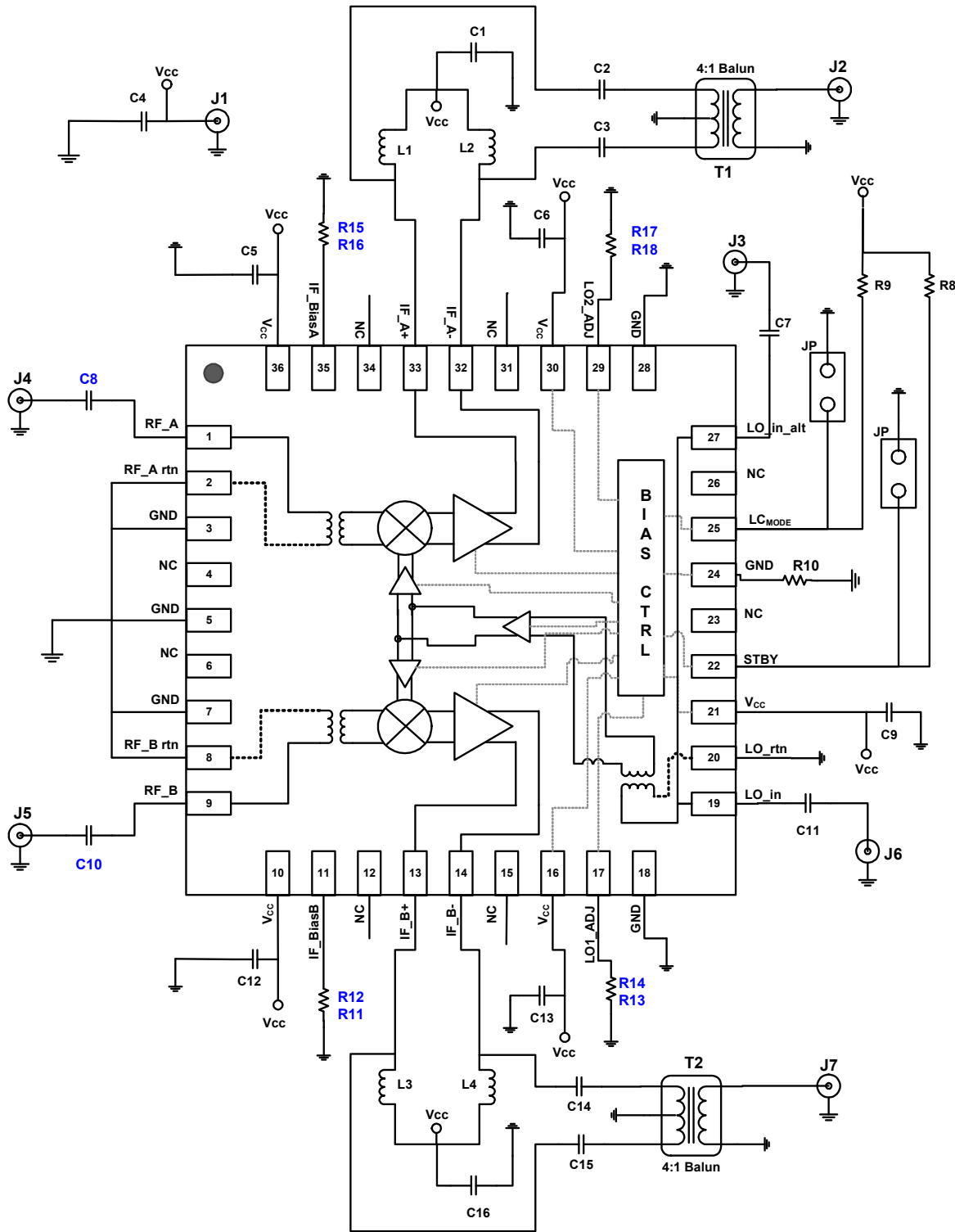
- Only connect to one LO feed
- Choose Either Pin 19 or Pin 27
- Do not connect the unused LO pin to ensure good LO return loss



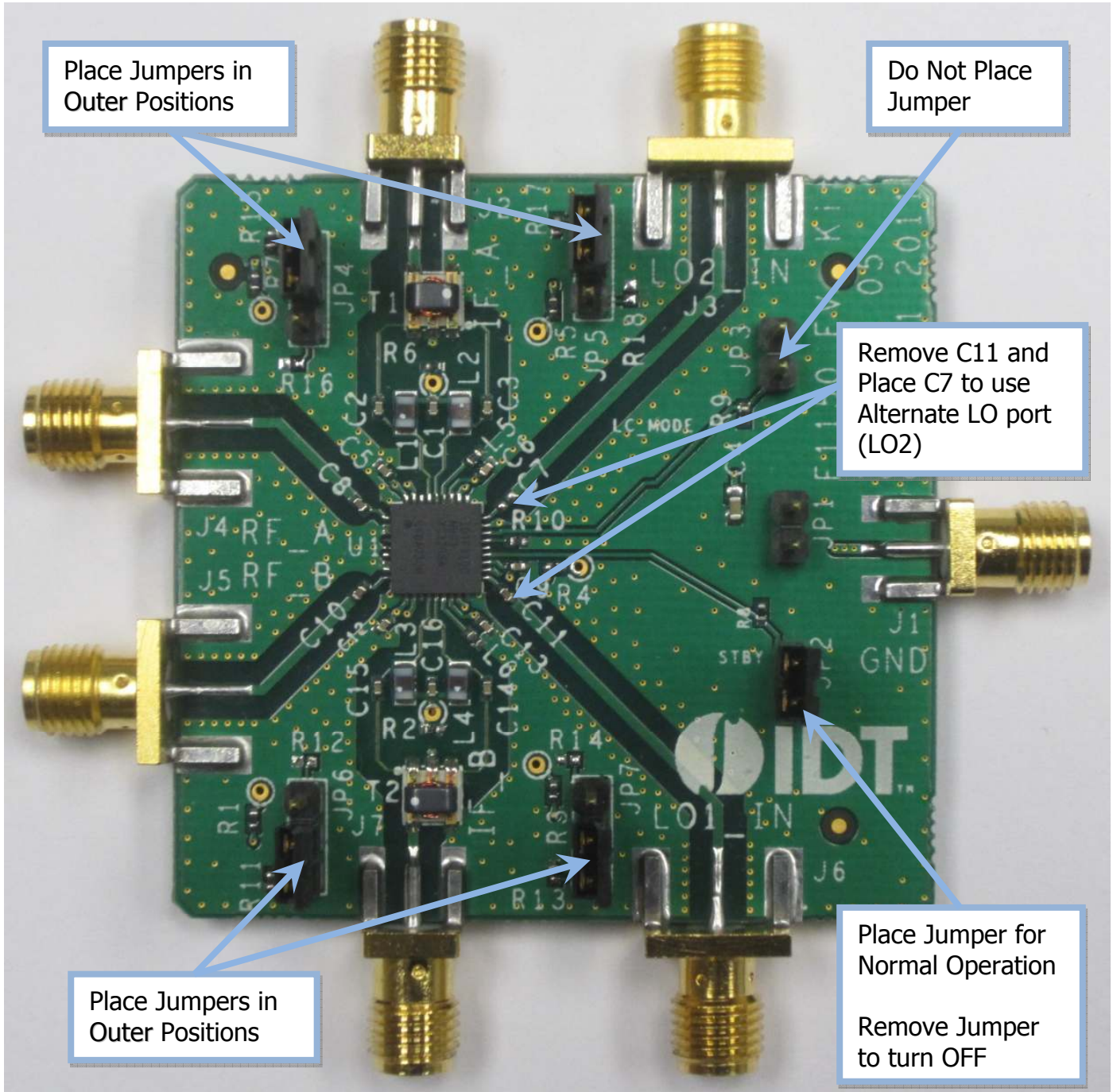
PIN DESCRIPTIONS

Pin	Name	Function
1	RF_A	Main Channel RF Input. Internally matched to 50Ω. DO NOT apply DC to these pins
2, 8, 20	RF_Artn, RF_Brtn, LO_rtn	Transformer Ground Returns. Ground these pins.
3, 5, 7, 18, 24, 28	GND	Ground these pins.
4, 6, 12, 15, 31, 23, 26, 34	N.C.	No Connection. Not internally connected. OK to connect to Vcc. OK to connect to GND
10, 16, 21, 30, 36	VCC	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
9	RF_B	Diversity Channel RF Input. Internally matched to 50Ω
11	IF_BiasB	Connect the specified resistor from this pin to ground to set the bias for the Diversity IF amplifier. This is NOT a current set resistor
13, 14	IFB+, IFB-	Diversity Mixer Differential IF Output. Connect pullup inductors from each of these pins to VCC (see the Typical Application Circuit).
17	LO1_ADJ	Connect the specified resistor for either Standard or LC mode from this pin to ground to set the LO common buffer Icc
19, 27	LO_in LO_in_alt	Local Oscillator Input. Connect the LO to this port through the recommended coupling capacitor. Note that you can only drive one LO port at a time. Remove the series capacitor from the unused port.
25	NC	Make Certain this pin is not connected. It is normally reserved for selecting <i>low current</i> mode which the F1100 does not offer
22	STBY	STBY Mode. Pull this pin high for Standby mode (~28 mA). Pull low or Ground for normal Operation
29	LO2_ADJ	Connect the specified resistor for either Standard or LC mode from this pin to ground to set the LO drive buffers Icc
32, 33	IFA-, IFA+	Main Mixer Differential IF Output. Connect pullup inductors from each of these pins to VCC (see the Typical Application Circuit).
35	IF_BiasA	Connect the specified resistor from this pin to ground to set the bias for the Main IF amplifier. This is NOT a current set resistor
	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance.

EVKIT SCHEMATIC



EVKIT PICTURE/LAYOUT/OPERATION



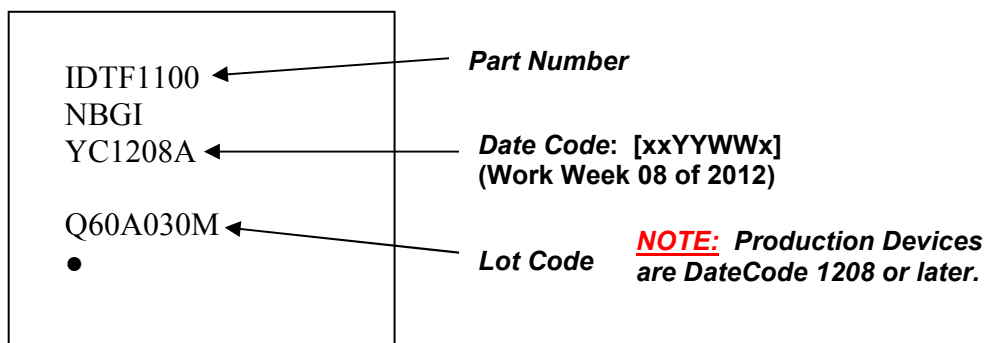
EVKIT BOM

For Normal Operation, Make sure the LC_{MODE} jumper is open and that the dual jumpers are set to the outer position.

F1100 PCB Rev 5 BOM Rev 02

Item #	Value	Size	Desc	Mfr. Part #	Mfr.	Part Reference	Qty
1	10nF	0402	CAP CER 10000PF 16V 10% X7R 0402	GRM155R71C103KA01D	MURATA	C1,5,6,9,12,13,16	7
2	1000pF	0402	CAP CER 1000PF 50V C0G 0402	GRM1555C1H102JA01D	MURATA	C2,3,14,15	4
3	150pF	0402	CAP CER 150PF 50V C0G 0402	GRM1555C1H151JA01D	MURATA	C8,10,11	3
4	150pF	NOTE: C7 and C11 cannot be installed together. C7 for Pin27 LO feed. C11 for Pin19 LO feed				C7	1
5	10uF	0603	CAP CER 10UF 6.3V X5R 0603	GRM188R60J106ME47D	MURATA	C4	1
6	Header 2 Pin	TH 2	CONN HEADER VERT SGL 2POS GOLD	961102-6404-AR	3M	JP1,2,3	3
7	Header 3 Pin	TH 3	CONN HEADER VERT SGL 3POS GOLD	961103-6404-AR	3M	JP4,5,6,7	4
8	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (Small)	142-0711-821	Emerson Johnson	J1,2,7	3
9	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (Big)	142-0701-851	Emerson Johnson	J3,4,5,6	4
10	270nH	0805	0805CS (2012) Ceramic Chip Inductor	0805CS-271XJLB	COILCRAFT	L1,2,3,4	4
11	20	0402	RES 20 OHM 1/10W 1% 0402 SMD	ERJ-2RKF27R0X	Panasonic	R11,15	2
12	40.2	0402	RES 40.2 OHM 1/10W 1% 0402 SMD	ERJ-2RKF40R2X	Panasonic	R13	1
13	1.21K	0402	RES 1.21K OHM 1/10W 1% 0402 SMD	ERJ-2RKF1211X	Panasonic	R17	1
14	47K	0402	RES 47.0K OHM 1/16W 1% 0402 SMD	RC0402FR-0747KL	Yageo	R8,9	2
15	0	0402	RES 0.0 OHM 1/10W 0402 SMD	ERJ-2GE0R00X	Panasonic	R1,2,3,4,5,6,7,10	8
16	4:1 Balun	SM-22	4:1 Center Tap Balun	TC4-6TG2+	Mini Circuits	T1,2	2
17	F1100	QFN-36	DUAL RF MIXER	F1100NBGI	IDT	U1	1
18	PCB		EV Kit	F11XXEV Kit Rev 05			1

Total 52

TOPMARKINGS


IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.