F1423 Datasheet

TX Differential Input RF Amplifier — *600 MHz to 3000 MHz*

GENERAL DESCRIPTION

The F1423 is a 600 MHz to 3000 MHz TX differential input / single-ended output RF amplifier used in transmitter applications.

The F1423 TX Amp provides 13.1 dB gain with +41.8 dBm OIP3 and 5.1 dB noise figure at 2000 MHz. This device uses a single 5 V supply and 120 mA of I_{CC}.

This device is packaged in a 4mm x 4mm, 24-pin Thin QFN with 50 ohm differential RF input and 50 ohm single ended RF output impedances for ease of integration into the signal-path.

COMPETITIVE ADVANTAGE

In typical Base Stations, RF Amplifiers are used in the TX traffic paths to drive the transmit power amplifier. The F1423 TX Amplifier offers very high reliability due to its construction using silicon die in a QFN package. The F1423 includes a broadband differential input to accept AC-coupled signals directly from a balanced modulator or RF DAC architecture.

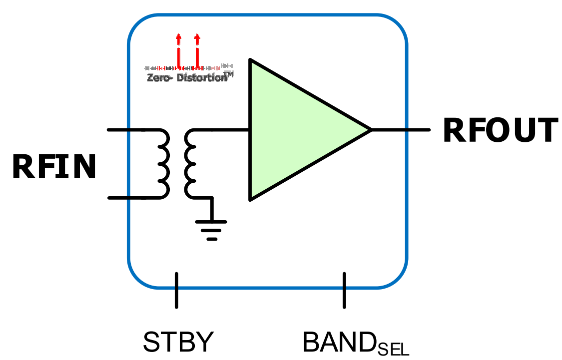
APPLICATIONS

- Multi-mode, Multi-carrier Transmitters
- GSM850/900 Base Stations
- PCS1900 Base Stations
- DCS1800 Base Stations
- WiMAX and LTE Base Stations
- UMTS/WCDMA 3G Base Stations
- PHS/PAS Base Stations
- Public Safety Infrastructure

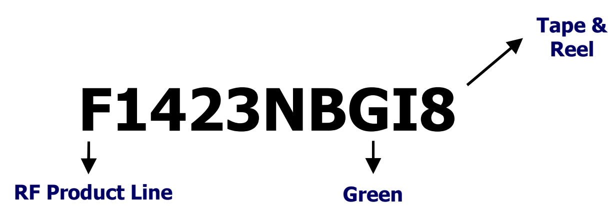
FEATURES

- Broadband 600 MHz – 3000 MHz
- 13.1 dB typical gain @ 2000 MHz
- 5.1 dB NF @ 2000 MHz
- +41.8 dBm OIP3 @ 2000 MHz
- +21.5 dBm output P1dB @ 2000 MHz
- Single 5 V supply voltage
- I_{CC} = 120 mA
- Up to +105 °C T_{CASE} operating temperature
- 50 Ω differential input impedance
- 50 Ω single ended output impedance
- Positive gain slope for board loss compensation
- Standby mode for power savings
- 4 mm x 4 mm, 24-pin TQFN package

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
V_{CC} to GND	V_{CC}	-0.3	+5.5	V
STBY, Band_Sel	V_{Cntl}	-0.3	V_{CC} + 0.25	V
RBIAS1	I_{RB1}		+1.5	mA
RBIAS2	I_{RB2}		+0.8	mA
RFIN+, RFIN-, Voltage[1]	V_{RFin}	-0.02	+0.02	V
RFIN+, RFIN-, Current[1]	I_{RFin}	-5	+5	mA
RFOUT externally applied DC voltage	V_{RFout}	V_{CC} - 0.15	V_{CC} + 0.15	V
RF Differential Input Power (applied for 24 hours maximum)	P_{in}		+22	dBm
Continuous Power Dissipation	P_{diss}		1.5	W
Junction Temperature	T_j		150	°C
Storage Temperature Range	T_{st}	-65	150	°C
Lead Temperature (soldering, 10s)			260	°C
ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2014)			Class 2 (2000 V)	
ElectroStatic Discharge – CDM (JESD 22-C101F)			Class C3 (1000 V)	

Note 1: The RFIN+ and RFIN- pins connect to an internal balun that presents a very low impedance to ground.

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

θ_{JA} (Junction – Ambient)	40 °C/W
θ_{JC} (Junction – Case) [The Case is defined as the exposed paddle]	4 °C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL1

F1423 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage(s)	V_{CC}	All V_{CC} pins	4.75		5.25	V
Operating Temperature Range	T_{CASE}	Case Temperature	-40		+105	°C
RF Frequency Range	F_{RF}	Operating Range	600		3000[1]	MHz
RF Source Impedance	Z_{RFI}	Differential		50		Ω
RF Load Impedance	Z_{RFO}	Single Ended		50		Ω
RF Band Designation[2]						
RF Frequency Range	F_{RF_LB}	Low-band	600		1100	MHz
	F_{RF_MB}	Mid-band	1400		2100	
	F_{RF_HB}	High-band	2100		3000[1]	
	F_{RF_BB}	Broad-band	600		3000[1]	

Note 1: Though device linearity is specified over the range from 700 MHz to 2700 MHz, gain flatness up to 3000 MHz is specified in the high-band and broadband tables to account for extended DPD bandwidth requirements.

Note 2: To optimize RF performance, a different output match will be used for each of the 4 RF bands listed (see Table 2). In addition, different value amplifier bias resistors will be used to optimize performance in each of the 4 bands.

F1423 SPECIFICATION - GENERAL

See F1423 Typical Application Circuit. Unless otherwise stated, specifications apply when operated as a TX RF Amplifier, V_{CC} = +5.0 V, T_C = +25 °C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Logic Input High	V_{IH}		***1.1***			V
Logic Input Low	V_{IL}				***0.63***	
Logic Current	I_{STBY}	STBY pin	***-10***		***+10***	µA
	I_{BAND}	Band_Sel pin	***-10***		***+10***	
Supply Current[3]	I_{CC_LB}	Low-band bias setting		103		mA
	I_{CC_MB}	Mid-band bias setting		120		
	I_{CC_HB}	High-band bias setting		120		
	I_{CC_BB}	Broad-band bias setting		120	***135***[1]	
Standby Current	I_{CC_STBY}	STBY = 5V		0.8	***1.0***	mA
Power ON switching time	T_{ON}	50% STBY to RF output settled to within ±0.5dB		1		µs
Power OFF switching time	T_{OFF}	50% STBY to DC standby current settled to within ±2mA of final I_{CC} value		1		µs

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: Use external resistors to set amplifier bias currents to optimize device linearity. See Table 2.

F1423 SPECIFICATION – LOW-BAND

See F1423 Typical Application Circuit. Unless otherwise stated, specifications apply when operated as a TX RF Amplifier, V_{CC} = +5.0 V, T_C = +25 °C, F_{RF} = 700 MHz, Pout = +7 dBm, R8 =2.1 kΩ, R9 =9.1 kΩ, C1 = 9 pF, Rsource = 50 Ω differential, Rload = 50 Ω single-ended, Band_Sel = open, EVKit trace connector and transformer losses are de-embedded.

Parameter	Symbol	Condition	Min	Typ	Max	Units
RF Input Return Loss	$RFIN_{RL\_LB}$			17		dB
RF Output Return Loss	$RFOUT_{RL\_LB}$			12.8		dB
Common Mode Rejection	$CMRR_{LB}$	700 MHz to 1100 MHz		20.7		dB
Gain	G_{LB}		***12.0*** [1]	12.6	***13.2***	dB
Gain Flatness	G_{FLAT_LB}	Any 400 MHz BW from 700 MHz to 1100 MHz		0.4		dB
Gain Ripple	G_{RIPPLE_LB}	In any 20 MHz range over RF Band		±0.04		dB
Noise Figure[3]	NF_{LB}			4.5		dB
		T_{case} = +105 °C		5.4		
Output Third Order Intercept Point[3]	$OIP3_{LB}$	Pout = +4 dBm/tone 5 MHz tone separation	39[2]	42.5		dBm
Output 1dB Compression[3]	$OP1dB_{LB}$		20	21.1		dBm

F1423 SPECIFICATION – MID-BAND

See F1423 Typical Application Circuit Unless otherwise stated, specifications apply when operated as a TX RF Amplifier, V_{CC} = +5.0 V, T_C = +25 °C, F_{RF} = 2000 MHz, Pout = +7 dBm, R8 =2.4 kΩ, R9 =60.4 kΩ, C1 = 9 pF, Rsource = 50 Ω differential, Rload = 50 Ω single-ended, Band_Sel = GND, EVKit trace connector and transformer losses are de-embedded.

Parameter	Symbol	Condition	Min	Typ	Max	Units
RF Input Return loss	$RFIN_{RL\_MB}$			15		dB
RF Output Return Loss	$RFOUT_{RL\_MB}$			16.5		dB
Common Mode Rejection	$CMRR_{MB}$	1400 MHz to 2100 MHz		19.0		dB
Gain	G_{MB}		***12.5*** [1]	13.1	***13.7***	dB
Gain Flatness	G_{FLAT_MB}	Any 400MHz BW from 1400 MHz to 2100 MHz		0.17		dB
Gain Ripple	G_{RIPPLE_MB}	In any 20 MHz range over RF Band		±0.01		dB
Noise Figure[3]	NF_{MB}			5.1		dB
		T_{case} = +105 °C		5.8		
Output Third Order Intercept Point[3]	$OIP3_{MB}$	Pout = +4 dBm/tone 5MHz tone separation	38.8[2]	41.8		dBm
Output 1dB Compression[3]	$OP1dB_{MB}$		20.3	21.5		dBm

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: Measured using external 1:1 transformer at the RF input.

F1423 Specification – High-Band

See F1423 Typical Application Circuit. Unless otherwise stated, specifications apply when operated as a TX RF Amplifier, V_{CC} = +5.0 V, T_C = +25 °C, F_{RF} = 2700 MHz, Pout = +7 dBm, R8 =2.4 kΩ, R9 =60.4 kΩ, C1 = 6 pF, Rsource = 50 Ω differential, Rload = 50 Ω single-ended, Band_Sel = GND, EVKit trace connector and transformer losses are de-embedded.

Parameter	Symbol	Condition	Min	Typ	Max	Units
RF Input Return loss	$RFIN_{RL\_HB}$			15.5		dB
RF Output Return Loss	$RFOUT_{RL\_HB}$			20		dB
Common Mode Rejection	$CMRR_{HB}$	2100 MHz to 3000 MHz		18.5		dB
Gain	G_{HB}		***12.4***[1]	13.1	***13.9***	dB
Gain Flatness	G_{FLAT_HB}	Any 400 MHz BW from 2100 MHz to 3000 MHz		0.23		dB
Gain Ripple	G_{RIPPLE_HB}	In any 20 MHz range over RF Band		±0.015		dB
Noise Figure[3]	NF_{HB}			6.0		dB
		T_{case} = +105 °C		6.6		
Output Third Order Intercept Point[3]	$OIP3_{HB}$	Pout = +4 dBm/tone 5MHz tone separation		37.3		dBm
Output 1dB Compression[3]	$OP1dB_{HB}$		20.0[2]	20.6		dBm

F1423 Specification – Broad-Band

See F1423 Typical Application Circuit. Unless otherwise stated, specifications apply when operated as a TX RF Amplifier, V_{CC} = +5.0 V, T_C = +25 °C, F_{RF} = 2200 MHz, Pout = +7 dBm, R8 =2.4 kΩ, R9 =60.4 kΩ, C1 = 9 pF, Rsource = 50 Ω differential, Rload = 50 Ω single-ended, Band_Sel = GND, EVKIT trace connector and transformer losses are de-embedded.

Parameter	Symbol	Condition	Min	Typ	Max	Units
RF Input Return loss	$RFIN_{RL\_BB}$			15.0		dB
RF Output Return Loss	$RFOUT_{RL\_BB}$			18.5		dB
Common Mode Rejection	$CMRR_{BB}$	700 MHz to 3000 MHz		18.5		dB
Gain	G_{BB}		***12.6***[1]	13.2	***13.8***	dB
Gain Flatness	G_{FLAT_BB}	Any 400 MHz BW from 700 MHz to 3000 MHz		0.4		dB
Gain Ripple	G_{RIPPLE_BB}	In any 20 MHz range over 400 MHz BW		±0.04		dB
Gain Slope	G_{SLOPE_BB}			±0.002		dB/MHz
Noise Figure[3]	NF_{BB}			5.2		dB
		T_{case} = +105 °C		5.8		
Output Third Order Intercept Point[3]	$OIP3_{BB}$	Pout = +4 dBm/tone 5 MHz tone separation		41.4		dBm
Output 1dB Compression[3]	$OP1dB_{BB}$		20.5[2]	21.4		dBm

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: Measured using external 1:1 transformer at the RF input.

Table1: STBY Truth Table

Parameter	Level	Function
STBY	Logic Low or Open Circuit	Powered On
	Logic High	Powered Off

Table2: Component Settings for Optimized Linearity Performance per RF band

Band	Frequency Range (MHz)	Band_Sel (Pin 11)	Pin 14 to GND (kΩ)	Pin 15 to GND (kΩ)	C1 (pF)	I_{CC} (mA)
Low - Band	600 - 1100	Open	2.1	9.1	9	104
Mid - Band	1400 - 2100	GND	2.4	60.4	9	120
High - Band	2100 - 3000	GND	2.4	60.4	6	120
Broad - Band	700 - 3000	GND	2.4	60.4	9	120

TYPICAL OPERATING CONDITIONS (TOC)

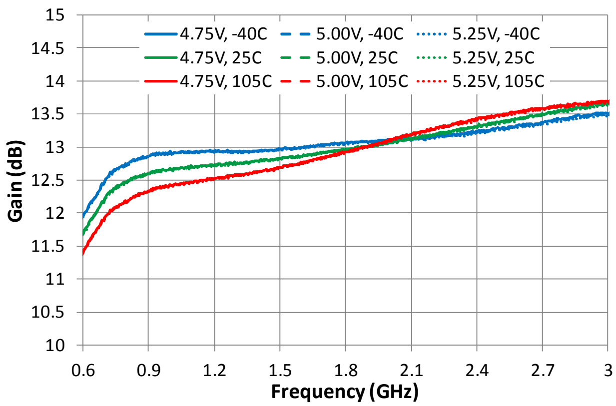
Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

- **Vcc= 5.0 V**
- **Tcase = 25 °C (All temperatures are referenced to the exposed paddle).**
- **Z_S = 50 Ohms Differential**
- **Z_L = 50 Ohms Single Ended**
- **Board configured as defined in Table 2 for each band.**
- **Pout = 4 dBm / Tone**
- **5 MHz Tone Spacing**
- **EVKIT traces, connectors, and transformer losses are de-embedded.**
- **S-parameters (S11, S21, S12, and S22) measured using a de-embedded Differential Board EVKit and the inputs are mathematically combined using an ideal 1:1 (50 Ω : 50 Ω) transformer to produce the 2 port S-parameters.**
- **Amplitude and phase imbalances measures RFIN+ to RFOUT and compares to RFIN- to RFOUT. Phase imbalance is the deviation from an ideal 180 degrees.**
- **OIP3, Output P1dB and Noise Figure measured using a Transformer Board EVKit.**

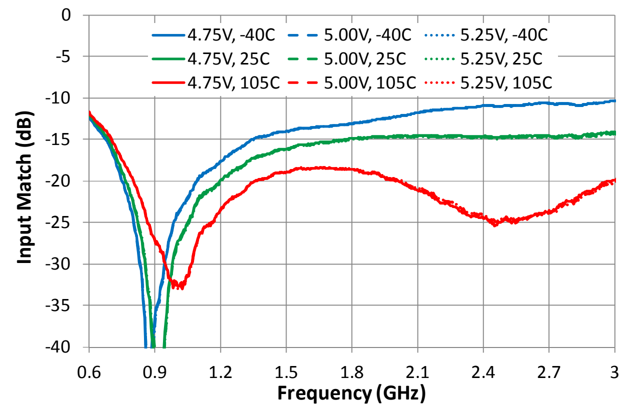
Note: The use of the external transformer T1 is included for simple 2 port evaluation purposes. At some frequencies the external transformer interacts with the on-chip balun affecting the gain and noise figure flatness responses. These interactions have been removed from the noise figure TOCs.

TOCs [Differential Board S-Pars, Amplitude and Phase Imbalance, Broad-Band Bias](-1-)

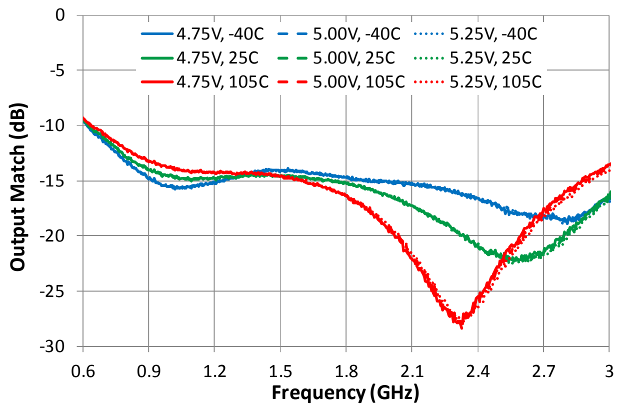
RF Gain vs. Vcc and T_{CASE}



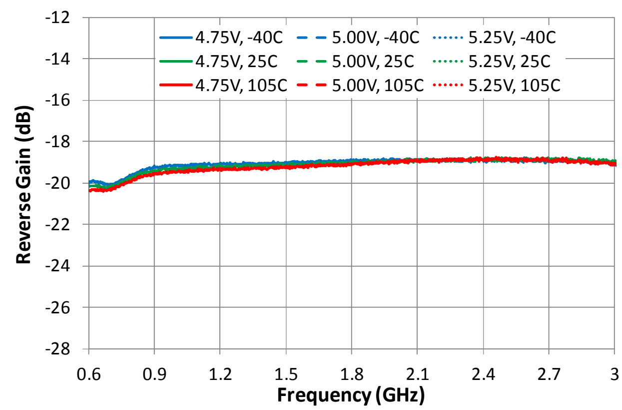
Input Match vs. Vcc and T_{CASE}



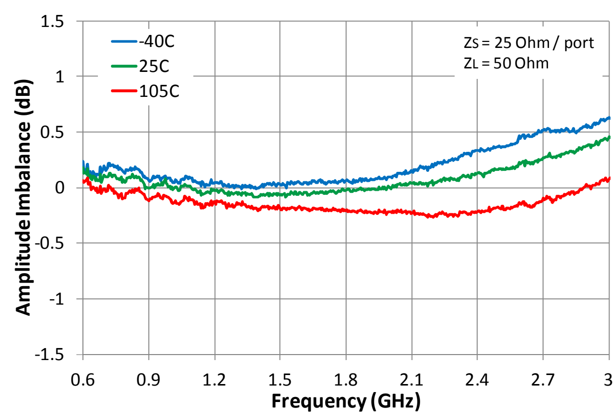
Output Match vs. Vcc and T_{CASE}



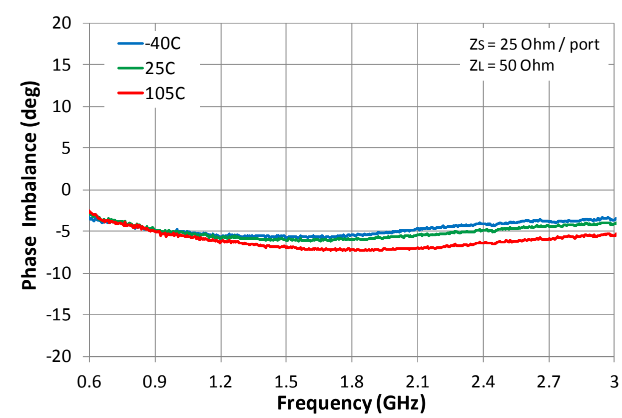
Reverse Gain vs. Vcc and T_{CASE}



Amplitude Imbalance vs. T_{CASE}

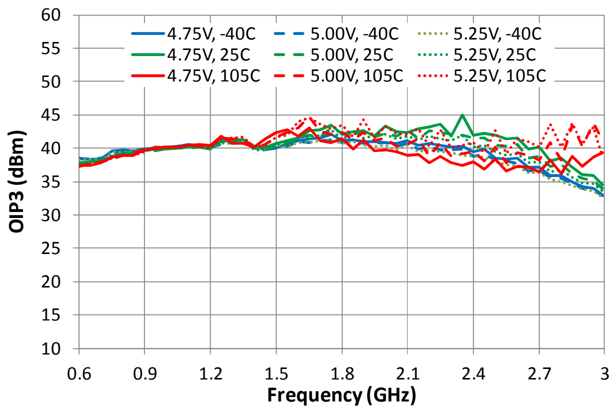


Phase Imbalance vs. T_{CASE}

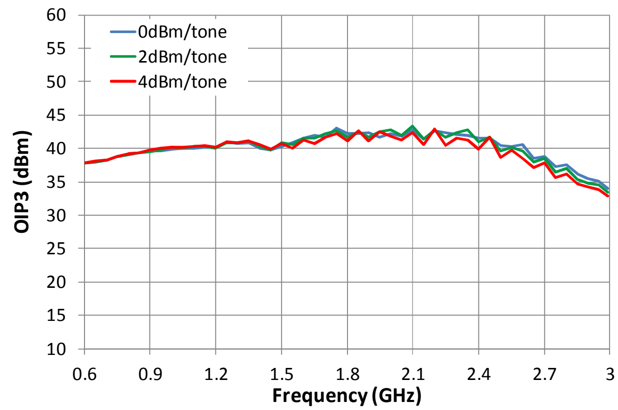


TOCs [Transformer Board, OIP3, P1dB, Noise Figure, Icc, Broad-Band Bias](-2-)

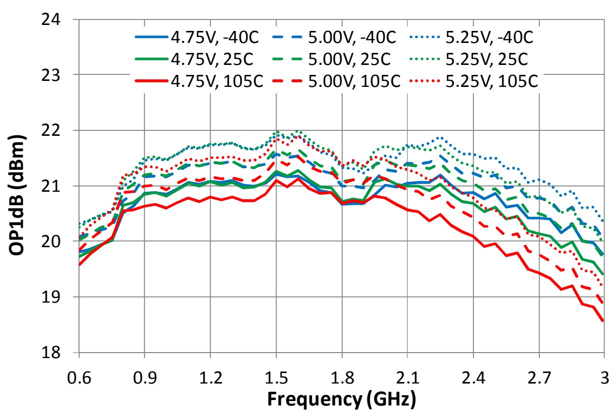
OIP3 vs. Vcc and T_{CASE}



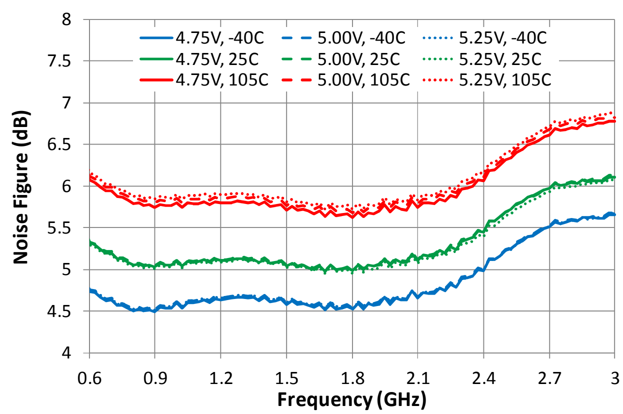
OIP3 vs. Pout Level



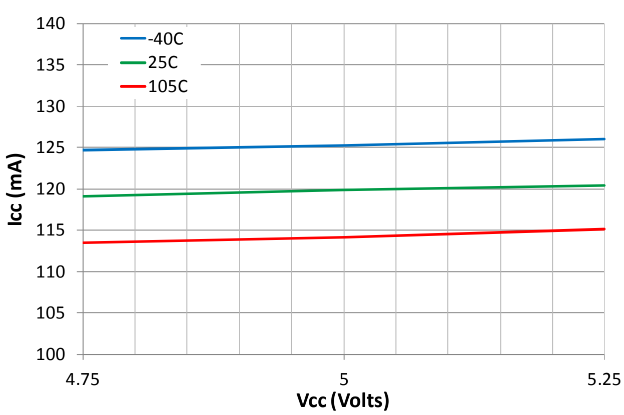
Output P1dB vs. Vcc and T_{CASE}



Noise Figure vs. Vcc and T_{CASE}

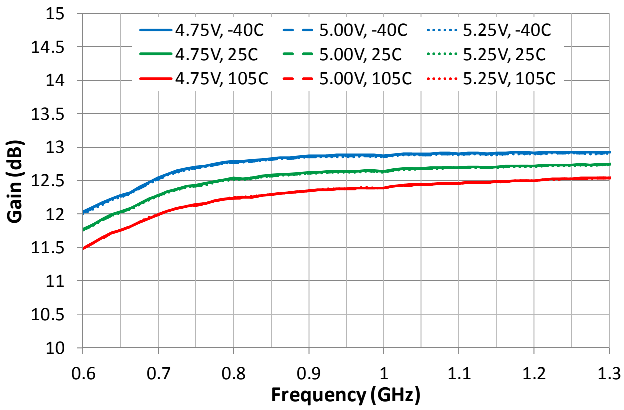


Icc vs. Vcc and T_{CASE}

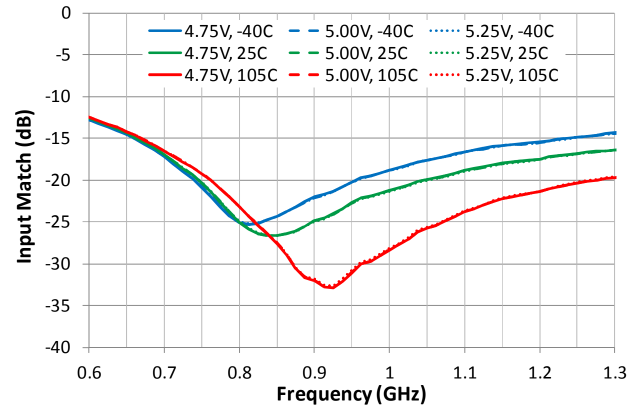


TOCs [Differential Board S-Pars, Amplitude and Phase Imbalance, Low-Band Bias](-3-)

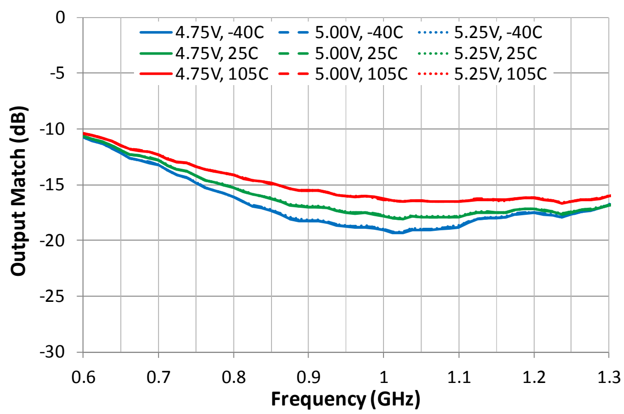
RF Gain vs. Vcc and T_{CASE}



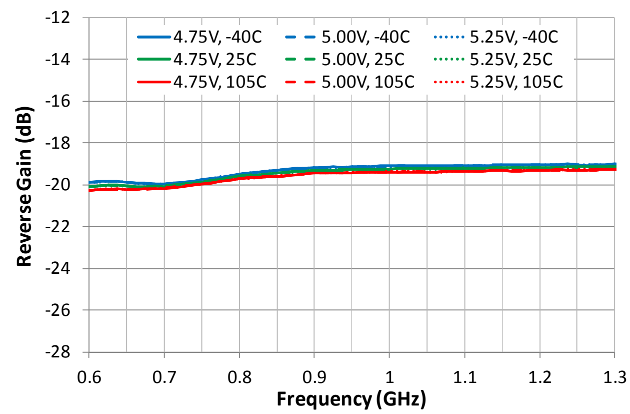
Input Match vs. Vcc and T_{CASE}



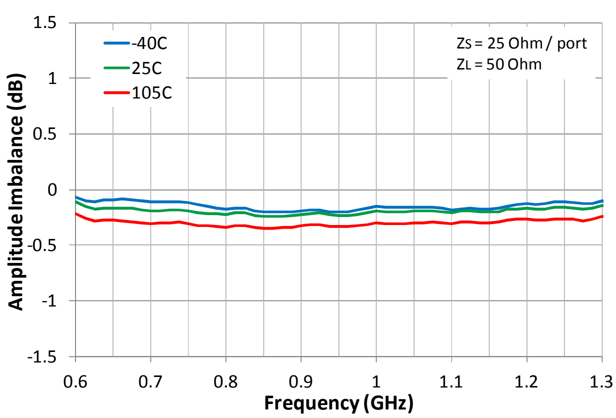
Output Match vs. Vcc and T_{CASE}



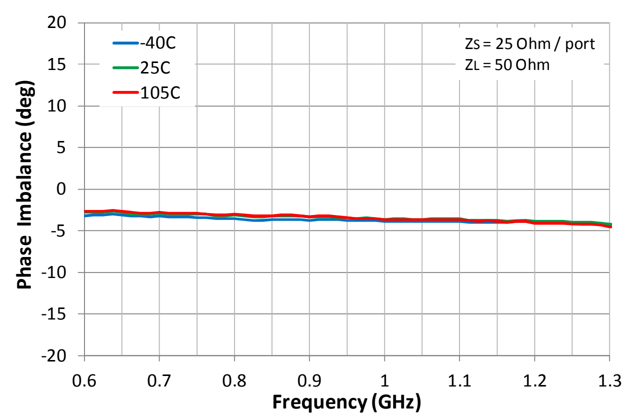
Reverse Gain vs. Vcc and T_{CASE}



Amplitude Imbalance vs. T_{CASE}

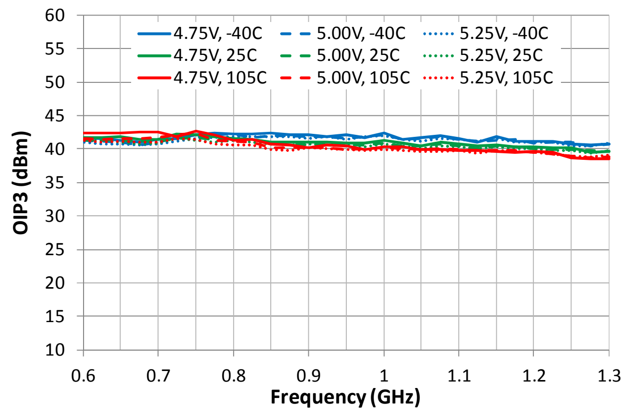


Phase Imbalance vs. T_{CASE}

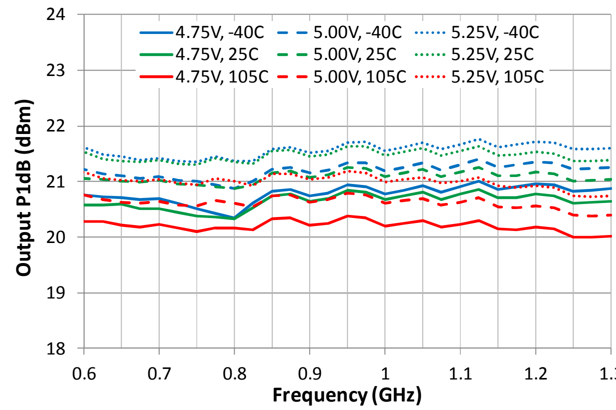


TOCs [Transformer Board, OIP3, P1dB, Noise Figure, Icc, Low-Band Bias](-4-)

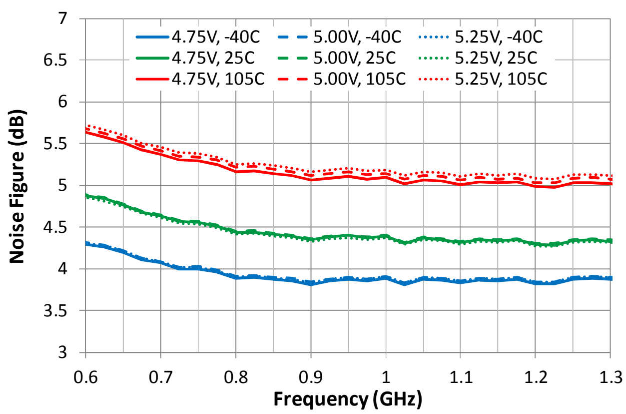
OIP3 vs. Vcc and T_{CASE}



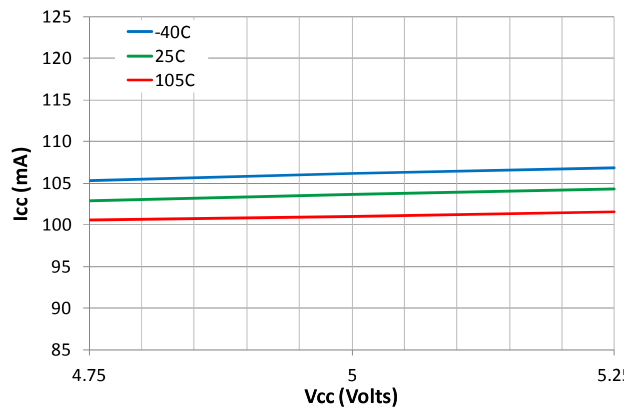
Output P1dB vs. Vcc and T_{CASE}



Noise Figure vs. Vcc and T_{CASE}

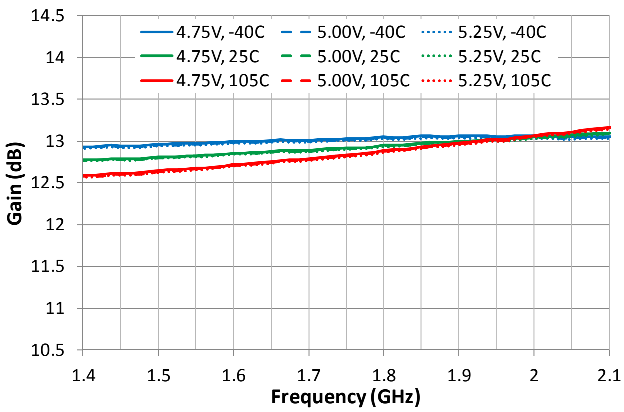


Icc vs. Vcc and T_{CASE}

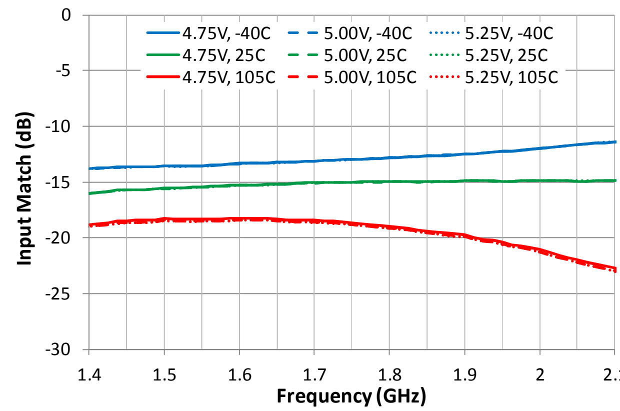


TOCs [Differential Board S-Pars, Amplitude and Phase Imbalance, Mid-Band Bias](-5-)

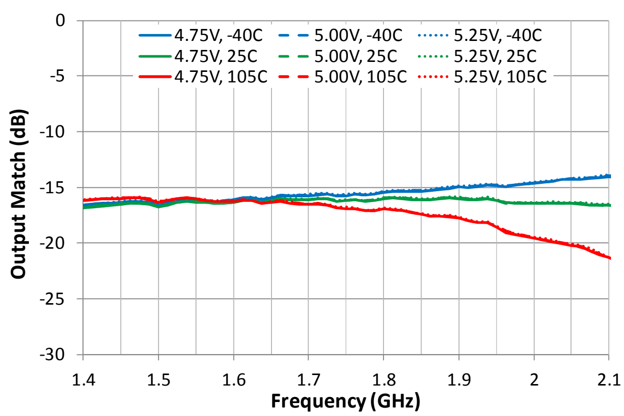
RF Gain vs. Vcc and T_{CASE}



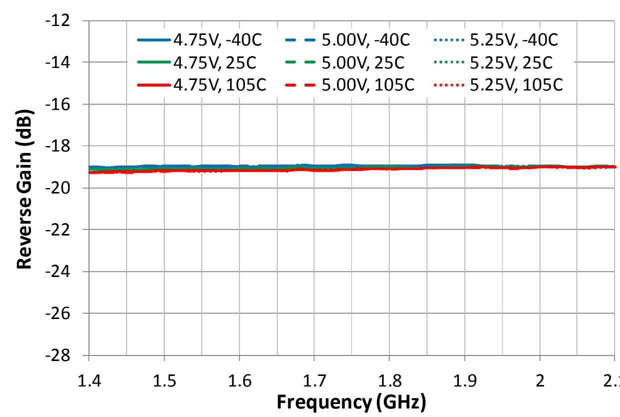
Input Match vs. Vcc and T_{CASE}



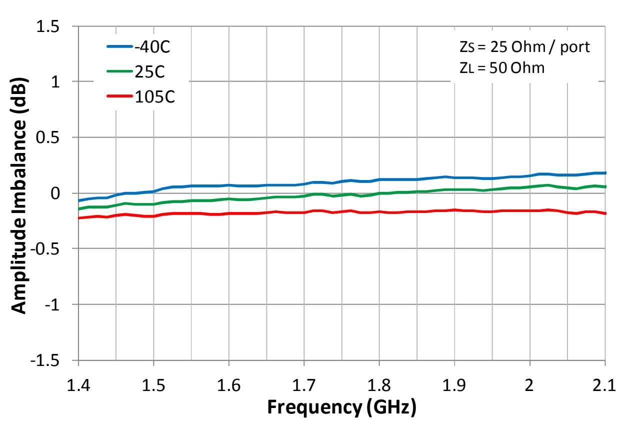
Output Match vs. Vcc and T_{CASE}



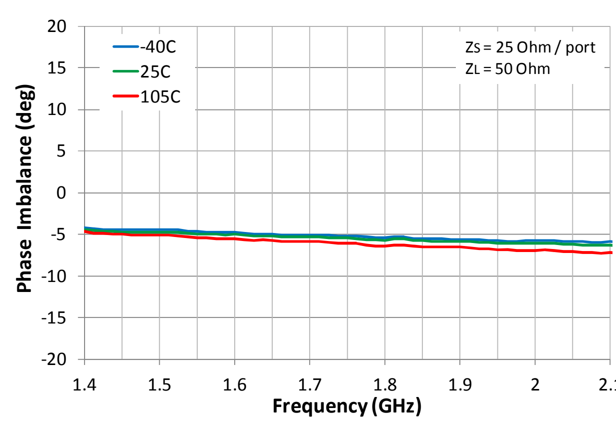
Reverse Gain vs. Vcc and T_{CASE}



Amplitude Imbalance vs. T_{CASE}

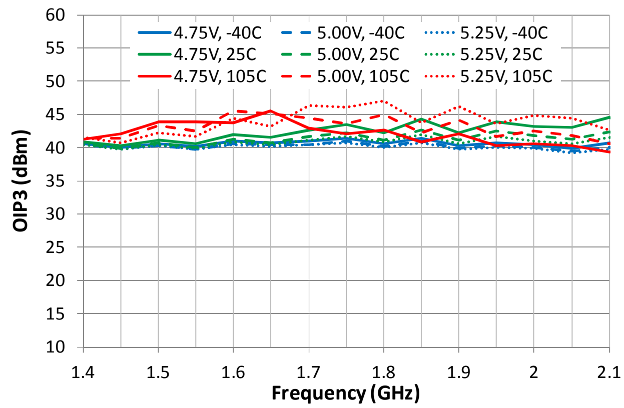


Phase Imbalance vs. T_{CASE}

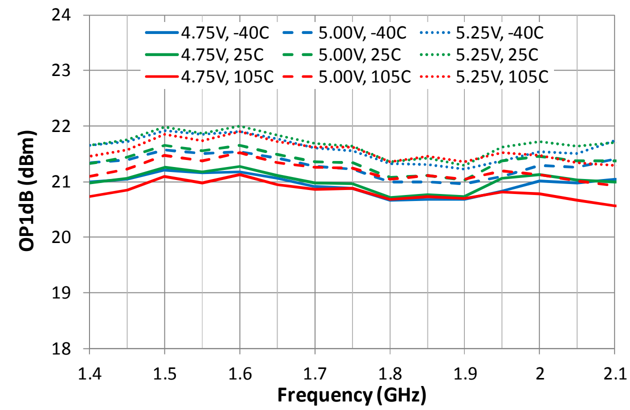


TOCs [Transformer Board, OIP3, P1dB, Noise Figure, Icc, Mid-Band Bias](-6-)

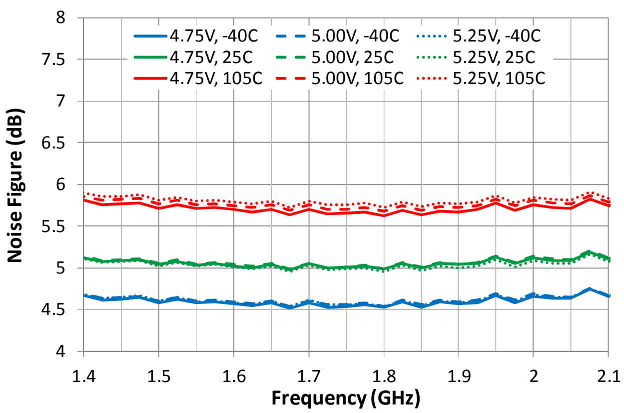
OIP3 vs. Vcc and T_{CASE}



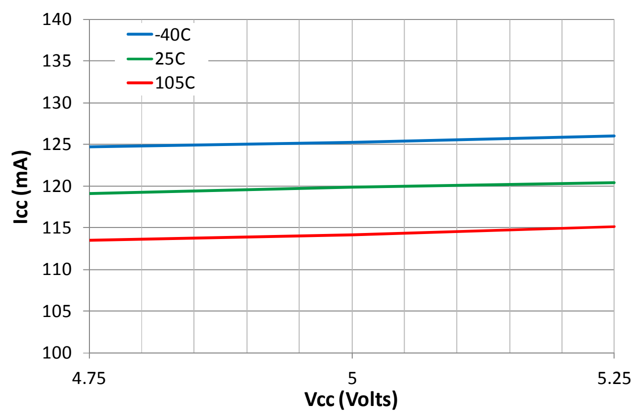
Output P1dB vs. Vcc and T_{CASE}



Noise Figure vs. Vcc and T_{CASE}

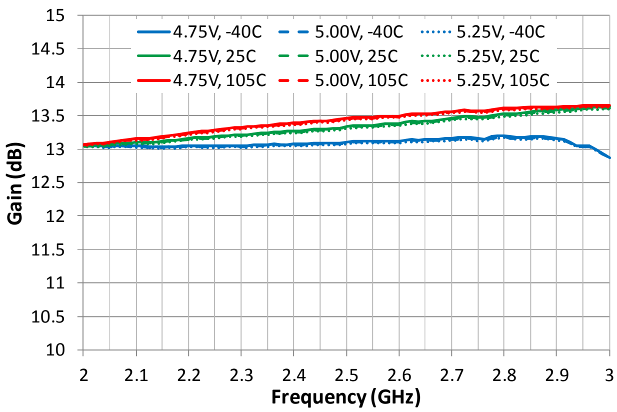


Icc vs. Vcc and T_{CASE}

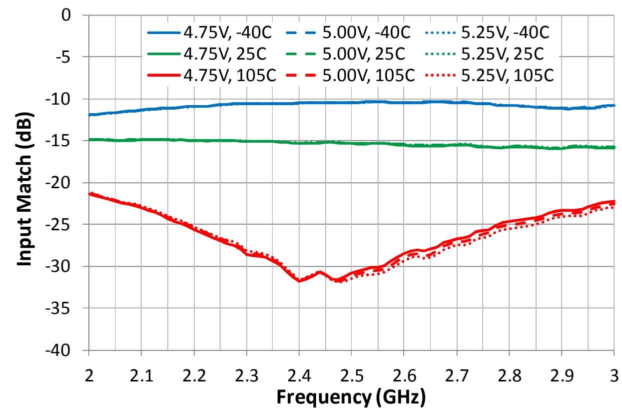


TOCs [Differential Board S-Pars, Amplitude and Phase Imbalance, High-Band Bias](-7-)

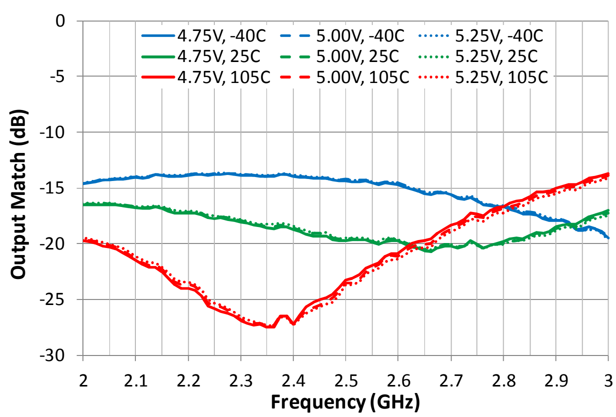
RF Gain vs. Vcc and T_{CASE}



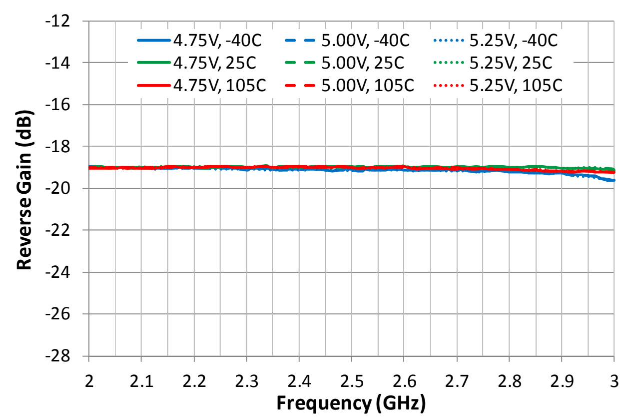
Input Match vs. Vcc and T_{CASE}



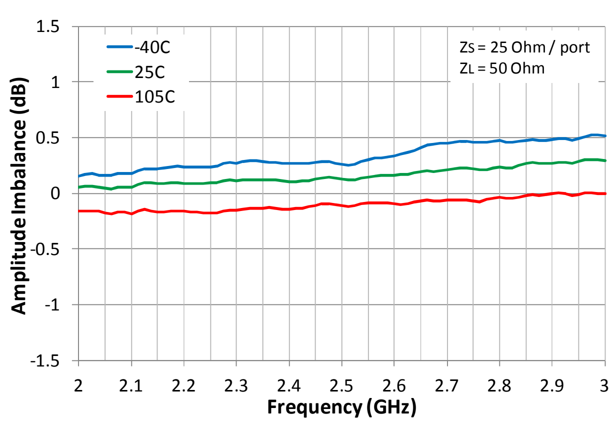
Output Match vs. Vcc and T_{CASE}



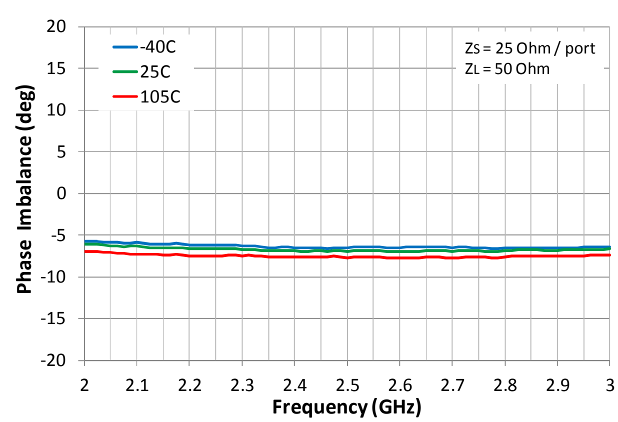
Reverse Gain vs. Vcc and T_{CASE}



Amplitude Imbalance vs. T_{CASE}

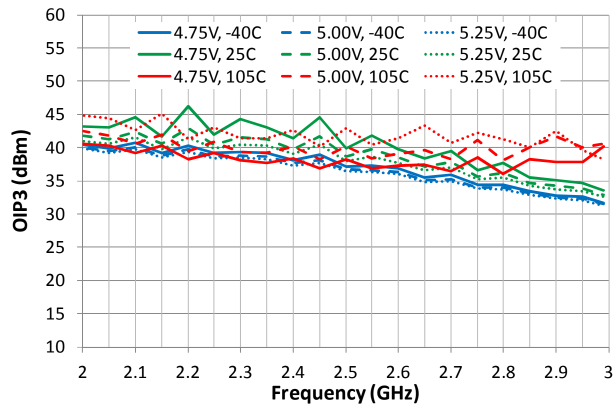


Phase Imbalance vs. T_{CASE}

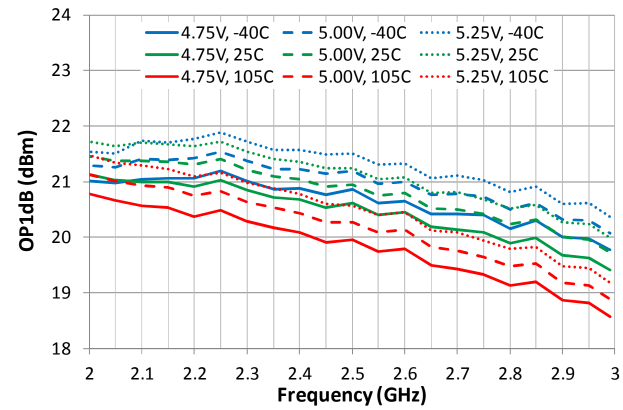


TOCs [Transformer Board, OIP3, P1dB, Noise Figure, Icc, ACLR, High-Band Bias](-8-)

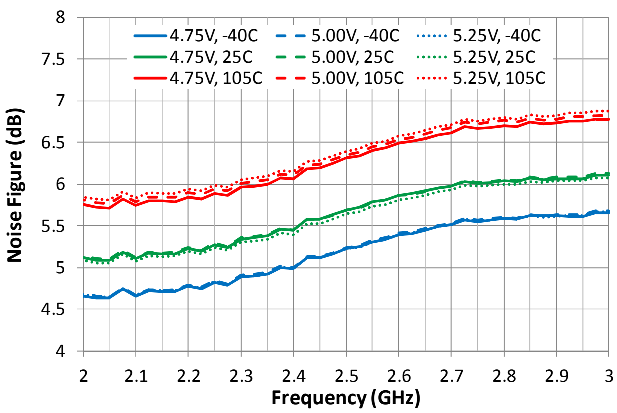
OIP3 vs. Vcc and T_{CASE}



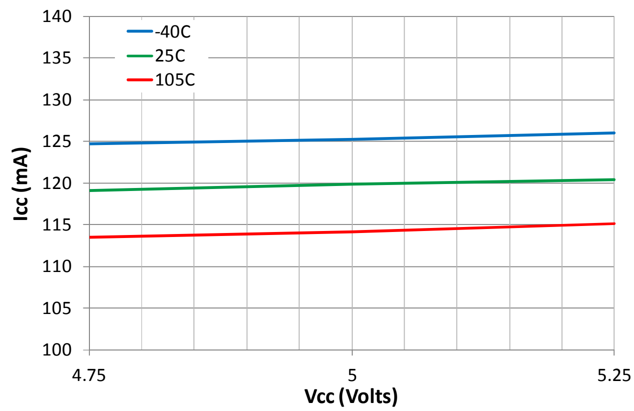
Output P1dB vs. Vcc and T_{CASE}



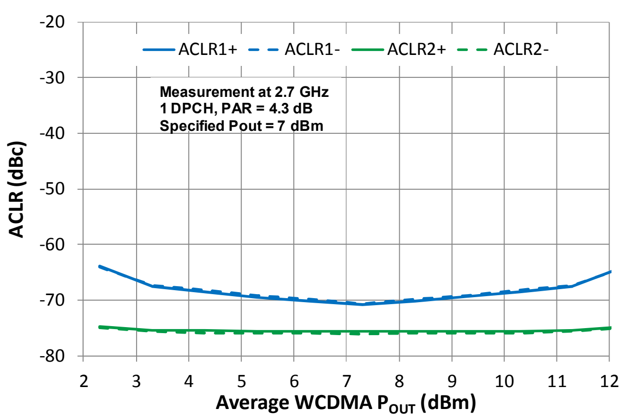
Noise Figure vs. Vcc and T_{CASE}



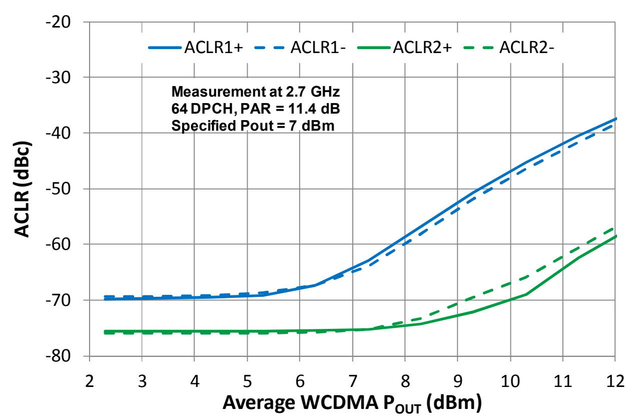
Icc vs. Vcc and T_{CASE}



WCDMA ACLR vs. Pout (PAR = 4.3 dB)



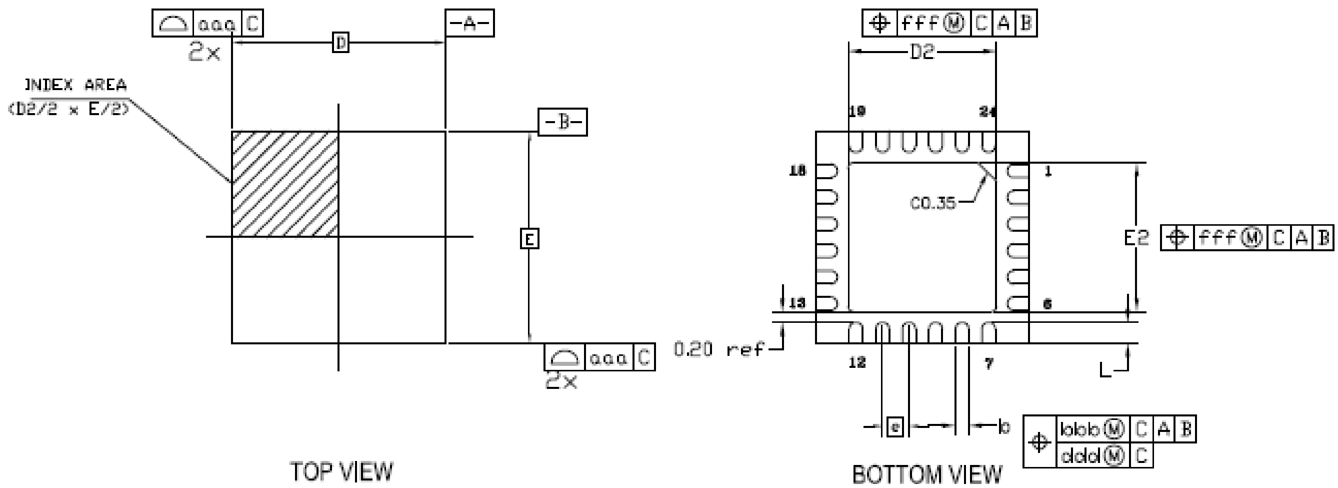
WCDMA ACLR vs. Pout (PAR = 11.4 dB)

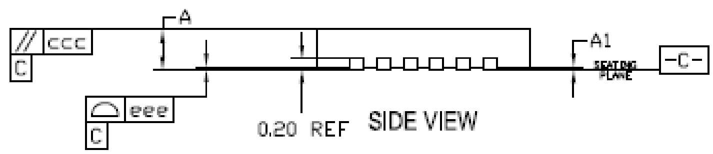


PACKAGE DRAWING

(4 mm x 4 mm 24-pin TQFN), NBG24

NOTE: THE F1423 USES THE P2 EXPOSED PADDLE DIMENSIONS NOTED BELOW





SYMBOL	DIMENSION		
	MIN	NOM	MAX
D2	SEE EPAD OPTION		
E2	SEE EPAD OPTION		
L	0.30	0.40	0.50
D	4.00 BSC		
E	4.00 BSC		
e	0.50 BSC		
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

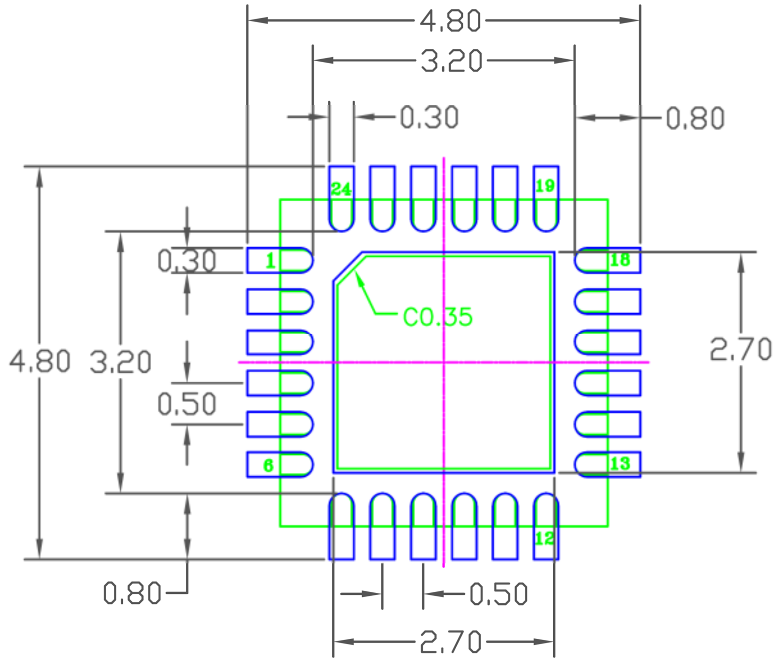
EPAD OPTIONS:

SYMBOL	P2		
	MIN	NOM	MAX
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

LAND PATTERN DIMENSION

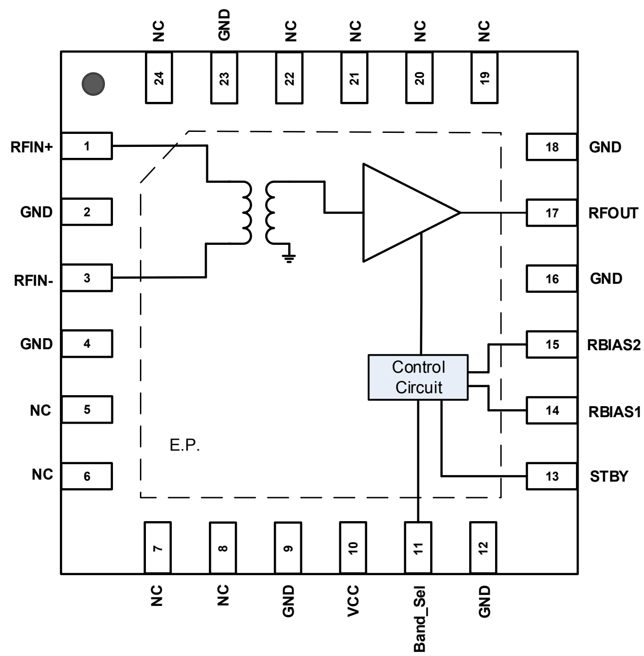


Land Pattern to Support 2.6 mm x 2.6 mm Exposed Paddle Version
(See Version P2 of Package Drawing)

RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

PIN DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1	RFIN+	Differential Input +. Pin looks like a DC short to ground. Must use external DC block if DC is present on RF line.
2, 4, 9, 12, 16, 18, 23	GND	Ground these pins. These pins are internally connected to the exposed paddle.
3	RFIN-	Differential Input -. Pin looks like a DC short to ground. Must use external DC block if DC is present on RF line.
5, 6, 7, 8, 19, 20, 21, 22, 24	NC	No internal connection. OK to connect to GND, OK to connect to VCC. Application circuit ties these pins to ground.
10	VCC	5 V Power Supply. Connect to VCC and use bypass capacitors as close to the pin as possible.
11	Band_Sel	Leave pin open circuited for low-band select and connect 0 Ω resistor to GND for high-band select. Internally this pin has a 1.5 MΩ pull-up resistor that connects to VCC.
13	STBY	Standby (High= device power OFF, Low/Open = device power ON). Internally this pin has a 1 MΩ pull-down resistor that is connected to GND.
14	RBIAS1	Connect external resistor to GND. Use value in Table 2.
15	RBIAS2	Connect external resistor to GND. Use value in Table 2.
17	RFOUT	RF output. Must use external DC block as close to the pin as possible.
	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

APPLICATIONS INFORMATION

The F1423 has been optimized for use in high performance RF applications from 600 MHz to 3000 MHz.

STBY

The STBY control pin allows for power saving when the device is not in use. Setting the STBY pin to a logic low, or leaving the pin open, will put the device in normal operation mode. The STBY pin has an internal 1 Meg ohm resistor to ground. Applying a logic high to this pin will put the part in standby mode. Voltage should not be applied to the STBY pin without VCC present.

Band_Sel

The Band_Sel control pin can be used to adjust the current in the device for Mid Band, High Band, and Wide Band frequency applications. This is done by grounding the Band_Sel pin. Internally there is a 1.5 Meg ohm pull-up resistor. Voltage should not be applied to the Band_Sel pin without VCC present.

RBias1 and RBias2

RBIAS1 (pin 14) and RBIAS2 (pin 15) use a single external resistor to ground on each pin to set the DC current in the device and to optimize the linearity performance of the amplifier stage. The resistor values in Table 2 can be used as a guide for the RF band of interest. By decreasing the resistor value to ground on the RBIAS1 pin will increase the DC current in the amplifier stage. The resistor to ground on RBIAS2 is used to optimize the linearity performance in conjunction with the resistor on RBIAS1.

Amplifier Stability

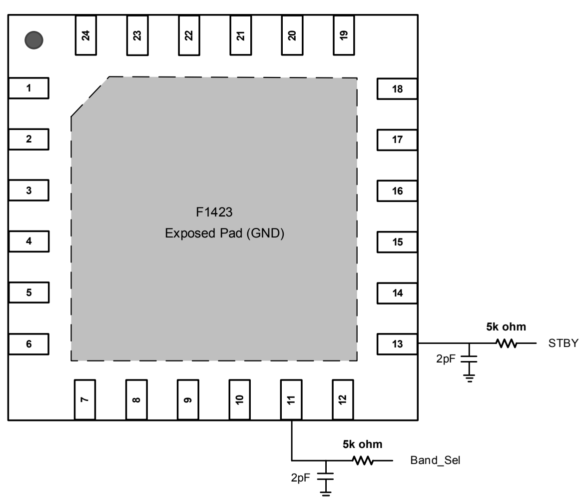
To ensure unconditional stability the value of R1 should be set to 510 Ohms. This will reduce the RF Gain, OIP3, and OP1dB by approx 0.4 dB. Additionally, shunt resistors to ground of approximately 1k ohm should be connected from pin 1 to ground and pin 3 to ground. This will stabilize the circuit due to common mode source impedances. The installed 1k resistor will add 0.1 dB degradation to the Gain and Noise Figure. The 1k ohm will also dampen any common mode amplitude and phase interactions from the differential source impedance and the F1423 differential input impedance.

Power Supplies

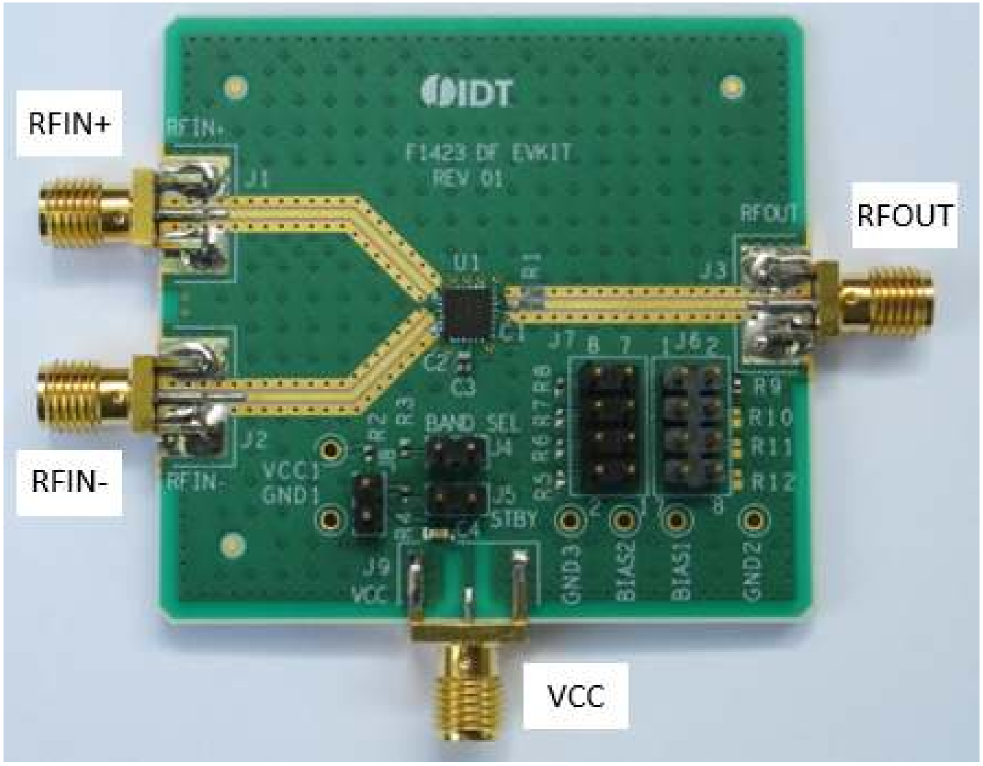
A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1 V / 20 µs. In addition, all control pins should remain at 0 V (+/-0.3 V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

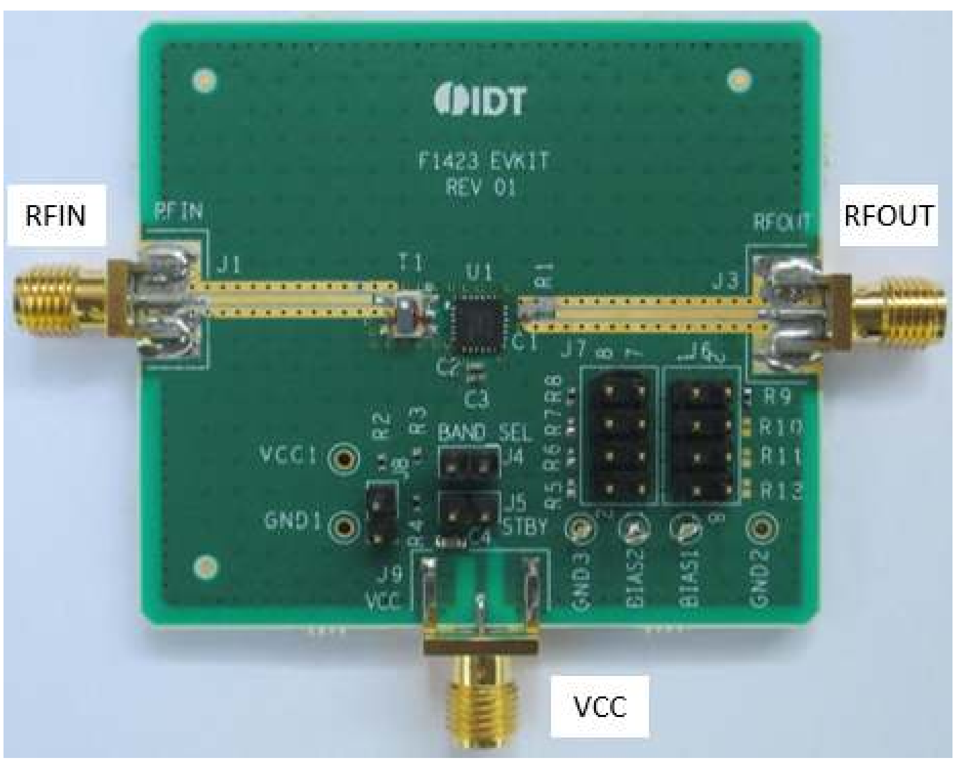
If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to all control pins 11 and 13. Note the recommended resistor and capacitor values do not necessarily match the EV kit BOM for the case of poor control signal integrity.



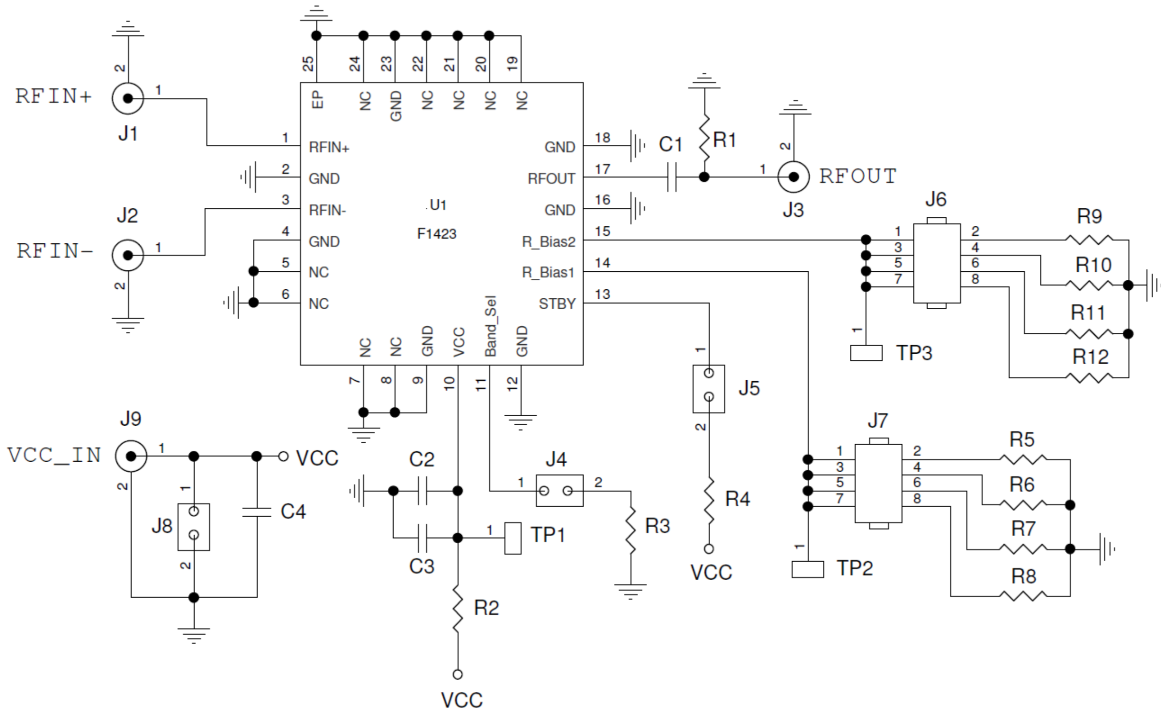
EVKIT PICTURE (DIFFERENTIAL BOARD)



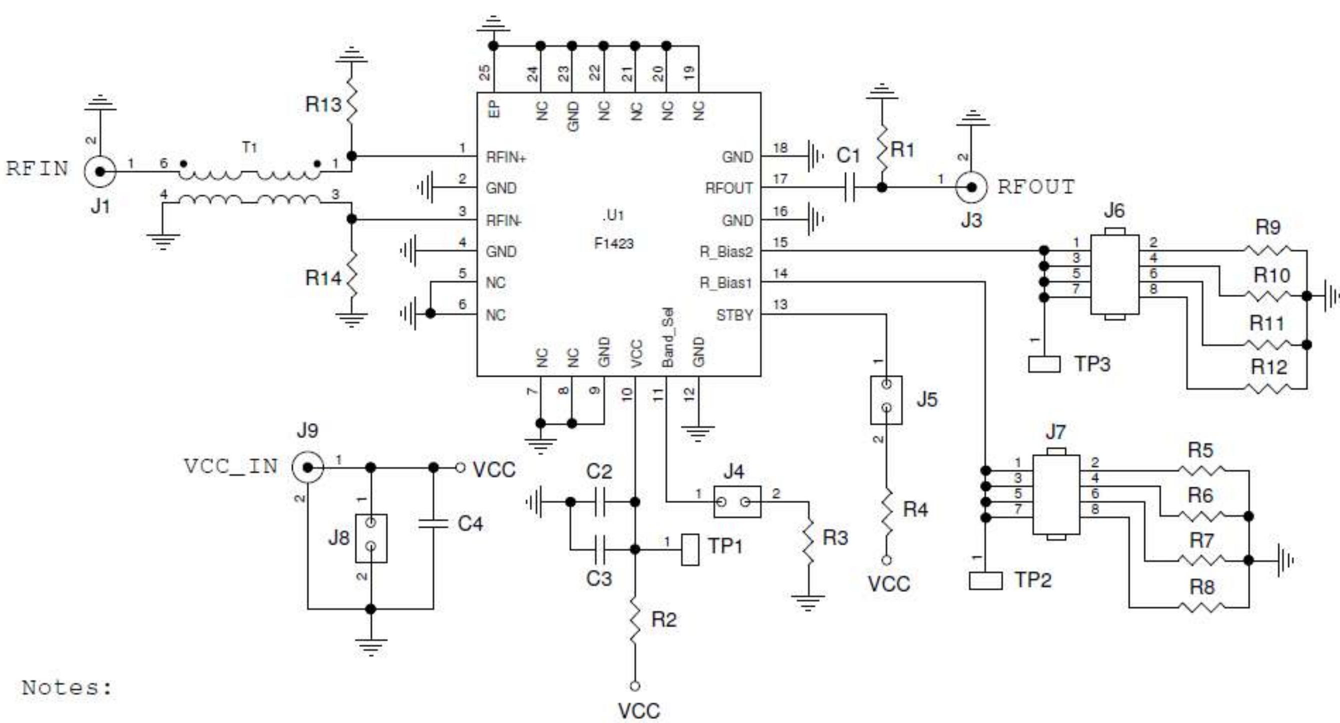
EVKIT PICTURE (TRANSFORMER BOARD)



EVKIT / APPLICATIONS CIRCUIT (DIFFERENTIAL BOARD)



EVKit / Applications Circuit (Transformer Board)



Notes:

T1 used to allow 2 port single ended measurements

R13 and R14 used to dampen T1 common mode resonance with on-chip balun

EVKIT BOM (DIFFERENTIAL BOARD)

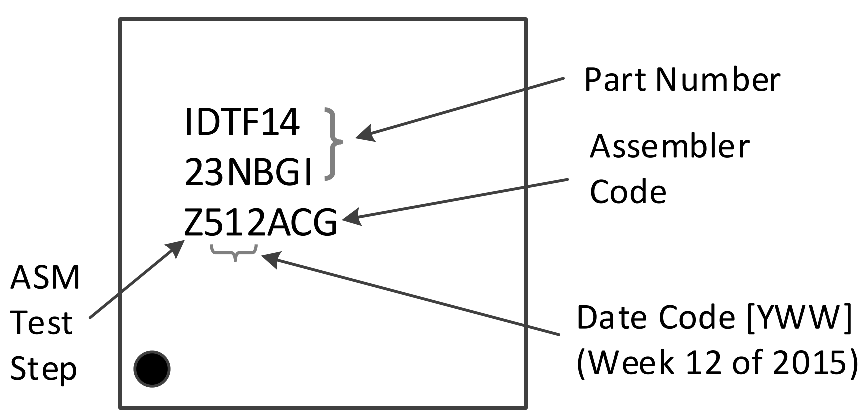
Part Ref	QTY	DESCRIPTION	Mfr. Part #	Mfr.
C1	1	9.0 pF ±0.25 pF, 50 V, C0G, Ceramic Capacitor (0402)	GRM1555C1H9R0C	Murata
C2	1	1000 pF ±5%, 50 V, C0G, Ceramic Capacitor (0402)	GRM1555C1H102J	Murata
C3	1	0.1 µF ±10%, 16 V, X7R, Ceramic Capacitor (0402)	GRM155R71C104K	Murata
C4	1	10 µF ±20%, 6.3 V, X5R, Ceramic Capacitor (0603)	GRM188R60J106M	Murata
R1	1	Not installed (0402)		
R2, R3, R4	3	0 Ω Resistor, 1/10W, (0402)	ERJ-2GE0R00X	Panasonic
R5, R6	0	Not installed		
R7	1	2.1k Ω ±1%, Resistor, 1/10W, (0402)	ERJ-2RKF2101X	Panasonic
R8	1	2.4k Ω ±1%, Resistor, 1/10W, (0402)	ERJ-2RKF2401X	Panasonic
R9	1	60.4k Ω ±1%, Resistor, 1/10W, (0402)	ERJ-2RKF6042X	Panasonic
R10	1	9.1k Ω ±1%, Resistor, 1/10W, (0402)	ERJ-2RKF9101X	Panasonic
R11	1	Not installed		
R12	1	Not installed		
J1, J2, J3, J9	4	SMA_END_LAUNCH (small)	142-0711-821	Emerson Johnson
J4, J5, J8	3	CONN HEADER VERT 2 x 1 Gold	961102-6404-AR	3M
J6, J7	2	CONN HEADER VERT 2 x 4 Gold	67997-108HLF	FCI
U1	1	RF Amplifier	F1423NBGI	IDT
	1	Printed Circuit Board (3 port)	F1423 EVKIT (3 port)	

EVKIT BOM (TRANSFORMER BOARD)

Part Ref	QTY	DESCRIPTION	Mfr. Part #	Mfr.
C1	1	9.0 pF ±0.25 pF, 50 V, C0G, Ceramic Capacitor (0402)	GRM1555C1H9R0C	Murata
C2	1	1000 pF ±5%, 50 V, C0G, Ceramic Capacitor (0402)	GRM1555C1H102J	Murata
C3	1	0.1 µF ±10%, 16 V, X7R, Ceramic Capacitor (0402)	GRM155R71C104K	Murata
C4	1	10 µF ±20%, 6.3 V, X5R, Ceramic Capacitor (0603)	GRM188R60J106M	Murata
R1	1	Not installed (0402)		
R2, R3, R4	3	0 Ω Resistor, 1/10W, (0402)	ERJ-2GE0R00X	Panasonic
R5, R6	0	Not installed		
R7	1	2.1k Ω ±1%, Resistor, 1/10W, (0402)	ERJ-2RKF2101X	Panasonic
R8	1	2.4k Ω ±1%, Resistor, 1/10W, (0402)	ERJ-2RKF2401X	Panasonic
R9	1	60.4k Ω ±1%, Resistor, 1/10W, (0402)	ERJ-2RKF6042X	Panasonic
R10	1	9.1k Ω ±1%, Resistor, 1/10W, (0402)	ERJ-2RKF9101X	Panasonic
R11	1	Not installed		
R12	1	Not installed		
R13, R14	2	510 Ω ±1%, Resistor, 1/10W, (0402) (Note 1)	ERJ-2RKF5100X	Panasonic
T1	1	1:1 wideband transformer	TC1-1-43+	Mini Circuits
J1, J3, J9	3	SMA_END_LAUNCH (small)	142-0711-821	Emerson Johnson
J4, J5, J8	3	CONN HEADER VERT 2 x 1 Gold	961102-6404-AR	3M
J6, J7	2	CONN HEADER VERT 2 x 4 Gold	67997-108HLF	FCI
U1	1	RF Amplifier	F1423NBGI	IDT
	1	Printed Circuit Board (Transformer)	F1423 EVKIT XFMR	

Note 1: When using an external transformer for evaluation, a common mode resonance interaction can occur with the on-chip balun. Resistors R13 and R14 will dampen the resonance but affects the Gain and NF by approx 0.2dB.

TOP MARKINGS



EVKIT OPERATION

The F1423 EVkits (single ended and differential) have a number of control features available.

STBY (2 pin Header J5)

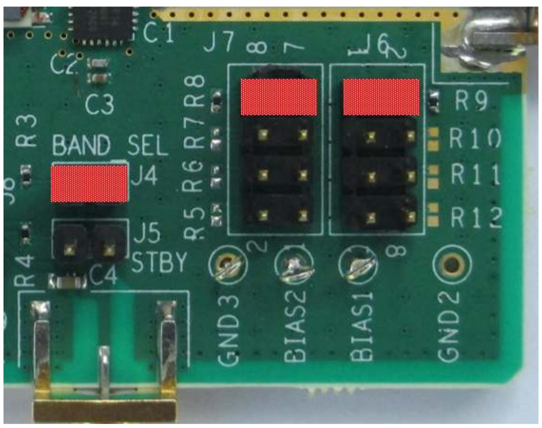
Two-pin header J5 can be used to set the part for operational or standby mode. Leaving the two J5 pins unconnected will place it in the operational mode. Connecting the two J5 pins together will pull up the STBY pin to Vcc through R4 and place the part into the standby mode.

Band_Sel (2 pin Header J4)

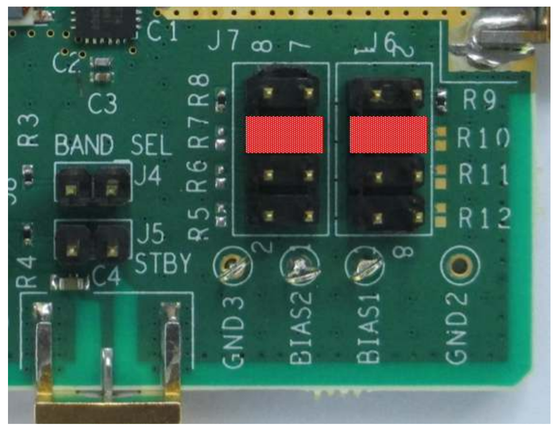
Two-pin header J4 can be used to set the part for best operational performance in different RF bands. Based on Table 2 above the Low-Band performance is best with these two J4 pins left open while the other bands typically have these two pins shorted together.

RF Band Biasing (RBIAS1, RBIAS2, Band_Sel)

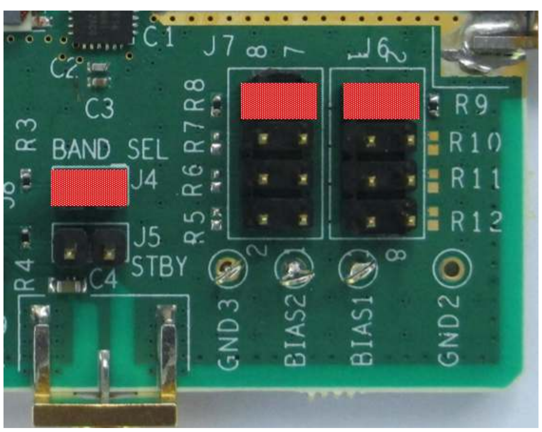
Below are 4 settings showing the recommended J4, J7, and J8 jumper connections for best linearity performance in the different RF bands. The jumpers (shown in red below) select the RBIAS1 and RBIAS2 resistor values along with the Band_Sel setting (see Table 2 above). Never have two shunts installed at the same time on header J7 since this may produce excessive bias current and damage the part.



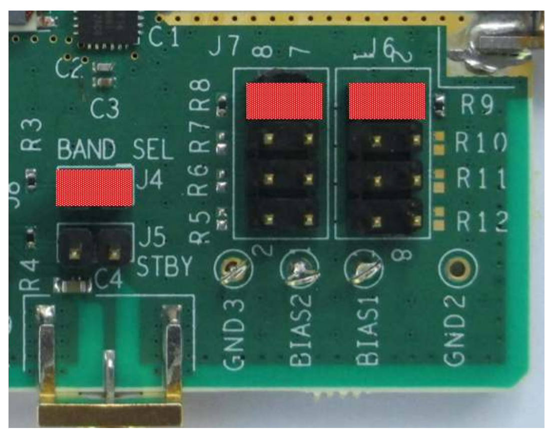
Broad-Band



Low-Band



Mid-Band



High-Band

REVISION HISTORY SHEET

Rev	Date	Page	Description of Change
O	2015- Nov-6		Initial Release

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