Description

This document describes the specification for the F1950 Digital Step Attenuator. The F1950 is part of a family of *Glitch-Free* DSAs optimized for the demanding requirements of communications Infrastructure. These devices are offered in a compact 4x4 QFN package with 50Ω impedances for ease of integration into the radio system.

Competitive Advantage

Digital step attenuators are used in Receivers and Transmitters to provide gain control. The F1950 is a 7-bit step attenuator optimized for these demanding applications. The silicon design has very low insertion loss and low distortion (+65 dBm $IP3_I$). The device has pinpoint accuracy and settles to final attenuation value within 400 ns. Most importantly, the F1950 includes Renesas' *Glitch-Free* technology which results in less than 0.6 dB of overshoot ringing during MSB transitions. This is in stark contrast to competing DSAs that *glitch as much as 10 dB* during MSB transitions (see p.10).

- ✓ Lowest insertion loss for best SNR
- ✓ Glitch-Free when transitioning – won't damage PA or ADC
- ✓ Extremely accurate with low distortion

Glitch-Free™

Applications

- Base Station 2G, 3G, 4G, TDD radiocards
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios
- RFID handheld and portable readers
- Cable Infrastructure

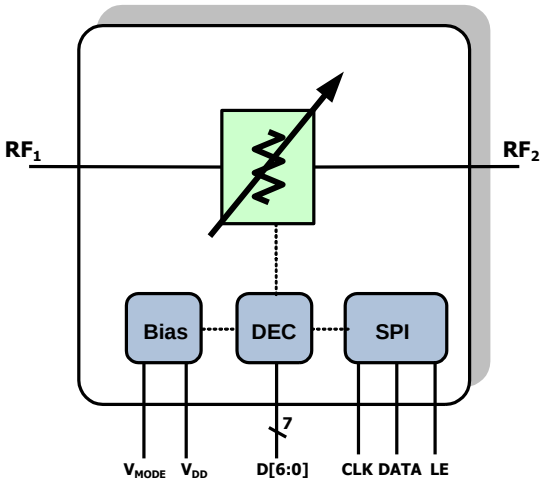
Part# Matrix

Part#	Freq range	Resolution / Range	Control	IL	Pinout
F1950	150 - 5000	0.25 / 31.75	Parallel & Serial	-1.3	PE
F1951	100 - 5000	0.50 / 31.5	Serial Only	-1.2	HITT
F1952	100 – 4000	0.50 / 15.5	Serial Only	-0.9	HITT

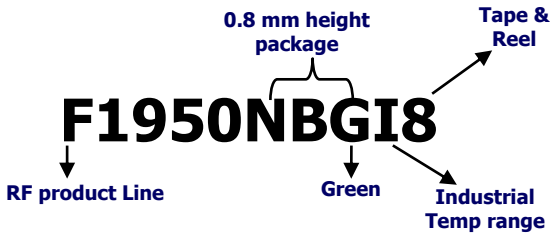
Features

- *Glitch-Free*, < 0.6 dB transient overshoot
- Spurious Free Design
- 3V to 5V supply
- Attenuation Error < 0.3 dB @ 2 GHz
- Low Insertion Loss < 1.3 dB @ 2 GHz
- Excellent Linearity +65 dBm $IP3_I$
- Fast settling time, < 400 ns
- Class 2 JEDEC ESD (> 2kV HBM)
- Serial & Parallel Interface 31.75 dB Range
- 4 x 4 mm Thin QFN 24 pin package

Block Diagram



Ordering Information



ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND	-0.3 V to +5.5 V
D[6:0], DATA, CLK, LE, V_{MODE}	-0.3 V to 3.6 V
RF Input Power (RF1, RF2) calibration and testing	+29 dBm
RF Input Power (RF1, RF2) continuous RF operation	+23 dBm
θ_{JA} (Junction – Ambient)	+50 °C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	+3 °C/W
Operating Temperature Range (Case Temperature)	T_C = -40 °C to +100 °C
Maximum Junction Temperature	140 °C
Storage Temperature Range	-65 °C to +150 °C
Lead Temperature (soldering, 10s)	+260 °C

F1950 SPECIFICATION (31.75 dB Range)

Specifications apply at **V_{DD} = +3.3V**, **f_{RF} = 2000MHz**, and T_C= +25°C, EVkit losses are de-embedded (see p. 17) for spec purposes

Parameter	Comment	Sym.	Min	Typical	Max	Units
Logic Input High	CLK, LE, DATA, D[6:0], V_{MODE}	**V_{IH}**	***2.3***		3.6	V
Logic Input Low	CLK, LE, DATA, D[6:0], V_{MODE}	**V_{IL}**			***0.7***	V
Logic Current	V_{MODE}	**I_{IH}, I_{IL}**	***-5***		***+5***	µA
Supply Voltage(s)	Main Supply	**V_{DD}**	3.0	3.30	5.25	V
Supply Current	Total	**I_{DD}**		***0.25***	***0.5***[1]	mA
Temperature Range	Operating Range (Case)	**T_C**	-40		+100	°C
Frequency Range	Operating Range	**F_{RF}**	***150***		***5000***	MHz
RF1, RF2 Return Loss	dB(s11), dB(s22)	**S_{11}, S_{22}**		-22		dB
Minimum Attenuation	D[6:0] = [0000000]	**A_{MIN}** or **IL**		***1.3***	***1.9***	dB
Maximum Attenuation	D[6:0] = [1111111]	**A_{MAX}**	32.6	33.0		dB
Minimum Gain Step	Least Significant Bit	**LSB**		0.25		dB
Phase Delta	Phase change A_{MIN} vs. A_{MAX}	**Φ_Δ**		34		deg
Differential Non-Linearity	Max error between adjacent steps	**DNL**		0.10		dB
Integral Non-Linearity	Max Error vs. line (A_{MIN} ref) to 13.75 dB ATTN	**INL_1**		***0.02***	***0.30***	dB
Integral Non-Linearity	Max Error vs. line (A_{MIN} ref) to 31.75 dB ATTN	**INL_2**		0.27	0.45	dB
Input IP3	D[6:0] = [0000000] = A_{MIN} D[6:0] = [0111111] = $A_{15.75}$ D[6:0] = [1111111] = A_{MAX} ▪ P_{IN} = +10 dBm per tone ▪ 50 MHz Tone Separation	**$IP3I_1$** **$IP3I_2$** **$IP3I_3$**	+60[2] +59 +57	+63 +61 +61		dBm
0.1 dB Compression *Please note ABS MAX Input power on Page 2*	▪ D[6:0] = [0001010] = $A_{2.5}$ ▪ Baseline P_{IN} = 20 dBm	**$P_{0.1}$**		27.5		dBm
Settling Time	▪ Start LE rising edge > V_{IH} ▪ End +/-0.10 dB Pout settling ▪ 15.75 – 16.00 transition	**T_{LSB}**		400		ns
Serial Clock Speed	SPI 3 wire bus	**F_{CLK}**		***20***	***50***	MHz
Parallel to Serial Setup	SPI 3 wire bus	**A**	***100***			ns
Serial Data Hold Time	SPI 3 wire bus	**B**	***10***			ns
LE delay from final serial clock rising edge	SPI 3 wire bus	**C**	***10***			ns

SPECIFICATION NOTES:

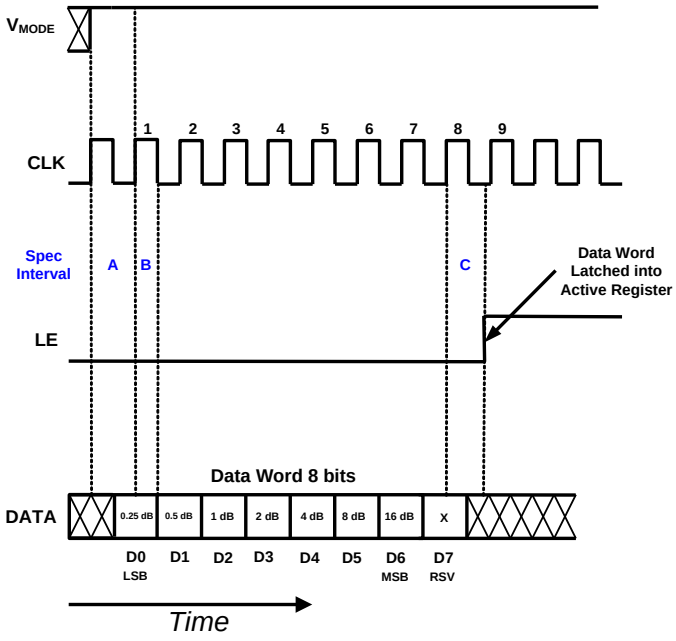
1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test
2 – All other Items in min/max columns are Guaranteed by Design Characterization

SERIAL CONTROL MODE

Serial mode is selected by floating V_{MODE} (pin3) or pulling it to a voltage > V_{IH}. In serial mode data is clocked in LSB first. Note the timing diagram below.

Note – *The F1950 includes a CLK inhibit feature designed to minimize sensitivity to CLK bus noise when the device is not being programmed. When Latch enable is high (> V_{IH}), the CLK input is disabled and DATA will not be clocked into the shift register. It is recommended that LE be pulled high (> V_{IH}) when the device is not being programmed.*

SERIAL REGISTER TIMING DIAGRAM: (Note the Timing Spec Intervals in **Blue**)



SERIAL MODE DEFAULT CONDITION:

When the device is powered up it will default to the **Maximum Attenuation** setting as described below:
Note that for the F1950 in all cases (High or 1) = Attenuation Stepped IN. (0 or Low) = Attenuation Stepped OUT.

Default Register Settings

D7 RSV	D6 MSB	D5	D4	D3	D2	D1	D0 LSB
0	1	1	1	1	1	1	1

SERIAL MODE TIMING TABLE:

Interval Symbol	Description	Min Spec	Max Spec	Units
A	Parallel to Serial Setup Time	100		ns
B	Serial Data Hold Time	10		ns
C	LE delay from final serial clock rising edge	10		ns

PARALLEL CONTROL MODE

The user has the option of running in one of two parallel modes: *Direct Parallel Mode* or *Latched Parallel Mode.*

DIRECT PARALLEL MODE:

Direct Parallel Mode is selected when V_{MODE} (pin 3) is < V_{IL} and LE (pin 16) is > V_{IH}. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 19, 20, 21, 22, 23, 24, 1]. Use direct parallel mode for the fastest settling time.

LATCHED PARALLEL MODE:

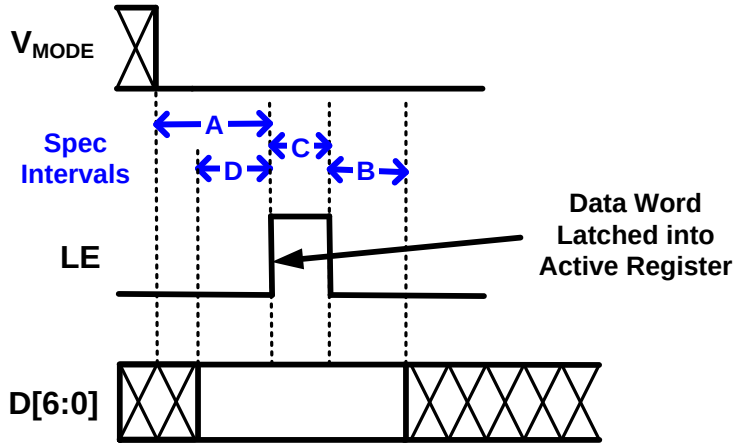
Latched Parallel Mode is selected when V_{MODE} (pin 3) is < V_{IL} and LE (pin 16) is toggled from < V_{IL} to > V_{IH}

To utilize Latched Parallel Mode:

- Set LE < V_{IL}
- Adjust pins [19, 20, 21, 22, 23, 24, 1] to the desired attenuation setting. (Note the device will not react to these pins while LE < V_{IL}.)
- Pull LE > V_{IH}. The device will then transition to the attenuation settings reflected by these pins.

Latched Parallel Mode implies a default state for when the device is powered up with V_{MODE} < V_{IL} and LE < V_{IL}. In this case the default setting is MAXIMUM Attenuation.

LATCHED PARALLEL MODE TIMING DIAGRAM: (Note the Timing Spec Intervals in **Blue**)

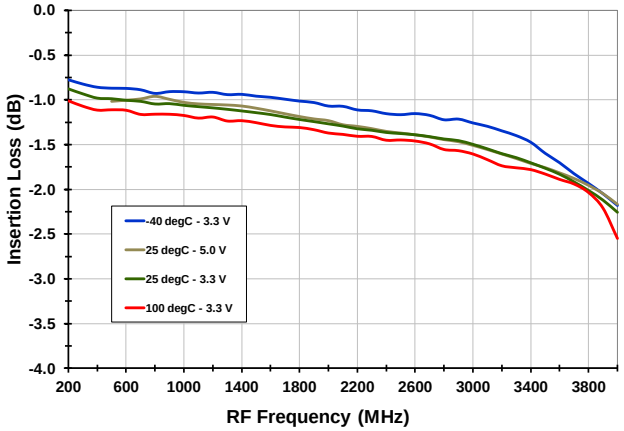


LATCHED PARALLEL MODE TIMING TABLE:

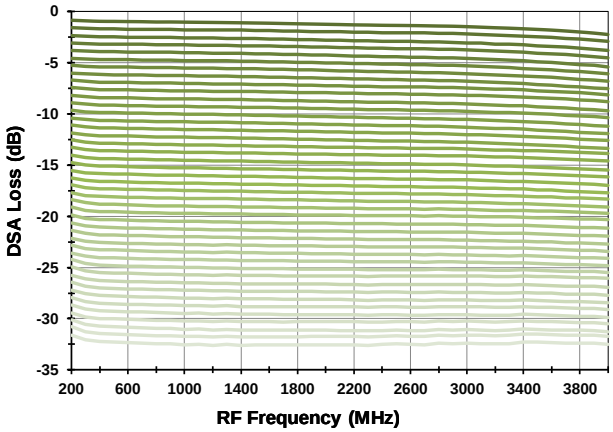
Interval Symbol	Description	Min Spec	Max Spec	Units
A	Serial to Parallel Mode Setup Time	100		ns
B	Parallel Data Hold Time	10		ns
C	LE minimum pulse width	10		ns
D	Parallel Data Setup Time	10		ns

TYPICAL OPERATING PARAMETRIC CURVES (EVKit loss de-embedded unless otherwise noted)

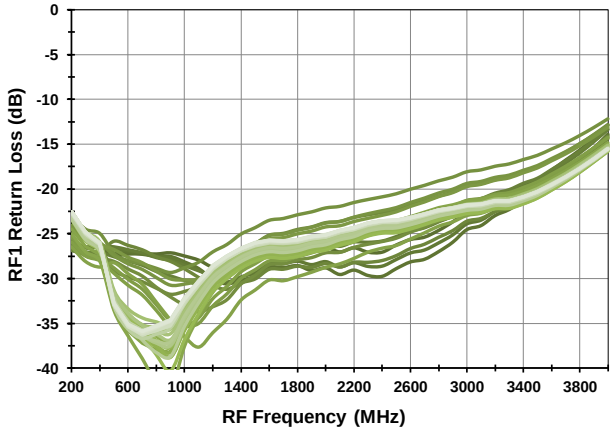
Insertion Loss vs. Frequency [A_{MIN}]



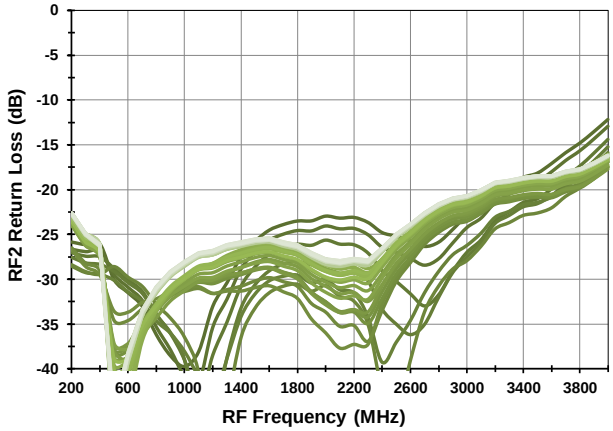
Attenuation vs. Freq [T_{CASE} = +25C, 0.75 dB steps]



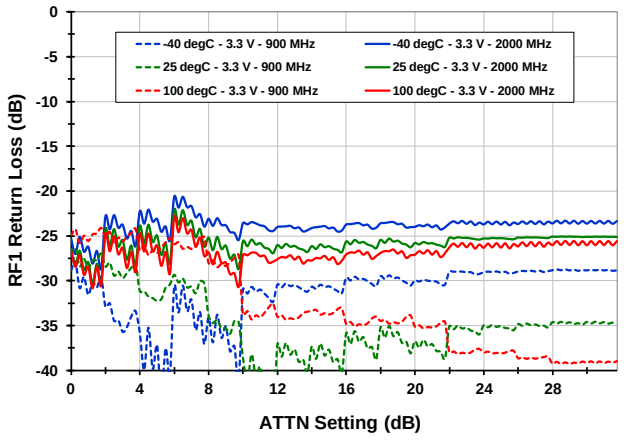
S_{11} vs. Frequency [T_{CASE} = +25C, 0.75 dB steps]



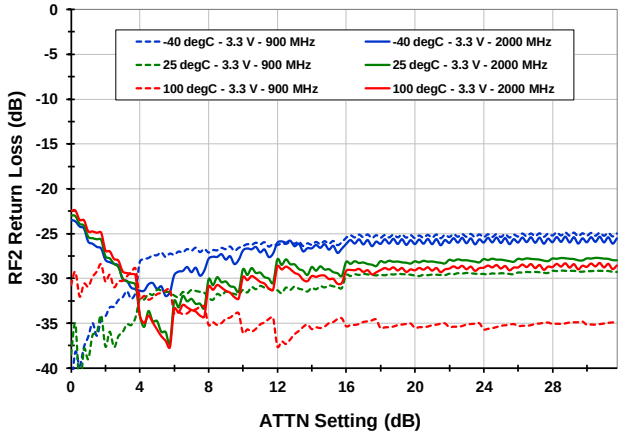
S_{22} vs. Frequency [T_{CASE} = +25C, 0.75 dB steps]



S_{11} vs. Attenuation State

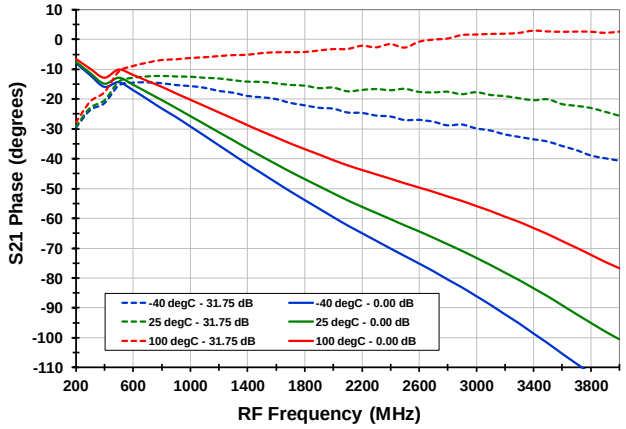


S_{22} vs. Attenuation State

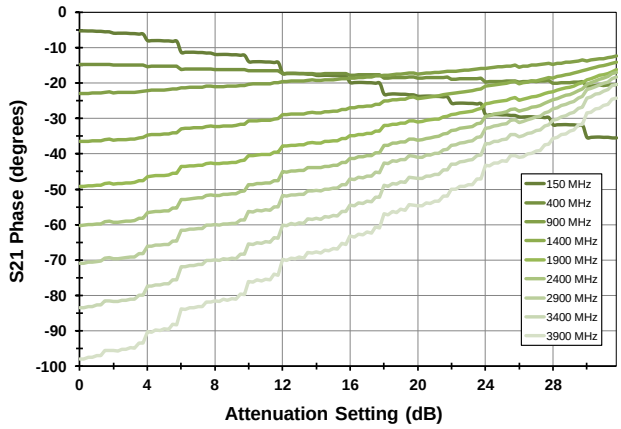


TOCs CONTINUED (-2-)

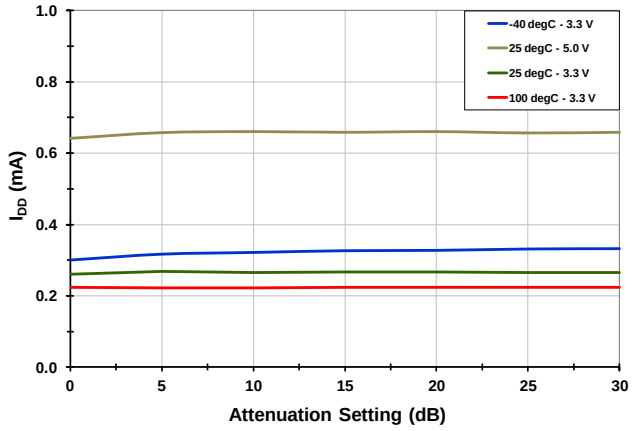
Phase vs. Frequency



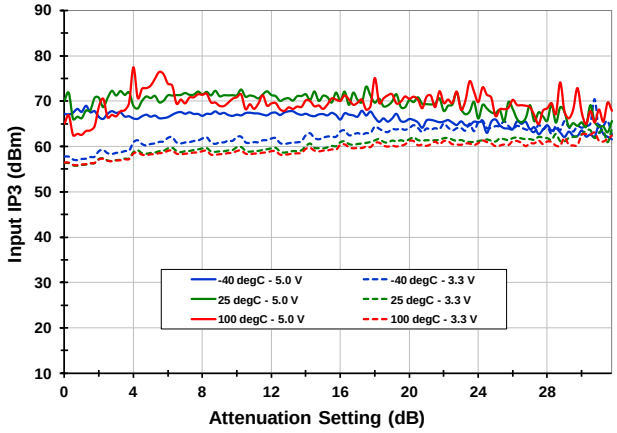
Phase vs. Attenuation Setting



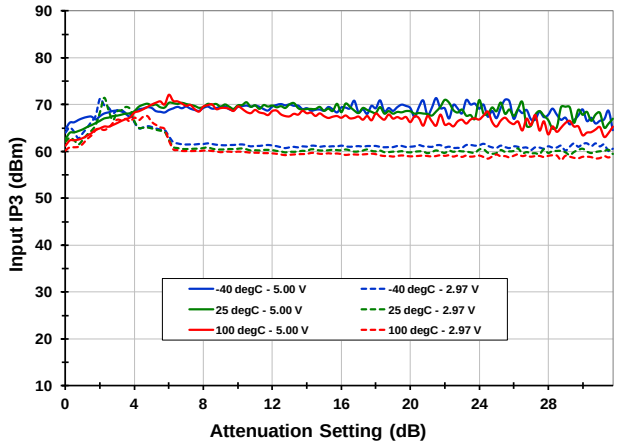
Supply Current I_{DD}



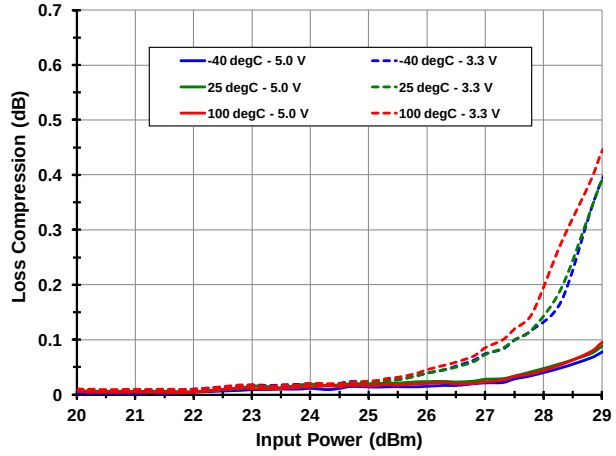
Input IP3 [f_{RF} = 900 MHz]



Input IP3 [f_{RF} = 1900 MHz]

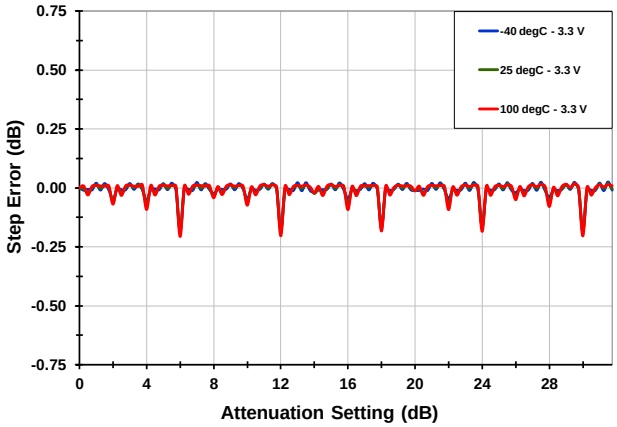


Compression [f_{RF} = 2000 MHz, ATTN = 2.5 dB]

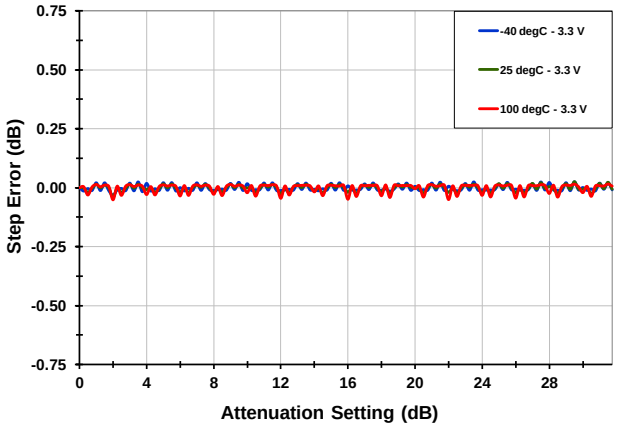


TOCs CONTINUED (-3-)

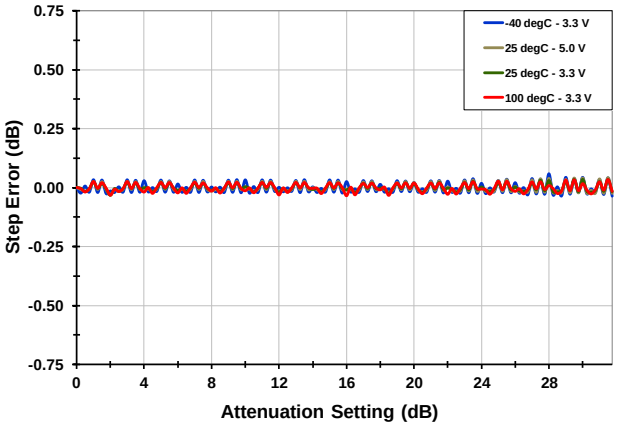
DNL [150 MHz]



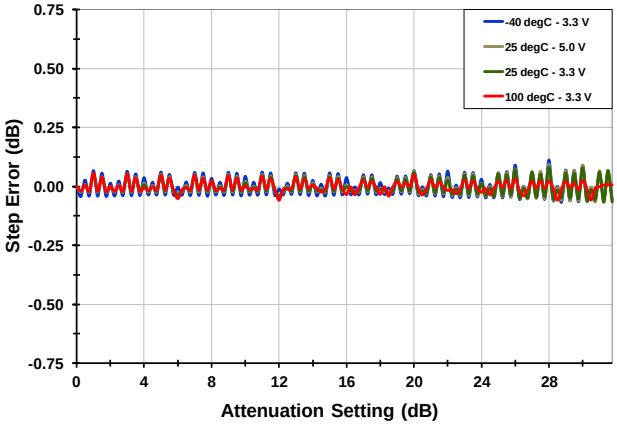
DNL [450 MHz]



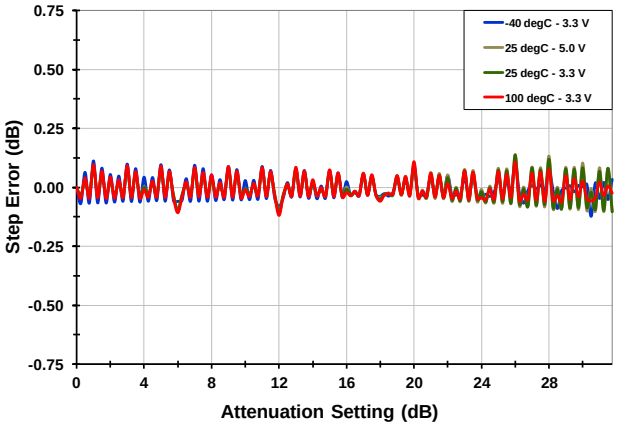
DNL [900 MHz]



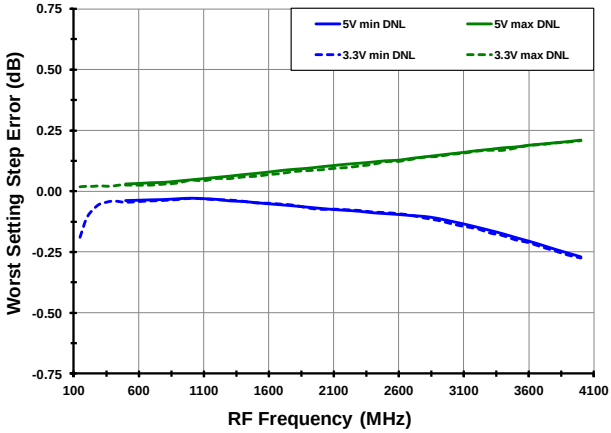
DNL [1900 MHz]



DNL [2800 MHz]

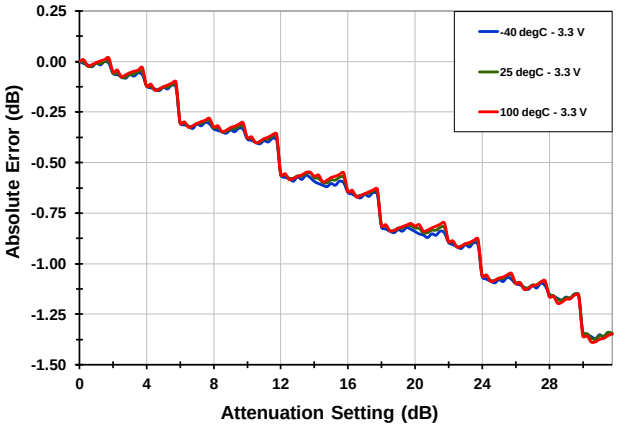


Worst Setting DNL

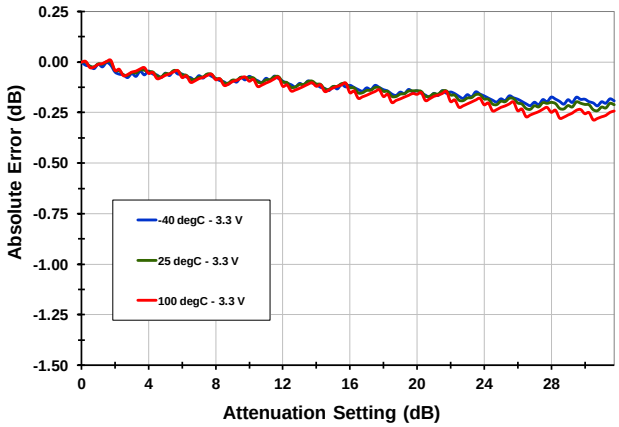


TOCs CONTINUED (-4-)

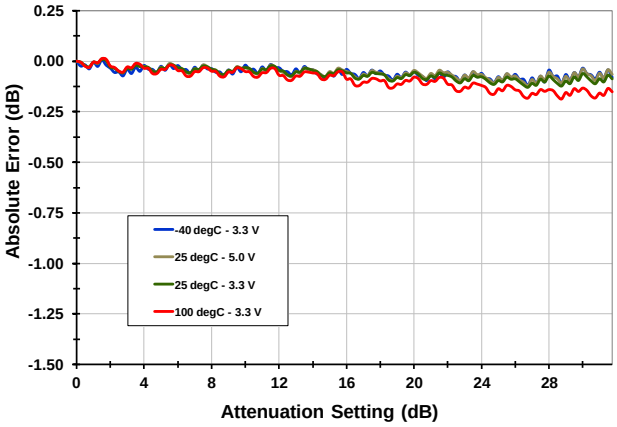
INL [150 MHz]



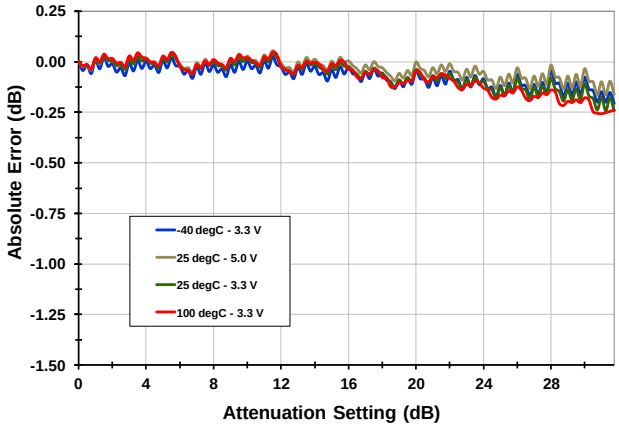
INL [450 MHz]



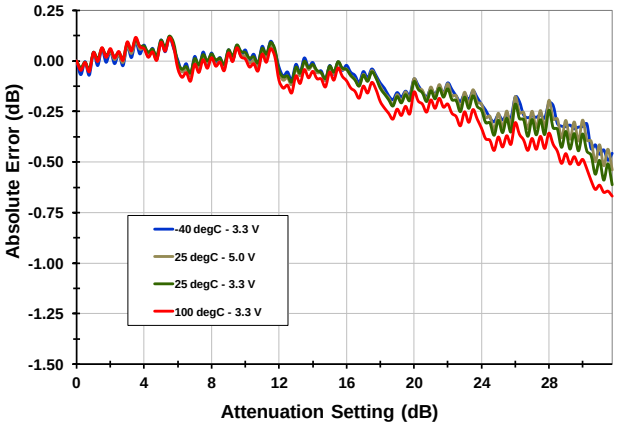
INL [900 MHz]



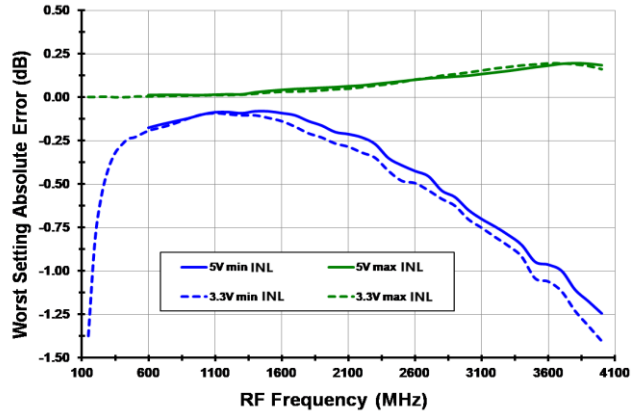
INL [1900 MHz]



INL [2800 MHz]

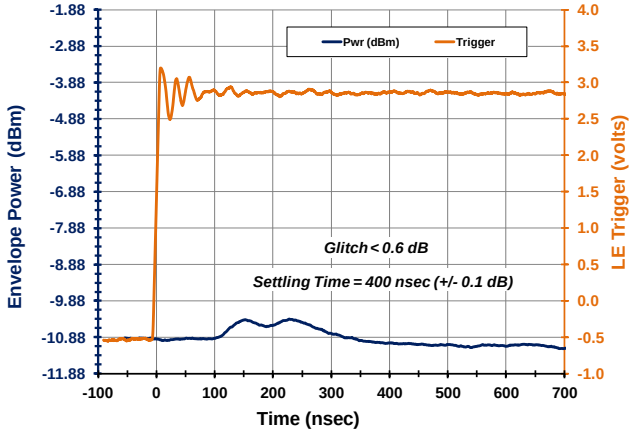


Worst Setting INL

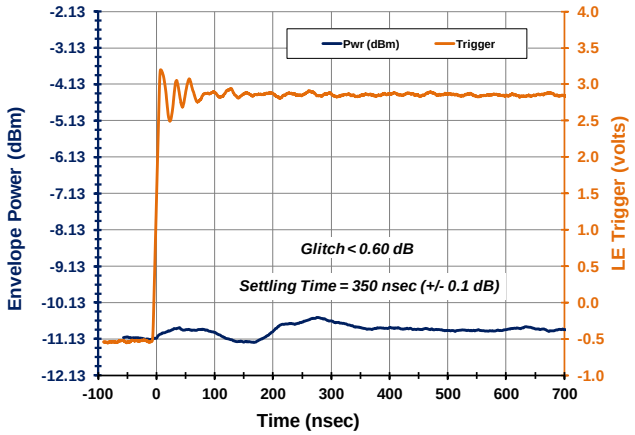


TOCs CONTINUED (-5-) [f_{RF} = 900 MHz]

Transient [15.75 to 16.00 (MSB+) 3.3V *F1950*]



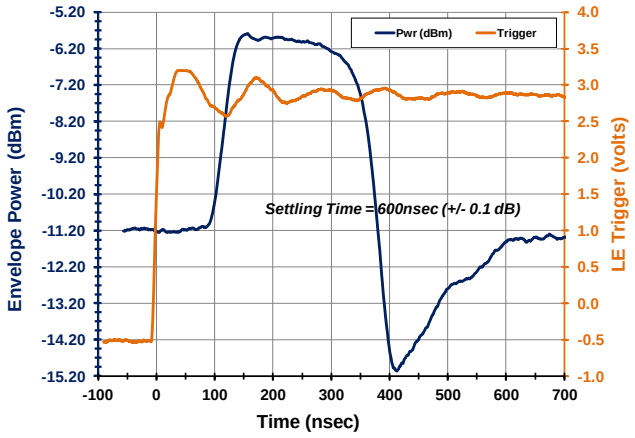
Transient [16.00 to 15.75 (MSB-) 5.0V *F1950*]



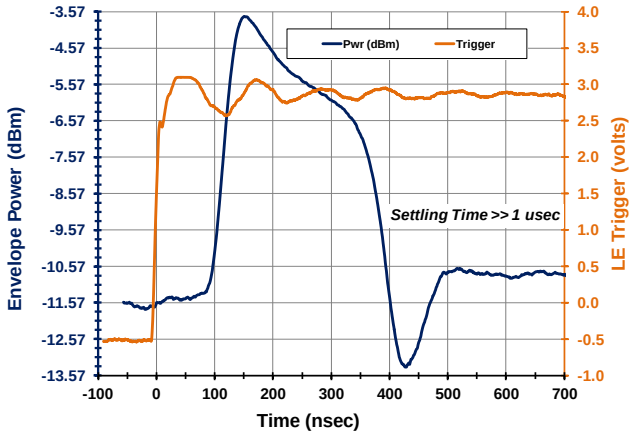
The graphs above show the transient overshoot and settling time performance for both the MSB+ and MSB- cases for the F1950. The device settles very quickly (~400) nsec with benign (~0.5) dB overshoot.

The graphs below show the transient overshoot and settling time performance for a popular competing DSA. *Note the overshoot/undershoot excursion of almost 10 dB* and the very long settling time. For the MSB- case, the settling time is off the scale, ~ 3 usec.

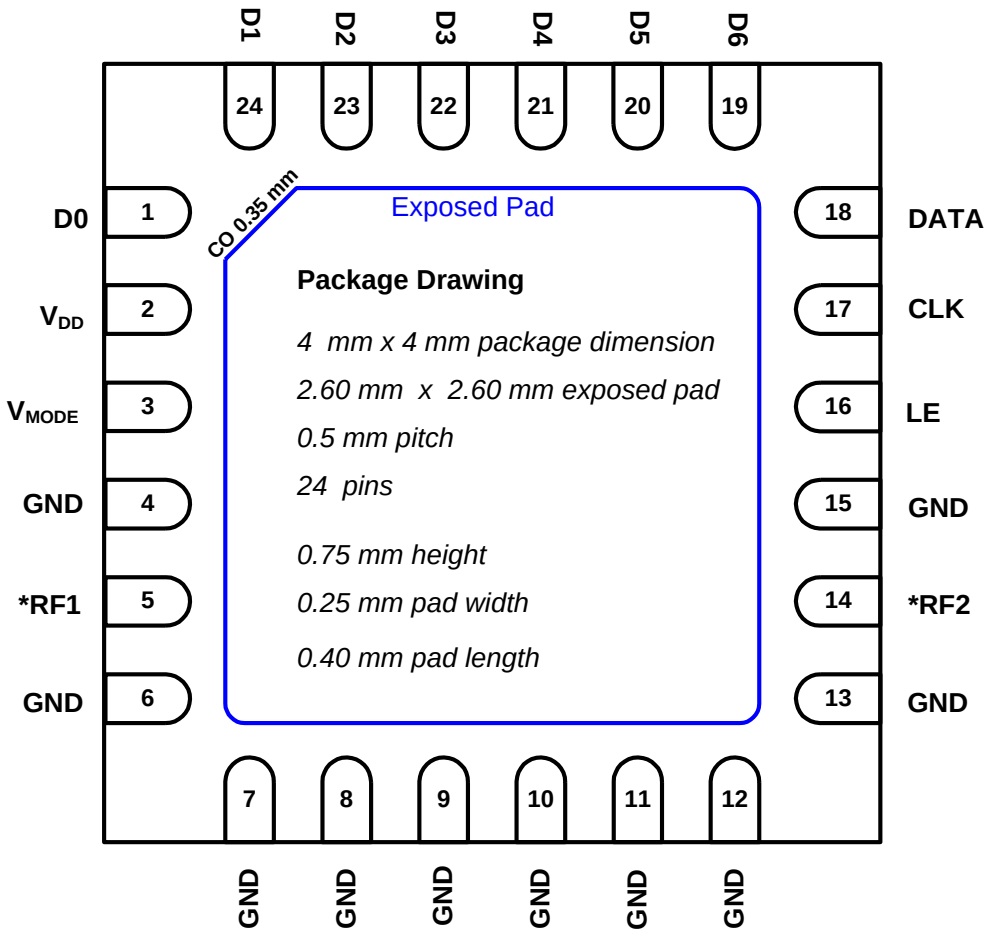
Transient [15.75 to 16.00 (MSB+) *Standard DSA*]



Transient [16.00 to 15.75 (MSB-) *Standard DSA*]



PIN DIAGRAM (F1950)



** Device is RF Bi-Directional*

PACKAGE OUTLINE DRAWING

The package outline drawings are located at the end of this document and are accessible from the link below. The package information is the most current data available.

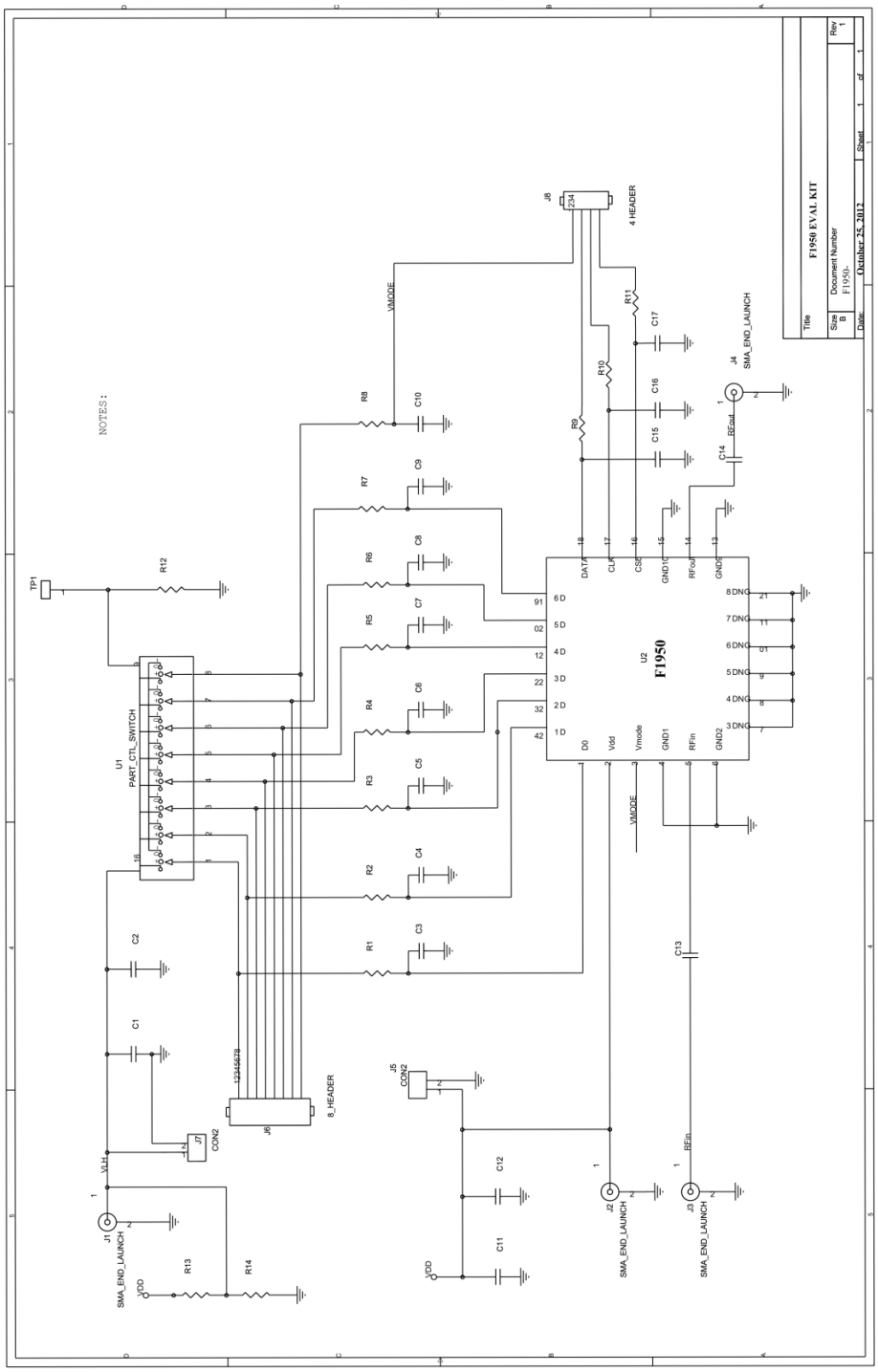
https://www.renesas.com/us/en/document/psc/24-vfqfpn-package-outline-drawing-40-x-40-x-075-mm-body-05mm-pitch-epad-26-x-26-mm-nbnbg24p2?language=en?language=en

PIN DESCRIPTIONS

Pin #	Pin Name	Pin Function
1	D0	Parallel Control – 0.25 dB attenuation step. Pull high for 0.25 dB Attenuation.
2	V_{DD}	Main Supply. Use 3.3V or 5V. Current is < 1 mA.
3	V_{MODE}	Pull low for parallel mode. Pull high or leave unconnected for serial mode.
4	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
5	RF1	Device RF input or output (bi-directional). Must AC couple to this pin.
6	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
7	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
8	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
9	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
10	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
11	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
12	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
13	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
14	RF2	Device RF input or output (bi-directional). Must AC couple to this pin.
15	GND	Connect directly to paddle ground or as close as possible to pin with thru via.
16	LE	Latch Enable. Serial Data latched into active register on rising edge.
17	CLK	Serial Clock Input
18	DATA	Serial Data Input
19	D6	Parallel Control – 16 dB attenuation step. Pull high for 16 dB Attenuation.
20	D5	Parallel Control – 8 dB attenuation step. Pull high for 8 dB Attenuation.
21	D4	Parallel Control – 4 dB attenuation step. Pull high for 4 dB Attenuation.
22	D3	Parallel Control – 2 dB attenuation step. Pull high for 2 dB Attenuation.
23	D2	Parallel Control – 1 dB attenuation step. Pull high for 1 dB Attenuation.
24	D1	Parallel Control – 0.5 dB attenuation step. Pull high for 0.5 dB Attenuation.
EP	Exposed Paddle	Connect to Ground with multiple vias for good thermal relief.

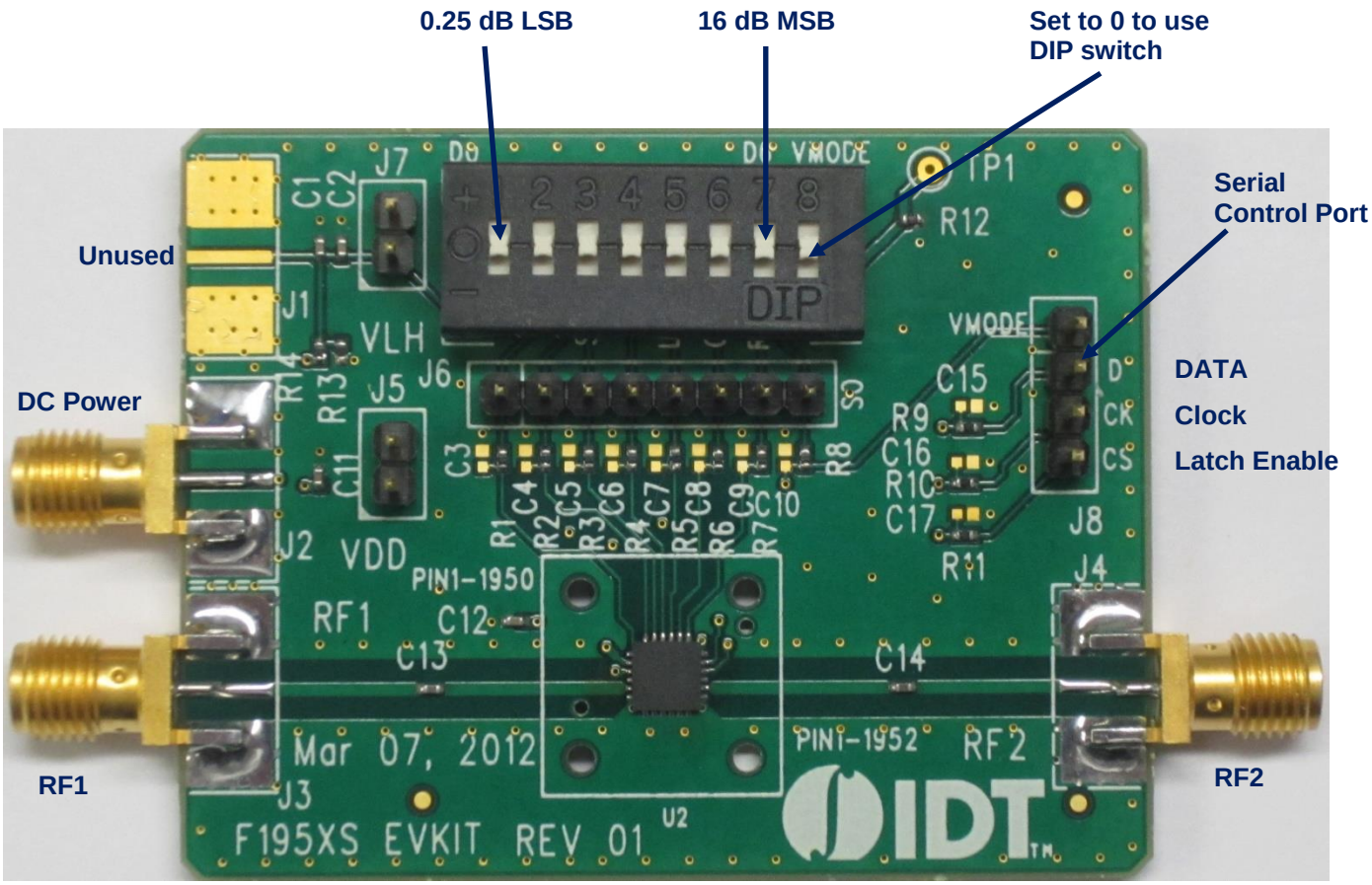
EVKIT SCHEMATIC

The diagram below describes the recommended applications / EVkit circuit:



EVKIT OPERATION

The picture and graphic below describe how to operate the Evkit.

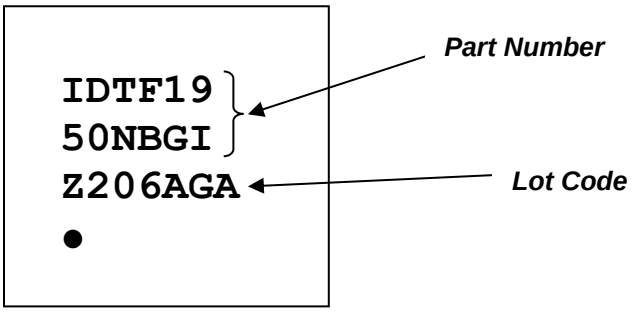


EVKIT BOM

F1950 BOM Rev 02 PCB Rev 01

Item #	Value	Size	Desc	Mfr. Part #	Mfr.	Part Reference	Qty
1	1000pF	0402	CAP CER 1000PF 50V C0G 0402	GRM1555C1H102JA01D	MURATA	C13,14	2
2	10nF	0402	CAP CER 10000PF 16V 10% X7R 0402	GRM155R71C103KA01D	MURATA	C2,12	2
3	0.1uF	0402	CAP CER 0.1UF 16V 10% X7R 0402	GRM155R71C104KA88D	MURATA	C1,11	2
4	Header 2 Pin	TH 2	CONN HEADER VERT SGL 2POS GOLD	961102-6404-AR	3M	J5,7	2
5	Header 4 Pin	TH 4	CONN HEADER VERT SGL 4POS GOLD	961104-6404-AR	3M	J8	1
6	Header 8 Pin	TH 8	CONN HEADER VERT SGL 8POS GOLD	961108-6404-AR	3M	J6	1
7	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (Small)	142-0711-821	Emerson Johnson	J2,3,4	3
8	0	0402	RES 0.0 OHM 1/10W 0402 SMD	ERJ-2GE0R00X	Panasonic	R1-8,12	9
9	3K	0402	RES 3.00K OHM 1/10W 1% 0402 SMD	ERJ-2RKF3001X	Panasonic	R9-11	3
10	100K	0402	RES 100KOHM 1/10W 0402 SMD	ERJ-2GEJ104X	Panasonic	R13,14	2
11	DIPSwitch	TH 10	8 POSITION DIP SWITCH	KAT1108E	E-Switch	U1	1
12	Digital Step Attenuator		F1950Z	F1950Z	IDT	U2	1
13	PCB		PCB Rev 01	F195XS Evkit Rev 01			1
						Total	**30**

TOP MARKING



EVKIT THROUGH-REFLECT-LINE (TRL) CALIBRATION

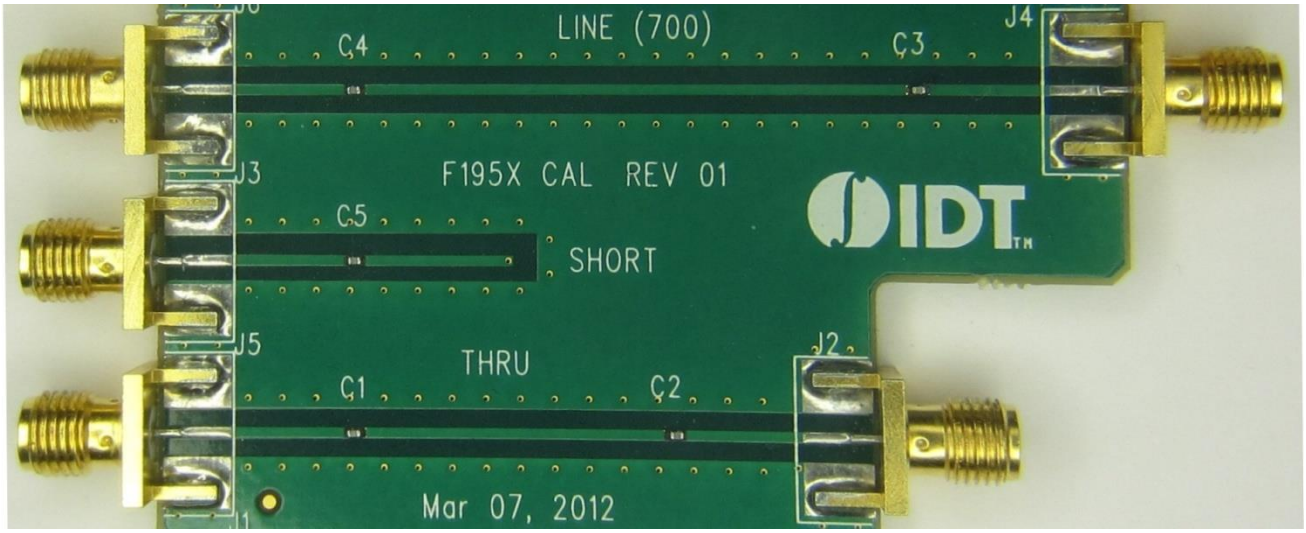
The “Through-Reflect-Line” (TRL) method [1] is used to de-embed the evaluation board losses from the S-parameter measurements of the F1950. This method requires the use of three standards: a through, a reflection, and a line. The TRL method has the advantage over other calibration methods in that it requires only one of these three standards to be well defined.

The TRL through which is used for the F1950 TRL calibration was constructed identically to the evaluation board, minus the DUT and its corresponding length. Therefore, the through corresponds to a precise zero length connection between the input and output reference planes of the DUT. This through satisfies the requirement of the TRL method that one of the three standards be precisely specified.

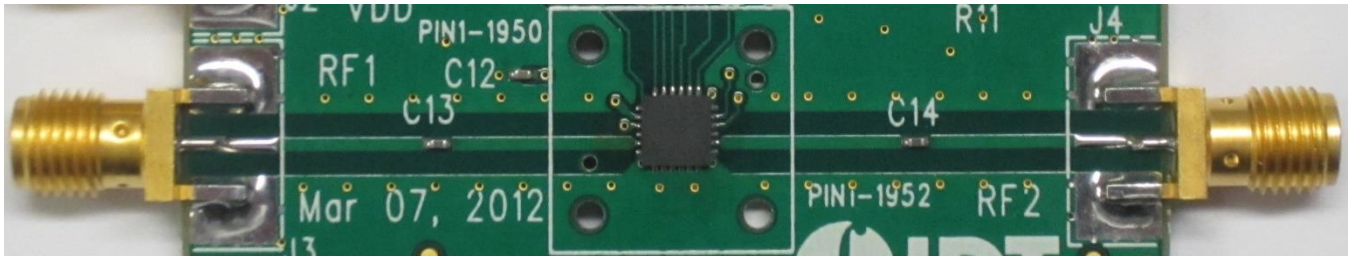
The TRL reflection standard used is constructed identically to the input and output lines of the evaluation board, with a short placed at the reference plane of the DUT. In accordance with the TRL method’s requirements, the actual magnitude and phase were not accurately specified, but the phase was known to within 90 degrees and the TRL reflection standard has a magnitude close to one.

The TRL line standard is identical to the TRL through, but with an additional length of 0.8 inches (2 cm). This satisfies the TRL method’s requirement that the TRL be a different length than the TRL through, that it have the same impedance and propagation constant as the through, and that the phase difference between the through and the line be between 20 degrees and 160 degrees. The difference in length yields a phase difference of approximately 20 degrees at 500 MHz, and a phase difference of 160 degrees at 4 GHz.

For characterization of performance from 150 to 500 MHz a separate TRL board with different “Line” length is used.



Standards used for F195x TRL calibration



F1950 evaluation circuit

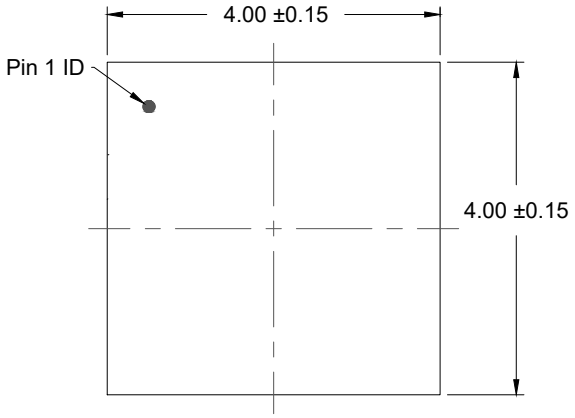
Engen, G.F.; Hoer, C.A.; “Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer,” **IEEE Transactions on Microwave Theory and Techniques**, Volume: 27 Issue:12, pp. 987 – 993, Dec 1979

REVISION HISTORY

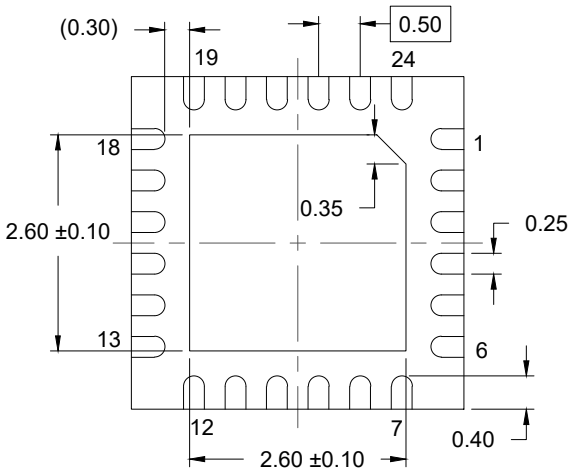
Date	Page	Description of Change
2021-Jul-12	9	Corrected "Worst Setting INL" plot error Completed other minor changes
2020-Aug-6	1,3, 12	Updated operating range max to 5GHz Updated the package outline drawings; however, no mechanical changes
2017-Jul-18	2 18	Corrected Absolute Maximum Supply Voltage. Added Revision History Sheet.
2013-Jan-15	 3 5	Corrected Footer Corrected Maximum Insertion Loss. Added Parallel Latch Diagram.
2012-Nov-04		Initial Release

Package Outline Drawing

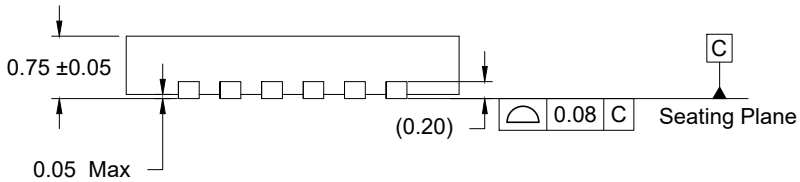
Package Code:NBG24P2
24-VFQFPN 4.0 x 4.0 x 0.75 mm Body, 0.50 mm Pitch
PSC-4313-02, Revision: 03, Date Created: Jul 20, 2023



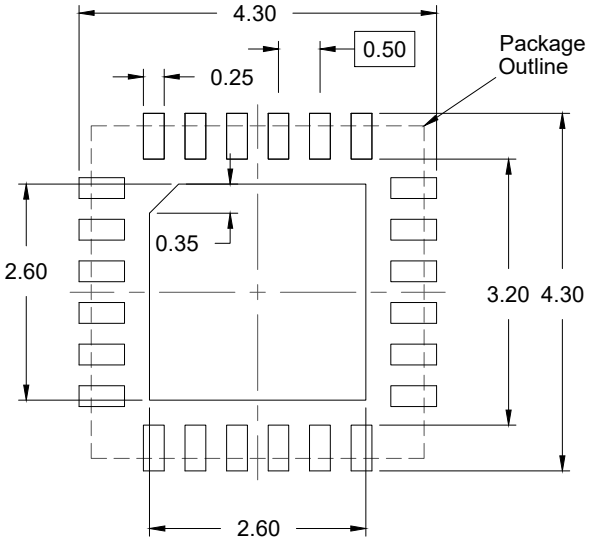
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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