

### Description

The F2251 is a low insertion loss Voltage Variable RF Attenuator (VVA) designed for a multitude of wireless and RF applications. The device covers a broad frequency range from 50MHz to 6000MHz. In addition to providing low insertion loss, the F2251 provides excellent linearity performance over its entire voltage control and attenuation range.

The F2251 uses a single positive supply voltage of 3.15V to 5.25V. Other features include an enhancement to the Phase Noise performance of the device compared to its predecessor (F2250). The device also features a positive attenuation slope only.

### Competitive Advantage

The F2251 provides extremely low insertion loss and superb IP3, IP2, Return Loss, and Slope Linearity across the control range. Comparing to the previous state-of-the-art for silicon VVAs, this device provides superior performance:

- Insertion loss at 2000MHz: 1.4dB
- Insertion loss at 6000MHz: 2.6dB
- Maximum attenuation slope: 29dB/Volt
- Minimum return loss up to 6000MHz: 14dB
- Minimum output IP3 at maximum attenuation: 34dBm
- Minimum input IP2: 95dBm
- Maximum operating temperature: +105°C

### Typical Applications

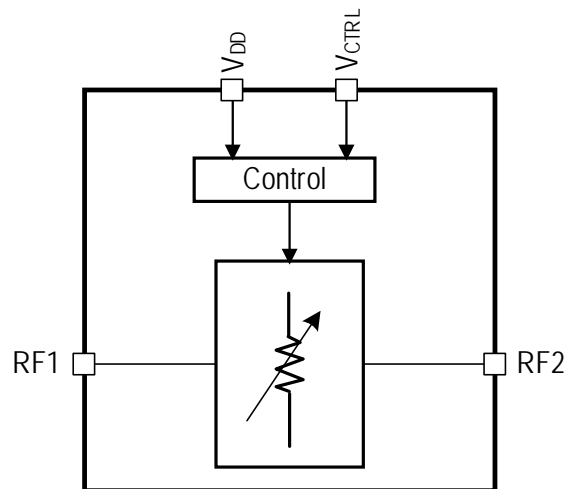
- Base station 2G, 3G, 4G
- Portable wireless
- Repeaters and E911 systems
- Digital pre-distortion
- Point-to-Point infrastructure
- Public safety infrastructure
- WIMAX receivers and transmitters
- Military systems, JTRS radios
- RFID handheld and portable readers
- Cable infrastructure
- Wireless LAN
- Test / ATE equipment

### Features

- Frequency range: 50MHz to 6000MHz
- Low insertion loss: 1.4dB at 2000MHz
- Typical/Minimum IIP3: 67dBm / 47dBm
- Typical/Minimum IIP2: 105dBm / 95dBm
- 33.6dB attenuation range
- Bi-directional RF ports
- +34.4dBm Input P1dB compression
- Enhanced phase noise performance
- Linear-in-dB attenuation characteristic
- Supply voltage: 3.15V to 5.25V
- $V_{CTRL}$  range: 0V to 3.6V using 5V supply
- +105°C maximum operating temperature
- 3 × 3 mm 16-VFQFPN package

### Block Diagram

Figure 1. Block Diagram



## Contents

|  |    |
|--|----|
| Pin Assignments.....   | 4  |
| Pin Descriptions.....  | 4  |
| Absolute Maximum Ratings.....  | 5  |
| Recommended Operating Conditions .....                                 | 6  |
| Electrical Characteristics .....                                       | 7  |
| Thermal Characteristics.....   | 8  |
| Typical Operating Conditions (TOCs).....                               | 8  |
| Typical Operating Conditions ( $V_{DD} = 3.3V$ ).....                  | 9  |
| Typical Operating Conditions ( $V_{DD} = 3.3V$ ).....                  | 10 |
| Typical Operating Conditions ( $V_{DD} = 3.3V$ ).....                  | 11 |
| Typical Operating Conditions (Frequency = 2GHz, $V_{DD} = 3.3V$ )..... | 12 |
| Typical Operating Conditions (Frequency = 2GHz, $V_{DD} = 3.3V$ )..... | 13 |
| Typical Operating Conditions ( $V_{DD} = 3.3V$ ).....                  | 14 |
| Applications Information .....   | 15 |
| $V_{CTRL}$ Pin.....  | 15 |
| Bypass Pin.....  | 15 |
| RF1 and RF2 Ports.....   | 15 |
| Power Supplies.....  | 15 |
| Control Pin Interface.....   | 16 |
| Evaluation Kit/ Applications Circuit .....                             | 17 |
| Evaluation Kit BOM .....   | 19 |
| Package Outline Drawings .....   | 19 |
| Marking Diagram .....  | 19 |
| Ordering Information.....  | 20 |
| Revision History.....  | 20 |

## List of Figures

|   |    |
|---|----|
| Figure 1. Block Diagram .....   | 1  |
| Figure 2. Pin Assignments for 3mm × 3mm 16-VFQFPN-Package – Top View..... | 4  |
| Figure 3. Maximum RF Input Power vs. RF Frequency.....                    | 6  |
| Figure 4. Attenuation .....   | 9  |
| Figure 5. Attenuation Slope .....   | 9  |
| Figure 6. Input Return Loss .....   | 9  |
| Figure 7. Output Return Loss .....  | 9  |
| Figure 8. Insertion Phase $\Delta$ .....                                  | 9  |
| Figure 9. Insertion Phase Slope .....                                     | 9  |
| Figure 10. Attenuation .....  | 10 |
| Figure 11. Attenuation Slope .....  | 10 |

Figure 12. Input Return Loss .....10

Figure 13. Output Return Loss .....10

Figure 14. Insertion Phase  $\Delta$  .....10

Figure 15. Insertion Phase Slope .....10

Figure 16. Input Return Loss (vs Temperature).....11

Figure 17. Input Return Loss (vs Frequency) .....11

Figure 18. Output Return Loss (vs Temperature) .....11

Figure 19. Output Return Loss (vs Frequency) .....11

Figure 20. Insertion Phase  $\Delta$  (vs Temperature).....11

Figure 21. Insertion Phase Slope (vs Frequency).....11

Figure 22. Input IP3 .....12

Figure 23. Output IP3 .....12

Figure 24. Input IP2 .....12

Figure 25. Output IP2 .....12

Figure 26. 2<sup>nd</sup> Harmonic Intercept Point .....12

Figure 27. 3<sup>rd</sup> Harmonic Intercept Point .....12

Figure 28. Input IP3 .....13

Figure 29. Output IP3 .....13

Figure 30. Input IP2 .....13

Figure 31. Output IP2 .....13

Figure 32. 2<sup>nd</sup> Harmonic Intercept Point .....13

Figure 33. 3<sup>rd</sup> Harmonic Intercept Point .....13

Figure 34. 1dB Compression .....14

Figure 35. Phase Noise at 350MHz, 0dBm and Frequency Offset = 1kHz.....14

Figure 36. Min and Max Attenuation.....14

Figure 37. Min and Max Attenuation Slope.....14

Figure 38. Attenuation vs. Frequency.....14

Figure 39. Control Pin Interface Diagram .....16

Figure 40. Evaluation Kit Applications Circuit Diagram.....17

Figure 41. Evaluation Kit Picture / Layout (Top Side) .....18

Figure 42. Evaluation Kit Picture / Layout (Bottom Side).....18

## List of Tables

Table 1. Pin Descriptions.....4

Table 2. Absolute Maximum Ratings.....5

Table 3. Recommended Operating Conditions .....6

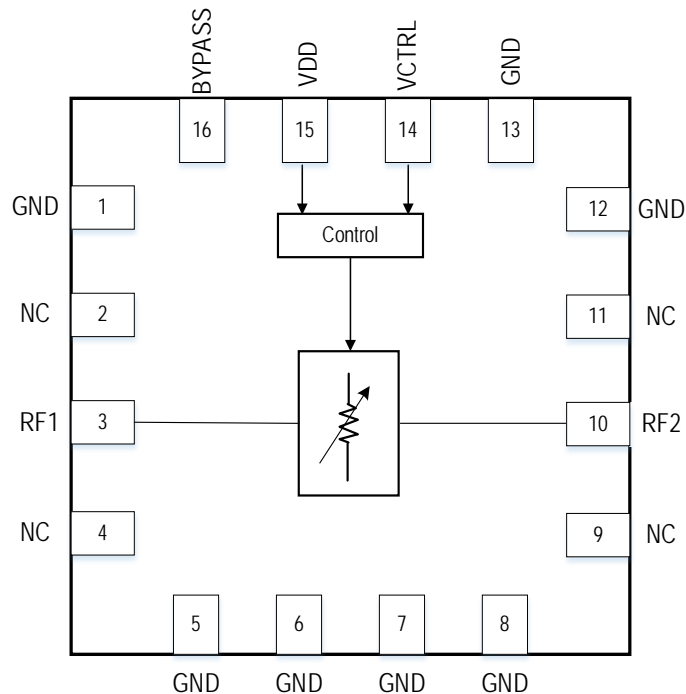
Table 4. Electrical Characteristics .....7

Table 5. Thermal Characteristics.....8

Table 6. Evaluation Kit Bill-of Materials (BOM).....19

## Pin Assignments

Figure 2. Pin Assignments for 3 × 3 mm 16-VFQFPN-Package – Top View



## Pin Descriptions

Table 1. Pin Descriptions

| Pin Number            | Name   | Description  |
|-----------------------|--------|--|
| 1, 5, 6, 7, 8, 12, 13 | GND    | Ground these pins as close to the device as possible.  |
| 2, 4, 9, 11           | NC     | No internal connection. These pins can be left unconnected or connected to ground (recommended).   |
| 3                     | RF1    | RF port 1. Matched to 50 ohms. Must use an external AC coupling capacitor as close to the device as possible. For low frequency operation, increase the capacitor value to result in a low reactance at the frequency of interest. |
| 10                    | RF2    | RF port 2. Matched to 50 ohms. Must use an external AC coupling capacitor as close to the device as possible. For low frequency operation, increase the capacitor value to result in a low reactance at the frequency of interest. |
| 14                    | VCTRL  | Attenuator control voltage. Apply a voltage in the range as specified in the Operating Conditions. See application section for details about $V_{CTRL}$ .  |
| 15                    | VDD    | Power supply input. Bypass to GND with capacitors close as possible to pin.  |
| 16                    | BYPASS | Bypass to GND with capacitors close as possible to the pin. This pin works with an internal resistor and thereby adds low pass filtering.  |
|                       | EP     | Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to achieve the specified RF performance.   |

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F2251 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

| Symbol              | Parameter   | Conditions                                | Minimum | Maximum                            | Units |
|---------------------|---|---|---------|------------------------------------|-------|
| V <sub>DD</sub>     | V <sub>DD</sub> to GND                              |   | -0.3    | 5.5                                | V     |
| V <sub>CTRL</sub>   | V <sub>CTRL</sub> to GND                            | V <sub>DD</sub> = 0V to 5.25V             | -0.3    | Minimum<br>(V <sub>DD</sub> , 4.0) | V     |
| V <sub>RF</sub>     | RF1, RF2 to GND                                     |   | -0.3    | 0.3                                | V     |
| P <sub>MAX24</sub>  | RF1 or RF2 Input Power applied for 24 hours maximum | V <sub>DD</sub> applied at 2GHz and +85°C |         | 30                                 | dBm   |
| P <sub>MAX_OP</sub> | RF1 or RF2 Continuous Operating Power               |   |         | See Figure 3                       | dBm   |
| T <sub>JMAX</sub>   | Maximum Junction Temperature                        |   |         | +150                               | °C    |
| T <sub>ST</sub>     | Storage Temperature Range                           |   | -65     | +150                               | °C    |
| T <sub>LEAD</sub>   | Lead Temperature                                    | Soldering, 10s                            |         | +260                               | °C    |
| V <sub>ESDHBM</sub> | ESD Voltage–HBM (Per ESD STM5.1-2007)               |   |         | 1000                               | V     |
| V <sub>ESDCDM</sub> | ESD Voltage–CDM (Per ESD STM5.3.1-2009)             |   |         | 250                                | V     |

## Recommended Operating Conditions

Table 3. Recommended Operating Conditions

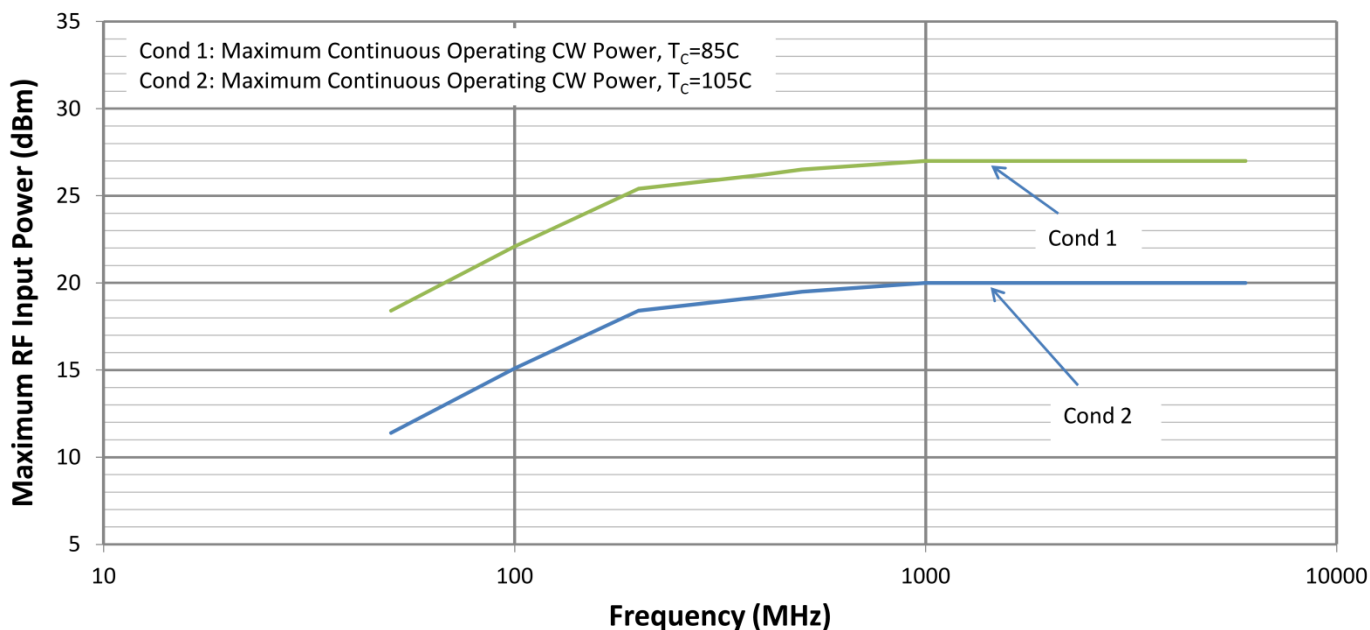
| Symbol        | Parameter                   | Conditions                 | Minimum        | Typical | Maximum      | Units       |
|---------------|-----------------------------|----------------------------|----------------|---------|--------------|-------------|
| $f_{RF}$      | Operating Frequency Range   |                            | 50             |         | 6000         | MHz         |
| $V_{DD}$      | Supply Voltage              |                            | 3.15           |         | 5.25         | V           |
| $V_{CTRL}$    | $V_{CTRL}$ Range            | $V_{DD} = 3.9V$ to $5.25V$ | 0              |         | 3.6          | V           |
|               |                             | $V_{DD} = 3.15V$ to $3.9V$ | 0              |         | $V_{DD}-0.3$ |             |
| $I_{DD}$      | Supply Current              |                            | <b>0.1</b> [a] | 0.8     | <b>2</b>     | mA          |
| $I_{CTRL}$    | $I_{CTRL}$ Current          |                            | <b>-1</b>      |         | <b>14</b>    | $\mu A$     |
| $P_{MAX, CW}$ | RF Operating Power [c]      |                            |                |         | See Figure 3 | dBm         |
| $Z_{RF1}$     | RF1 Port Impedance          |                            |                | 50      |              | $\Omega$    |
| $Z_{RF2}$     | RF2 Port Impedance          |                            |                | 50      |              |             |
| $T_{CASE}$    | Operating Temperature Range | Exposed paddle temperature | -40            |         | +105         | $^{\circ}C$ |

[a] Items in min/max columns in **bold italics** are guaranteed by test.

[b] Items in min/max columns that are not bold italics are guaranteed by design characterization.

[c] Refer to Figure 3.

Figure 3. Maximum RF Input Power vs. RF Frequency



## Electrical Characteristics

Refer to the Evaluation Kit/ Applications Circuit.  $V_{DD} = +3.3V$ ,  $T_C = +25^\circ C$ . The specifications in this table apply at RF1 input,  $f_{RF} = 2000MHz$ , minimum attenuation,  $P_{IN} = 0dBm$  for small signal parameters,  $+20dBm$  for single tone linearity tests,  $+20dBm$  per tone for two tone tests, two tone delta frequency =  $50MHz$ , PCB board traces and connector losses are de-embedded unless otherwise noted. Refer to Typical Operating Curves for performance over entire frequency band.

Table 4. Electrical Characteristics

| Parameter  | Symbol                | Conditions  | Minimum           | Typical | Maximum                  | Units     |
|--|-----------------------|---|-------------------|---------|--------------------------|-----------|
| Insertion Loss, IL<br>(minimum attenuation)              | $A_{MIN}$             | $f_{RF} = 2GHz$   |                   | 1.4     | <b>1.9<sup>[a]</sup></b> | dB        |
|  |                       | $f_{RF} = 3GHz$   |                   | 1.6     |                          |           |
|  |                       | $f_{RF} = 6GHz$   |                   | 2.6     | 3.1                      |           |
| Maximum Attenuation                                      | $A_{MAX}$             |   | 34 <sup>[b]</sup> | 35      |                          | dB        |
| Insertion Phase $\Delta$                                 | $\Phi_{\Delta MAX}$   | At 36dB attenuation relative to insertion loss  |                   | 28      |                          | deg       |
|  | $\Phi_{\Delta MID}$   | At 18dB attenuation relative to insertion loss  |                   | 20      |                          |           |
| Input 1dB Compression <sup>[c]</sup>                     | P1dB                  |   |                   | 34.4    |                          | dBm       |
| Minimum RF1 Return Loss<br>over Control Voltage<br>Range | S11                   | $f_{RF} = 50MHz$ <sup>[d]</sup>   |                   | 16      |                          | dB        |
|  |                       | $f_{RF} = 700MHz$   |                   | 17      |                          |           |
|  |                       | $f_{RF} = 2000MHz$  |                   | 17      |                          |           |
|  |                       | $f_{RF} = 6000MHz$  |                   | 15      |                          |           |
| Minimum RF2 Return Loss<br>over Control Voltage<br>Range | S22                   | $f_{RF} = 50MHz$  |                   | 16      |                          | dB        |
|  |                       | $f_{RF} = 700MHz$   |                   | 15      |                          |           |
|  |                       | $f_{RF} = 2000MHz$  |                   | 16      |                          |           |
|  |                       | $f_{RF} = 6000MHz$  |                   | 13      |                          |           |
| Input IP3  | IIP3                  |   |                   | 67      |                          | dBm       |
| Input IP3 over Attenuation                               | IIP3 <sub>ATTEN</sub> | All attenuation settings  | 44                | 47      |                          |           |
| Minimum Output IP3                                       | OIP3 <sub>MIN</sub>   | Maximum attenuation   |                   | 34      |                          |           |
| Input IP2  | IIP2                  | $P_{IN} + IM2_{dBC}$ , IM2 term is F1+F2  |                   | 105     |                          | dBm       |
| Minimum Input IP2  | IIP2 <sub>MIN</sub>   | All attenuation settings  |                   | 95      |                          | dBm       |
| Input IH2  | HD2                   | $P_{IN} + H2_{dBC}$   |                   | 107     |                          | dBm       |
| Input IH3  | HD3                   | $P_{IN} + (H3_{dBC}/2)$   |                   | 70      |                          | dBm       |
| Settling Time  | $T_{SETTL0.1dB}$      | Any 1dB step in the 0dB to 33dB control range<br>50% $V_{CTRL}$ to RF settled to within $\pm 0.1dB$ |                   | 15      |                          | $\mu sec$ |

[a] Items in minimum/maximum columns in bold italics are guaranteed by test.

[b] Items in minimum/maximum columns that are not bold/italics are guaranteed by design characterization.

[c] The input 1dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section along with Figure 3 for the maximum RF input power vs. RF frequency.

[d] Set blocking capacitors C7 and C8 to  $0.01\mu F$  to achieve best return loss performance at 50MHz.

## Thermal Characteristics

Table 5. Thermal Characteristics

| Symbol        | Parameter  | Value | Units                       |
|---------------|--|-------|-----------------------------|
| $\theta_{JA}$ | Theta JA. Junction to ambient.                                     | 80.6  | $^{\circ}\text{C}/\text{W}$ |
| $\theta_{JC}$ | Theta JC. Junction to case (case is defined as the exposed paddle) | 5.1   | $^{\circ}\text{C}/\text{W}$ |
|               | Moisture Sensitivity Rating (per J-STD-020)                        | MSL 1 |                             |

## Typical Operating Conditions (TOCs)

Unless otherwise noted:

- $V_{DD} = +3.3\text{V}$  or  $+5.0\text{V}$
- $T_C = +25^{\circ}\text{C}$
- $P_{IN} = 0\text{dBm}$  for all small signal tests
- $P_{IN} = +20\text{dBm}$  for single tone linearity tests (RF1 port driven)
- $P_{IN} = +20\text{dBm}/\text{tone}$  for two tone linearity tests (RF1 port driven)
- Two tone frequency spacing =  $50\text{MHz}$
- RF trace and connector losses are de-embedded for S-parameters



# Typical Operating Conditions ( $V_{DD} = 3.3V$ )

Figure 4. Attenuation

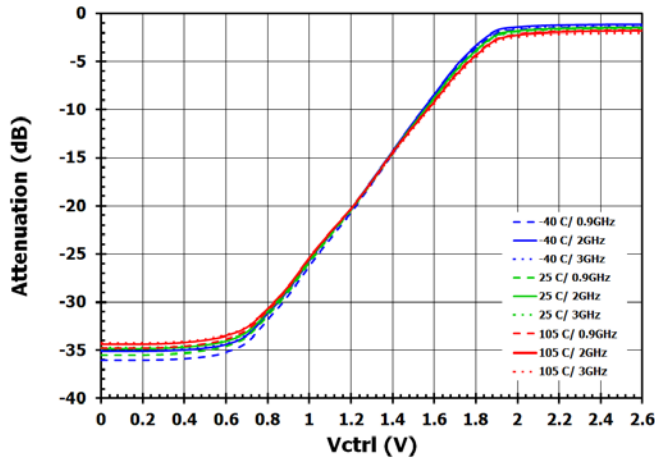


Figure 5. Attenuation Slope

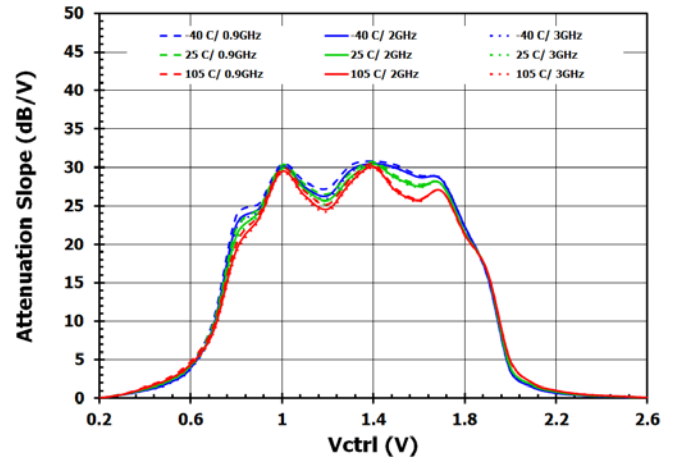


Figure 6. Input Return Loss

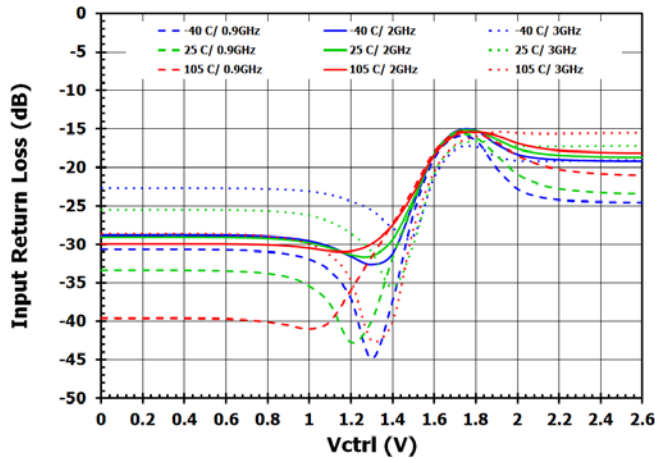


Figure 7. Output Return Loss

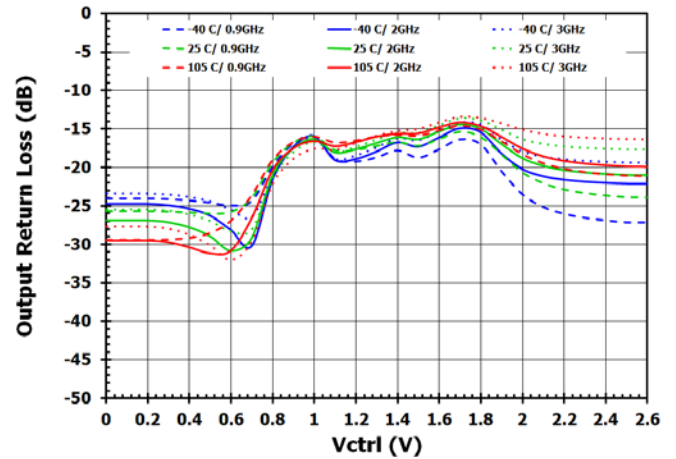


Figure 8. Insertion Phase  $\Delta$

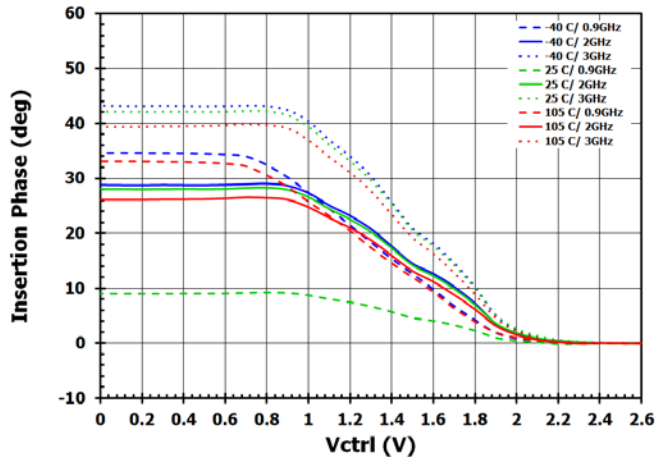
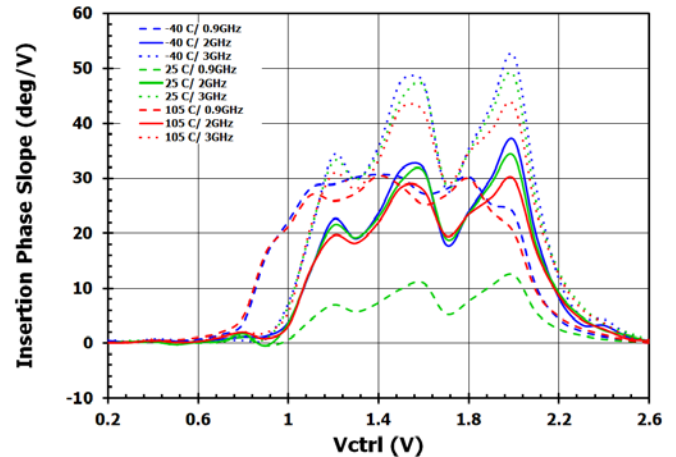


Figure 9. Insertion Phase Slope



# Typical Operating Conditions ( $V_{DD} = 3.3V$ )

Figure 10. Attenuation

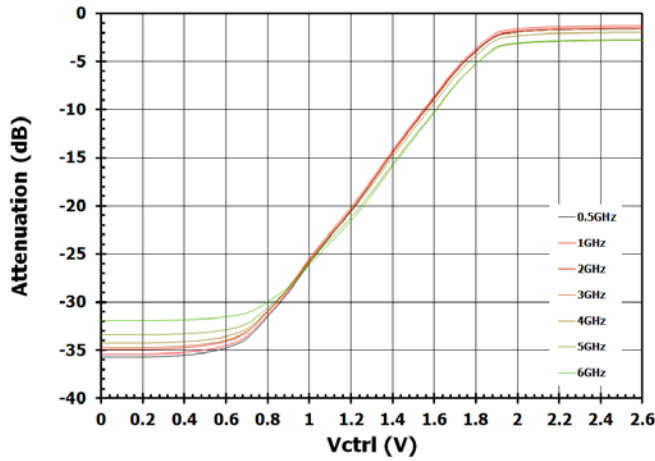


Figure 11. Attenuation Slope

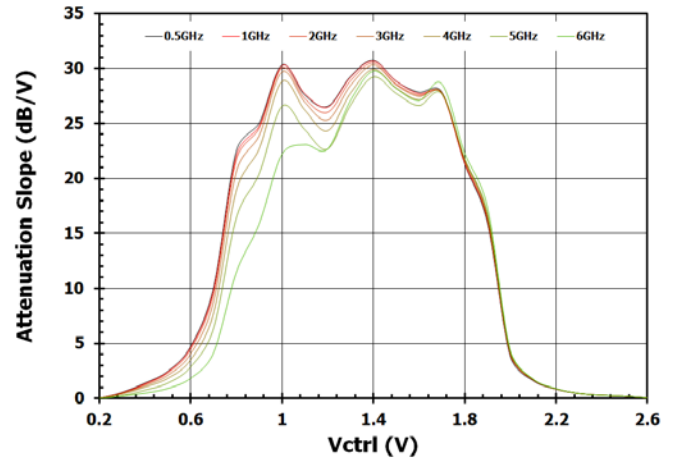


Figure 12. Input Return Loss

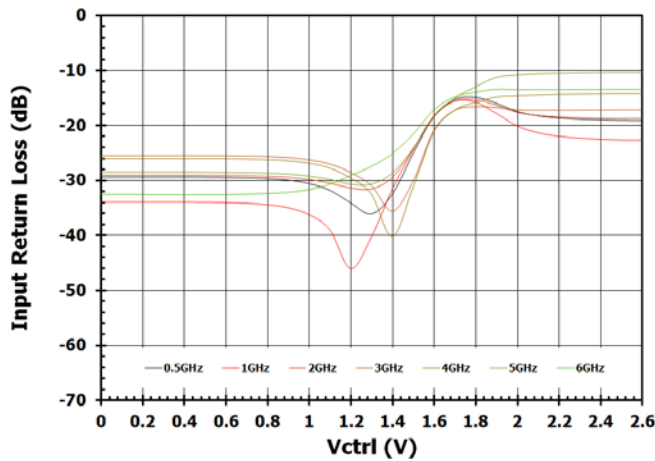


Figure 13. Output Return Loss

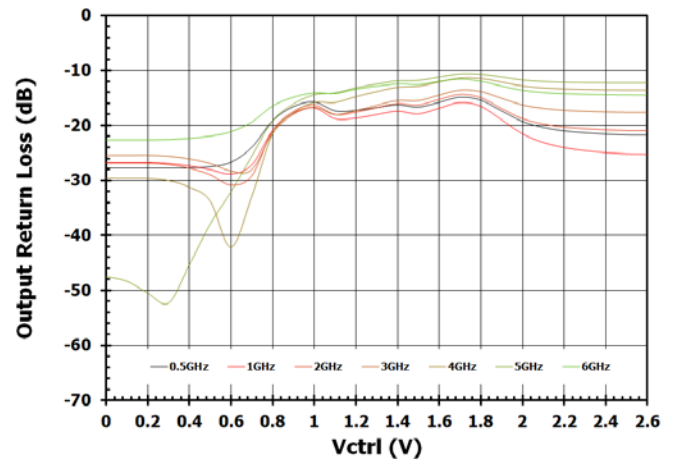


Figure 14. Insertion Phase  $\Delta$

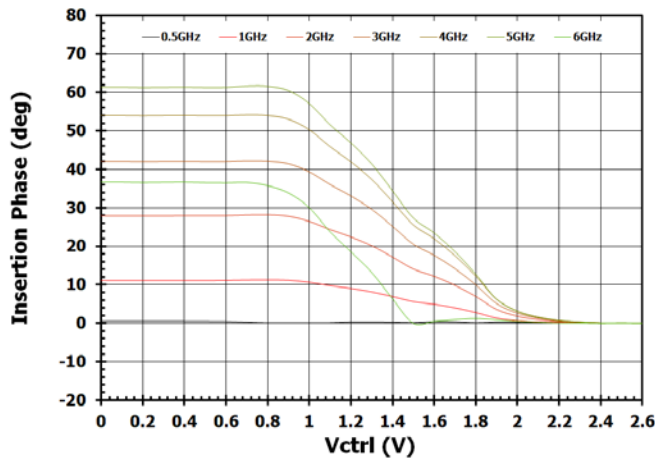
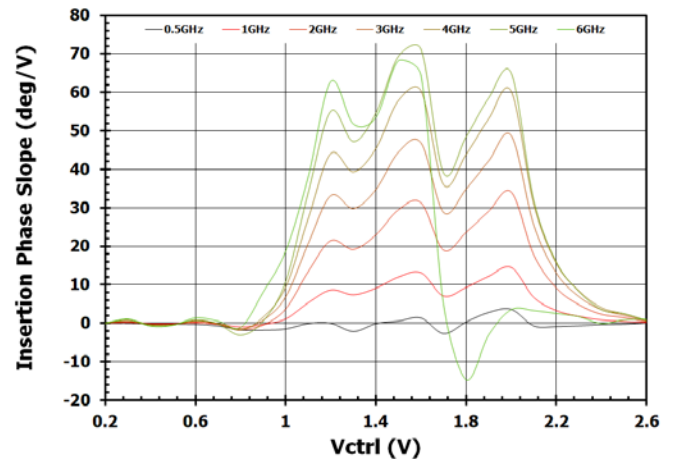


Figure 15. Insertion Phase Slope



## Typical Operating Conditions ( $V_{DD} = 3.3V$ )

Figure 16. Input Return Loss (vs Temperature)

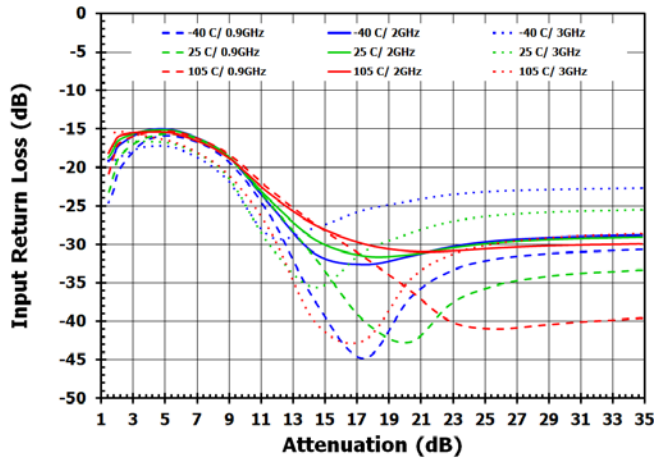


Figure 17. Input Return Loss (vs Frequency)

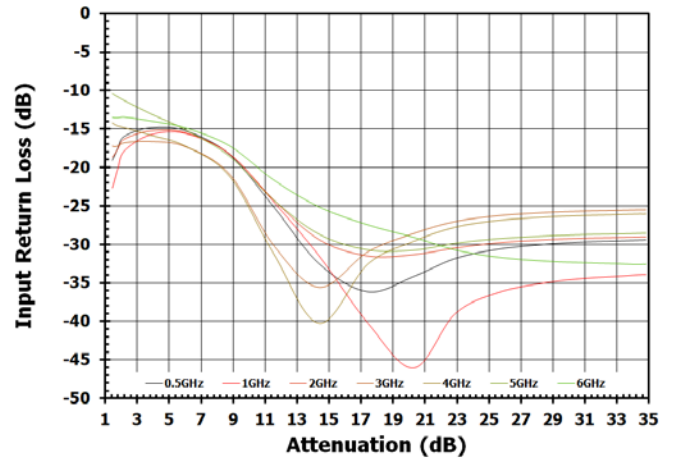


Figure 18. Output Return Loss (vs Temperature)

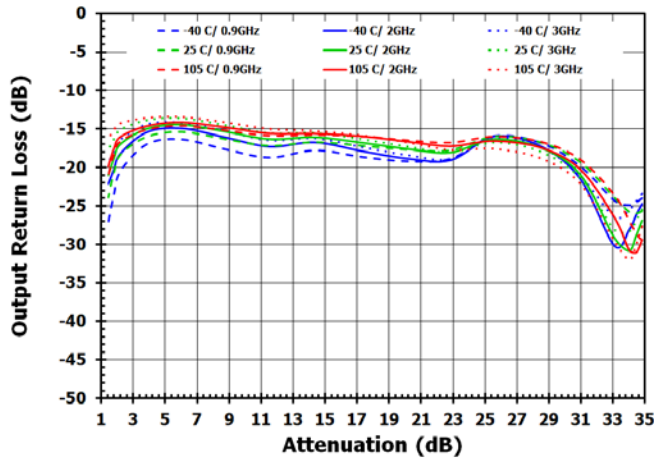


Figure 19. Output Return Loss (vs Frequency)

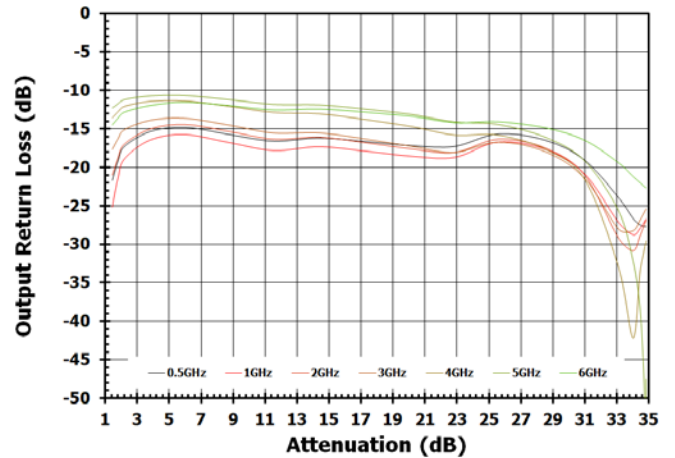


Figure 20. Insertion Phase  $\Delta$  (vs Temperature)

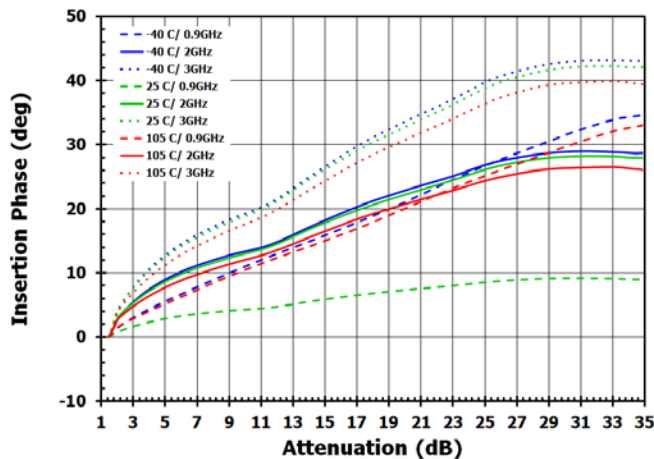
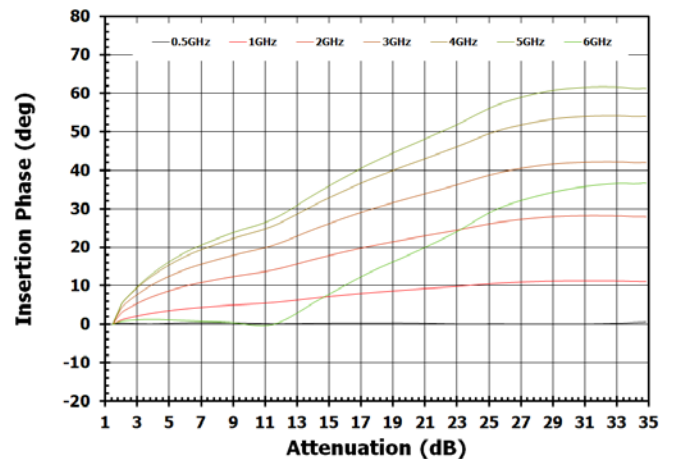


Figure 21. Insertion Phase Slope (vs Frequency)



# Typical Operating Conditions (Frequency = 2GHz, $V_{DD} = 3.3V$ )

Figure 22. Input IP3

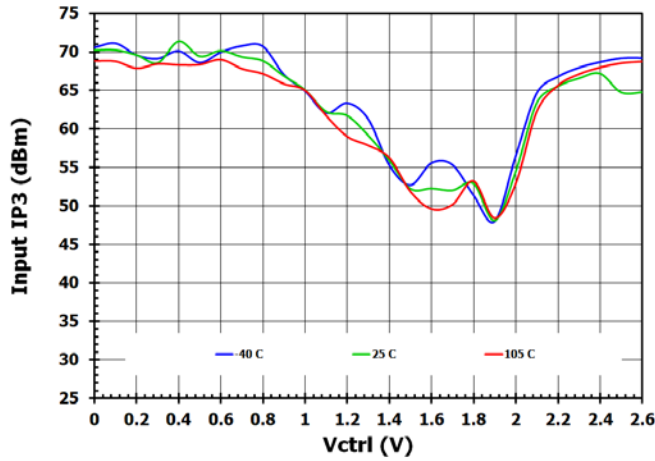


Figure 23. Output IP3

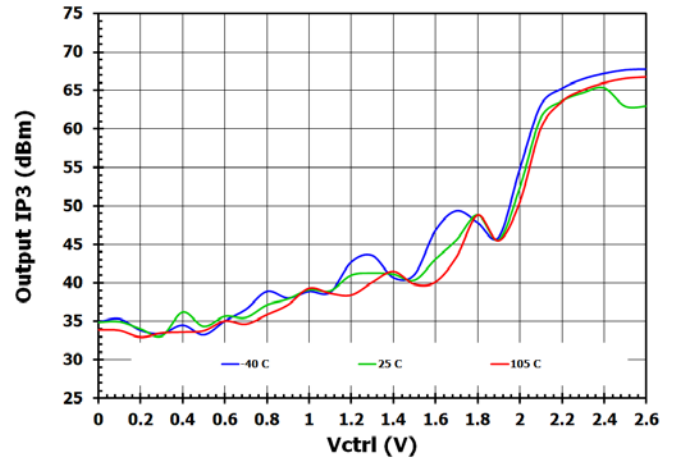


Figure 24. Input IP2

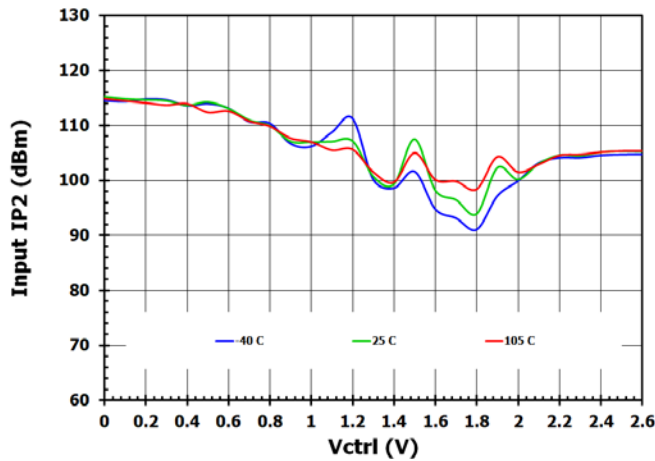


Figure 25. Output IP2

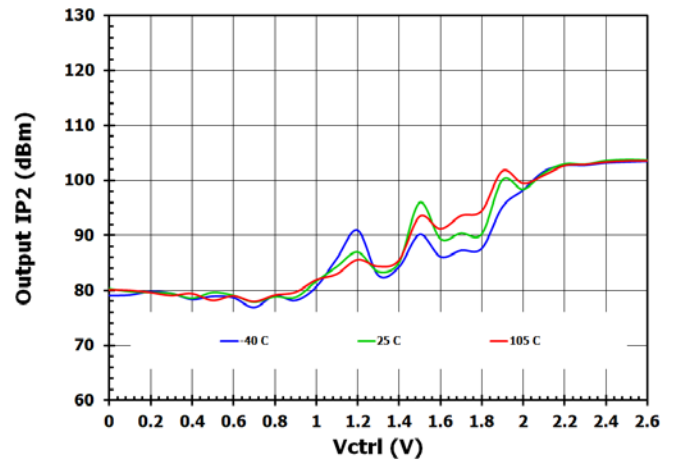


Figure 26. 2<sup>nd</sup> Harmonic Intercept Point

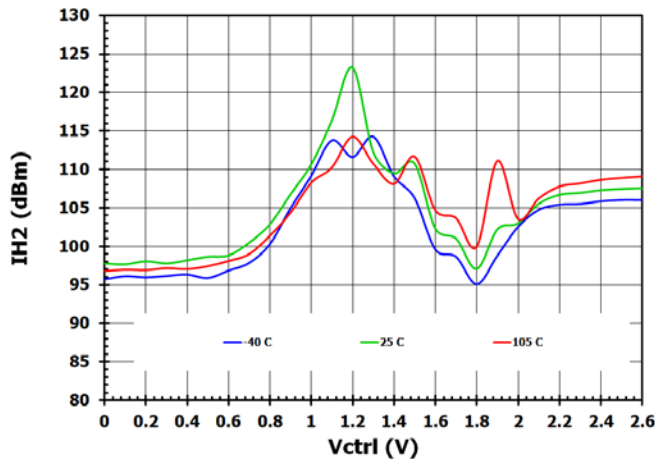
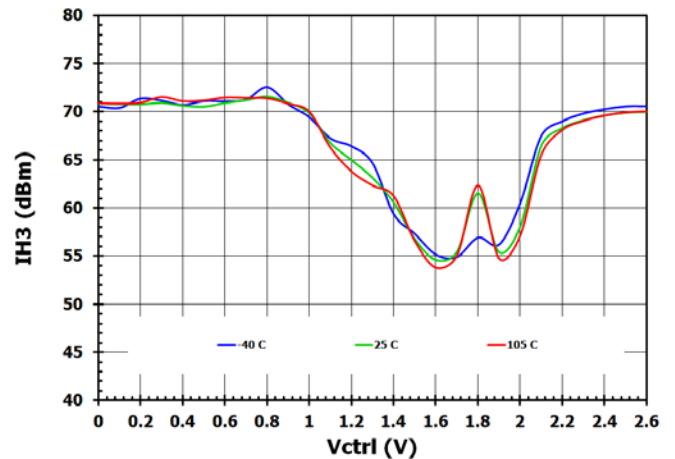


Figure 27. 3<sup>rd</sup> Harmonic Intercept Point



# Typical Operating Conditions (Frequency = 2GHz, $V_{DD} = 3.3V$ )

Figure 28. Input IP3

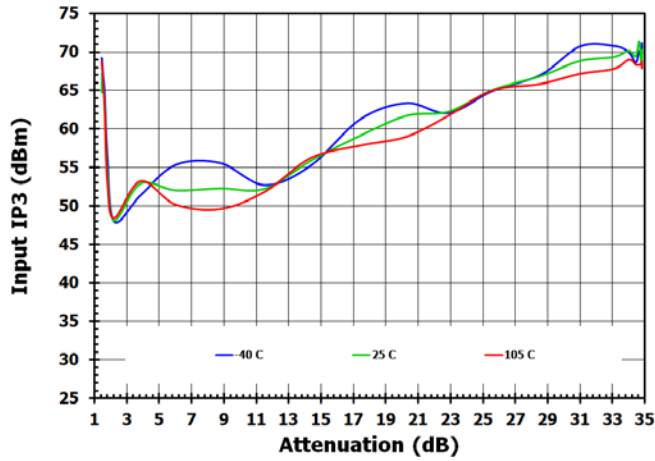


Figure 29. Output IP3

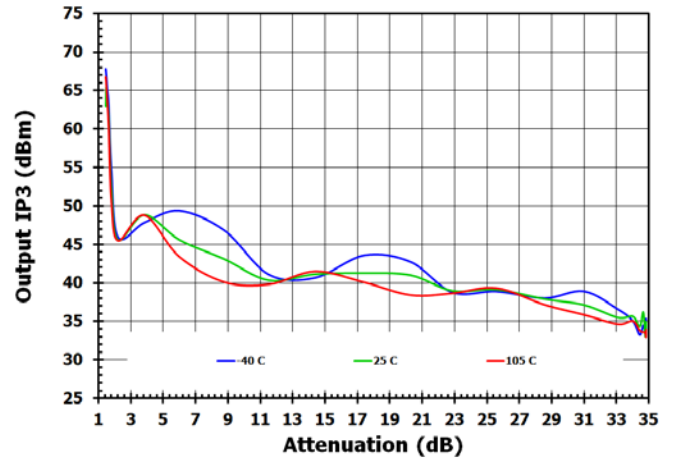


Figure 30. Input IP2

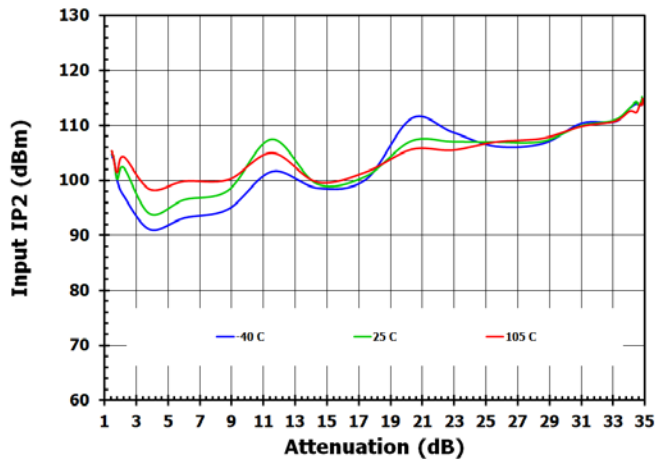


Figure 31. Output IP2

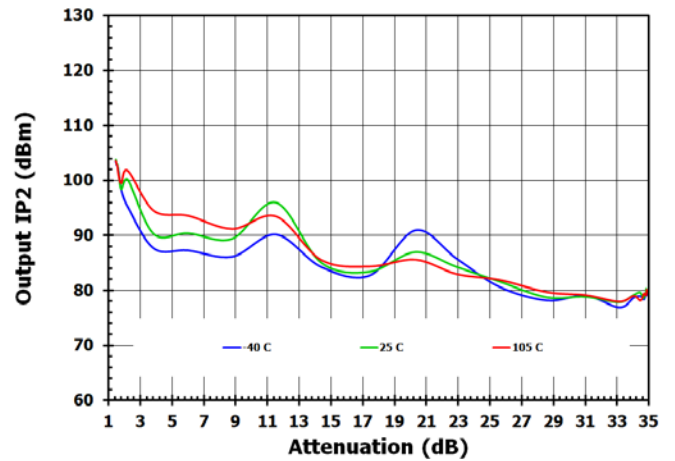


Figure 32. 2<sup>nd</sup> Harmonic Intercept Point

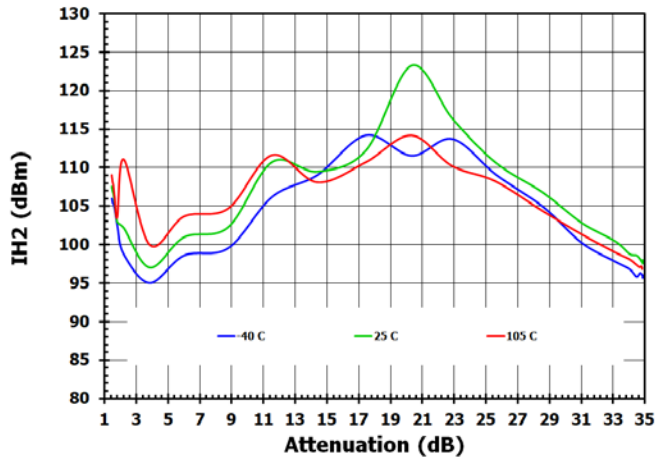
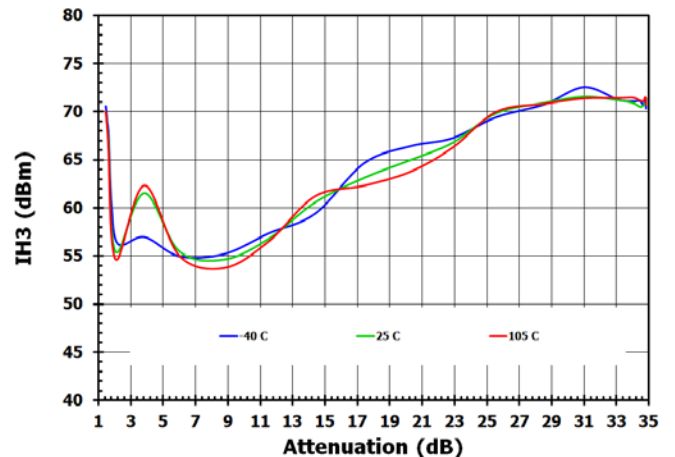


Figure 33. 3<sup>rd</sup> Harmonic Intercept Point



## Typical Operating Conditions ( $V_{DD} = 3.3V$ )

Figure 34. 1dB Compression

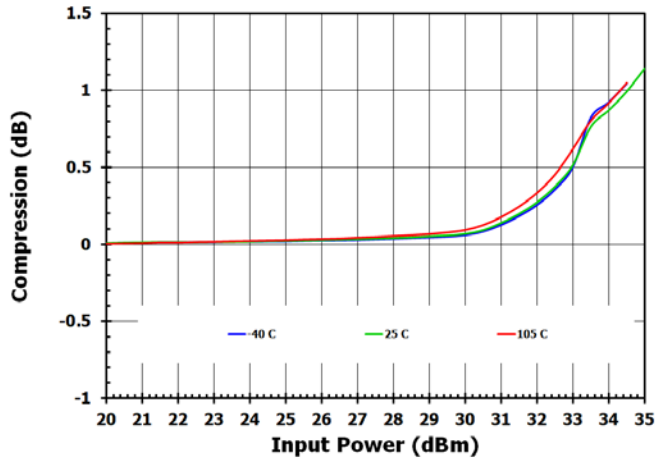


Figure 35. Phase Noise at 350MHz, 0dBm and Frequency Offset = 1kHz

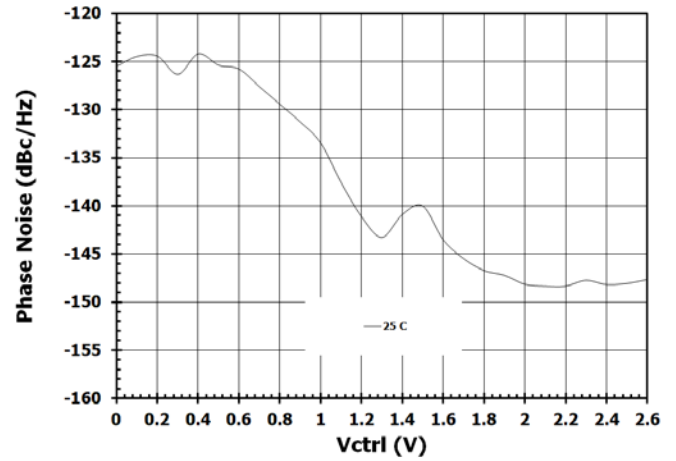


Figure 36. Min and Max Attenuation

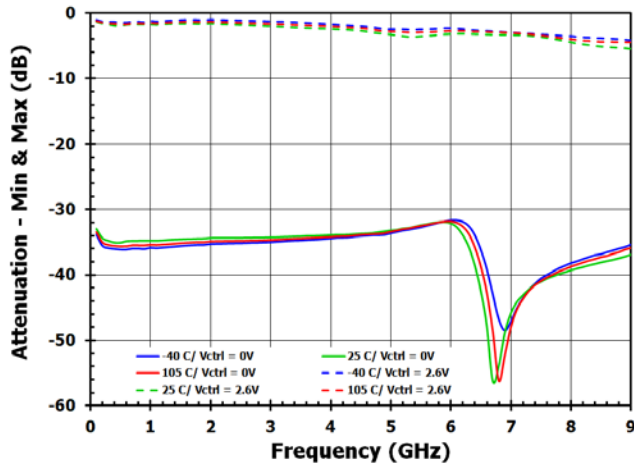


Figure 37. Min and Max Attenuation Slope

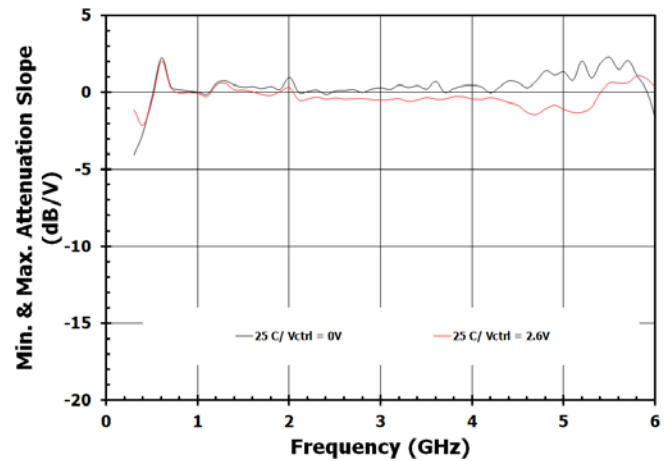
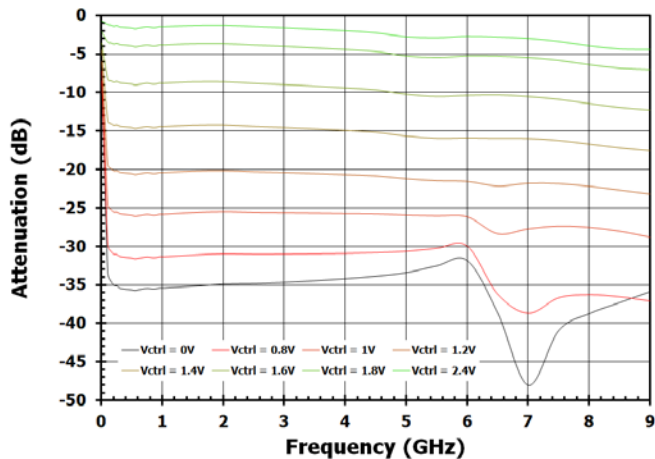


Figure 38. Attenuation vs. Frequency



## Applications Information

### $V_{CTRL}$ Pin

The  $V_{CTRL}$  pin controls the attenuation of the F2251. The  $V_{CTRL}$  pin has an on-chip pull-up ESD diode so  $V_{DD}$  should be applied before  $V_{CTRL}$  is applied. If this sequencing is not possible, then resistor R2 should be set for  $1k\Omega$  to limit the current into the  $V_{CTRL}$  pin.

### Bypass Pin

Bypass to GND with capacitors close as possible to the pin. This pin works with an internal resistor and thereby adds low pass filtering. For more information, see Figure 40.

### RF1 and RF2 Ports

The F2251 is a bi-directional device thus allowing RF1 or RF2 to be used as the RF input. As displayed in the Typical Operating Conditions curves, RF1 shows some enhanced linearity performance and therefore should be used as the RF input, if possible, for best results. This F2251 has been designed to accept high RF input power levels, therefore  $V_{DD}$  must be applied prior to the application of RF power to ensure reliability. DC blocking capacitors are required on the RF pins and should be set to a value that results in a low reactance over the frequency range of interest.

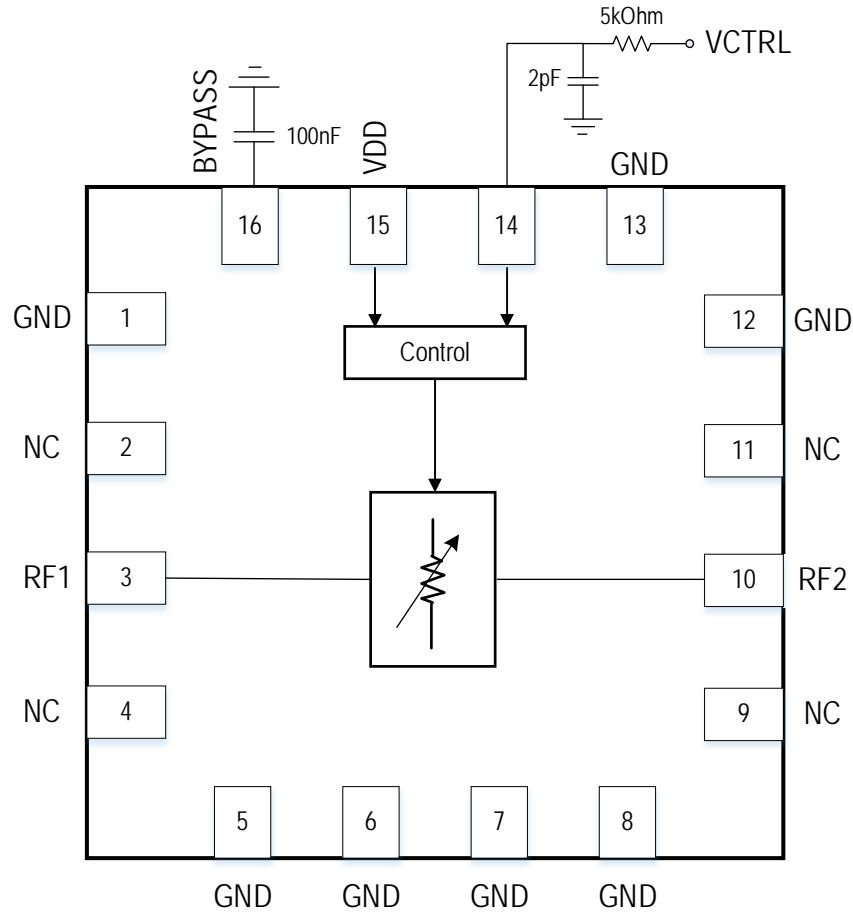
### Power Supplies

The supply pin should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than  $1V/20\mu s$ . In addition, all control pins should remain at  $0V (\pm 0.3V)$  while the supply voltage ramps or while it returns to zero.

### Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of control pin 14 is recommended as shown below.

Figure 39. Control Pin Interface Diagram





# Evaluation Kit/ Applications Circuit

Figure 40. Evaluation Kit Applications Circuit Diagram

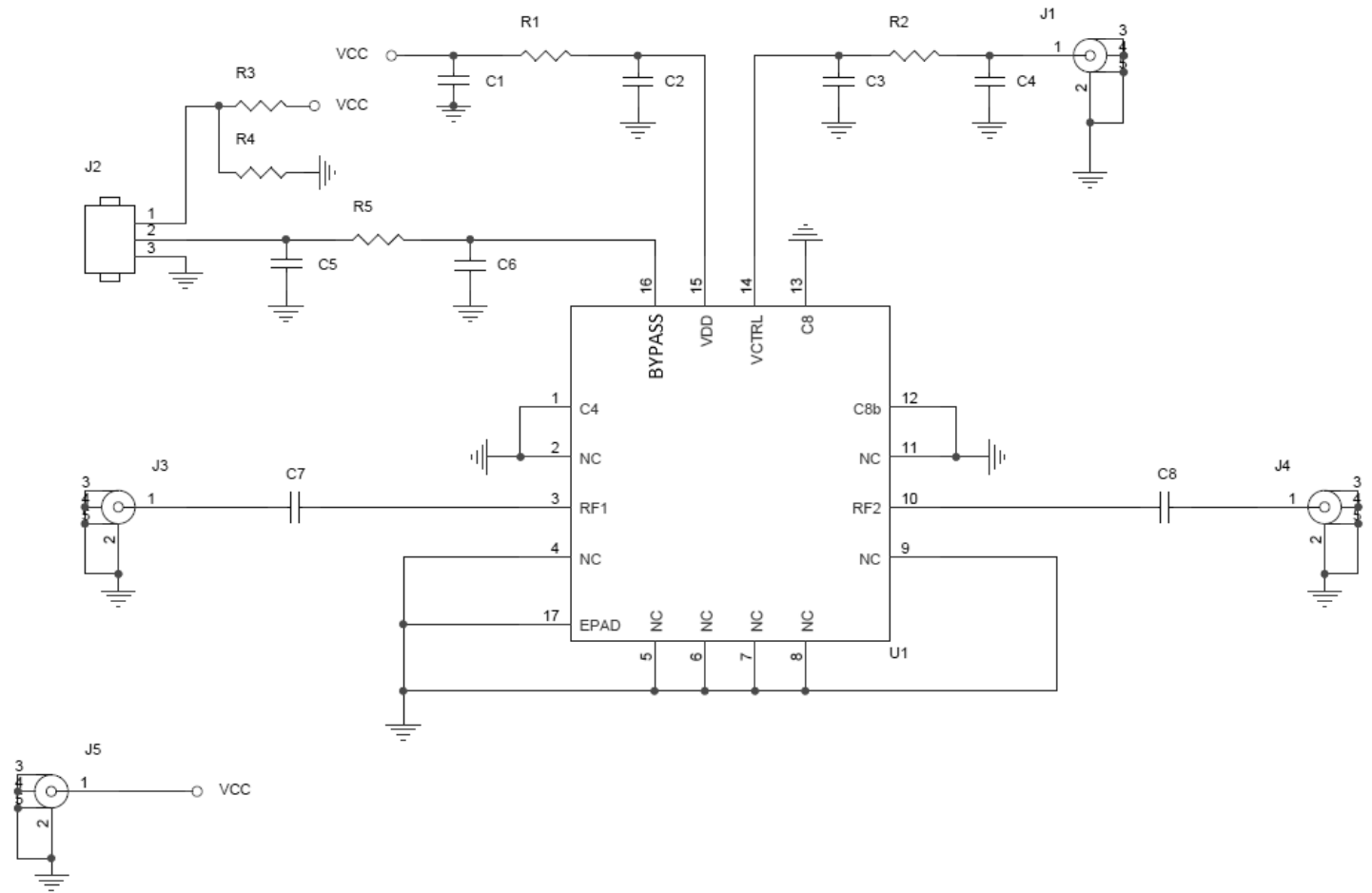


Figure 41. Evaluation Kit Picture / Layout (Top Side)

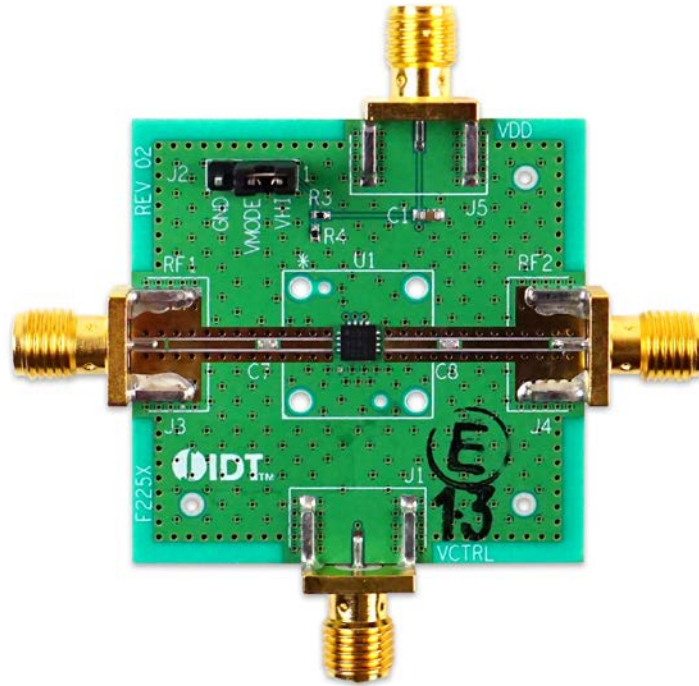
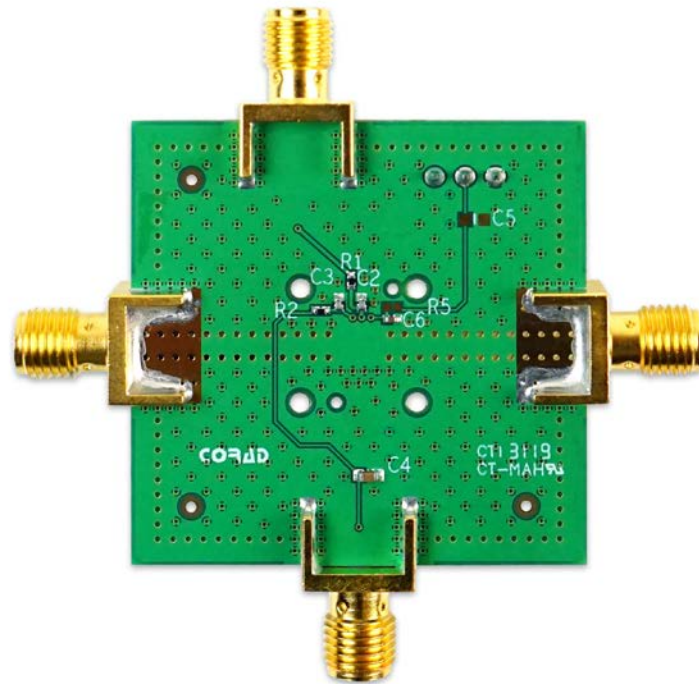


Figure 42. Evaluation Kit Picture / Layout (Bottom Side)



## Evaluation Kit BOM

Table 6. Evaluation Kit Bill-of Materials (BOM)

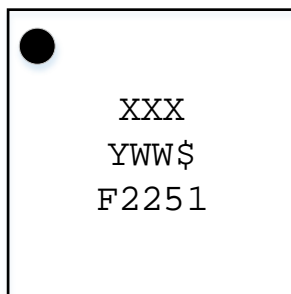
| Part Reference | Quantity | Description                                    | Manufacturer Part Number | Manufacturer    |
|----------------|----------|--|--------------------------|-----------------|
| C1, C4         | 2        | 10nF ±5%, 50V, X7R Ceramic Capacitors (0603)   | GRM188R71H103J           | Murata          |
| C2, C3, C7, C8 | 4        | 1000pF ±5%, 50V, C0G Ceramic Capacitors (0402) | GRM1555C1H102J           | Murata          |
| C6             | 1        | 0.1uF ±10%, 16V, X7R Ceramic Capacitors (0402) | GRM155R71C104K           | Murata          |
| R1, R2         | 2        | 0Ω Resistors (0402)                            | ERJ-2GE0R00X             | Panasonic       |
| R3, R4         | 2        | 100kΩ ±1%, 1/10W, Resistor (0402)              | ERJ-2RKF1003X            | Panasonic       |
| R5, C5         | 2        | DNP  |                          |                 |
| J1, J2, J3, J4 | 4        | Edge Launch SMA (0.375 inch pitch ground tabs) | 142-0701-851             | Emerson Johnson |
|                | 1        | Printed Circuit Board                          | F225x Rev (02)           | IDT (Renesas)   |

## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

<https://www.idt.com/document/psc/16-vfqfjn-package-outline-drawing-30-x-30-x-09-mm-05-mm-170-x-170-mm-epad-nlnlg16p2>

## Marking Diagram



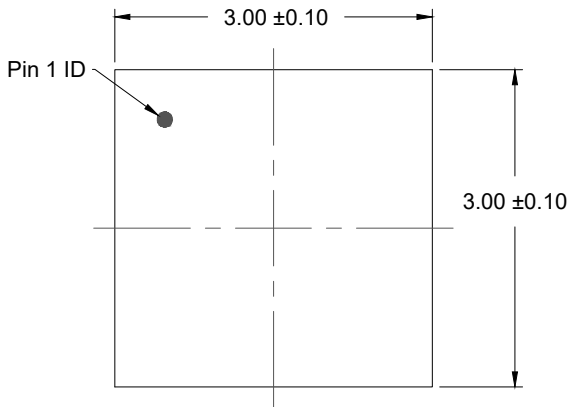
- Line 1 is the last 3 characters of the ASM lot number
- Line 2:
  - “YWW” is the last digit of the year and week that the part was assembled.
  - “\$” denotes the mark code.
- Line 3 is the truncated part number.

## Ordering Information

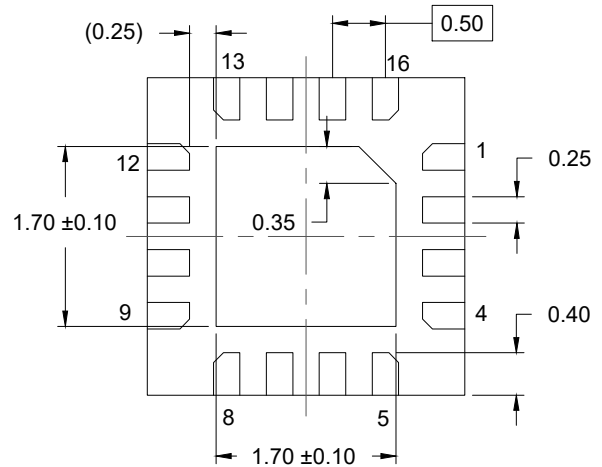
| Orderable Part Number | Description and Package      | MSL Rating | Carrier Type | Temperature     |
|-----------------------|------------------------------|------------|--------------|-----------------|
| F2251NLGI             | 3.0 × 3.0 × 0.9 mm 16-VFQFPN | 1          | Tray         | -40°C to +105°C |
| F2251NLG8             | 3.0 × 3.0 × 0.9 mm 16-VFQFPN | 1          | Reel         | -40°C to +105°C |
| F2251EVB              | Evaluation Board             |            |              |                 |

## Revision History

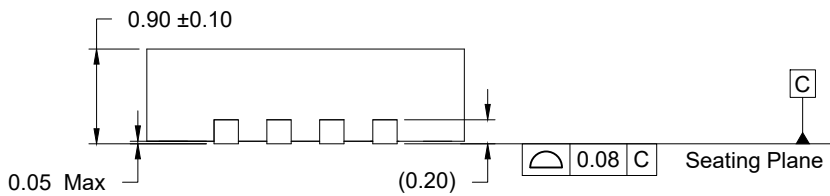
| Revision Date     | Description of Change               |
|-------------------|-------------------------------------|
| February 18, 2020 | Replotting Insertion phase figures. |
| February 14, 2020 | Initial release.                    |



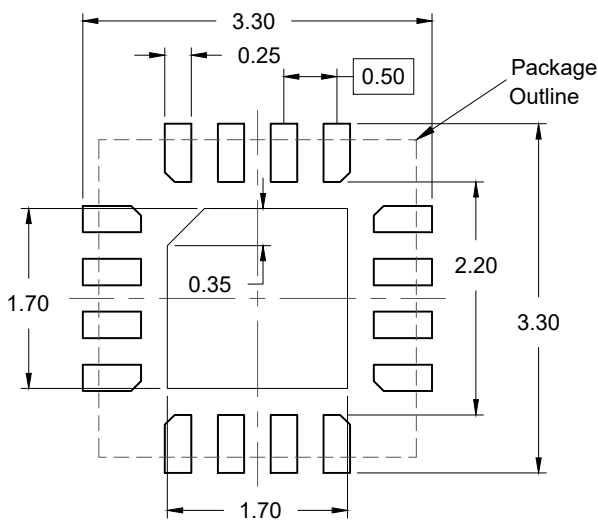
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

**NOTES:**

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).