RENESAS

F2255
Datasheet

Voltage Variable RF Attenuator **1MHz to 3000MHz**

GENERAL DESCRIPTION

The F2255 is a low insertion loss **V**oltage **V**ariable RF **A**ttenuator (VVA) designed for a multitude of wireless and other RF applications. This device covers a broad frequency range from 1MHz to 3000MHz. In addition to providing low insertion loss, the F2255 provides excellent linearity performance over its entire voltage control and attenuation range.

The F2255 uses a single positive supply voltage of 3.15V to 5.25V. Other features include the V_{MODE} pin allowing either positive or negative voltage control slope vs attenuation and multi-directional operation meaning the RF input can be applied to either RF1 or RF2 pins. Control voltage ranges from 0V to 3.6V using either positive or negative control voltage slope.

COMPETITIVE ADVANTAGE

The F2255 provides extremely low insertion loss and superb IP3, IP2, Return Loss and Slope Linearity across the control range. Comparing to competitive VVAs this device is better as follows:

- ✓ Operation down to 1MHz
- ✓ Insertion Loss @ 500MHz: 1.1dB
- ✓ Maximum Attenuation Slope: 33dB/Volt
- ✓ Minimum Output IP3: 35dBm
- ✓ Minimum Input IP2: 74dBm
- ✓ High Operating Temperature: +105°C

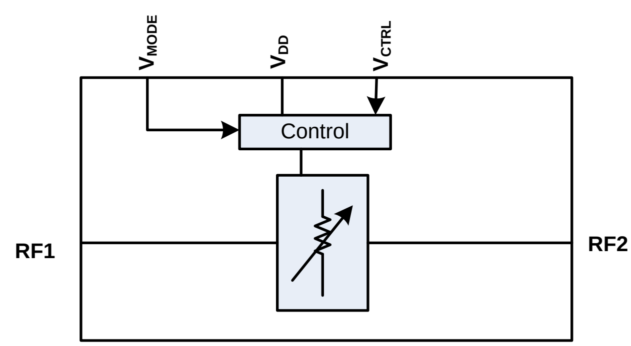
APPLICATIONS

- Base Station 2G, 3G, 4G
- Portable Wireless
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- Satellite Receivers and Modems
- WIMAX Receivers and Transmitters
- Military Radios covering HF, VHF, UHF
- RFID handheld and portable readers
- Cable Infrastructure
- Wireless LAN
- Test / ATE Equipment

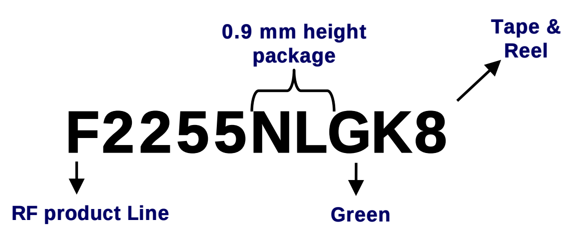
FEATURES

- Low Insertion Loss: 1.1dB @ 500MHz
- Typical / Min IIP3: 60dBm / 46dBm
- Typical / Min IIP2: 98dBm / 74dBm
- 33dB Attenuation Range
- Bi-directional RF ports
- +36dBm Input P1dB compression
- V_{MODE} pin allows either positive or negative control response
- Linear-in-dB attenuation characteristic
- Supply voltage: 3.15V to 5.25V
- V_{CTRL} range: 0V to 3.6V using 5V supply
- +105°C max operating temperature
- 3mm x 3mm, 16-pin QFN package

DEVICE BLOCK DIAGRAM



ORDERING INFORMATION



PART# MATRIX

Part#	RF Freq Range (MHz)	Insertion Loss (dB)	IIP3 (dBm)	Pinout Compatibility
F2250	50 - 6000	1.4 (at 2GHz)	+65	RFMD
F2255	**1 - 3000**	**1.1 (at 500MHz)**	**+60**	
F2258	50 - 6000	1.4 (at 2GHz)	+65	Hittite

Voltage Variable RF Attenuator **1MHz to 3000MHz**

ABSOLUTE MAXIMUM RATINGS

Parameter / Condition		Symbol	Min	Max	Units
V_{DD} to GND		V_{DD}	-0.3	5.5	V
V_{MODE} to GND		V_{MODE}	-0.3	Minimum (V_{DD}, 3.9)	V
V_{CTRL} to GND	V_{DD} = 0V to 5.25V	V_{CTRL}	-0.3	Minimum (V_{DD}, 4.0)	V
RF1, RF2 to GND		V_{RF}	-0.3	0.3	V
RF1 or RF2 Input Power applied for 24 hours maximum (V_{DD} applied @ 2GHz and Tc=+85°C)		P_{MAX24}		30	dBm
RF1 or RF2 Continuous Operating Power		P_{MAX_OP}		See Figure 1	dBm
Maximum Junction Temperature		T_{JMAX}		+150	°C
Storage Temperature Range		T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)		T_{LEAD}		+260	°C
ESD Voltage– HBM (Per ESD STM5.1-2007)		V_{ESDHBM}		Class 2	
ESD Voltage – CDM (Per ESD STM5.3.1-2009)		V_{ESDCDM}		Class C3	

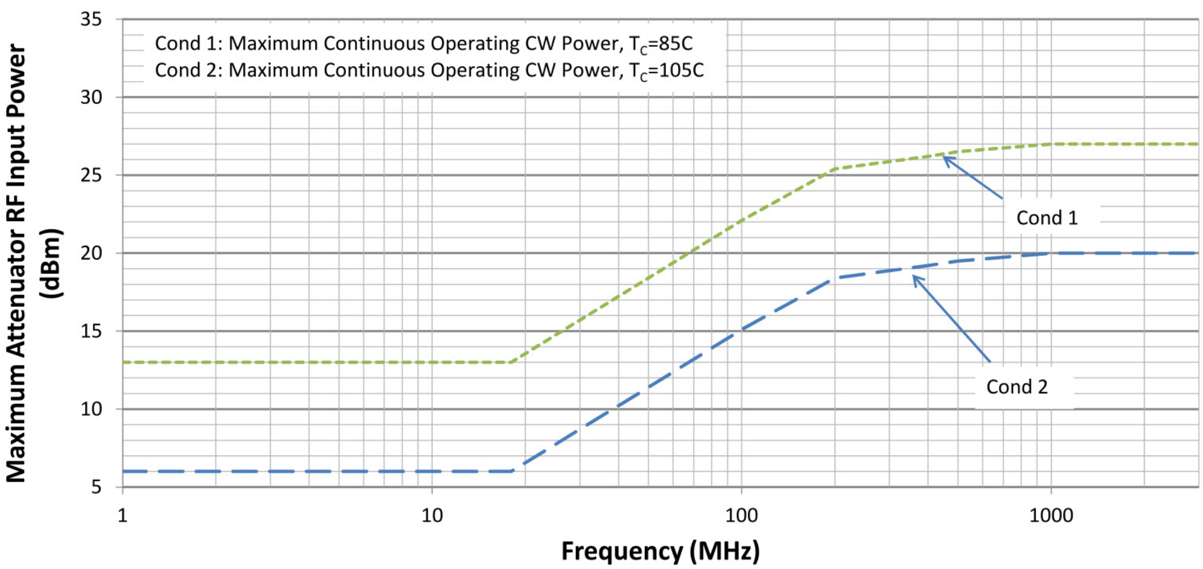


FIGURE 1: MAXIMUM OPERATING RF INPUT POWERS VS. RF FREQUENCY

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

Θ_{JA} (Junction – Ambient)	80.6°C/W
Θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	5.1°C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL 1

Voltage Variable RF Attenuator **1MHz to 3000MHz**

F2255 Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating Frequency Range	F_{RF}		1		3000	MHz
Supply Voltage	V_{DD}		3.15		5.25	V
V_{MODE} Logic	V_{IH}	V_{DD} > 3.9V	1.17		3.6 [2]	V
		V_{DD} = 3.15 to 3.9V	1.17		V_{DD} -0.3V	
	V_{IL}		0		0.63	
V_{CTRL} Range	V_{CTRL}	V_{DD} = 3.9V to 5.25V	0		3.6	V
		V_{DD} = 3.15V to 3.9V	0		V_{DD}-0.3	
Supply Current	I_{DD}		***0.50*** [1]	1.15	***2***	mA
Logic Current	I_{MODE}		***-1.0***		***38***	µA
I_{CTRL} Current	I_{CTRL}		***-1.0***		***14***	µA
RF Operating Power [3]	P_{MAXCW}				See Figure 1	dBm
RF1 Port Impedance	Z_{RF1}			50		Ω
RF2 Port Impedance	Z_{RF2}			50		
Operating Temperature Range	T_{CASE}	Exposed Paddle Temperature	-40		+105	°C

Operating Conditions Notes:

1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test.
2 – Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
3 – Refer to the Maximum **Operating** RF Input Power vs. RF Frequency curves in Figure 1.

Voltage Variable RF Attenuator **1MHz to 3000MHz**

F2255 SPECIFICATIONS

Refer to EVKit / Applications Circuit, V_{DD} = +3.3V, T_C = +25°C, signals applied to RF1 input, F_{RF} = 500MHz, minimum attenuation, P_{IN} = 0dBm for small signal parameters, +20dBm for single tone linearity tests, +20dBm per tone for two tone tests, two tone delta frequency = 80MHz, PCB board traces and connector losses are de-embedded unless otherwise noted. Refer to Typical Operating Curves for performance over entire frequency band.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Insertion Loss, IL	A_{MIN}	Minimum Attenuation		1.1	***1.7*** [1]	dB
Maximum attenuation	A_{MAX}		33	34.6		dB
Insertion Phase Δ	$\Phi_{\Delta MAX}$	At 36dB attenuation relative to Insertion Loss		27		deg
	$\Phi_{\Delta MID}$	At 18dB attenuation relative to Insertion Loss		8		
Input 1dB Compression [3]	P1dB			36		dBm
Minimum RF1 Return Loss over control voltage range	S11	20MHz		23		dB
		500MHz		22		
		2000MHz		23		
		3000MHz		30		
Minimum RF2 Return Loss over control voltage range	S22	20MHz		23		dB
		500MHz		22		
		2000MHz		23		
		3000MHz		24		
Input IP3	IIP3			60		dBm
Input IP3 over Attenuation	$IIP3_{ATTEN}$	All attenuation settings	44 [2]	46		
Minimum Output IP3	$OIP3_{MIN}$	Maximum attenuation		35		
Input IP2	IIP2	PIN + $IM2_{dBC}$, IM2 term is F1+F2		98		dBm
Minimum Input IP2	$IIP2_{MIN}$	All attenuation settings		74		dBm
Input IH2	HD2	PIN + $H2_{dBc}$		82		dBm
Input IH3	HD3	PIN + ($H3_{dBc}$/2)		49		dBm
Settling Time	$T_{SETTL0.1dB}$	Any 1dB step in the 0dB to 33dB control range 50% V_{CTRL} to RF settled to within ± 0.1dB		15		µSec

Specification Notes:

1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test.
2 – Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
3 – The input 1dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section along with Figure 1 for the maximum RF input power vs. RF frequency.

TYPICAL OPERATING CURVES

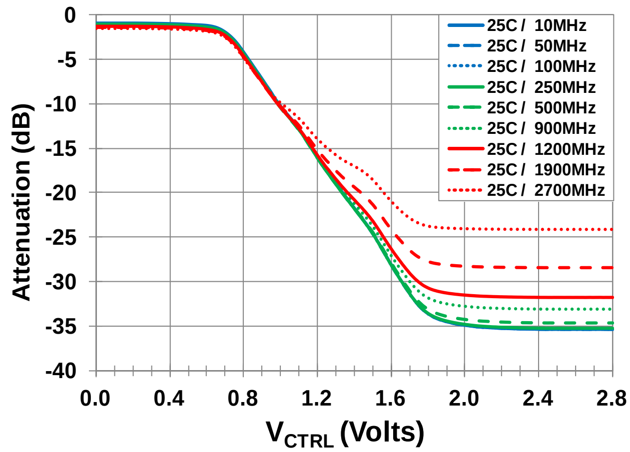
UNLESS OTHERWISE NOTED, THE FOLLOWING CONDITIONS APPLY:

- V_{DD} = +3.3V or +5.0V
- T_C = +25ºC
- V_{MODE} = 0V
- RF trace and connector losses are de-embedded for S-parameters
- Pin = 0dBm for all small signal tests
- Pin = +20dBm for single tone linearity tests (RF1 port driven)
- Pin = +20dBm/tone for two tone linearity tests (RF1 port driven)
- Two tone frequency spacing = 80MHz

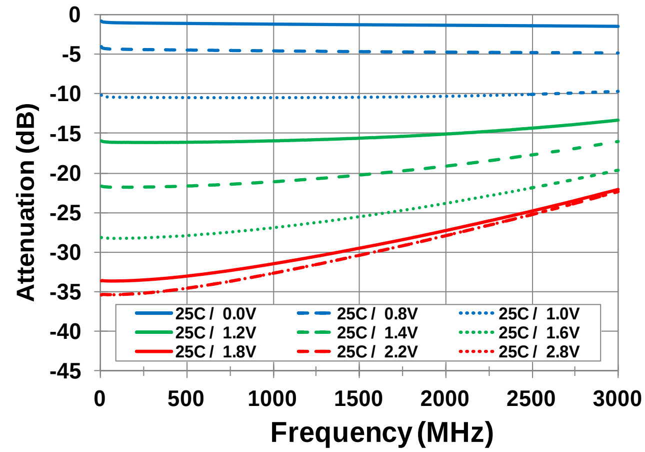
Voltage Variable RF Attenuator **1MHz to 3000MHz**

TYPICAL OPERATING CONDITIONS [S2P BROADBAND PERFORMANCE] (-1-)

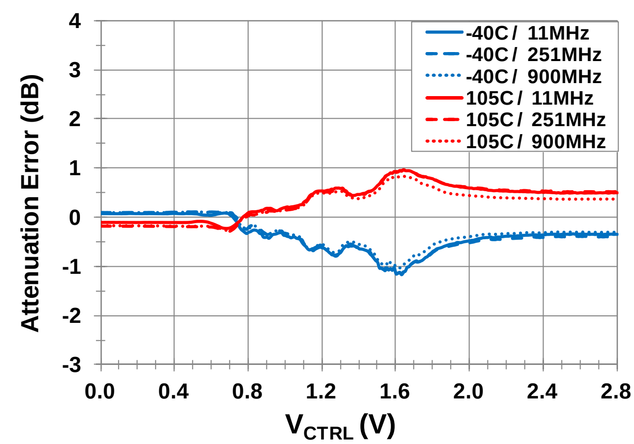
Attenuation vs. V_{CTRL}



Attenuation vs. Frequency

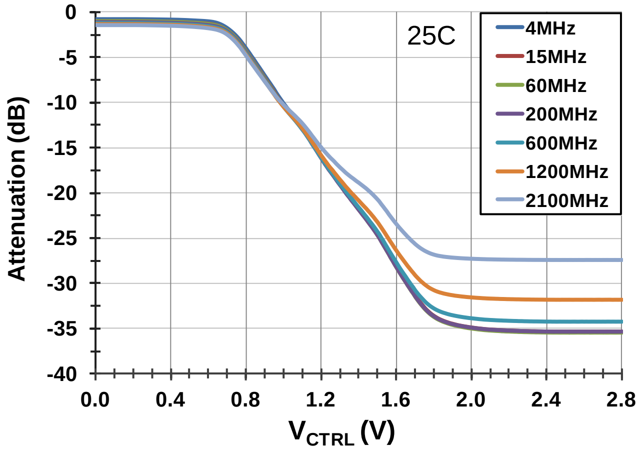


Attenuation Delta to 25C vs. V_{CTRL}

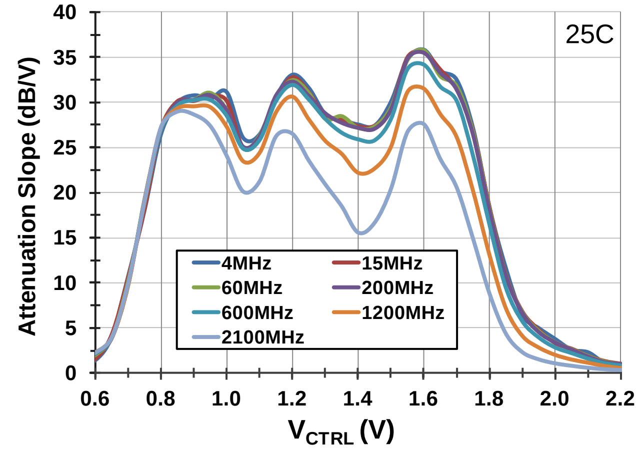


TYPICAL OPERATING CURVES [S2P VS. V_{CTRL}] (-2-)

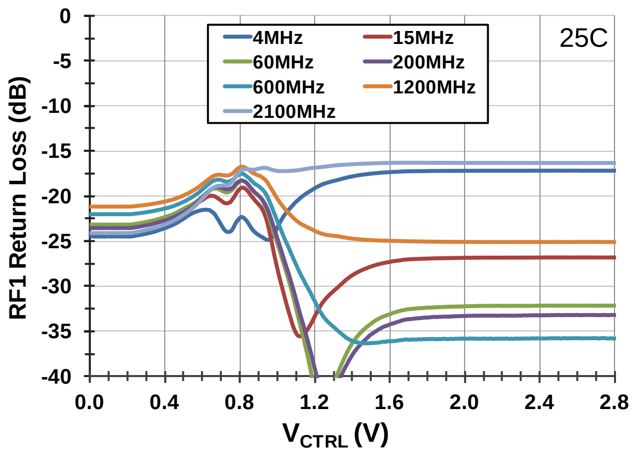
Attenuation vs. V_{CTRL}



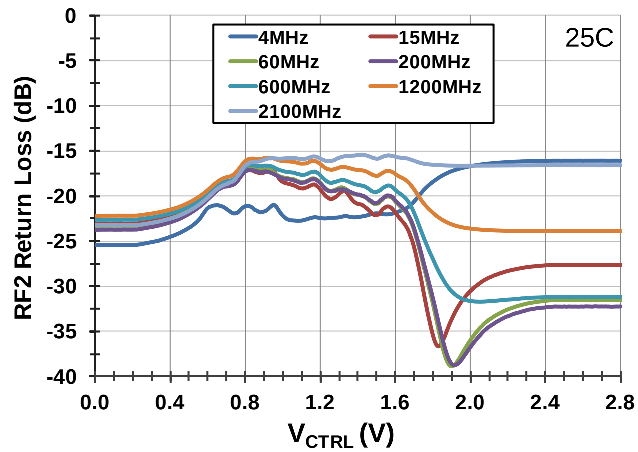
Attenuation Slope vs. V_{CTRL}



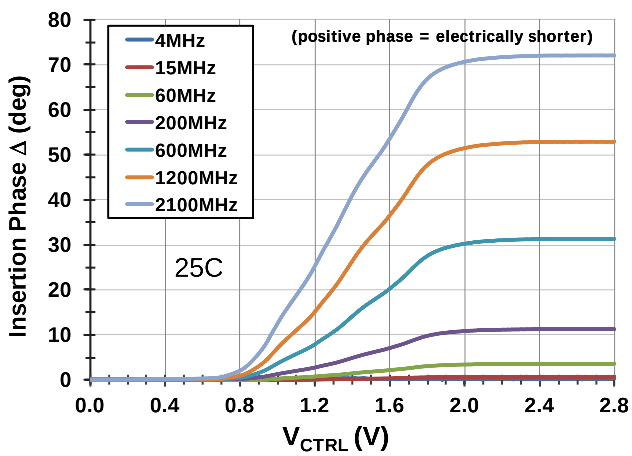
RF1 Return Loss vs. V_{CTRL}



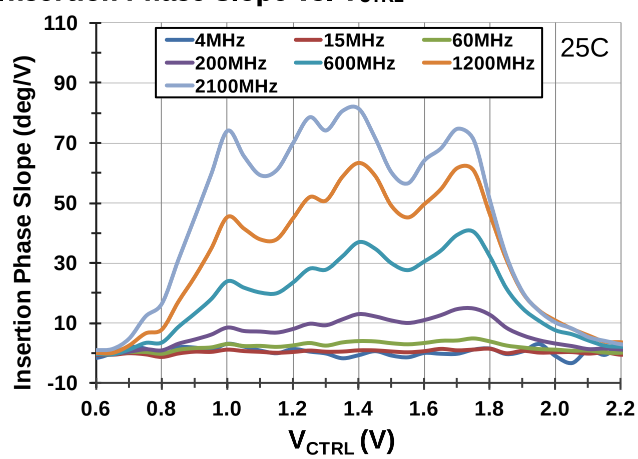
RF2 Return Loss vs. V_{CTRL}



Insertion Phase Δ vs. V_{CTRL}



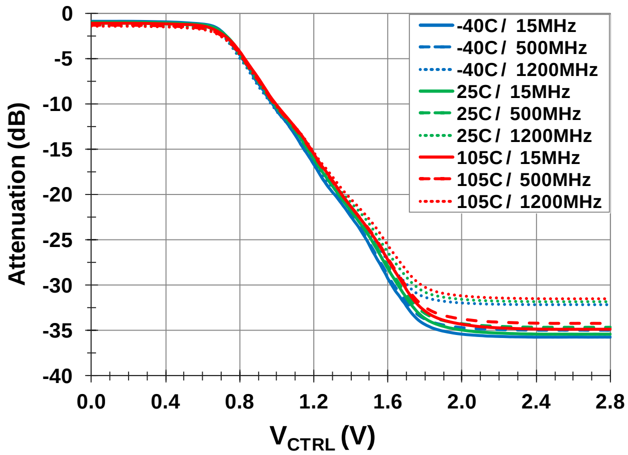
Insertion Phase Slope vs. V_{CTRL}



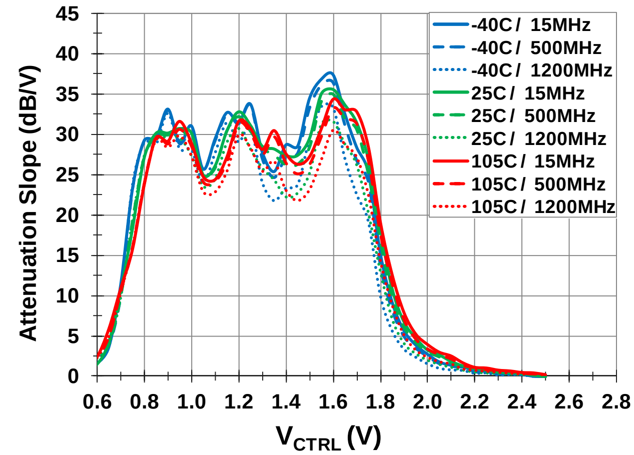
Voltage Variable RF Attenuator **1MHz to 3000MHz**

TYPICAL OPERATING CONDITIONS [S2P VS. V_{CTRL} & TEMPERATURE] (-3-)

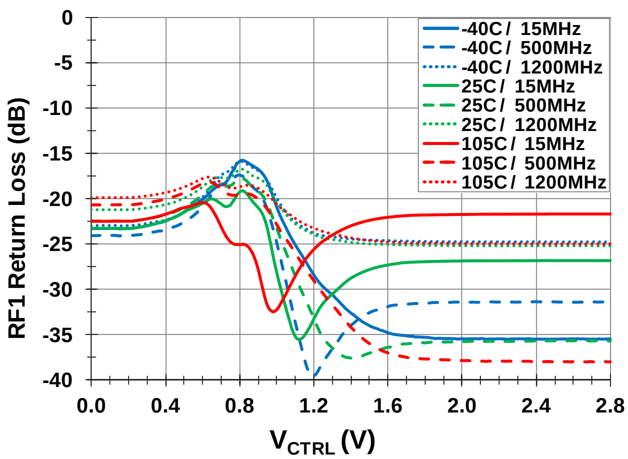
Attenuation Response vs. V_{CTRL}



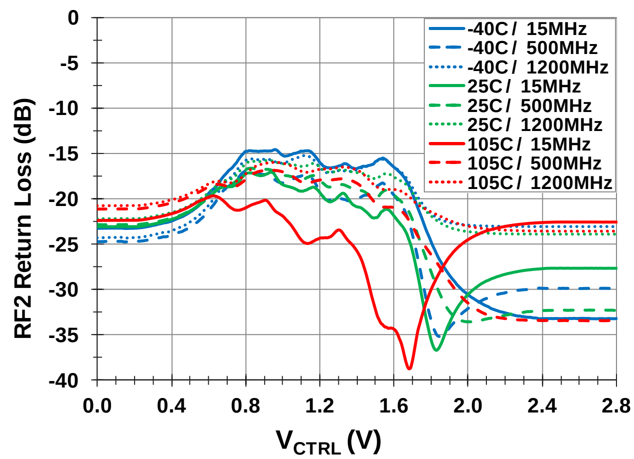
Attenuation Slope vs. V_{CTRL}



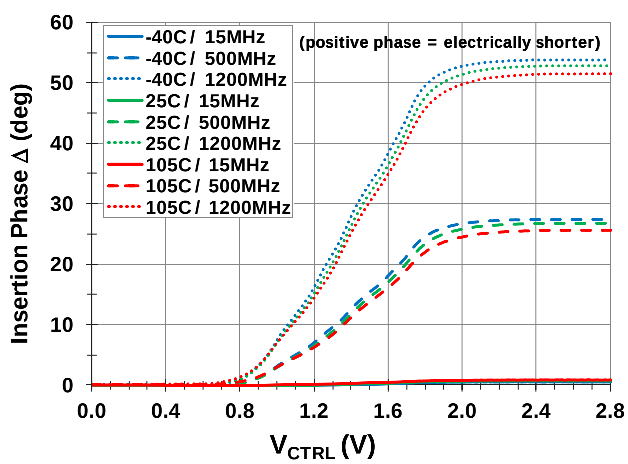
RF1 Return Loss vs. V_{CTRL}



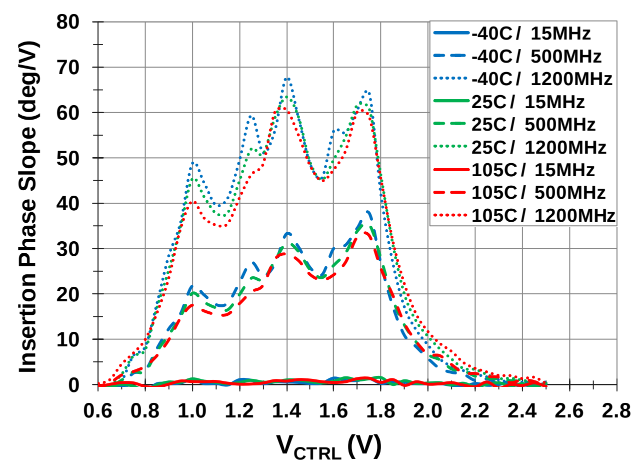
RF2 Return Loss vs. V_{CTRL}



Insertion Phase Δ vs. V_{CTRL}

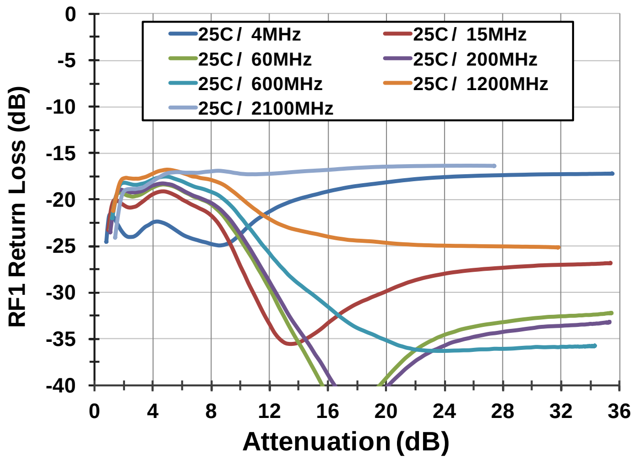


Insertion Phase Slope vs. V_{CTRL}

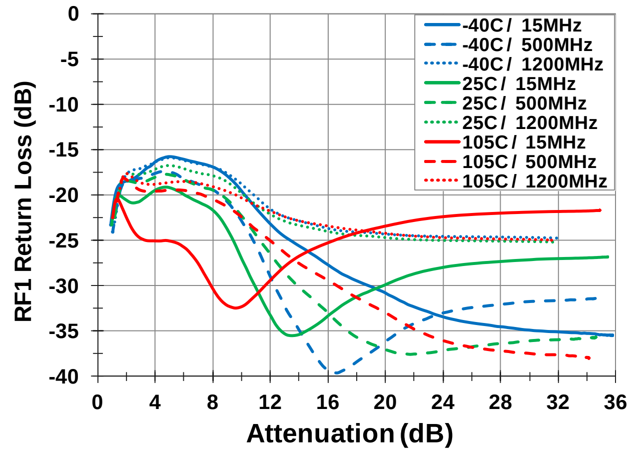


TYPICAL OPERATING CONDITIONS [S2P VS. ATTENUATION & TEMPERATURE] (-4-)

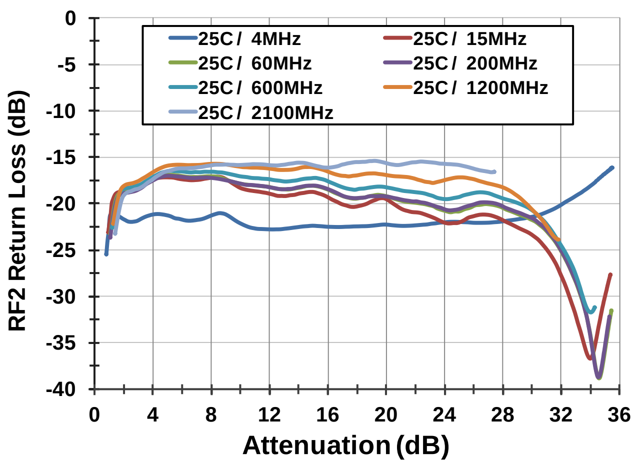
RF1 Return Loss vs. Attenuation



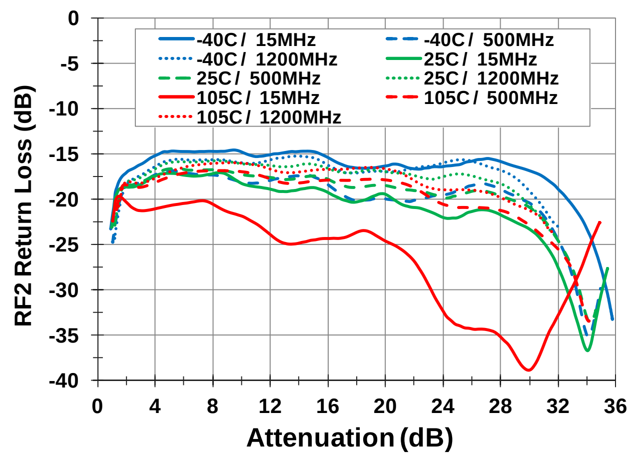
RF1 Return Loss vs. Attenuation



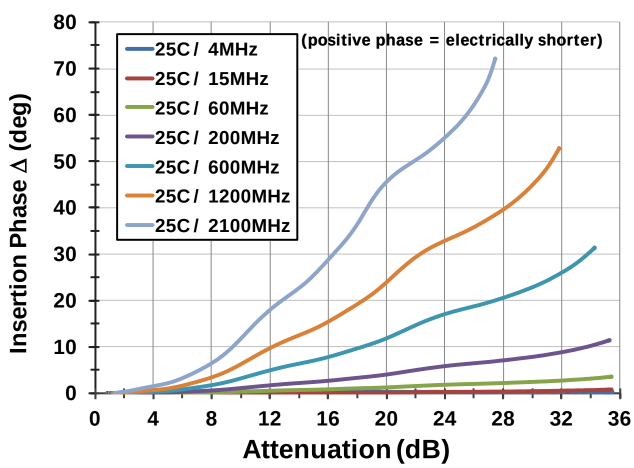
RF2 Return Loss vs. Attenuation



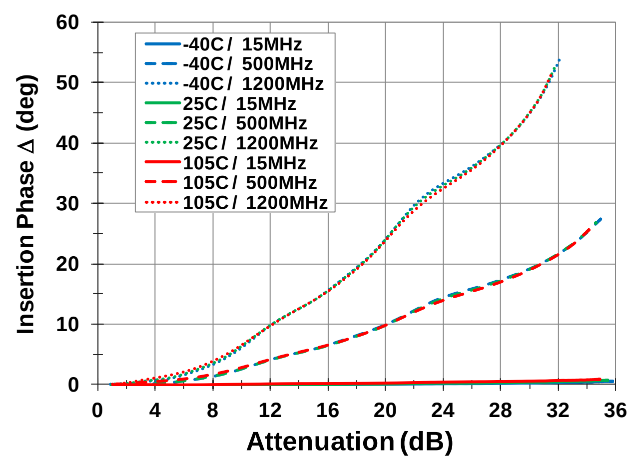
RF2 Return Loss vs. Attenuation



Insertion Phase Δ vs. Attenuation



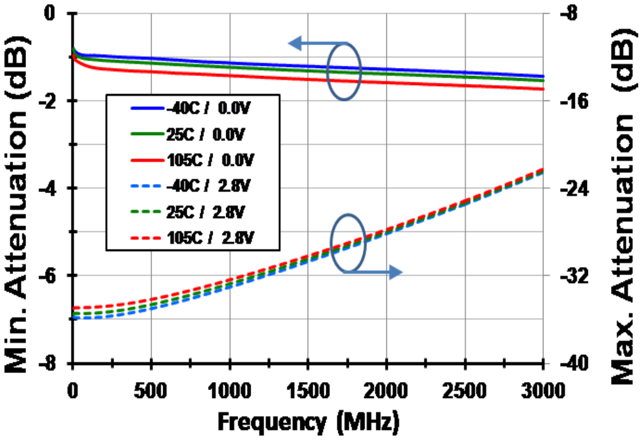
Insertion Phase Δ vs. Attenuation



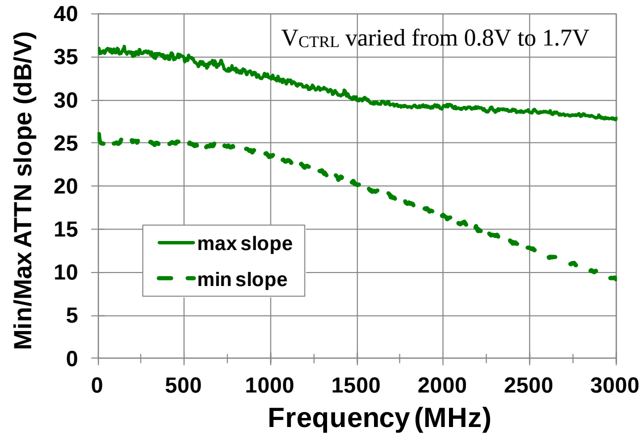
Voltage Variable RF Attenuator **1MHz to 3000MHz**

TYPICAL OPERATING CONDITIONS [S2P VS. FREQUENCY] (-5-)

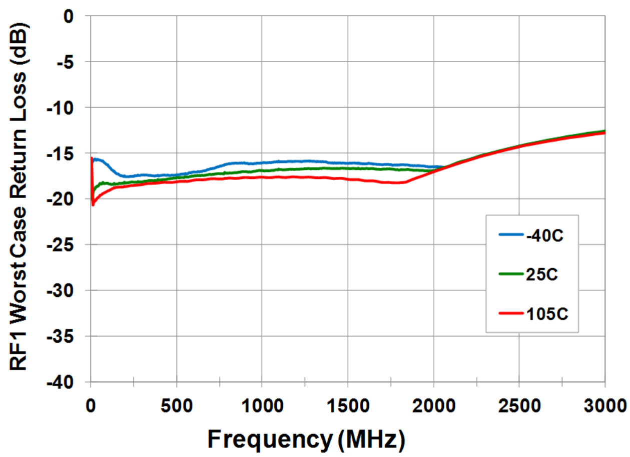
Min. & Max. Attenuation vs. Frequency



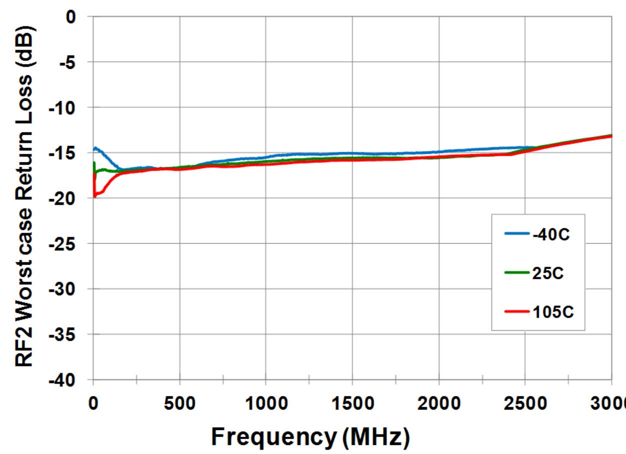
Min. & Max. Attenuation Slope vs. Frequency



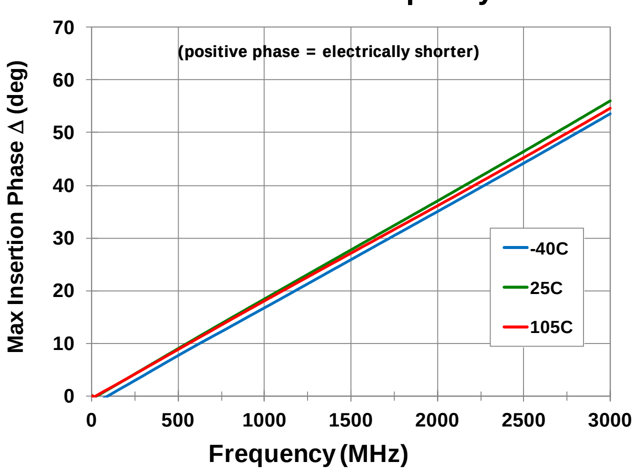
Worst-Case RF1 Return Loss vs. Frequency



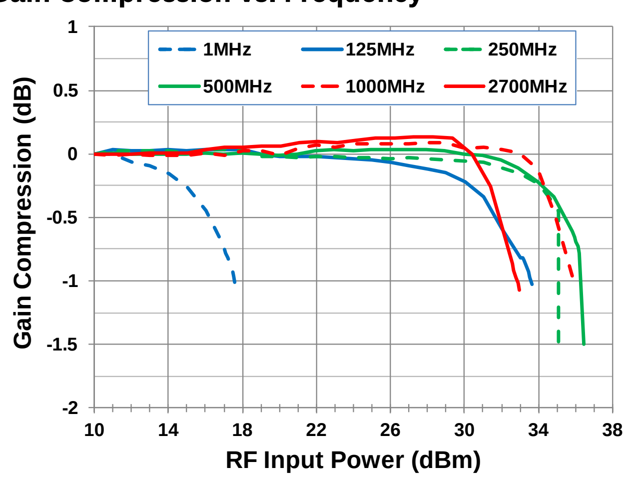
Worst-Case RF2 Return Loss vs. Frequency



Max. Insertion Phase Δ vs. Frequency

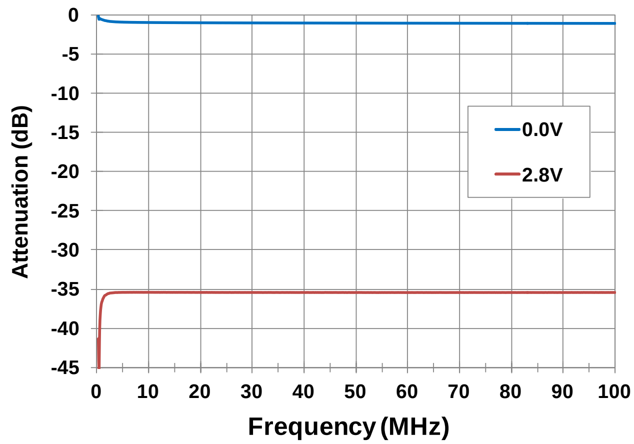


Gain Compression vs. Frequency

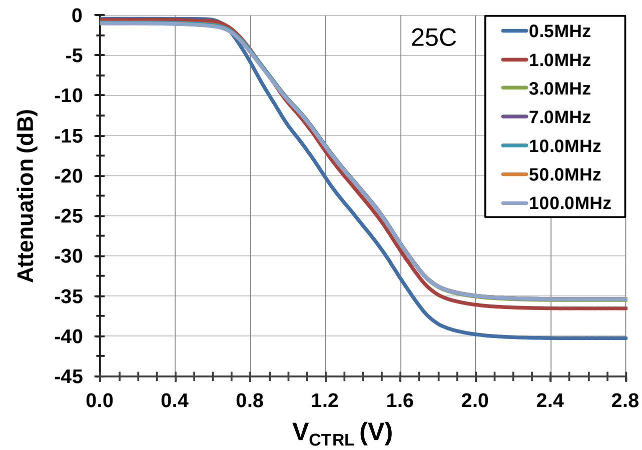


Typical Operating Conditions [S2P @ Low Frequency, Group Delay] (-6-)

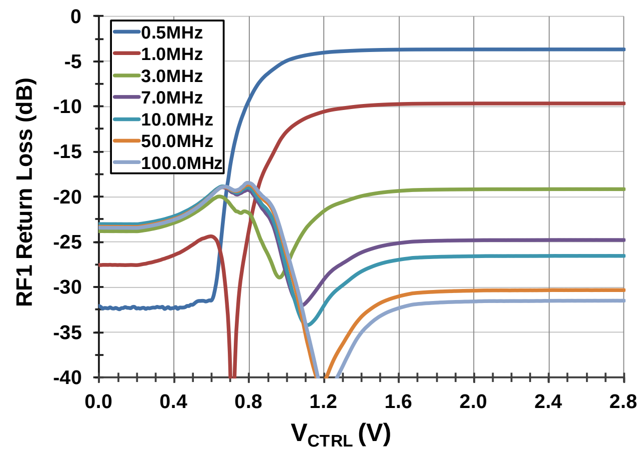
Min. & Max. Attenuation vs. Low Frequency



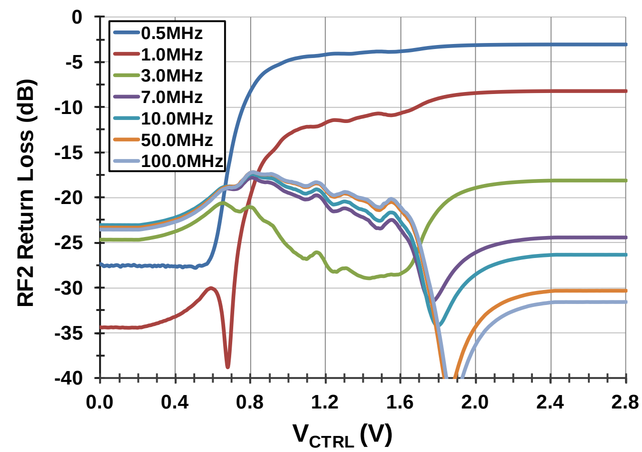
Low-Frequency Attenuation vs. V_{CTRL}



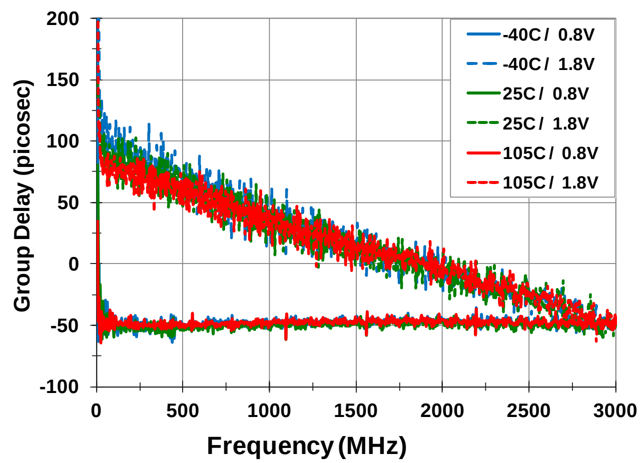
Low-Frequency RF1 Return Loss vs. V_{CTRL}



Low-Frequency RF2 Return Loss vs. V_{CTRL}



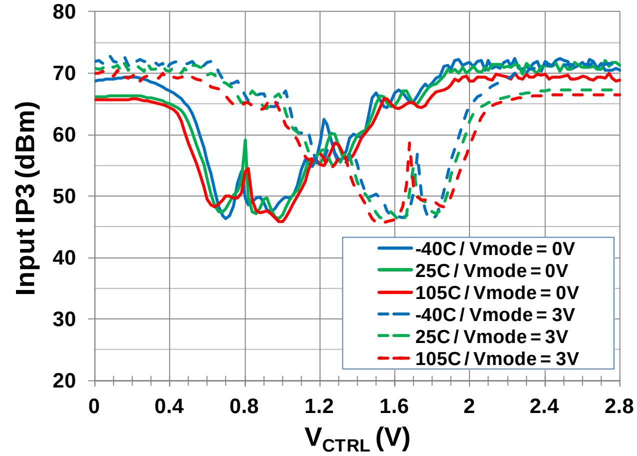
Group Delay vs. Frequency



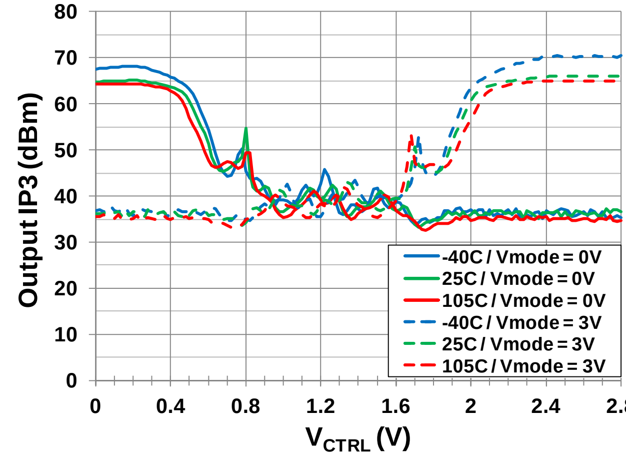
Voltage Variable RF Attenuator **1MHz to 3000MHz**

TYPICAL OPERATING CONDITIONS 500MHz, V_{DD}=3.3V [IP3, IP2, IH2, IH3 VS. V_{CTRL}, V_{MODE}] (-7-)

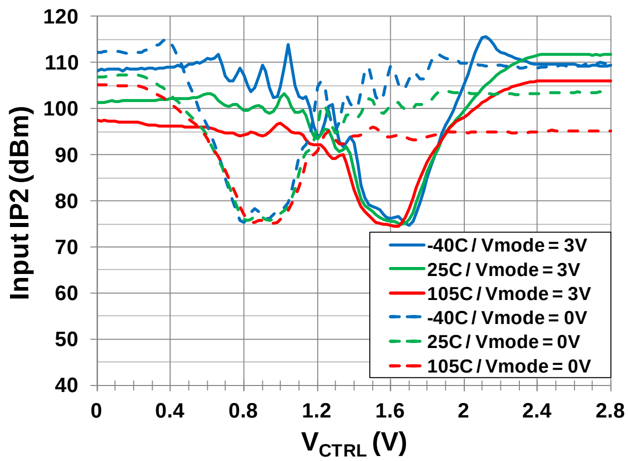
Input IP3 vs. V_{CTRL}



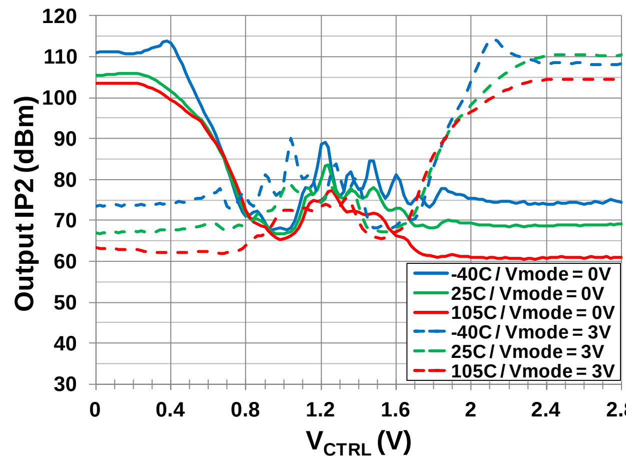
Output IP3 vs. V_{CTRL}



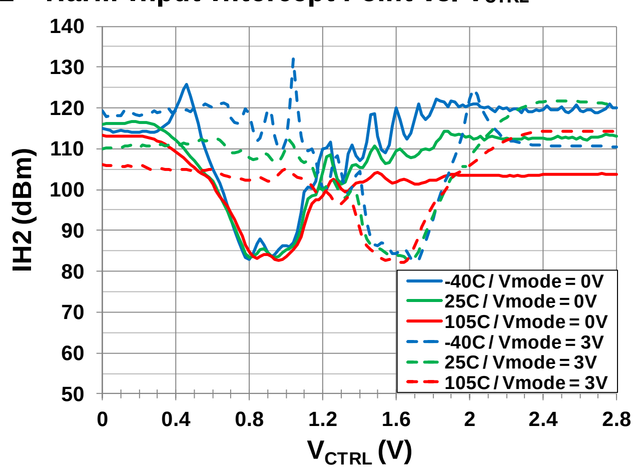
Input IP2 vs. V_{CTRL}



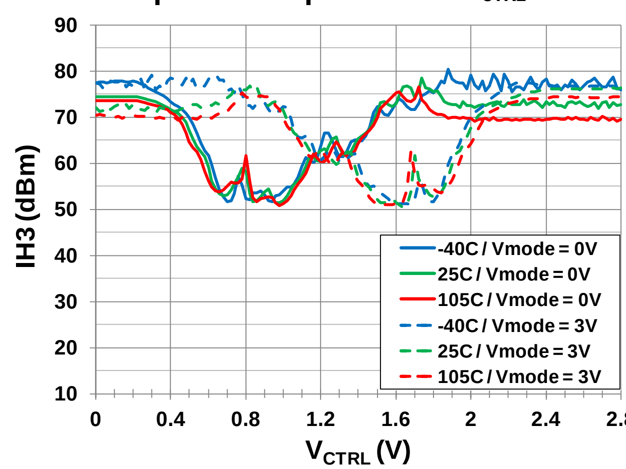
Output IP2 vs. V_{CTRL}



2nd Harm Input Intercept Point vs. V_{CTRL}

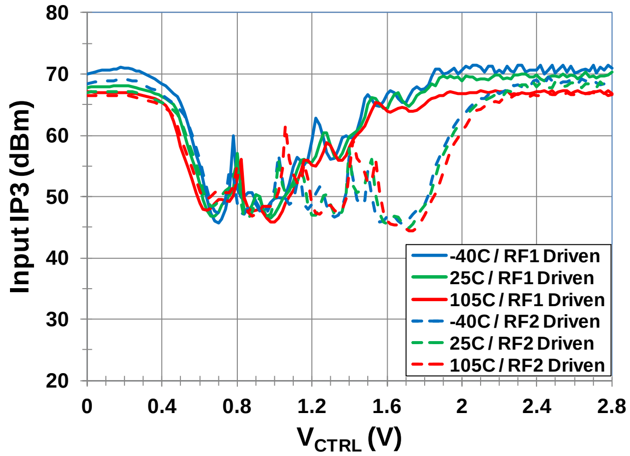


3rd Harm Input Intercept Point vs. V_{CTRL}

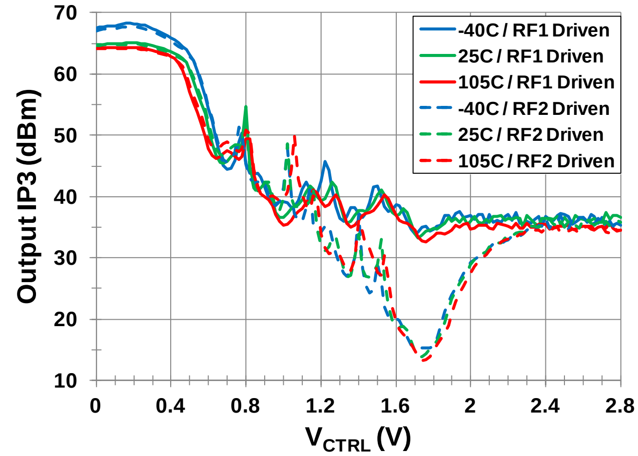


TYPICAL OPERATING CONDITIONS 500MHZ, V_{DD}=3.3V [IPX, IHX VS. V_{CTRL}, RF1/RF2 DRIVEN] (-8-)

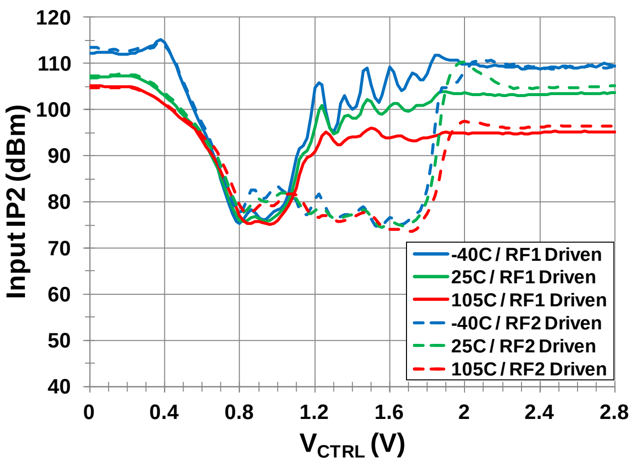
Input IP3 vs. V_{CTRL}



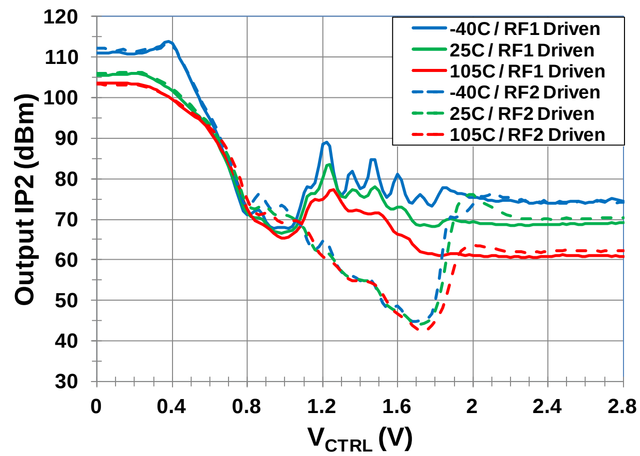
Output IP3 vs. V_{CTRL}



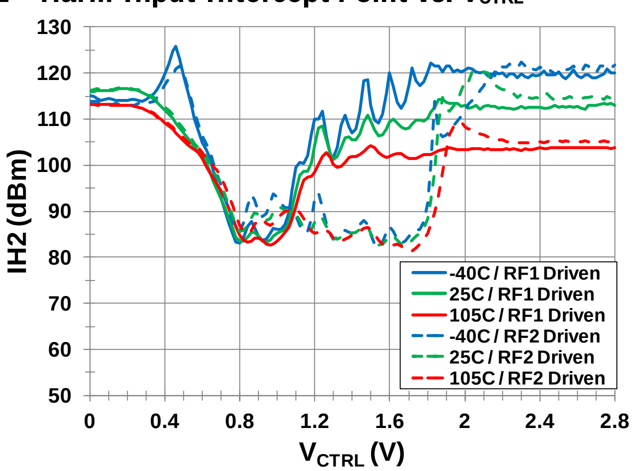
Input IP2 vs. V_{CTRL}



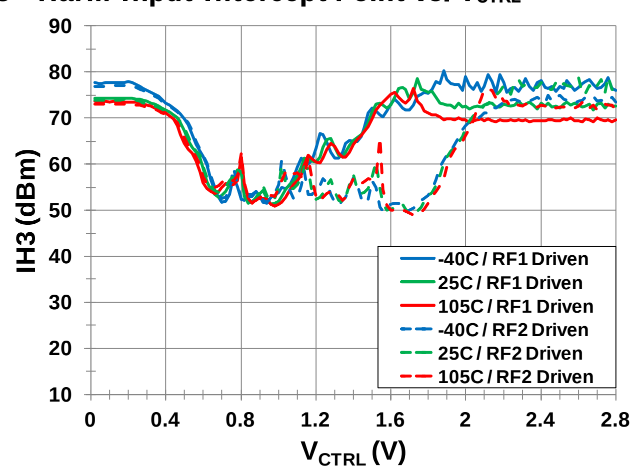
Output IP2 vs. V_{CTRL}



2nd Harm Input Intercept Point vs. V_{CTRL}

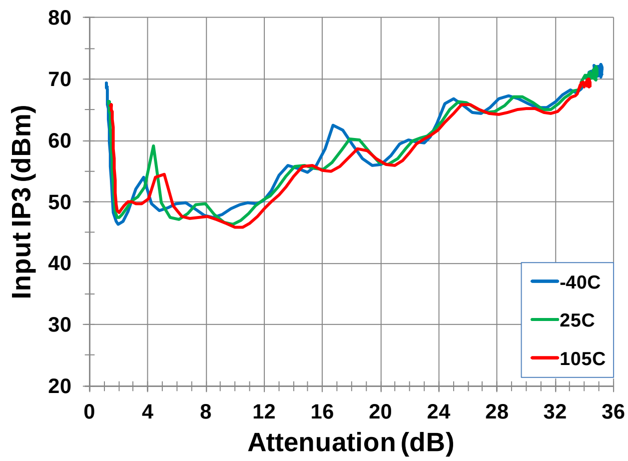


3rd Harm Input Intercept Point vs. V_{CTRL}

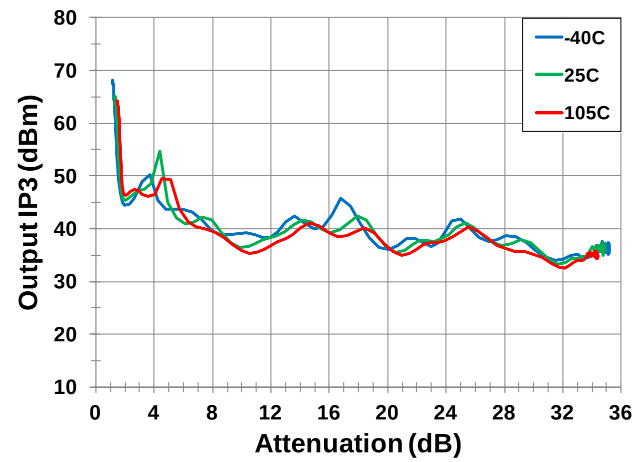


Typical Operating Conditions 500MHz, V_{DD}=3.3V [IP3, IP2, IH2, IH3 vs. Attenuation] (-9-)

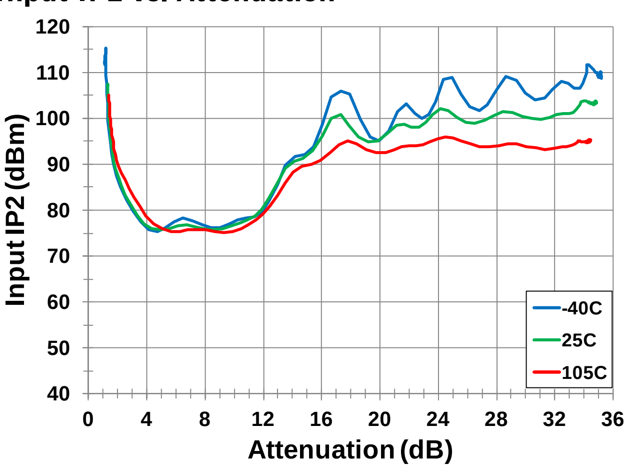
Input IP3 vs. Attenuation



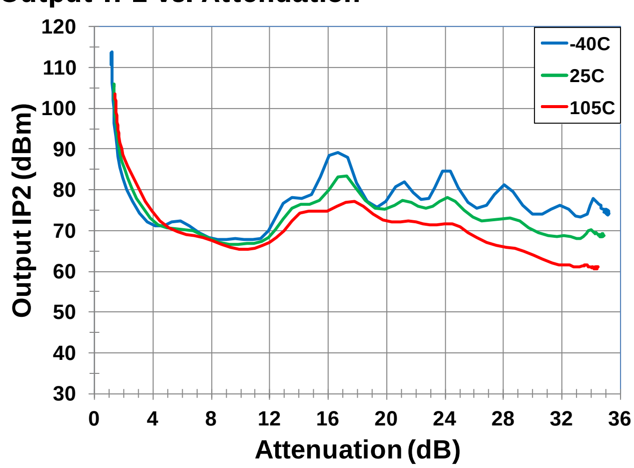
Output IP3 vs. Attenuation



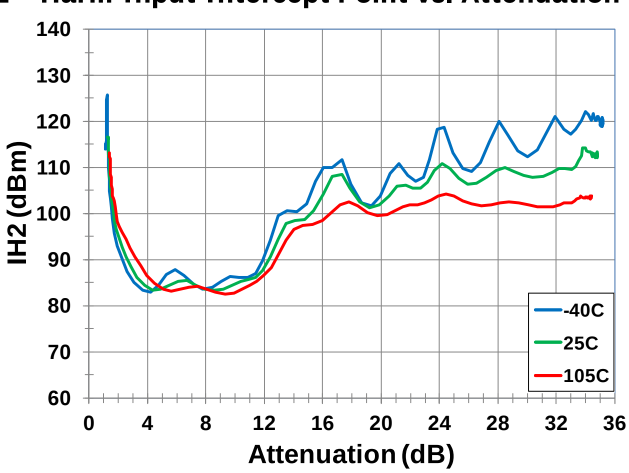
Input IP2 vs. Attenuation



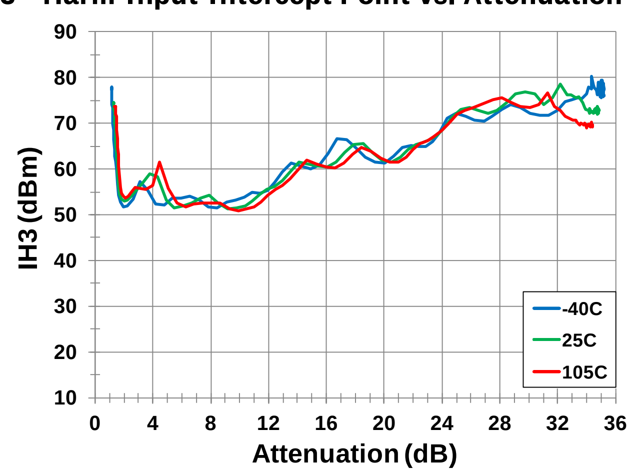
Output IP2 vs. Attenuation



2nd Harm Input Intercept Point vs. Attenuation

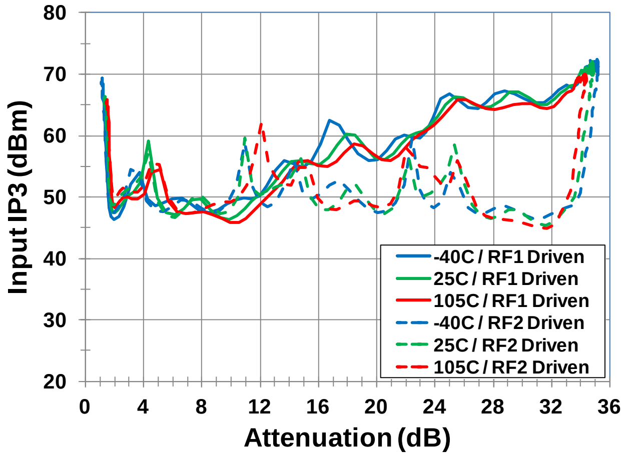


3rd Harm Input Intercept Point vs. Attenuation

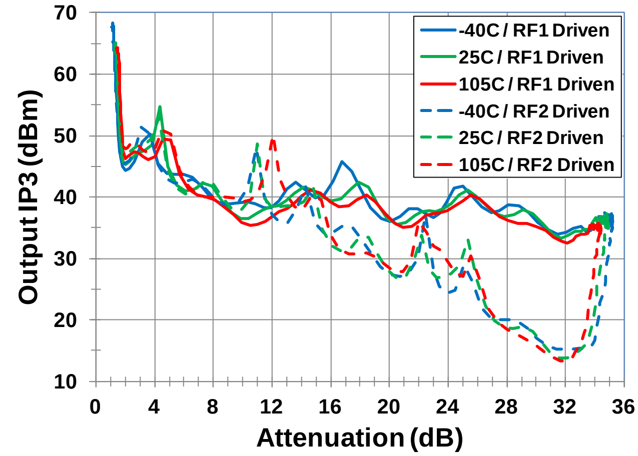


Typical Operating Conditions 500MHz, V_{DD}=3.3V [IPx, IHx vs. Atten, RF1/RF2 Driven] (-10-)

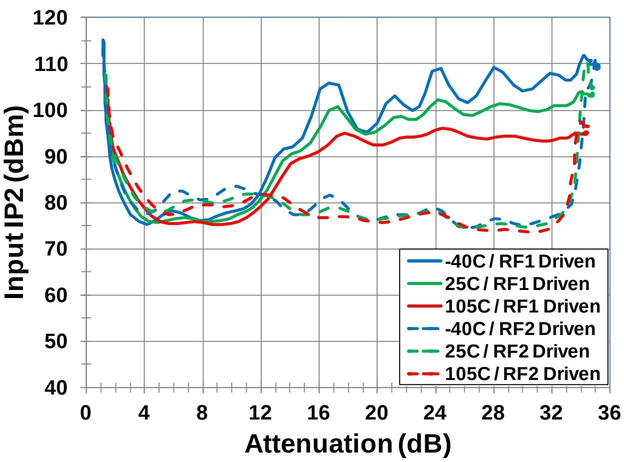
Input IP3 vs. Attenuation



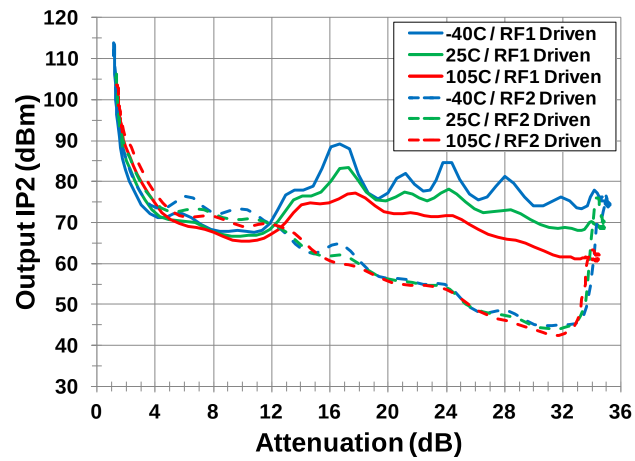
Output IP3 vs. Attenuation



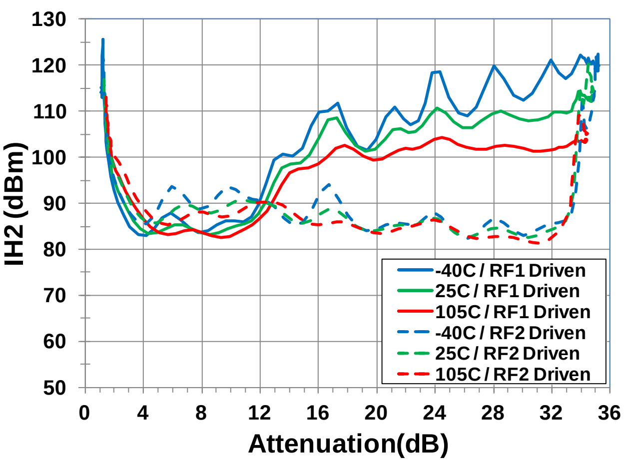
Input IP2 vs. Attenuation



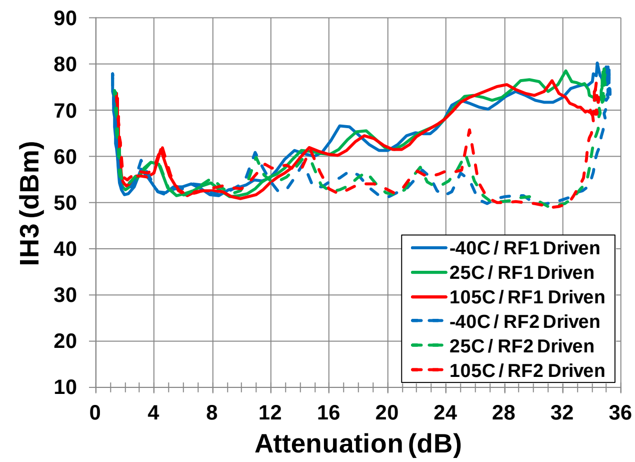
Output IP2 vs. Attenuation



2nd Harm Input Intercept Point vs. Attenuation



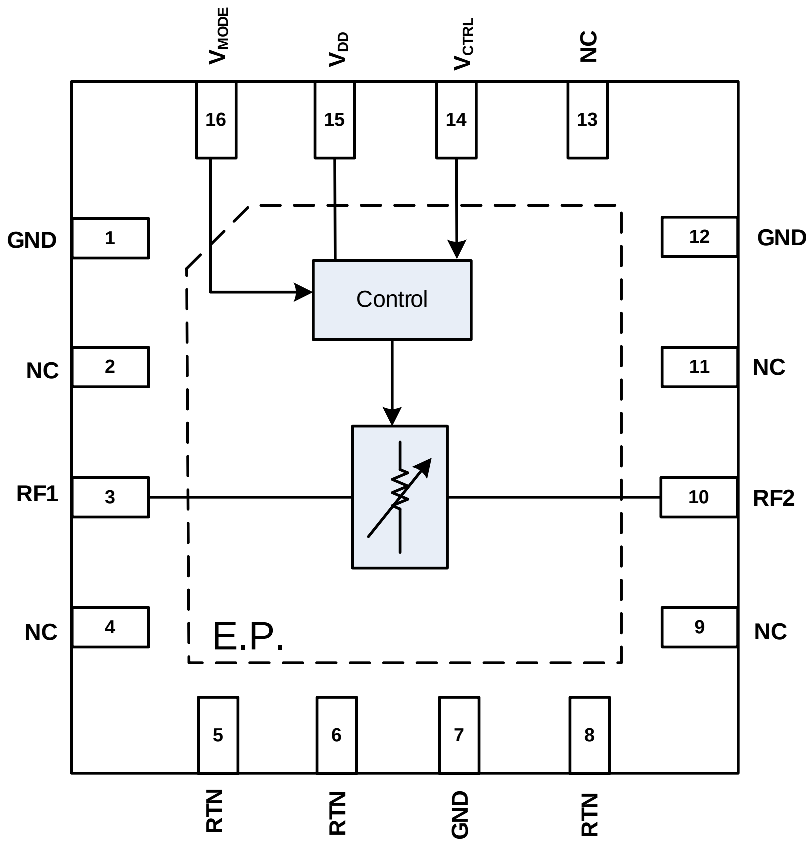
3rd Harm Input Intercept Point vs. Attenuation



Package Outline Drawing

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see also 16-VFQFPN). The package information is the most current data available and is subject to change without revision of this document.

Pinout & Block Diagram



PIN DESCRIPTION

Pin	Name	Function
1, 7, 12	GND	Ground these pins as close to the device as possible.
2, 4, 9, 11, 13	NC	No internal connection. Renesas recommends connecting these pins to GND.
3	RF1	RF Port 1. Matched to 50 ohms. Must use an external AC coupling capacitor as close to the device as possible. For low frequency operation increase the capacitor value to result in a low reactance at the frequency of interest.
5, 6, 8	RTN	Attenuator Ground Return. Each of these pins require a capacitor to GND to provide an RF return path. Place the capacitor as close to the device as possible.
10	RF2	RF Port 2. Matched to 50 ohms. Must use an external AC coupling capacitor as close to the device as possible. For low frequency operation increase the capacitor value to result in a low reactance at the frequency of interest.
14	V_{CTRL}	Attenuator control voltage. Apply a voltage in the range as specified in the Operating Conditions Table. See application section for details about V_{CTRL}.
15	V_{DD}	Power supply input. Bypass to GND with capacitors close as possible to pin.
16	V_{MODE}	Attenuator slope control. Set to logic LOW to enable negative attenuation slope. Set to logic HIGH to enable positive attenuation slope.
	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to achieve the specified RF performance.

APPLICATIONS INFORMATION

Default Start-up

V_{MODE} must be tied to either GND or Logic High. If the V_{CTRL} pin is left floating, the part will power up in the minimum attenuation state when V_{MODE} = GND, or the maximum attenuation state when V_{MODE} = High.

V_{CTRL}

The voltage level on the V_{CTRL} pin is used to control the attenuation of the F2255. At V_{CTRL} =0V, the attenuation is a minimum (maximum) in the negative (positive) slope mode. An increasing (decreasing) voltage on V_{CTRL} produces an increasing (decreasing) attenuation respectively. The V_{CTRL} pin has an on-chip pull-up ESD diode so V_{DD} should be applied before V_{CTRL} is applied (see Recommended Operating Conditions for details). If this sequencing is not possible, then resistor R2 in the application circuit should be set to 1kΩ to limit the current into the V_{CTRL} pin.

V_{MODE}

The V_{MODE} pin is used to set the slope of the attenuation. The attenuation is varied by V_{CTRL} as described in the next section. Setting V_{MODE} to a logic LOW (HIGH) will set the attenuation slope to negative (positive). A negative (positive) slope is defined as an increased (decreased) attenuation with increasing V_{CTRL} voltage. The Evaluation Kit provides an on-board jumper to manually set the V_{MODE}. Install a jumper on header J2 from V_{MODE} to the pin marked Lo (Hi) to set the device for a negative (positive) slope (see application circuit).

RF1 and RF2 Ports

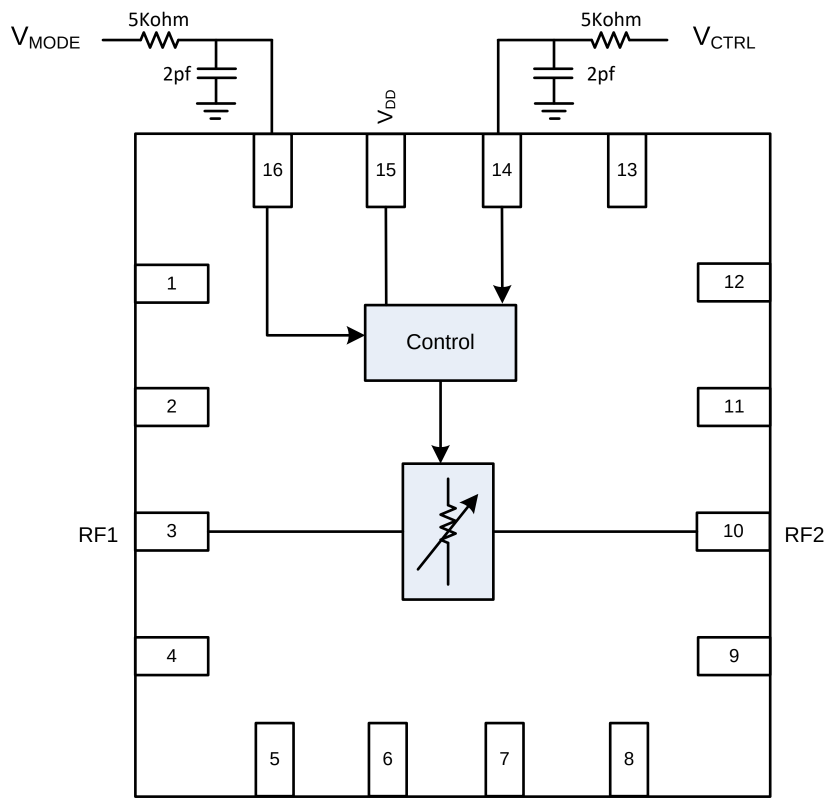
The F2255 is a bi-directional device, allowing RF1 or RF2 to be used as the RF input. RF1 has some enhanced linearity performance, and therefore should be used as the RF input, when possible, for best results. The F2255 has been designed to accept high RF input power levels; therefore, V_{DD} must be applied prior to the application of RF power to ensure reliability. DC blocking capacitors are required on the RF pins and should be set to a value that results in a low reactance over the frequency range of interest.

Power Supplies

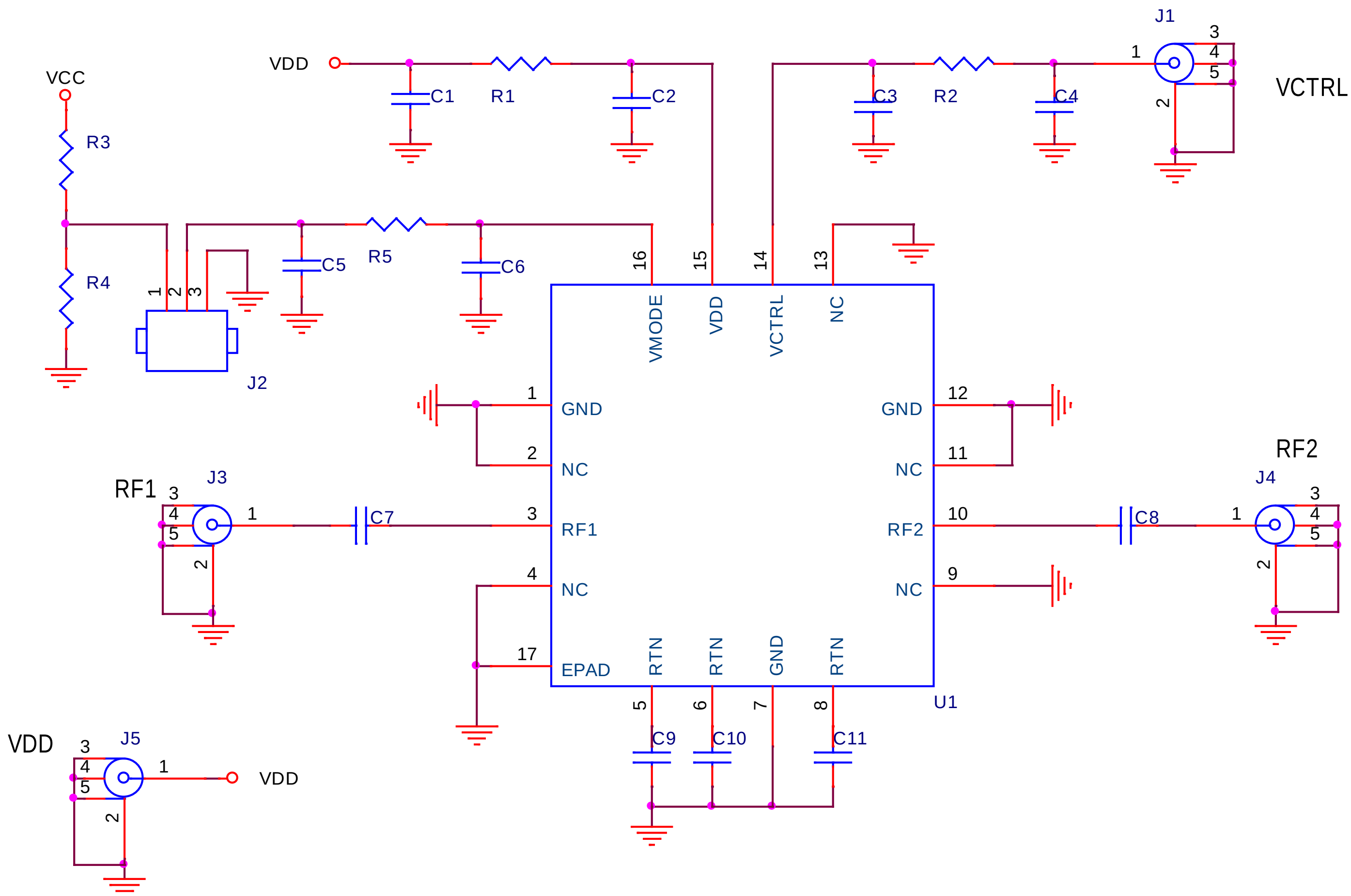
The supply pin should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

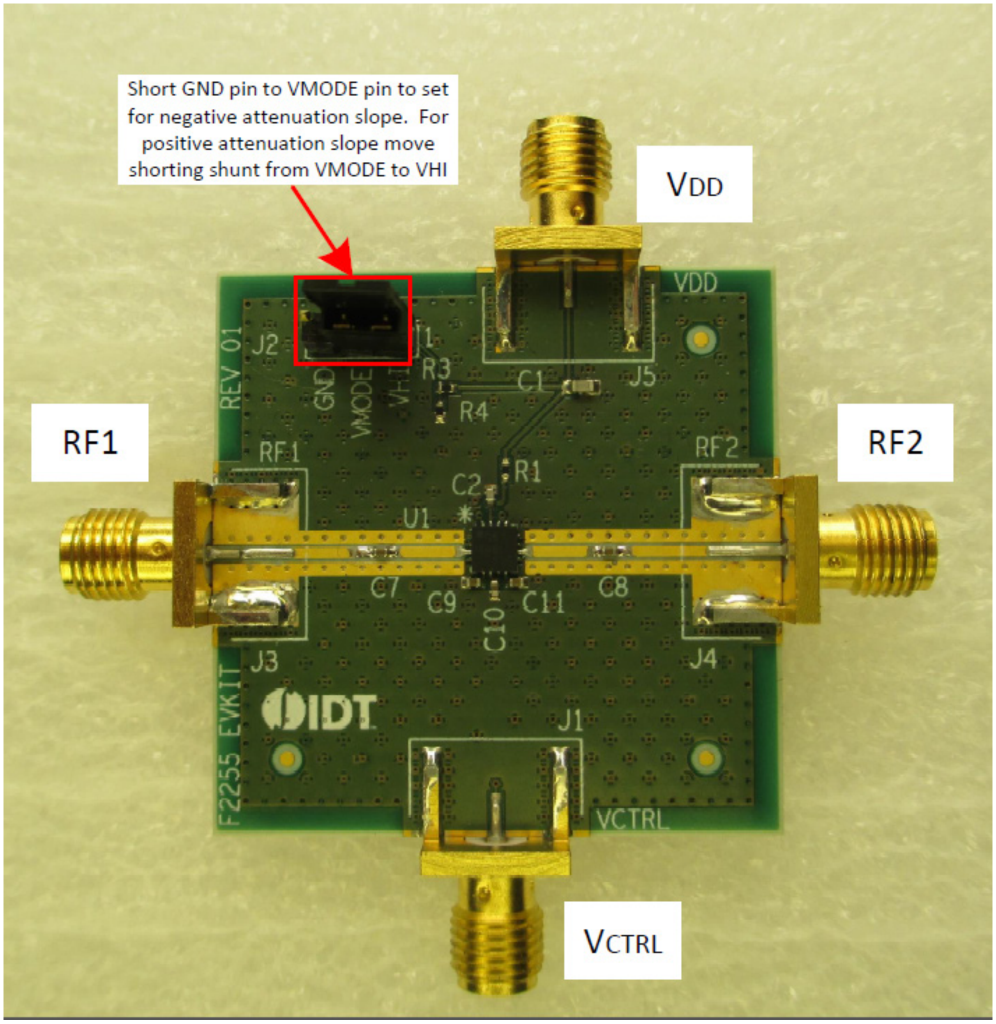
If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of control pins 14 and 16 is recommended as shown below.



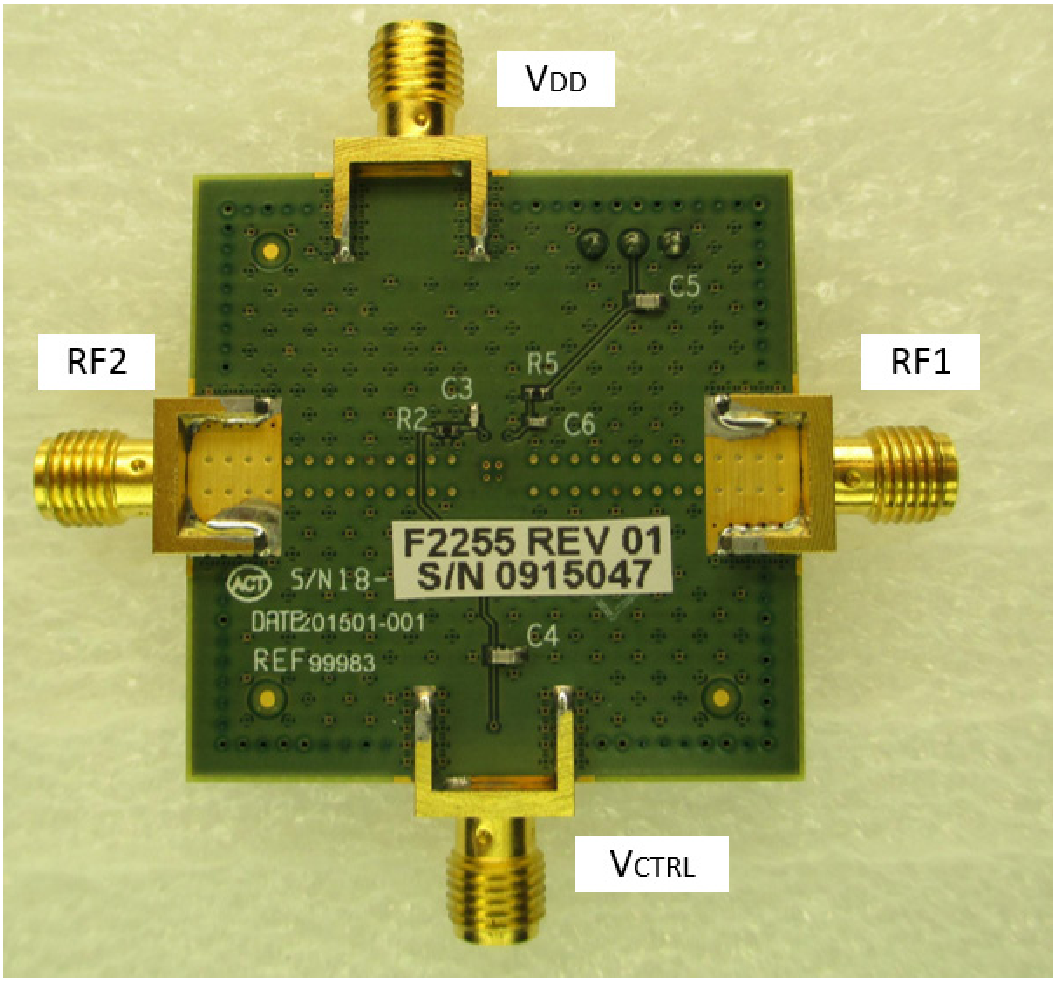
EVKIT / APPLICATIONS CIRCUIT



EVKIT PICTURE / LAYOUT (TOP VIEW)



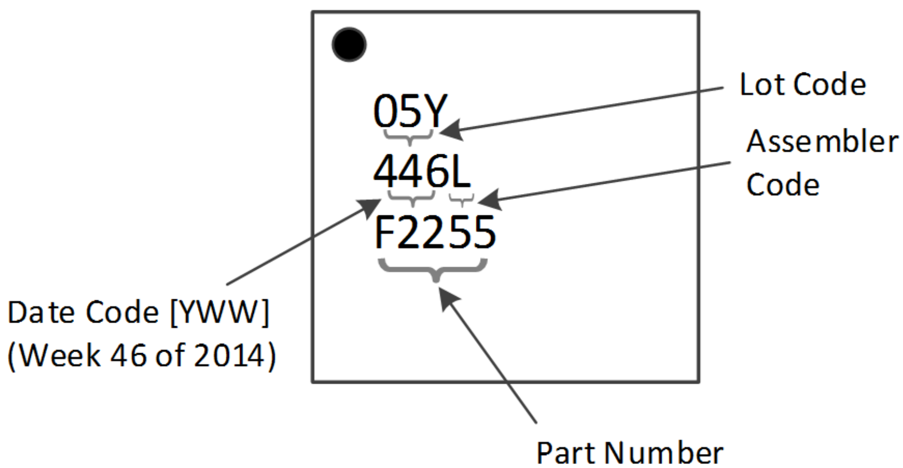
EVKIT PICTURE / LAYOUT (BOTTOM VIEW)



EVKIT BOM

Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
C1, C4, C5	3	10nF ±5%, 50V, X7R Ceramic Capacitors (0603)	GRM188R71H103J	Murata
C2, C3, C6	3	1000pF ±5%, 50V, C0G Ceramic Capacitors (0402)	GRM1555C1H102J	Murata
C7, C8, C9, C10, C11	5	100nF ±10%, 16V, X7R Ceramic Capacitors (0402)	GRM155R71C104K	Murata
R1, R2, R5	3	0Ω Resistors (0402)	ERJ-2GE0R00X	Panasonic
R3, R4	2	100kΩ ±1%, 1/10W, Resistors (0402)	ERJ-2RKF1003X	Panasonic
J1, J3, J4, J5	4	Edge Launch SMA (0.375 inch pitch ground tabs)	142-0701-851	Emerson Johnson
J2	1	CONN HEADER VERT SGL 3 X 1 POS GOLD	961103-6404-AR	3M
U1	1	Voltage Variable Attenuator	F2255NLGK	IDT
	1	Printed Circuit Board	F2255 REV 1	IDT

TOP MARKINGS



Revision History

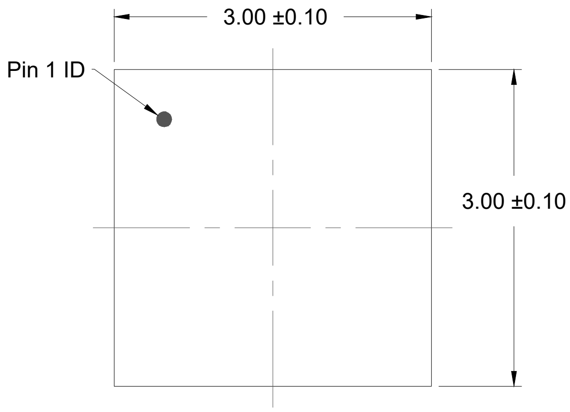
Revision Date	Description of Change
May 7, 2021	• Changed the corporate branding to Renesas. • Completed other minor changes.
February 9, 2018	Corrected POD drawing, added revision page.
January 30, 2017	Updated GBT limits for I_{DD}, V_{MODE} and V_{CTRL}.
November 5, 2015	Initial release.

Package Outline Drawing

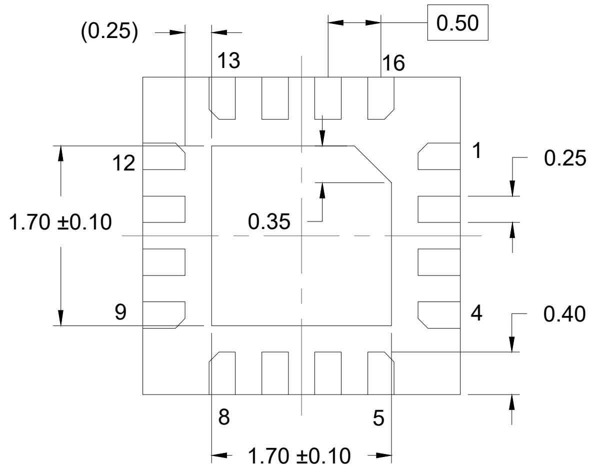
Package Code: NLG16P2

16-VFQFPN 3.0 x 3.0 x 0.9 mm Body, 0.5mm Pitch

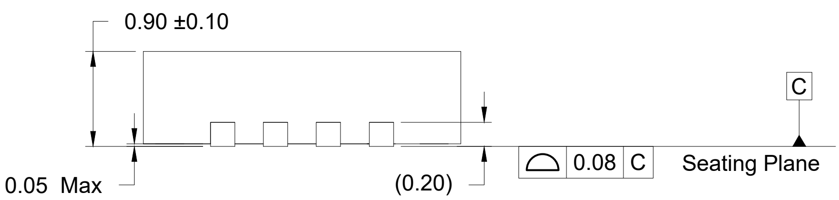
PSC-4169-02, Revision: 06, Date Created: Aug 18, 2023



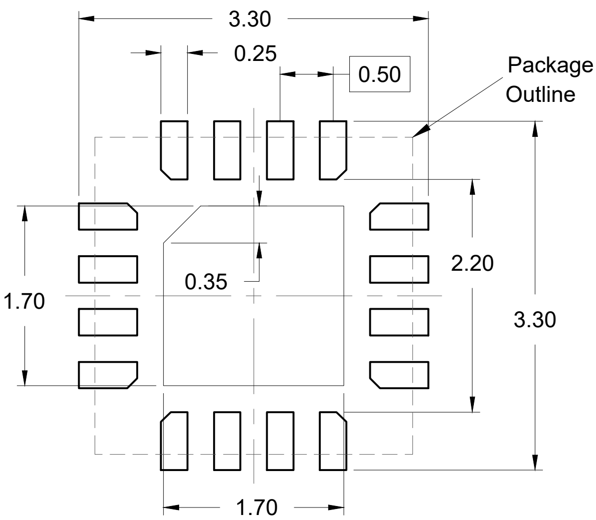
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.