

H5N5016PL-E0-E

500V - 50A - MOS FET
High Speed Power Switching

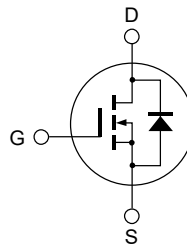
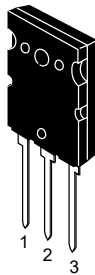
R07DS1200EJ0200
Rev.2.00
Nov.4.2021

Features

- Low on-resistance
 $R_{DS(on)} = 0.108 \Omega$ typ. (at $I_D = 25 \text{ A}$, $V_{GS} = 10 \text{ V}$, $T_a = 25^\circ\text{C}$)
- Low leakage current
- High speed switching
- Built-in fast recovery diode
- Quality grade: Standard

Outline

RENESAS Package code: PRSS0003ZN-A, PRSS0003ZC-A
(Package name:TO-264A, TO-264)



1. Gate
2. Drain
3. Source

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D	50	A
Drain peak current	I_D (pulse) ^{Notes1}	200	A
Body-drain diode reverse drain current	I_{DR}	50	A
Body-drain diode reverse drain peak current	I_{DR} (pulse) ^{Notes1}	200	A
Avalanche current	I_{AP} ^{Notes3}	10	A
Avalanche energy	E_{AR} ^{Notes3}	5.5	mJ
Channel dissipation	P_{ch} ^{Notes2}	250	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Note: Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect a reliability even if it is within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook (Recommendation for Handling and Usage of Semiconductor Devices) and individual reliability data .

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1 \%$
 2. Value at $T_c = 25^\circ\text{C}$
 3. $ST_{ch} = 25^\circ\text{C}$, $T_{ch} \leq 150^\circ\text{C}$

Thermal Resistance Characteristics

(Ta = 25 °C)

Item	Symbol	Max. Value ^{Notes4}	Unit
Channel to case thermal impedance	θ_{ch-c}	0.5	°C/W

Notes: 4. Designed target value on Renesas measurement condition. (Not tested)

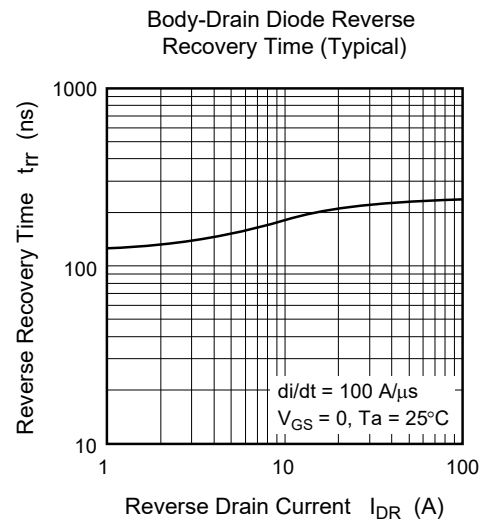
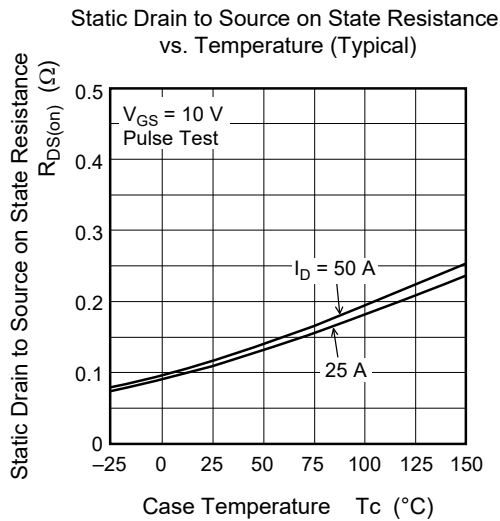
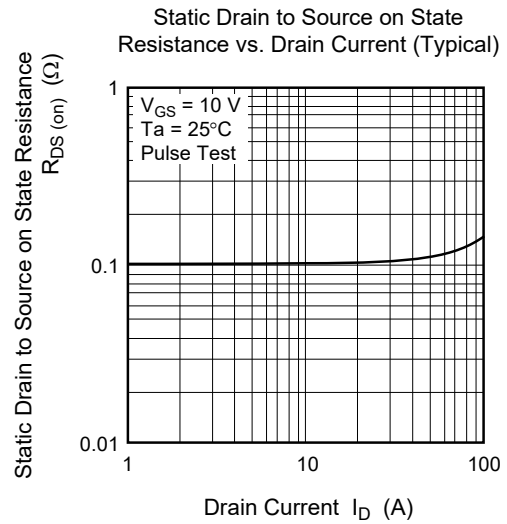
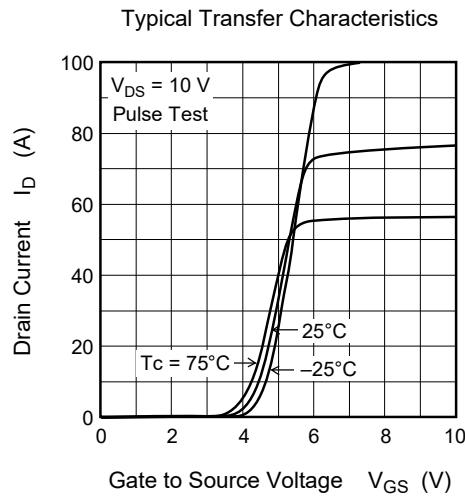
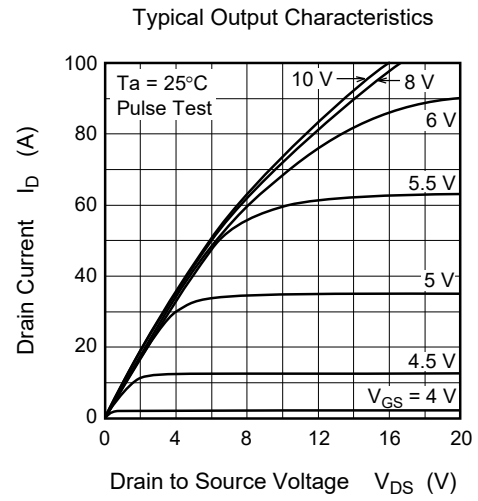
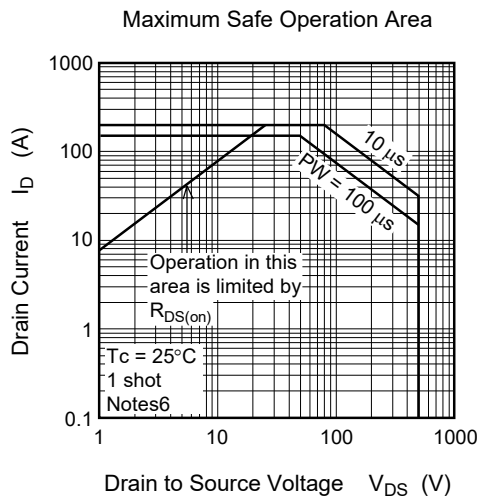
Electrical Characteristics

(Ta = 25 °C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 500 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	4.0	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	23	38	—	S	$I_D = 25 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Notes5}
Static drain to source on state resistance	$R_{DS(on)}$	—	0.108	0.128	Ω	$I_D = 25 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Notes5}
Input capacitance	C_{iss}	—	5300	—	pF	$V_{DS} = 25 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	720	—	pF	
Reverse transfer capacitance	C_{rss}	—	37	—	pF	
Turn-on delay time	$t_{d(on)}$	—	60	—	ns	$I_D = 25 \text{ A}$ $V_{GS} = 10 \text{ V}$ $R_L = 10 \Omega$ $R_g = 10 \Omega$
Rise time	t_r	—	190	—	ns	
Turn-off delay time	$t_{d(off)}$	—	250	—	ns	
Fall time	t_f	—	240	—	ns	
Total gate charge	Q_g	—	130	—	nC	$V_{DD} = 400 \text{ V}$ $V_{GS} = 10 \text{ V}$ $I_D = 50 \text{ A}$
Gate to source charge	Q_{gs}	—	25	—	nC	
Gate to drain charge	Q_{gd}	—	50	—	nC	
Body-drain diode forward voltage	V_{DF}	—	1.05	1.6	V	$I_F = 50 \text{ A}$, $V_{GS} = 0 \text{ V}$ ^{Notes5}
Body-drain diode reverse recovery time	t_{rr}	—	230	—	ns	$I_F = 50 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$
Body-drain diode reverse recovery charge	Q_{rr}	—	1.5	—	μC	

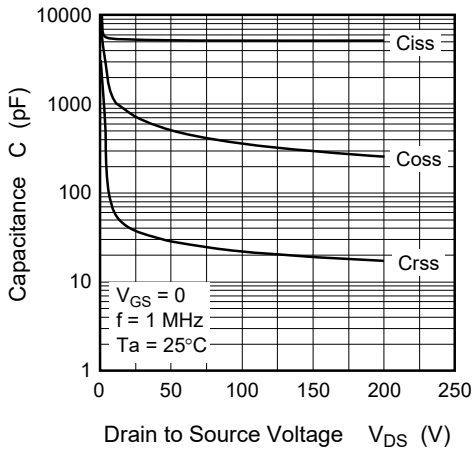
Notes: 5. Pulse test

Main Characteristics

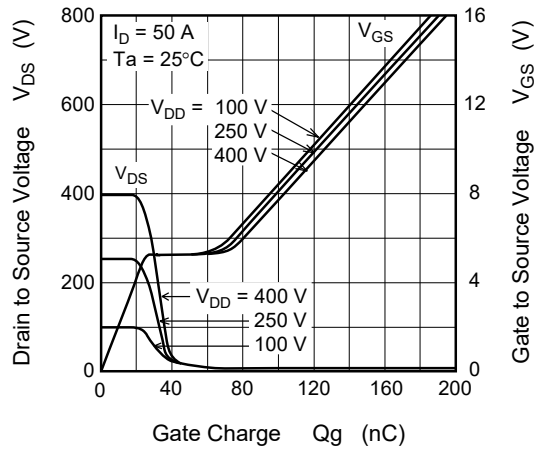


Notes: 6. Designed target value on Renesas measurement condition. (Not tested)
 Renesas recommends that operating conditions are designed according to a document "Power MOS FET · IGBT Attention of Handling Semiconductor Devices".

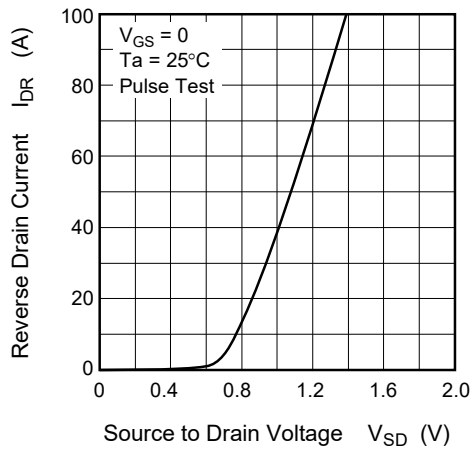
Typical Capacitance vs. Drain to Source Voltage



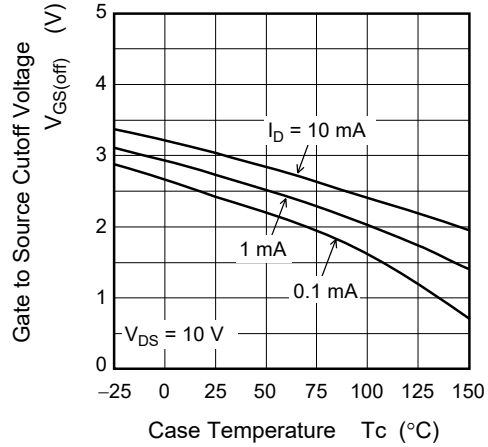
Dynamic Input Characteristics (Typical)

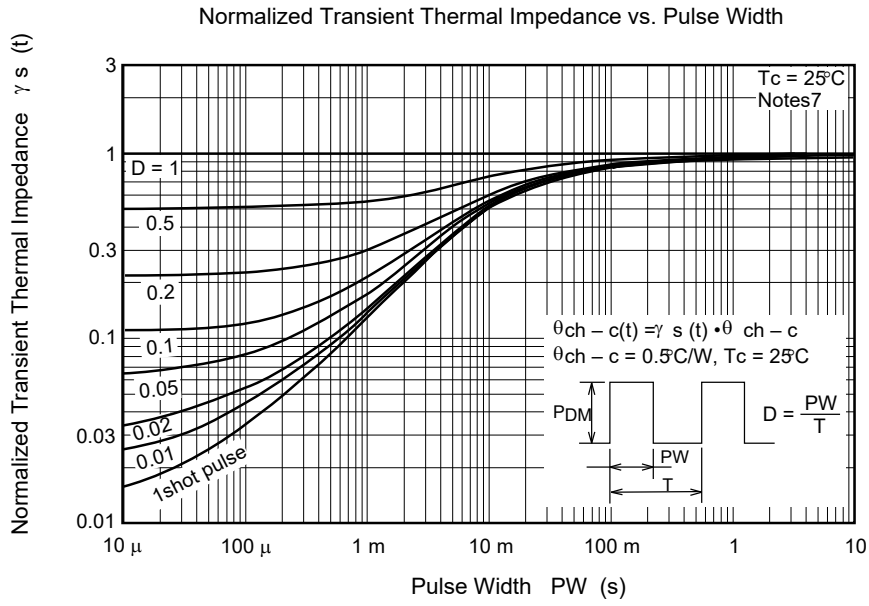


Reverse Drain Current vs. Source to Drain Voltage (Typical)

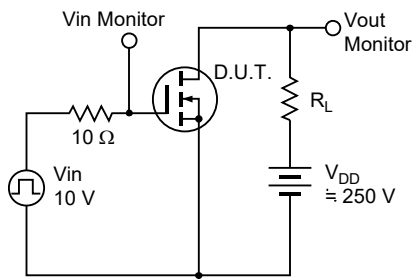


Gate to Source Cutoff Voltage vs. Case Temperature (Typical)

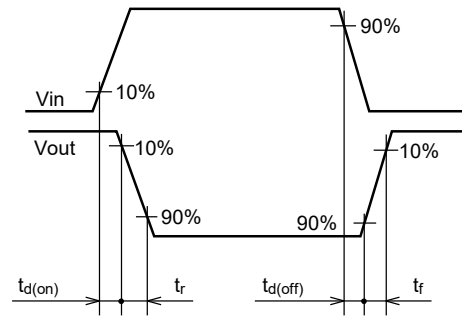




Switching Time Test Circuit



Waveform



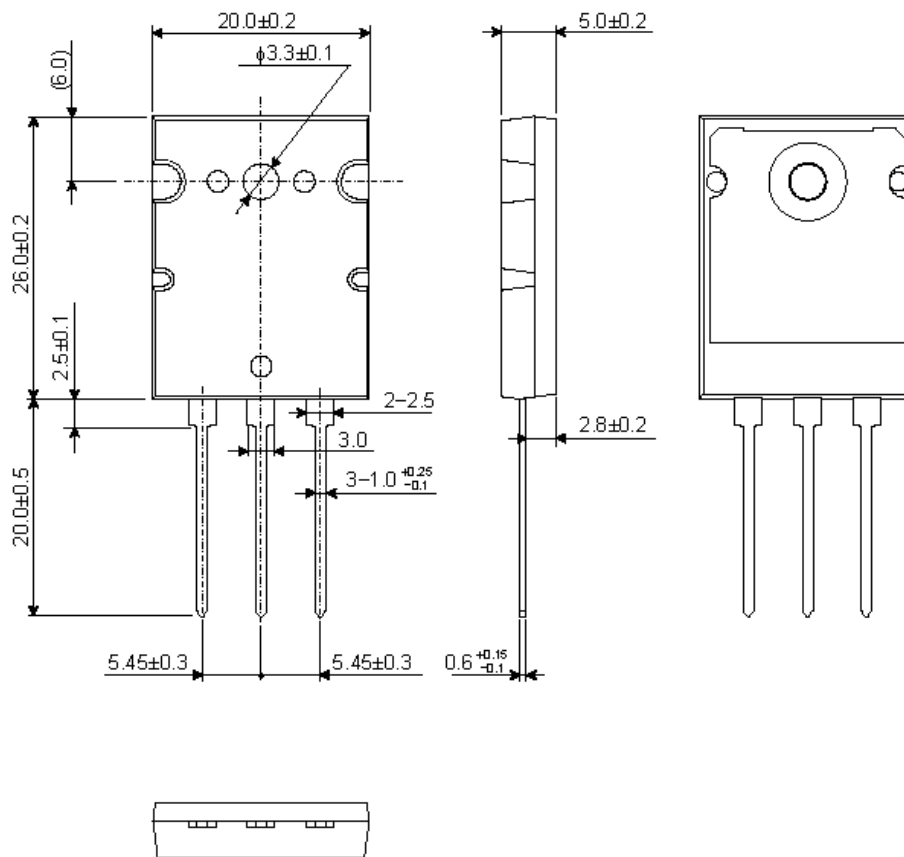
Notes: 7. Designed target value on Renesas measurement condition. (Not tested)

Package Dimensions

ASSEMBLED IN CHINA

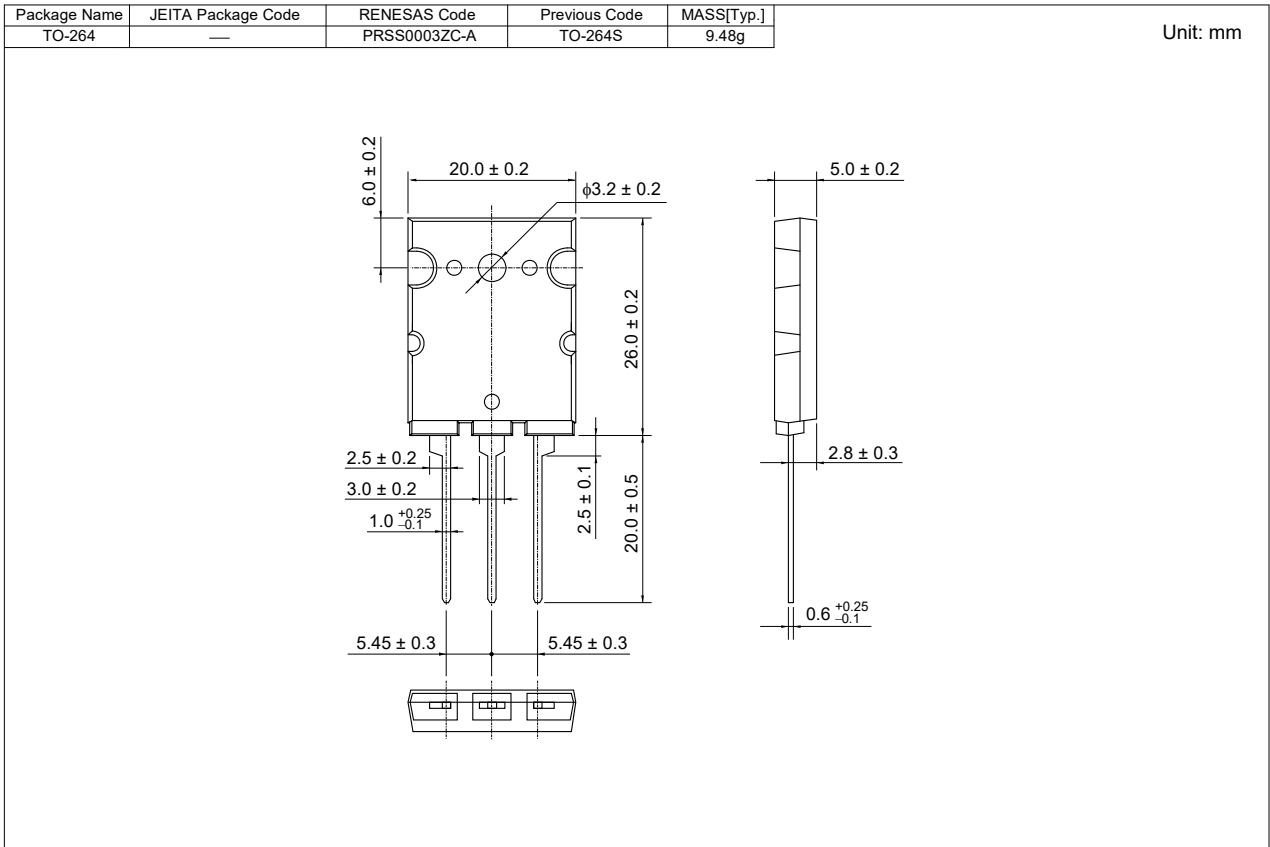
Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
TO-264A	—	PRSS0003ZN-A	TO-264A	9.7

Unit: mm



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ASSEMBLED IN KOREA



Ordering Information

Orderable Part No.	Quantity	Shipping Container
H5N5016PL-E0-E#T2	25 pcs	Tube

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