

## HA4344B

350MHz, 4x1 Video Crosspoint Switch with Synchronous Controls

FN3956  
 Rev 4.00  
 June 1, 2006

The HA4344B is a very wide bandwidth 4x1 crosspoint switch ideal for professional video switching, HDTV, computer display routing, and other high performance applications. This circuit features very low power dissipation, excellent differential gain and phase, high off isolation, symmetric slew rates, fast switching, and latched control signals. When disabled, the output is switched to a high impedance state, making the HA4344B ideal for matrix routers.

The latched control signals allow for synchronized channel switching. When  $\overline{CK1}$  is low, the master control latch loads the next switching address ( $A0$ ,  $A1$ ,  $\overline{CS}$ ), while the closed (assuming  $\overline{CK2}$  is the inverse of  $\overline{CK1}$ ) slave control latch maintains the crosspoint in its current state.  $\overline{CK2}$  switching low closes the master latch (with previous assumption), loads the now open slave latch, and switches the crosspoint to the newly selected channel. Channel selection is asynchronous (changes with any control signal change) if both  $\overline{CK1}$  and  $\overline{CK2}$  are low.

### Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA4344BCB	HA4344BCB	0 to 70	16 Ld SOIC	M16.15
HA4344BCBZ (Note)	4344BCBZ	0 to 70	16 Ld SOIC (Pb-free)	M16.15
HA4344BCBZ96 (Note)	4344BCBZ	0 to 70	16 Ld SOIC Tape & Reel (Pb-free)	M16.15

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

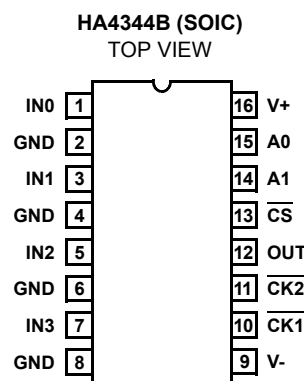
### Features

- Low Power Dissipation . . . . . 105mW
- Symmetrical Slew Rates . . . . . 1400V/μs
- 0.1dB Gain Flatness . . . . . 100MHz
- -3dB Bandwidth . . . . . 350MHz
- Off Isolation (100MHz) . . . . . 70dB
- Crosstalk Rejection (30MHz) . . . . . 80dB
- Differential Gain and Phase . . . . . 0.01%/0.01°
- High ESD Rating . . . . . >2000V
- TTL Compatible Control Signals
- Latched Control Lines for Synchronous Switching
- Pb-Free Plus Anneal Available (RoHS Compliant)

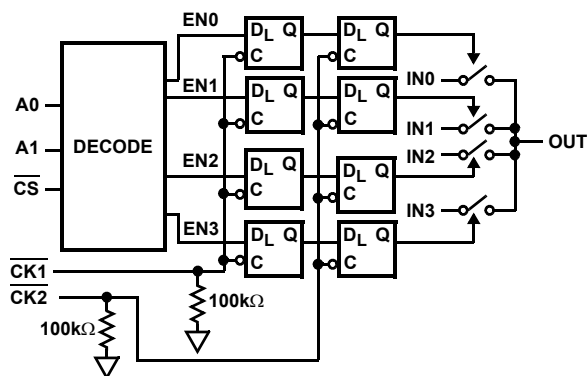
### Applications

- Professional Video Switching and Routing
- RGB Video Distribution Systems
- Computer Graphics
- RF Switching and Routing

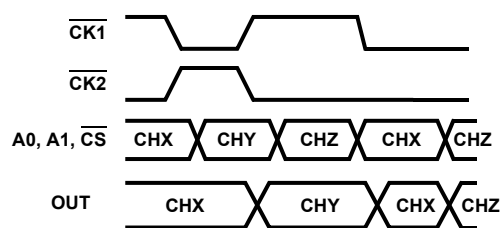
### Pinout



### Functional Diagram



### Timing Diagram



**Absolute Maximum Ratings**

Voltage Between V+ and V-	12V
Input Voltage	$V_{SUPPLY}$
Digital Input Current (Note 2)	$\pm 25\text{mA}$
Analog Input Current (Note 2)	$\pm 5\text{mA}$
Output Current	20mA
ESD Rating	
Human Body Model (Per MIL-STD-883 Method 3015.7)	2000V

**Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ ( $^{\circ}\text{C}/\text{W}$ )
SOIC Package	110
Maximum Junction Temperature (Die)	175 $^{\circ}\text{C}$
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}\text{C}$
Maximum Storage Temperature Range	-65 $^{\circ}\text{C}$ to 150 $^{\circ}\text{C}$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}\text{C}$ (SOIC - Lead Tips Only)

**Operating Conditions**

Temperature Range	0 $^{\circ}\text{C}$ to 70 $^{\circ}\text{C}$
-------------------	---

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**NOTES:**

- $\theta_{JA}$  is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief 379 for details.
- If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.

**Electrical Specifications**  $V_{SUPPLY} = \pm 5\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{CS} = 0.8\text{V}$ , Unless Otherwise Specified

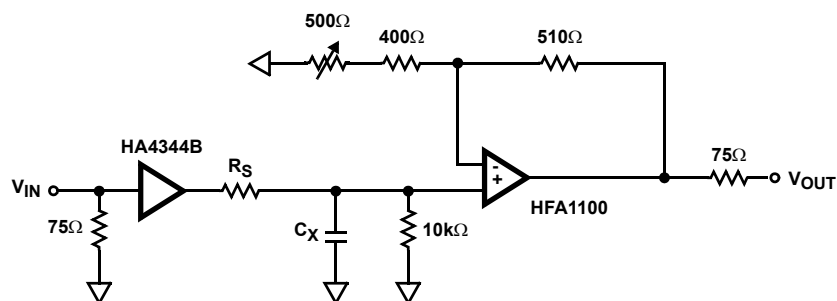
PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP. ( $^{\circ}\text{C}$ )	MIN	TYP	MAX	UNITS
<b>DC SUPPLY CHARACTERISTICS</b>						
Supply Voltage		Full	$\pm 4.5$	$\pm 5.0$	$\pm 5.5$	V
Supply Current ( $V_{OUT} = 0\text{V}$ )	$V_{CS} = 0.8\text{V}$	25, 70	-	10.5	13	mA
	$V_{CS} = 0.8\text{V}$	0	-	-	15.5	mA
	$V_{CS} = 2.0\text{V}$	25, 70	-	400	450	$\mu\text{A}$
	$V_{CS} = 2.0\text{V}$	0	-	400	580	$\mu\text{A}$
<b>ANALOG DC CHARACTERISTICS</b>						
Output Voltage Swing Without Clipping	$V_{OUT} = V_{IN} \pm V_{IO} \pm 20\text{mV}$	25, 70	$\pm 2.7$	$\pm 2.8$	-	V
		0	$\pm 2.4$	$\pm 2.5$	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	$\mu\text{A}$
Output Offset Voltage		Full	-10	-	10	mV
Output Offset Voltage Drift (Note 3)		Full	-	25	50	$\mu\text{V}/^{\circ}\text{C}$
<b>SWITCHING CHARACTERISTICS</b>						
Turn-On Time		25	-	160	-	ns
Turn-Off Time		25	-	320	-	ns
Output Glitch During Switching		25	-	$\pm 10$	-	mV
<b>DIGITAL DC CHARACTERISTICS</b>						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
$\overline{\text{CLK1}}$ , $\overline{\text{CLK2}}$ Input Current	0 to 4V	Full	-	40	50	$\mu\text{A}$
$\overline{\text{CS}}$ , A0, A1 Input Current	0 to 4V	Full	-2	-	2	$\mu\text{A}$
<b>AC CHARACTERISTICS</b>						
Insertion Loss	1V <sub>P-P</sub>	25	-	0.055	0.063	dB
		Full	-	0.07	0.08	dB
Channel-to-Channel Insertion Loss Match		Full	-	$\pm 0.004$	$\pm 0.006$	dB

**Electrical Specifications**  $V_{\text{SUPPLY}} = \pm 5\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{\text{CS}} = 0.8\text{V}$ , Unless Otherwise Specified **(Continued)**

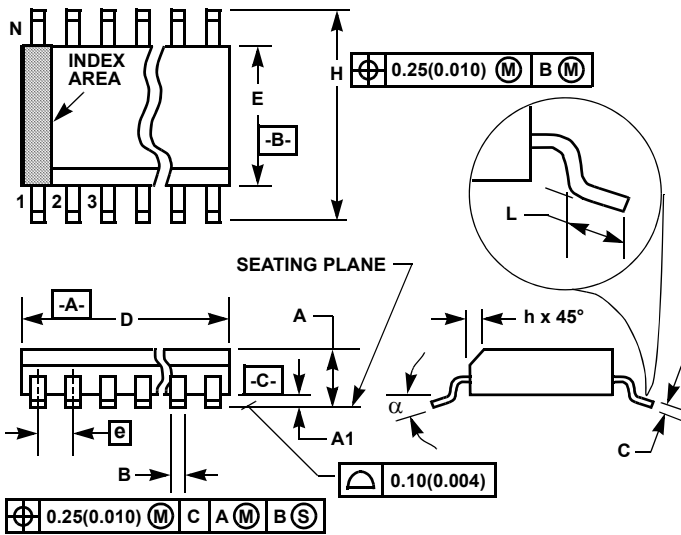
PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP. (°C)	MIN	TYP	MAX	UNITS
-3dB Bandwidth	$R_S = 47\Omega$ , $C_L = 10\text{pF}$	25	-	350	-	MHz
	$R_S = 29\Omega$ , $C_L = 20\text{pF}$	25	-	300	-	MHz
	$R_S = 16\Omega$ , $C_L = 33\text{pF}$	25	-	220	-	MHz
	$R_S = 9\Omega$ , $C_L = 52\text{pF}$	25	-	160	-	MHz
$\pm 0.1\text{dB}$ Flat Bandwidth	$R_S = 47\Omega$ , $C_L = 10\text{pF}$	25	-	150	-	MHz
	$R_S = 29\Omega$ , $C_L = 20\text{pF}$	25	-	110	-	MHz
	$R_S = 16\Omega$ , $C_L = 33\text{pF}$	25	-	100	-	MHz
	$R_S = 9\Omega$ , $C_L = 52\text{pF}$	25	-	70	-	MHz
Input Resistance		Full	200	400	-	$\text{k}\Omega$
Input Capacitance		Full	-	1.5	-	$\text{pF}$
Enabled Output Resistance		Full	-	15	-	$\Omega$
Disabled Output Capacitance	$V_{\text{CS}} = 2.0\text{V}$	Full	-	2.5	-	$\text{pF}$
Differential Gain	4.43MHz (Note 3)	25	-	0.01	0.02	%
Differential Phase	4.43MHz (Note 3)	25	-	0.01	0.02	°
Off Isolation	$1V_{\text{P-P}}$ , 100MHz, $V_{\text{CS}} = 2.0\text{V}$	Full	-	70	-	dB
Crosstalk Rejection	$1V_{\text{P-P}}$ , 30MHz	Full	-	80	-	dB
Slew Rate ( $1.5V_{\text{P-P}}$ , +SR/-SR)	$R_S = 47\Omega$ , $C_L = 10\text{pF}$	25	-	1400/1490	-	$\text{V}/\mu\text{s}$
	$R_S = 29\Omega$ , $C_L = 20\text{pF}$	25	-	1200/1260	-	$\text{V}/\mu\text{s}$
	$R_S = 16\Omega$ , $C_L = 33\text{pF}$	25	-	870/940	-	$\text{V}/\mu\text{s}$
	$R_S = 9\Omega$ , $C_L = 52\text{pF}$	25	-	750/710	-	$\text{V}/\mu\text{s}$
Total Harmonic Distortion (Note 3)		Full	-	0.01	0.1	%
Disabled Output Resistance	$V_{\text{CS}} = 2.0\text{V}$	Full	-	12	-	$\text{M}\Omega$

## NOTES:

- This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
- Units are 100% tested at 25°C; guaranteed, but not tested at 0°C and 70°C.

**AC Test Circuit**NOTE:  $C_L = C_X + \text{Test Fixture Capacitance}$ .

**Small Outline Plastic Packages (SOIC)**



**M16.15 (JEDEC MS-012-AC ISSUE C)  
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 1 6/05

© Copyright Intersil Americas LLC 2002-2006. All Rights Reserved.  
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see [www.intersil.com/en/products.html](http://www.intersil.com/en/products.html)

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at [www.intersil.com/en/support/qualandreliability.html](http://www.intersil.com/en/support/qualandreliability.html)

*Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)