To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD151011

Dual BCD Programmable Counter with Synchronous Preset Enable

REJ03D0298–0200Z
(Previous ADE-205-100 (Z))
Rev.2.00
Jul.16.2004

Description

The HD151011 has BCD decimal two digits down counter and D-type Flip Flop. The counter can set up to max 99 counts and synchronous preset ($\overline{SPE}$) input can preset the data. When the count value is 0, the next clock pulse presets the data to invert the output. D-type Flip Flop takes the counter output as clock pulse, whose data is transferred to output at the rise edge. It is applied to generate AC signal for STN type liquid crystal and general-use divider.

Features

- High speed operation
  tpd (CLK or $\overline{CLK}$ to Q) = 35 ns (typ)
- High output current
  Fanout of 10 LS TTL Loads
- Wide operating voltage
  V_{CC} = 2 to 6 V
- Low supply current (Ta = 25°C)
  I_{CC} (Static) = 4 µA (max)

- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD151011FPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD151011TELL	TSSOP-20 pin	TTP-20DAV	T	ELL (2,000 pcs/reel)

Note: Please consults the sales office for the above package availability.

Function Table

Control Inputs				Mode	Operation Description
CLR	PR	$\overline{SPE}$	C/$\overline{T}$		
H	H	H	X	Generally count	Down count at the rise edge of clock (CLK) Down count at the fall edge of clock ($\overline{CLK}$)
X	X	L	X	Synchronous preset	Jn data is preset at the rise of clock (CLK), the fall of clock ($\overline{CLK}$)
—	—	—	H	—	Clock inputs (CLK, $\overline{CLK}$) is CMOS level
—	—	—	L	—	Clock inputs (CLK, $\overline{CLK}$) is TTL level
L	H	—	—	Initialize of Q output	Initialize of Q = “L”
H	L	—	—	Initialize of Q output	Initialize of Q = “H”

Note: 1. Synchronous preset ($\overline{SPE}$) input can set max 99 down counts.
2. When the count value is 0, the next clock pulse presets the data to invert the output.
3. CLR and PR inputs initialize output state.
4. Clock inputs (CLK, $\overline{CLK}$) is selectable CMOS level (V_{CC} = 2.0 to 6.0 V) and TTL level (V_{CC} = 4.5 to 5.5V) (Jn, C/$\overline{T}$, PR, CLR and SPE inputs are CMOS level)

Don't set data exceeding 99 to Jn. (J0 : LSB, J7 : MSB)

H : High level
L : Low level
X : Immaterial
— : Irrespective of condition

Pin Arrangement

(Top view)

Pin Description

Pin Name		Pin Description	
Input pins	J0 to J7	Count data input for option	
	C/$\overline{T}$	Level change input for CLK, $\overline{CLK}$ (CMOS level or TTL level)	
	CLK, $\overline{CLK}$	Clock inputs	CLK : Rise edge trigger $\overline{CLK}$: Fall edge trigger
	$\overline{SPE}$	Preset input for Jn data	
	PR	Preset input for D-type Flip Flop (Initialize “L” at Q output)	
	CLR	Clear input for D-type Flip Flop (Initialize “H” at Q output)	
Output pins	$\overline{CO}$	Output for BCD decimal counter	
	Q	Output for D-type Flip Flop	

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	–0.5 to 7.0	V
Input/output voltage	V_{IN}/V_{OUT}	–0.5 to V_{CC} +0.5	V
V_{CC}, GND current	I_{CC}, I_{GND}	±50	mA
Output current/pin	I_{OUT}	±25	mA
Power dissipation	P_T	757	mW
Storage temperature	Tstg	–65 to 150	°C
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA

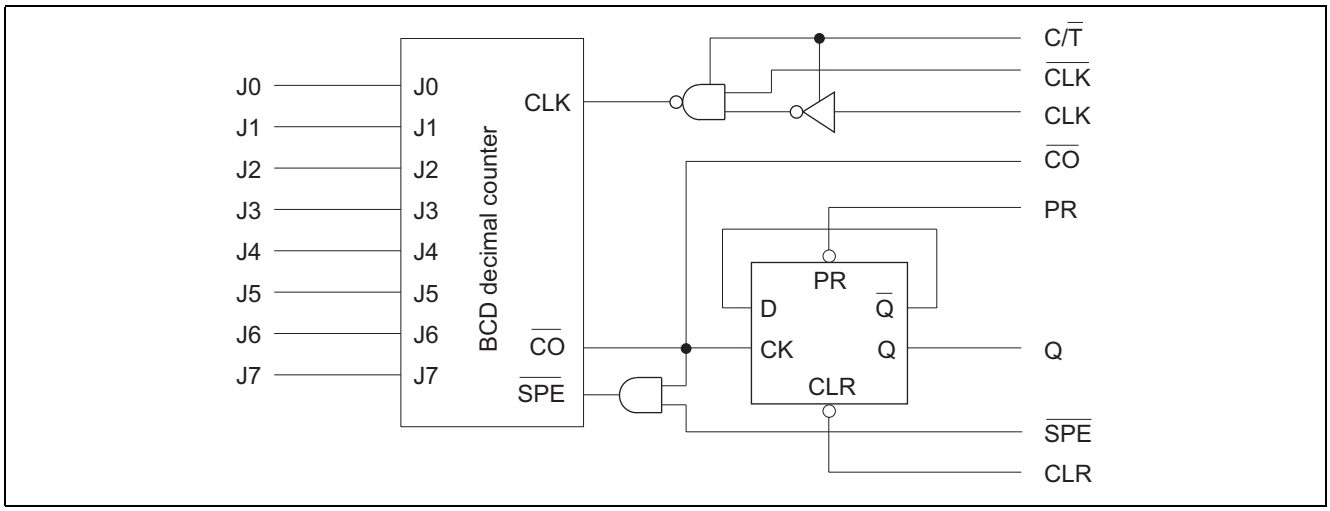
Notes: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.
2. All voltage values except for differential input voltage are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	2	—	6	V
Input/output voltage		$V_{IN}/_{OUT}$	0	—	V_{CC}	V
Operating temperature		Topr	–40	—	+85	°C
Input rise/fall time*[1]	V_{CC} = 2.5 V	t_r, t_f	0	—	1000	ns
	V_{CC} = 4.5 V		0	—	500	
	V_{CC} = 5.5 V		0	—	400	

Note: 1. This item guarantees maximum limit when one input switches.

Logic Diagram



Electrical Characteristics

Item	Sym-bol	V_{CC}	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
High level input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V	J0 to J7 C/T, $\overline{SPE}$ PR, CLR	
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
		2.0	1.5	—	—	1.5	—		$\overline{CLK}$, CLK	C/$\overline{T}$ = V_{IH}
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
		4.5 to 5.5	2.0	—	—	2.0	—			C/$\overline{T}$ = V_{IL}
Low level input voltage	V_{IL}	2.0	—	—	0.5	—	0.5	V	J0 to J7 C/T, $\overline{SPE}$ PR, CLR	
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
		2.0	—	—	0.5	—	0.5		$\overline{CLK}$, CLK	C/$\overline{T}$ = V_{IH}
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
		4.5 to 5.5	—	—	0.8	—	0.8			C/$\overline{T}$ = V_{IL}
High level output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –20 mA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	4.31	—	4.13	—			I_{OH} = –4 mA
		6.0	5.68	5.80	—	5.63	—			I_{OH} = –5.2 mA
Low level output voltage	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 mA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	0.17	0.26	—	0.33			I_{OL} = 4 mA
		6.0	—	0.18	0.26	—	0.33			I_{OL} = 5.2 mA
Input capacitance	I_{IN}	6.0	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
Supply current	I_{CC}	6.0	—	—	4.0	—	40.0	µA	V_{IN} = V_{CC} or GND	

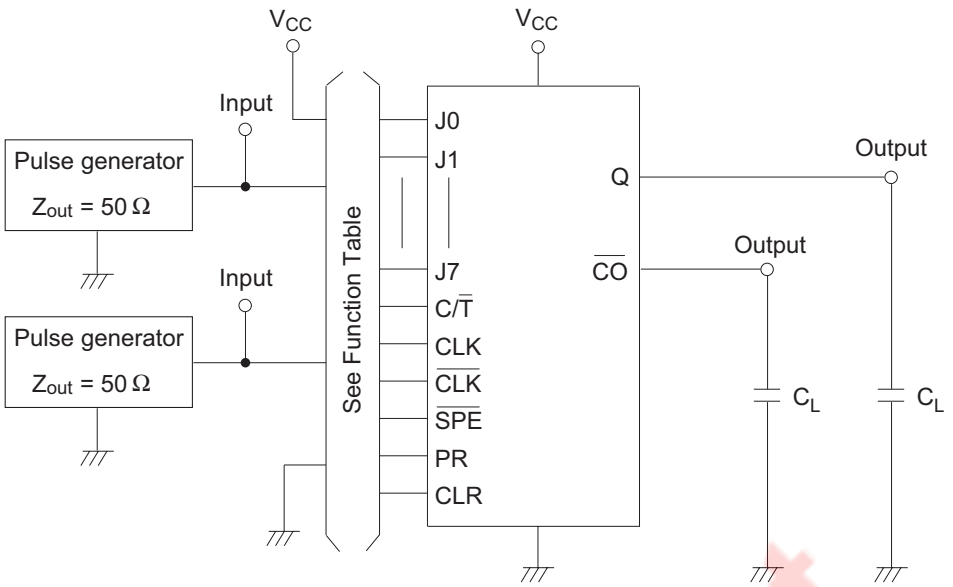
Switching Characteristics (C_L = 50 pF, t_r = t_f = 6 ns)

Item	Symbol	V_{CC}	Ta = 25°C			Ta = –40 to 85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	4	—	3	MHz	
		4.5	—	36	20	—	16		
		6.0	—	—	24	—	19		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	30	75	—	95	ns	
		4.5	—	8	15	—	19		
		6.0	—	7	13	—	16		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	250	—	318	ns	CLK or $\overline{CLK}$ to $\overline{CO}$
		4.5	—	30	50	—	63		
		6.0	—	—	45	—	53		
	t_{PLH} t_{PHL}	2.0	—	—	300	—	380		CLK or $\overline{CLK}$ to Q
		4.5	—	35	60	—	75		
		6.0	—	—	53	—	65		
	t_{PLH} t_{PHL}	2.0	—	—	150	—	185		PR or $\overline{CLK}$ to Q
		4.5	—	18	30	—	38		
		6.0	—	—	25	—	32		
Pulse width (CLK, CLK, PR, CLR)	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	—	—	20	—		
		6.0	14	—	—	17	—		
Setup time (Jn - CLK, CLK) (SPE, CLK, CLK)	t_s	2.0	100	—	—	125	—	ns	
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Hold time (Jn - CLK, CLK) (SPE, CLK, CLK)	t_h	2.0	15	—	—	15	—	ns	
		4.5	10	—	—	10	—		
		6.0	5	—	—	5	—		
Input capacitance	C_{IN}	—	—	5	10	—	10	pF	
Power dissipation capacitance*[1]	C_{PD}	—	—	48	—	—	—	pF	

Note: 1. CPD is equivalent capacitance inside of the IC calculated from the operating current without load (see test circuit). The average operating current without load is calculated according to the expression below.

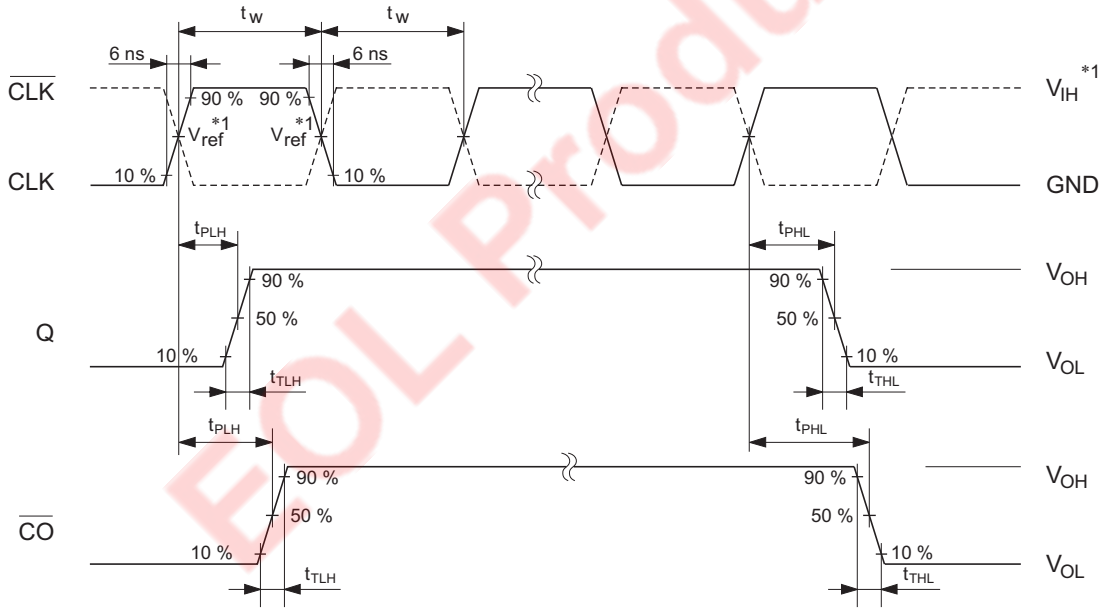
I_{CC} (opr) = C_{PD} • V_{CC} • f_{IN} + I_{CC}

Test Circuit



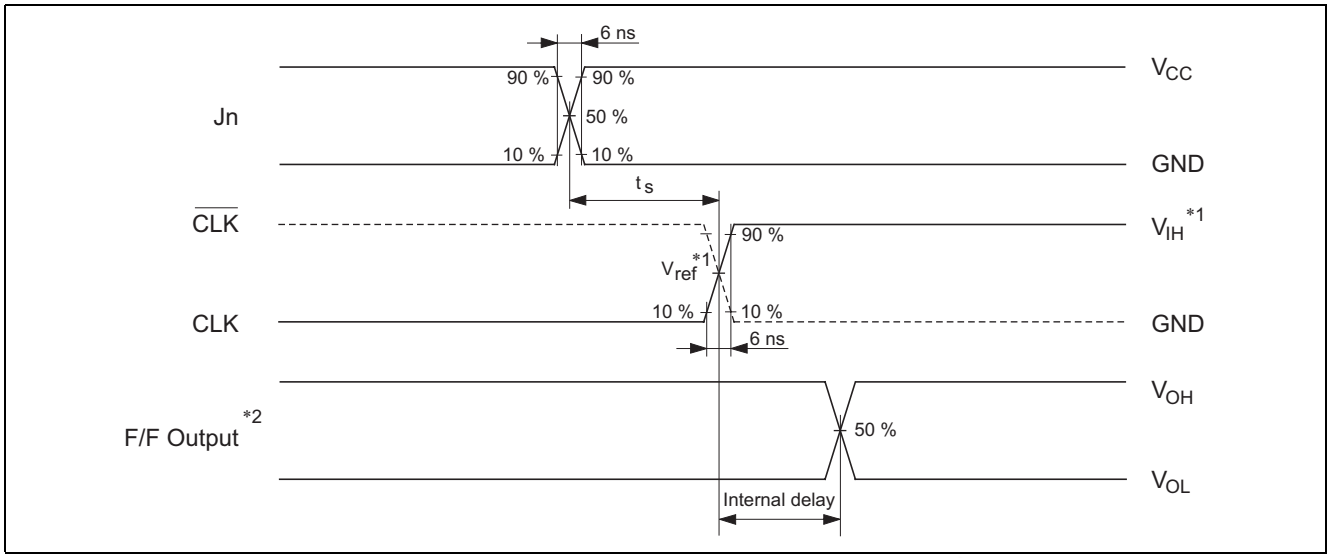
Note: 1. C_L includes probe and jig capacitance.

Waveforms – 1

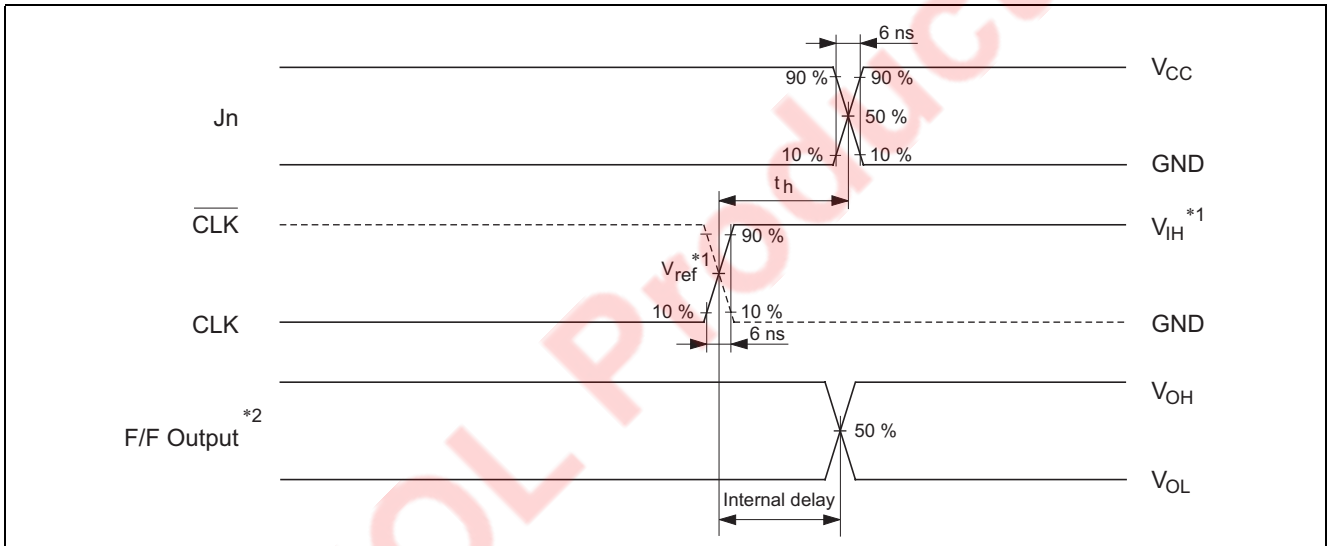


Note: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/$\overline{T}$ = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is V_{CC} × 50%

Waveforms – 2

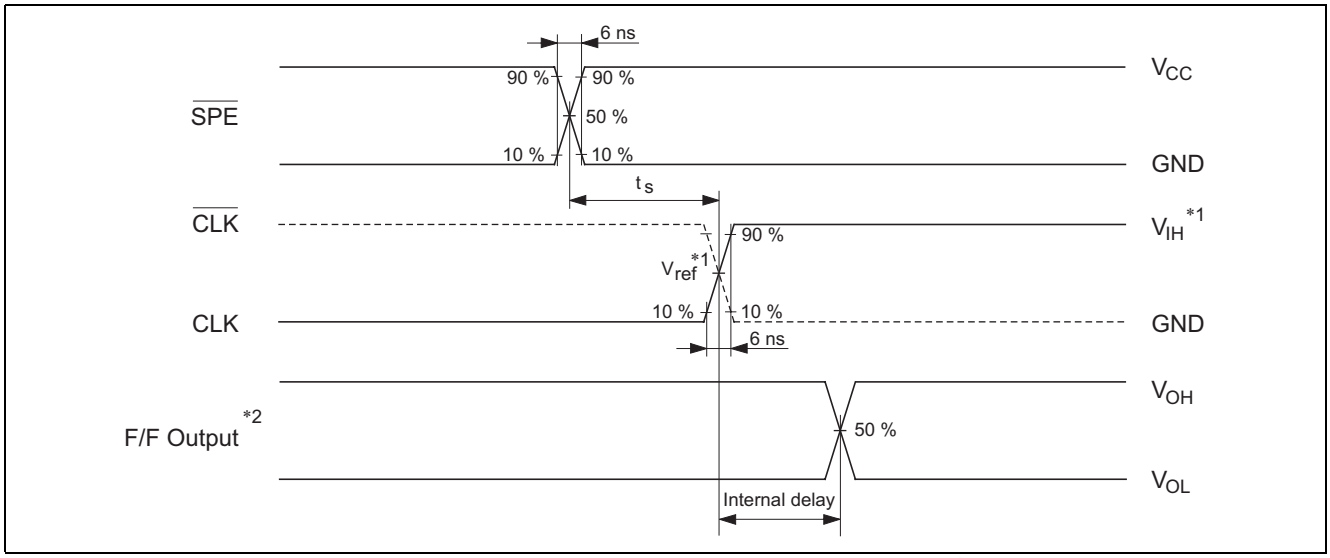


Waveforms – 3

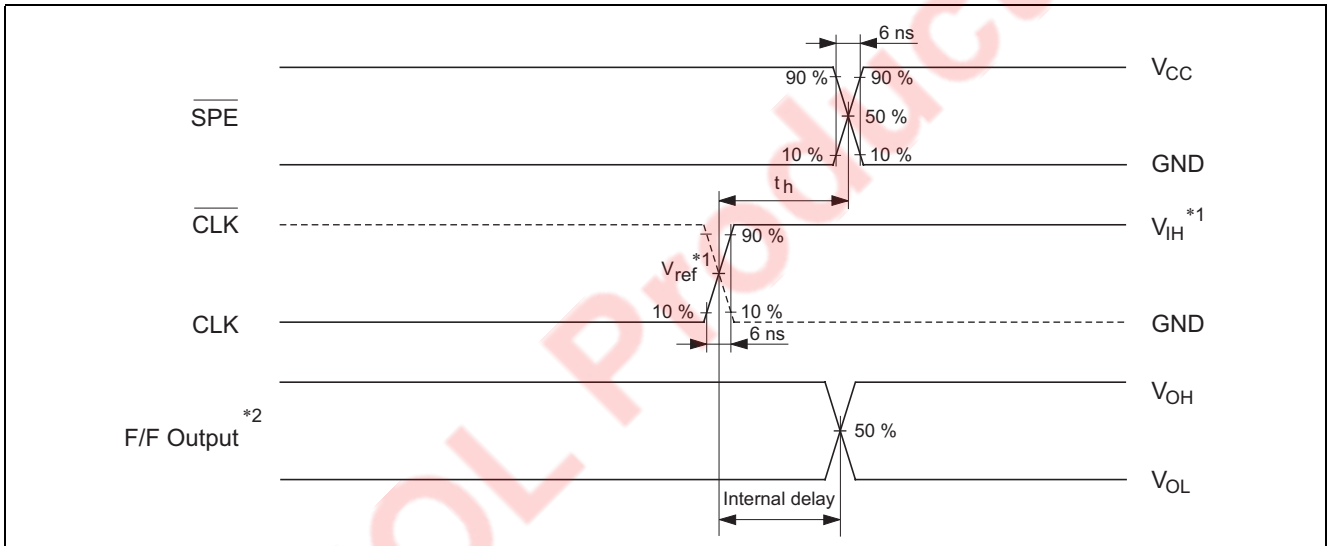


Notes: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/$\overline{T}$ = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is $V_{CC} \times 50\%$
2. F/F output is internal signal of IC.

Waveforms – 4

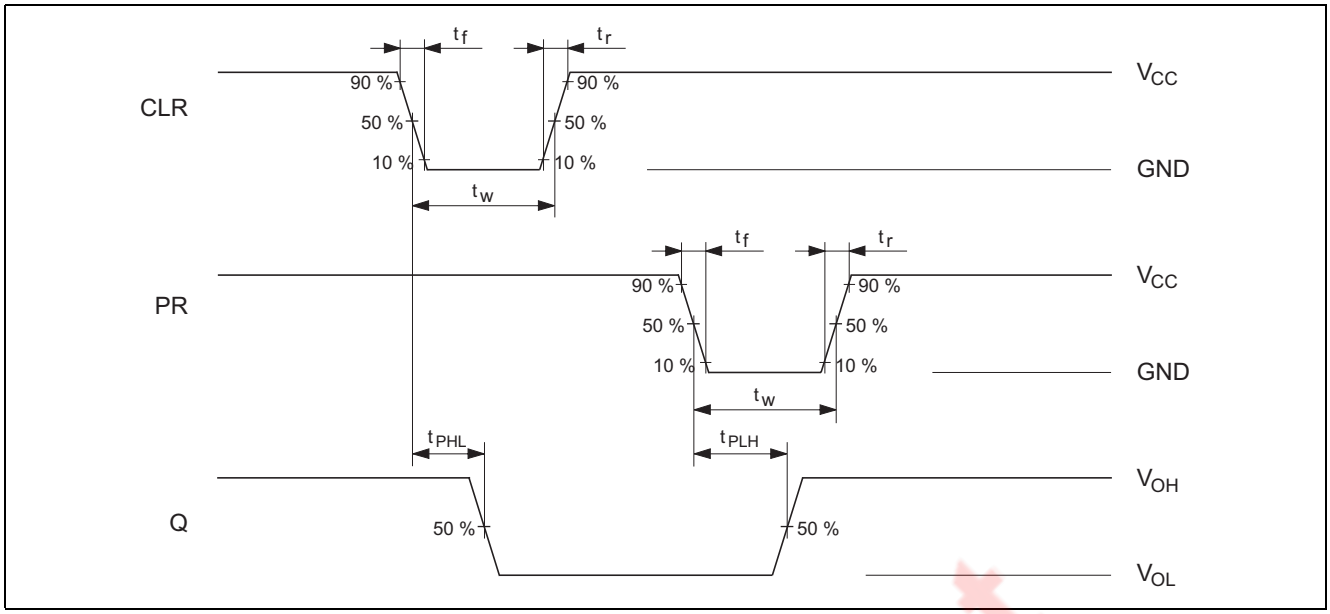


Waveforms – 5

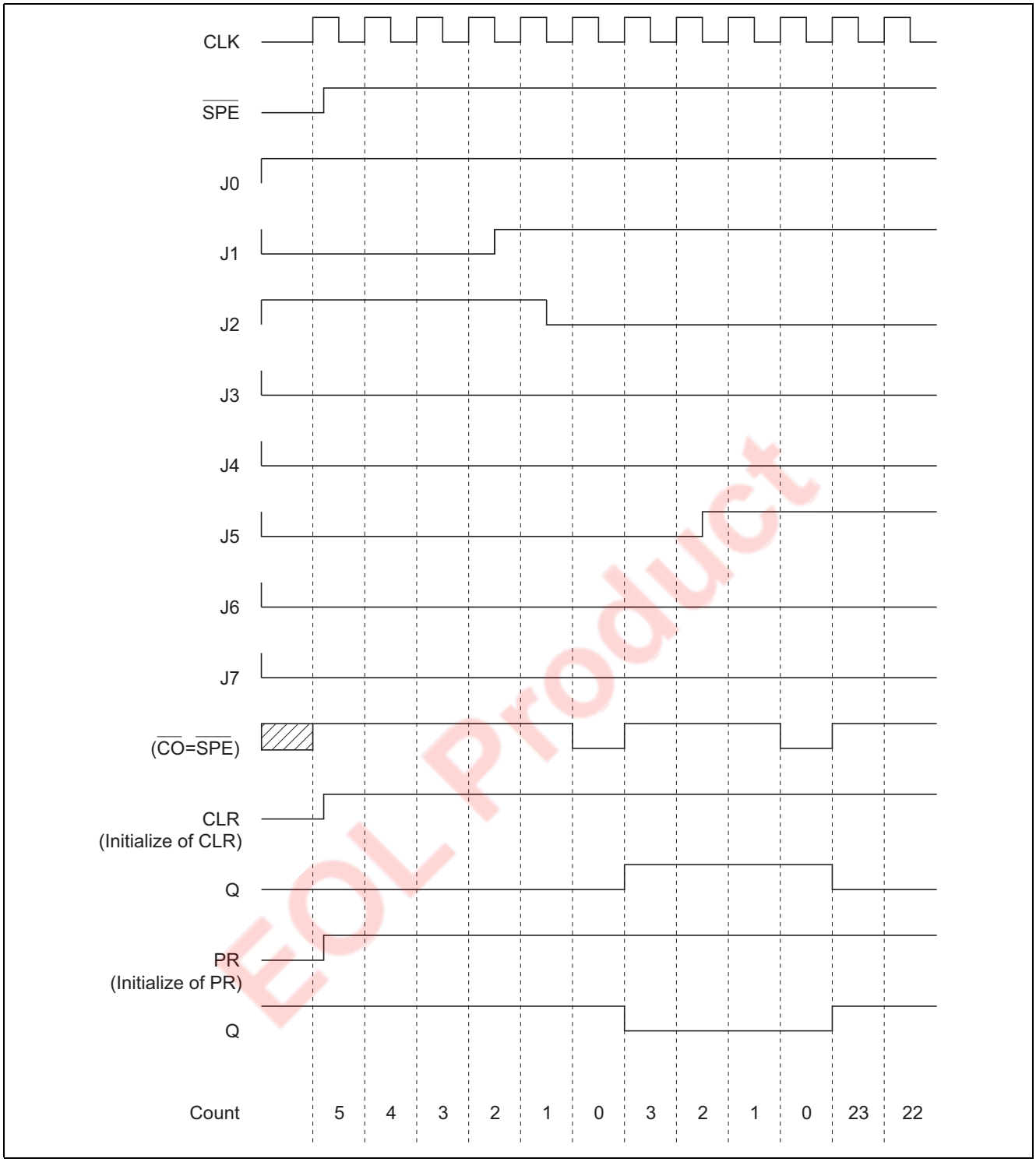


Notes: 1. In case of C/$\overline{T}$ = "L", CLK, $\overline{CLK}$ is V_{IH} = 3 V, Vref is 1.3 V
In case of C/$\overline{T}$ = "H", CLK, $\overline{CLK}$ is V_{IH} = V_{CC}, Vref is $V_{CC} \times 50\%$
2. F/F output is internal signal of IC.

Waveforms – 6



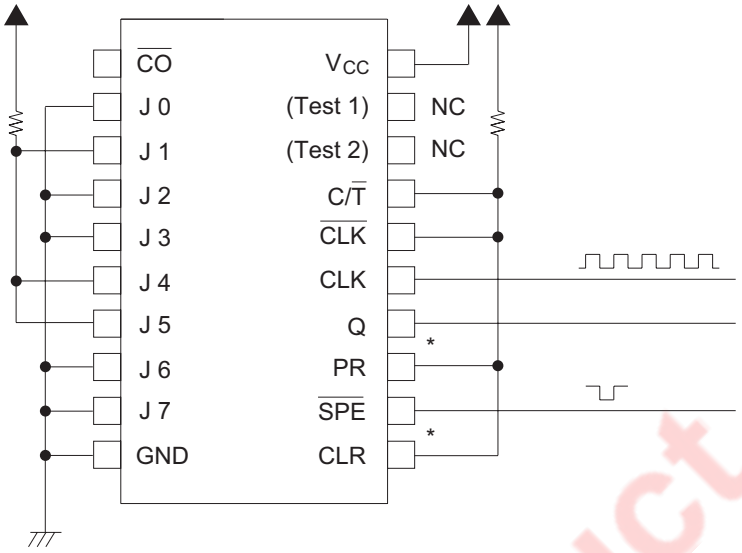
Timing Chart



Example of Application Circuit

AC Signal Generator for STN Type Liquid Crystal Panel

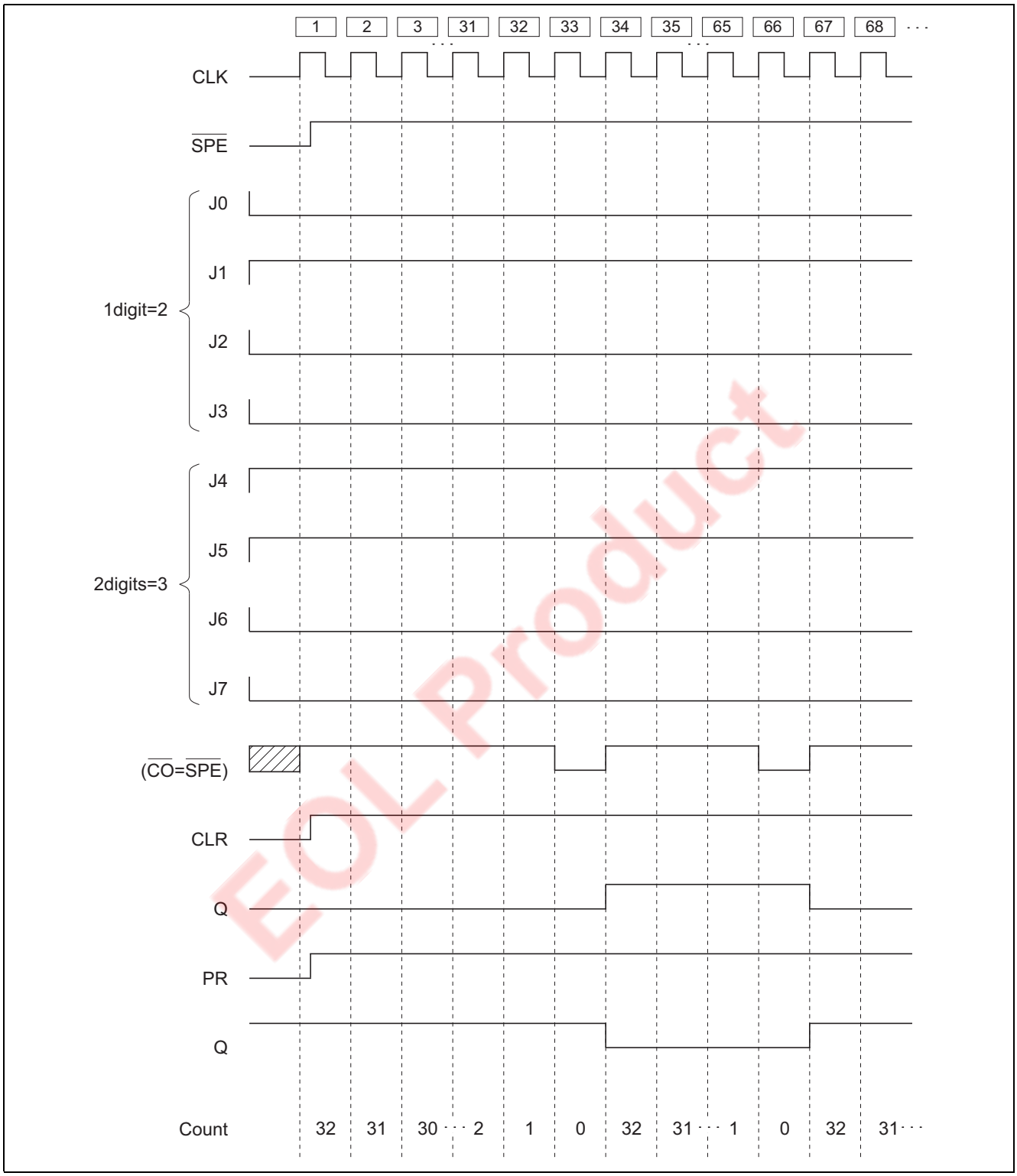
CLK ($\overline{CLK}$) : CMOS level input
Initialize counter : 32



Note: When initializing output D-F/F apply "L"

Timing Chart

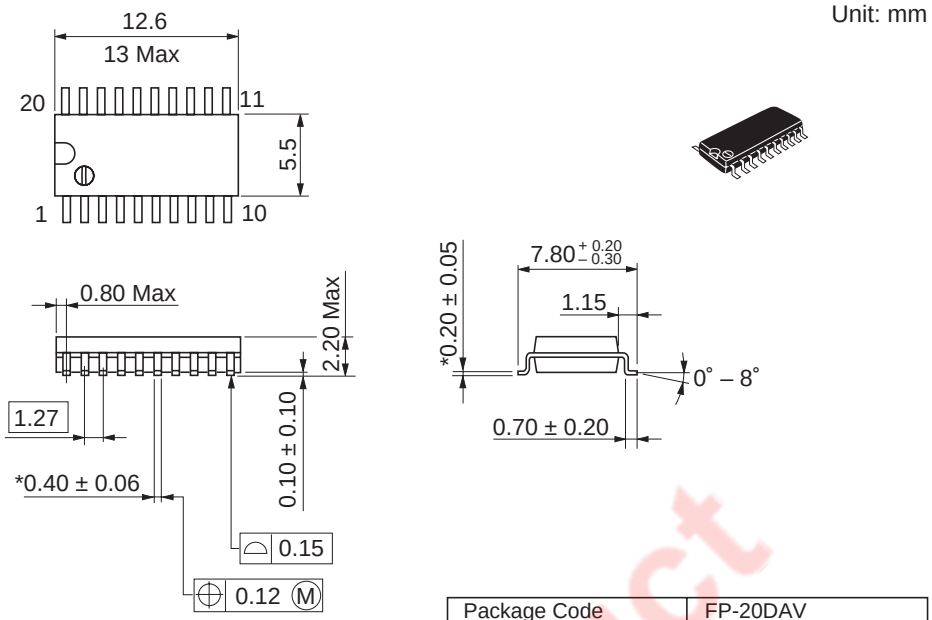
Example of AC Signal Generator



Package Dimensions

As of January, 2003

Unit: mm

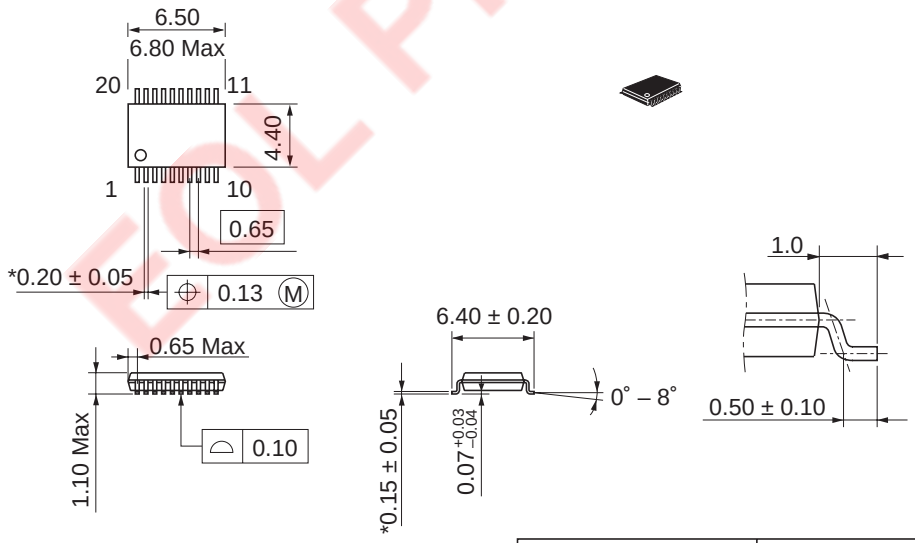


*Ni/Pd/Au plating

Package Code	FP-20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	TTP-20DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.07 g

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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