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April 1st, 2010 Renesas Electronics Corporation

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HD74ALVC1G80

Single Positive Edge-triggered D-type Flip Flop

REJ03D0127-0300Z (Previous ADE-205-638B (Z)) Rev.3.00 Nov.12.2003

Description

The HD74ALVC1G80 has D-type flip flop in a 5 pin package. The input data is transferred to the output at the rising edge of clock pulse CLK. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

Features

- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.

 $\pm 24 \text{ mA} (@V_{CC} = 3.0 \text{ V to } 3.6 \text{ V})$

- Supply voltage range: 1.2 to 3.6 V
 Operating temperature range: -40 to +85°C
- All inputs V_{IH} (Max.) = 3.6 V (@ V_{CC} = 0 V to 3.6 V)

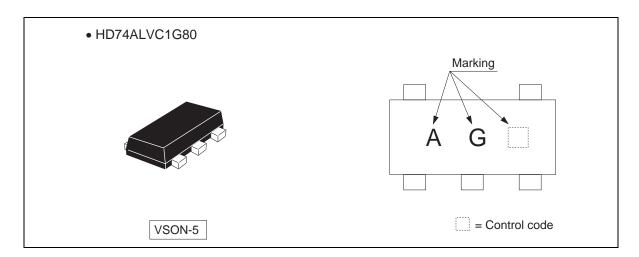
All outputs
$$V_0$$
 (Max.) = 3.6 V (@V_{CC} = 0 V)

$$\begin{array}{ll} \bullet & \text{Output current} & \pm 2 \text{ mA } (@V_{CC} = 1.2 \text{ V}) \\ & \pm 4 \text{ mA } (@V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}) \\ & \pm 6 \text{ mA } (@V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}) \\ & \pm 18 \text{ mA } (@V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}) \end{array}$$

Ordering Information

			Раскаде	l aping Appreviation
Part Name	Package Type	Package Code	Abbreviation	(Quantity)
HD74ALVC1G80VSE	VSON-5 pin	TNP-5DV	VS	E (3,000 pcs/reel)

Outline and Article Indication



Function Table

Inputs

CLK	D	Output Q
\uparrow	Н	L
↑	L	Н
L	X	$\overline{\overline{Q}}_{0}$

H: High level

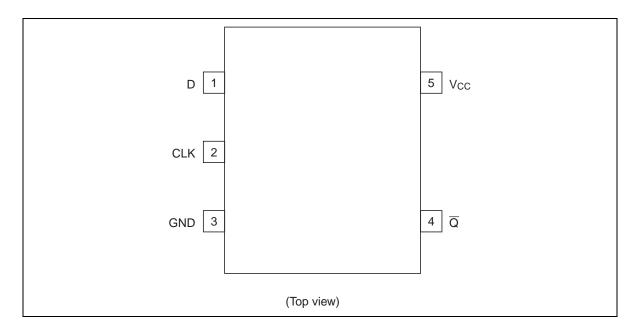
L: Low level

X: Immaterial

1: Low to high transition

 \overline{Q}_0 : Level of \overline{Q} before the indicated steady input conditions were established.

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	Vcc	-0.5 to 4.6	V	
Input voltage range *1	Vı	-0.5 to 4.6	V	
Output voltage range *1, 2	Vo	-0.5 to V _{CC} +0.5	V	Output : H or L
		-0.5 to 4.6		V _{CC} : OFF
Input clamp current	I _{IK}	-50	mA	V _I < 0
Output clamp current	I _{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I _O	±50	mA	$V_O = 0$ to V_{CC}
Continuous current through V _{CC} or GND	I _{CC} or I _{GND}	±100	mA	
Maximum power dissipation at Ta = 25°C (in still air) *3	P _T	200	mW	
Storage temperature	Tstg	-65 to 150	°C	

Notes:

The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

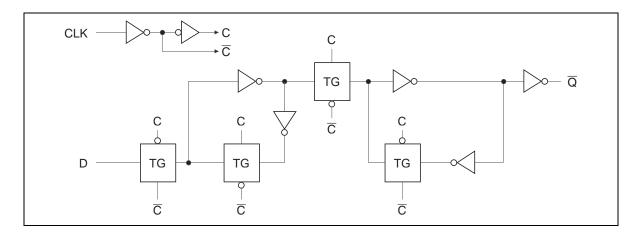
- 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V _{CC}	1.2	3.6	V	
Input voltage range	Vı	0	3.6	V	
Output voltage range	Vo	0	V _{CC}	V	
Output current	I _{OH}		-2	mA	V _{CC} = 1.2 V
		_	-4		V _{CC} = 1.4 V
		_	-6		V _{CC} = 1.65 V
		_	-18		$V_{CC} = 2.3 \text{ V}$
		_	-24		V _{CC} = 3.0 V
	I _{OL}	_	2		V _{CC} = 1.2 V
		_	4		V _{CC} = 1.4 V
		_	6		V _{CC} = 1.65 V
		_	18		$V_{CC} = 2.3 \text{ V}$
		_	24		$V_{CC} = 3.0 \text{ V}$
Input transition rise or fall rate	Δt / Δν	0	20	ns / V	V _{CC} = 1.2 to 2.7 V
		0	10		V _{CC} = 3.3±0.3 V
Operating free-air temperature	Та	-40	85	°C	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Electrical Characteristics

 $(Ta = -40 \text{ to } 85^{\circ}C)$

Item	Symbol	$V_{CC}(V)^*$	Min	Тур	Max	Unit	Test conditions
Input voltage	V _{IH}	1.2	V _{CC} ×0.75	_	_	V	
		1.4 to 1.6	V _{CC} ×0.7	_	_	_	
		1.65 to 1.95	V _{CC} ×0.7	_	_	_	
		2.3 to 2.7	1.7	_	_	_	
		3.0 to 3.6	2.0	_	_	_	
	V _{IL}	1.2	_	_	V _{CC} ×0.25	_	
		1.4 to 1.6	_	_	V _{CC} ×0.3	_	
		1.65 to 1.95	_	_	V _{CC} ×0.3	_	
		2.3 to 2.7	_	_	0.7	_	
		3.0 to 3.6	_	_	0.8	=	
Output voltage	V _{OH}	Min to Max	V _{CC} -0.2	_	_	V	$I_{OH} = -100 \mu A$
		1.2	0.9	_	_	=	$I_{OH} = -2 \text{ mA}$
		1.4	1.1	_	_	_	$I_{OH} = -4 \text{ mA}$
		1.65	1.2	_	_	_	$I_{OH} = -6 \text{ mA}$
		2.3	1.7	_	_	=	$I_{OH} = -18 \text{ mA}$
		3.0	2.2	_	_	_	$I_{OH} = -24 \text{ mA}$
	V _{OL}	Min to Max	_	_	0.2	_	$I_{OL} = 100 \mu A$
		1.2	_	_	0.3	_	I _{OL} = 2 mA
		1.4	_	_	0.3	_	I _{OL} = 4 mA
		1.65	_	_	0.3	_	I _{OL} = 6 mA
		2.3	_	_	0.55	=	I _{OL} = 18 mA
		3.0	_	_	0.55	_	I _{OL} = 24 mA
Input current	I _{IN}	3.6	_	_	±5	μΑ	V _{IN} = 3.6 V or GND
Quiescent supply current	I _{CC}	3.6	_	_	10	μΑ	$V_{IN} = V_{CC}$ or GND, $I_O = 0$
Output leakage current	I _{OFF}	0	_	_	5	μΑ	V_{IN} or $V_O =$ 0 to 3.6 V
Input capacitance	C _{IN}	3.3	_	4.0	_	рF	V _{IN} = V _{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

 $(Ta = -40 \text{ to } 85^{\circ}C)$

 $V_{CC} = 1.2 \text{ V}$

Item	Symbol	Min	Тур	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Maximum clock frequency	f _{max}	_	200	_	MHz	C _L = 15 pF		
Propagation delay time	t _{PLH} t _{PHL}	_	7.3	_	ns	C _L = 15 pF	CLK	Q
Setup time	t _{su}	_	4.5	_	ns		D	
Hold time	t _h	_	-4.5	_	ns			
Pulse width	t _w	_	2.0	_	ns		CLK "H"	or "L"

 $V_{CC}=1.5{\pm}0.1~V$

Item	Symbol	Min	Тур	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Maximum clock frequency	f _{max}	100	350	_	MHz	$C_L = 15 pF$		
Propagation delay time	t _{PLH} t _{PHL}	2.0	_	8.0	ns	C _L = 15 pF	CLK	Q
Setup time	t _{su}	4.5	_	_	ns		D	
Hold time	t _h	0.0	_	_	ns			
Pulse width	t _w	3.5	_	_	ns		CLK "H"	or "L"

 $V_{CC} = 1.8 \pm 0.15 \text{ V}$

Item	Symbol	Min	Тур	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Maximum clock frequency	f _{max}	160	350	_	MHz	$C_L = 30 pF$		
Propagation delay time	t _{PLH} t _{PHL}	1.5	_	7.0	ns	$C_L = 30 pF$	CLK	Q
Setup time	t _{su}	3.5	_	_	ns		D	
Hold time	t _h	0.0	_	_	ns			
Pulse width	t _w	2.5	_	_	ns		CLK "H"	or "L"

Switching Characteristics (cont)

 $V_{CC} = 2.5 \pm 0.2 \text{ V}$

Item	Symbol	Min	Тур	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Maximum clock frequency	f _{max}	160	400	_	MHz	$C_L = 30 pF$		
Propagation delay time	t _{PLH} t _{PHL}	1.0	_	4.0	ns	C _L = 30 pF	CLK	Q
Setup time	t _{su}	2.5	_	_	ns		D	
Hold time	t _h	0.0	_	_	ns			
Pulse width	t _w	2.5	_	_	ns		CLK "H"	or "L"

 $V_{CC} = 3.3 \pm 0.3 \text{ V}$

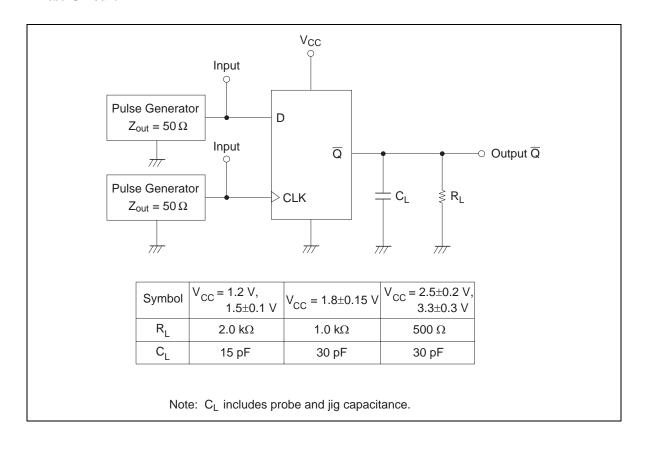
Item	Symbol	Min	Тур	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Maximum clock frequency	f _{max}	200	450	_	MHz	$C_L = 30 pF$		
Propagation delay time	t _{PLH} t _{PHL}	1.0	_	3.0	ns	C _L = 30 pF	CLK	Q
Setup time	t _{su}	2.0	_	_	ns		D	
Hold time	t _h	0.0	_	_	ns			
Pulse width	t _w	2.0	_	_	ns		CLK "H"	or "L"

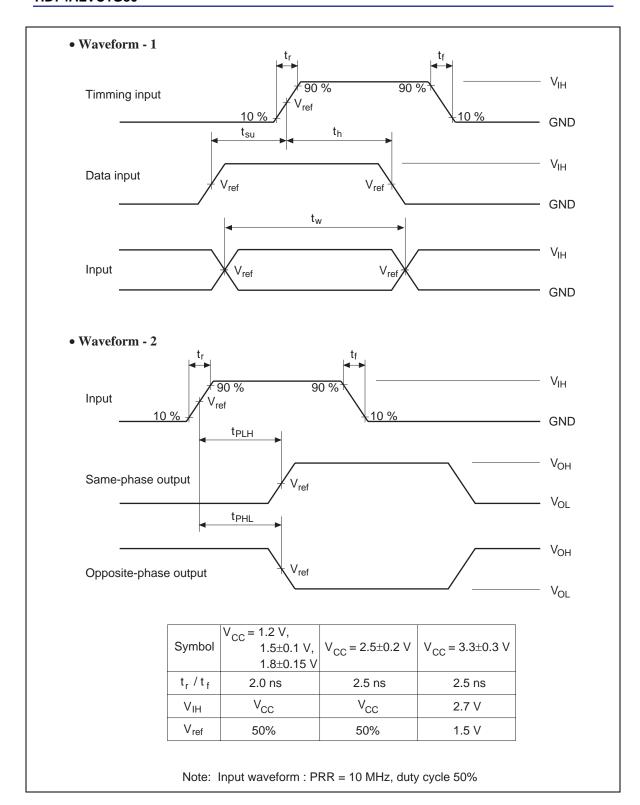
Operating Characteristics

 $(Ta = 25^{\circ}C)$

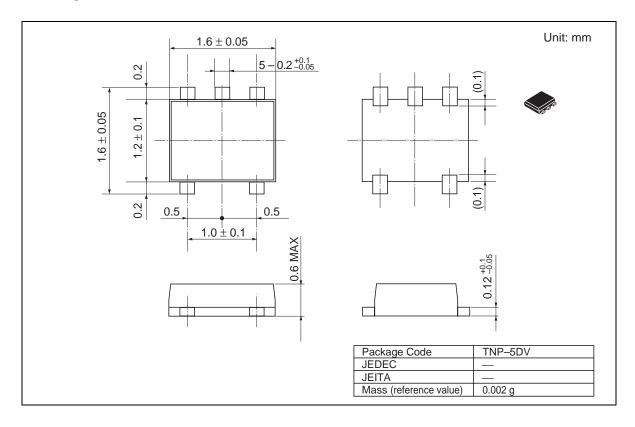
Item	Symbol	V _{CC} (V)	Min	Тур	Max	Unit	Test conditions
Power dissipation	C_{PD}	1.5	_	7.5	_	pF	f = 10 MHz
capacitance		1.8	_	7.5	_		
		2.5	_	8.0	_		
		3.3	_	11.0	_		

Test Circuit





Package Dimensions



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