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April 1st, 2010
Renesas Electronics Corporation

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HD74HCT137

3-to-8-line Decoder/Demultiplexer with Address Latch

REJ03D0658-0200
 (Previous ADE-205-546)
 Rev.2.00
 Mar 30, 2006

Description

The HD74HCT137 implements a three-to-eight line decoder with latches on the three address inputs. When \overline{GL} goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as \overline{GL} remains high no address changes will be recognized. Output enable controls, G_1 and \overline{G}_2 , control the state of the outputs independently of the select or latch-enable inputs.

All of the outputs are high unless G_1 is high and \overline{G}_2 is low. The HD74HCT137 is ideally suited for the implementation of glitch free decoders in stored-address applications in bus oriented systems.

Features

- High Speed Operation: t_{pd} (A, B, C to Y) = 16.5 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ V to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HCT137FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74HCT137RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

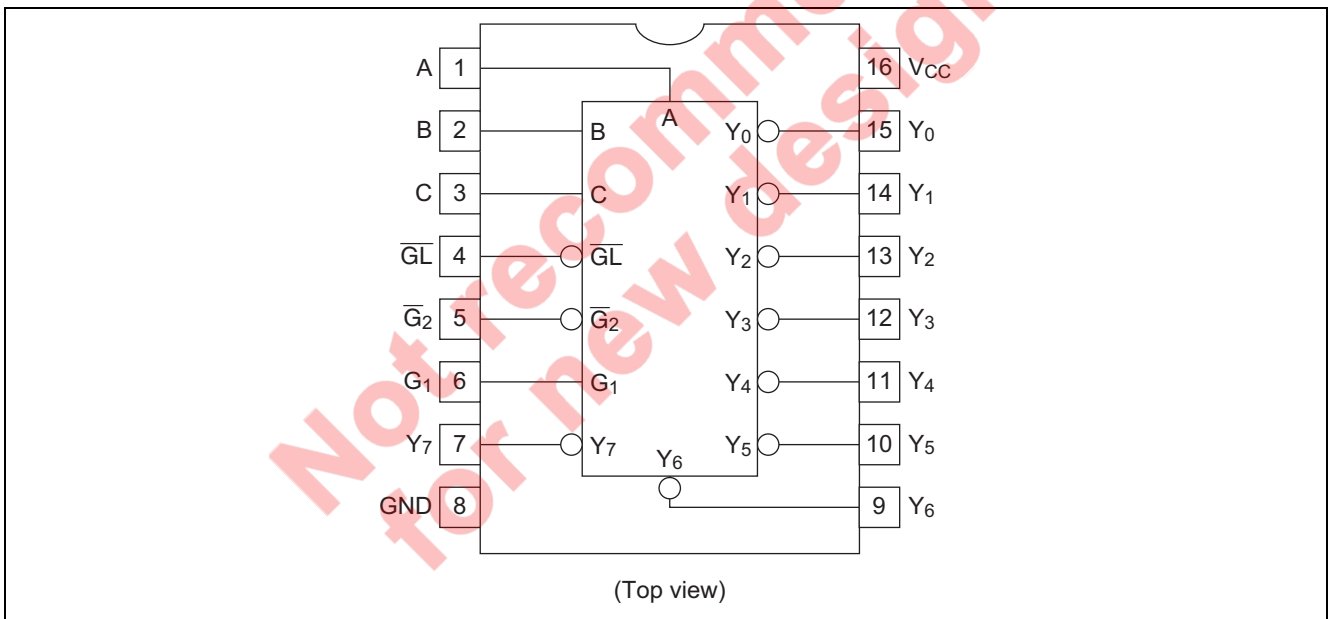
Note: Please consult the sales office for the above package availability.

Function Table

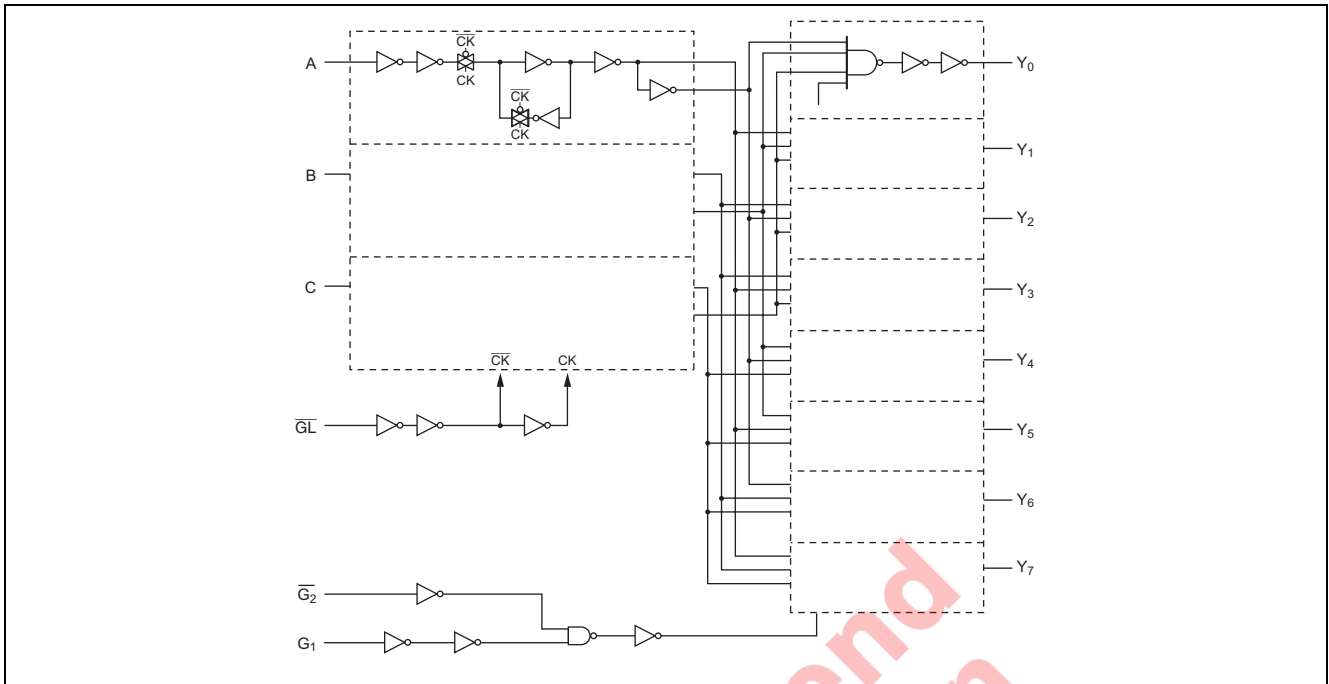
Inputs						Outputs							
Enable			Select										
\overline{GL}	G_1	$\overline{G_2}$	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output Corresponding to stored address L; all Others. H							

H : High level
 L : Low level
 X : Irrelevant

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Output current	I_{OUT}	± 25	mA
DC current drain per V_{CC} , GND	I_{CC} , I_{GND}	± 50	mA
DC input diode current	I_{IK}	± 20	mA
DC output diode current	I_{OK}	± 20	mA
Power dissipation per package	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	4.5 to 5.5	V	
Input / Output voltage	V_{IN} , V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	$^{\circ}C$	
Input rise / fall time ^{*1}	t_r , t_f	0 to 500	ns	$V_{CC} = 4.5 V$

Notes: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

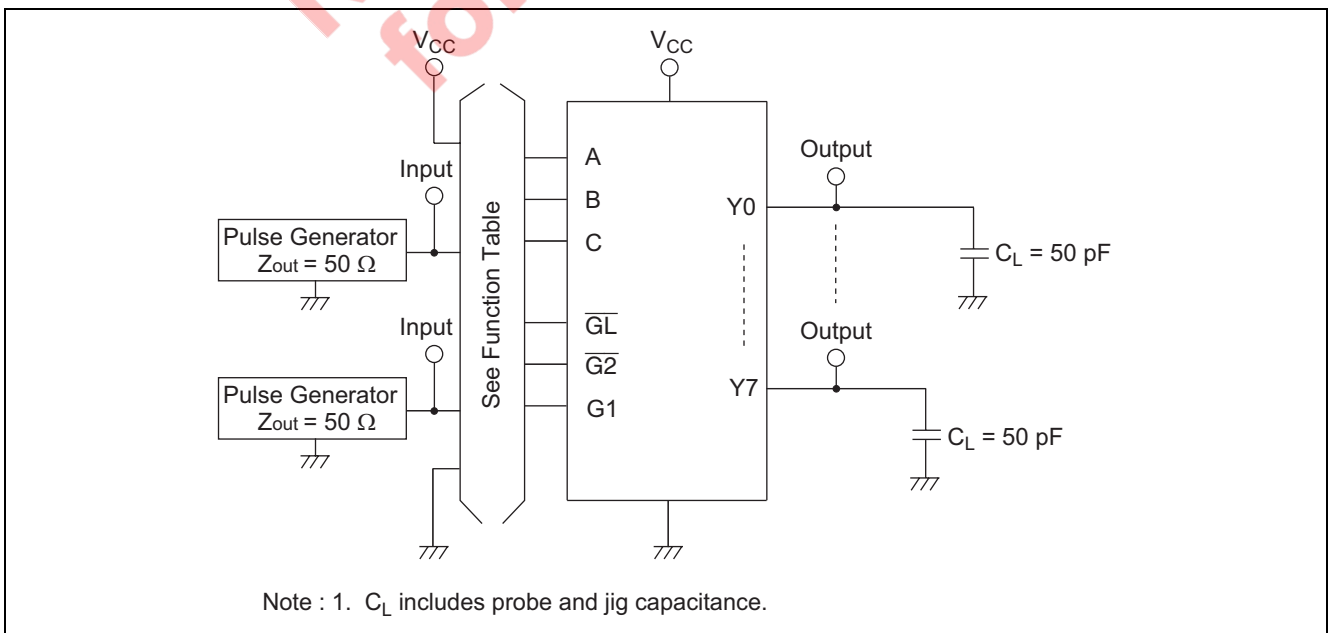
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to+85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	4.5 to 5.5	2.0	—	—	2.0	—	V		
	V _{IL}	4.5 to 5.5	—	—	0.8	—	0.8	V		
Output voltage	V _{OH}	4.5	4.4	—	—	4.4	—	V	V _{in} = V _{IH} or V _{IL}	I _{OH} = -20 μA
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
	V _{OL}	4.5	—	—	0.1	—	0.1	V	V _{in} = V _{IH} or V _{IL}	I _{OL} = 20 μA
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
Input current	I _{in}	5.5	—	—	±0.1	—	±1.0	μA	V _{in} = V _{CC} or GND	
Quiescent supply current	I _{CC}	5.5	—	—	4.0	—	40	μA	V _{in} = V _{CC} or GND, I _{out} = 0 μA	

Switching Characteristics

(C_L = 50 pF, Input t_r = t_f = 6 ns)

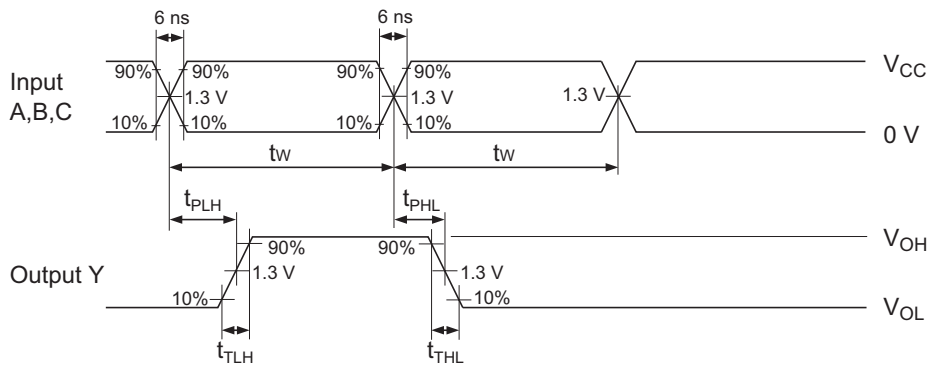
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	4.5	—	14	34	—	43	ns	A, B or C to Y		
											t _{PHL}
	t _{PLH}	4.5	—	11	26	—	33	ns	$\overline{G_2}$ to Y		
											t _{PHL}
	t _{PLH}	4.5	—	13	30	—	38	ns	G ₁ to Y		
											t _{PHL}
	t _{PLH}	4.5	—	16	35	—	44	ns	$\overline{G_L}$ to Y		
											t _{PHL}
	Pulse width	t _w	4.5	16	6	—	20	—	ns		
	Setup time	t _{su}	4.5	20	3	—	25	—	ns		
	Hold time	t _h	4.5	10	0	—	13	—	ns		
	Output rise/fall time	t _{TLH}	4.5	—	5	15	—	19	ns		
t _{THL}		4.5	—	5	15	—	19	ns			
Input capacitance	C _{in}	—	—	5	10	—	10	pF			

Test Circuit



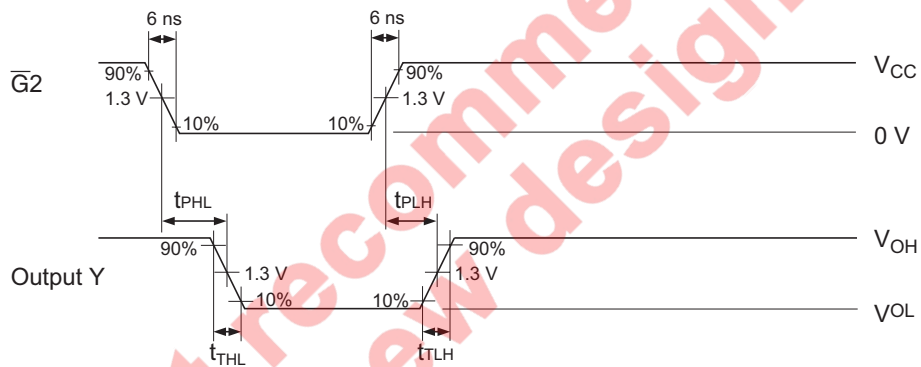
Waveforms

• Waveform – 1



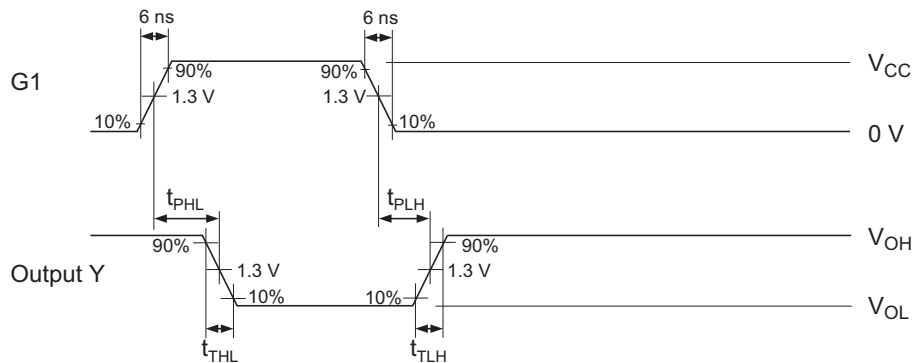
Notes: 1. Input waveform: $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. The output are measured one at a time with one transition per measurement.

• Waveform – 2



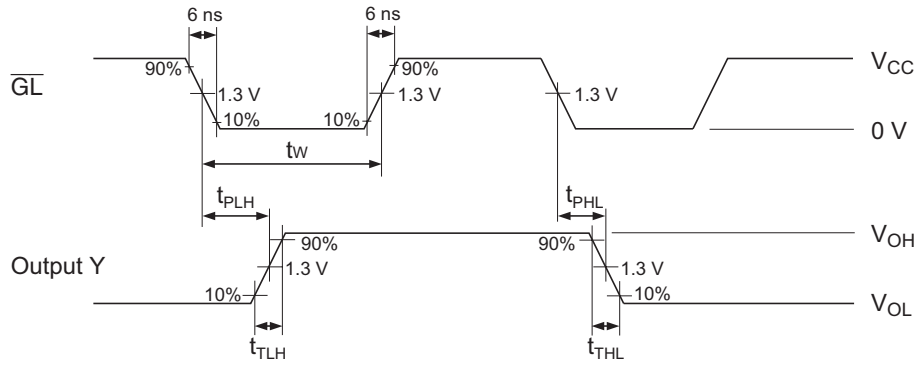
Notes: 1. Input waveform: $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. The output are measured one at a time with one transition per measurement.

• Waveform – 3



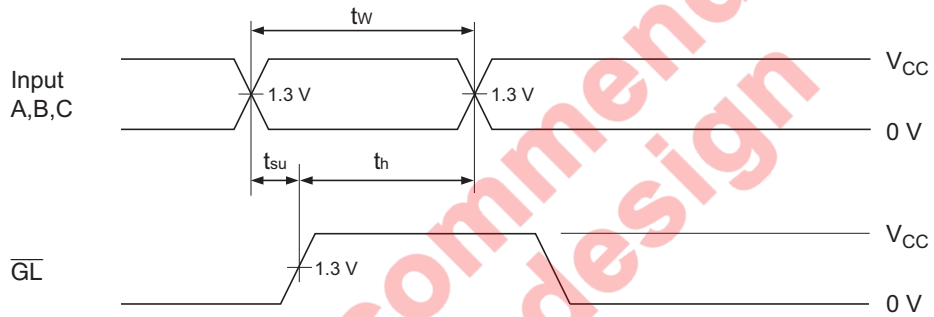
Notes: 1. Input waveform: $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. The output are measured one at a time with one transition per measurement.

• Waveform – 4



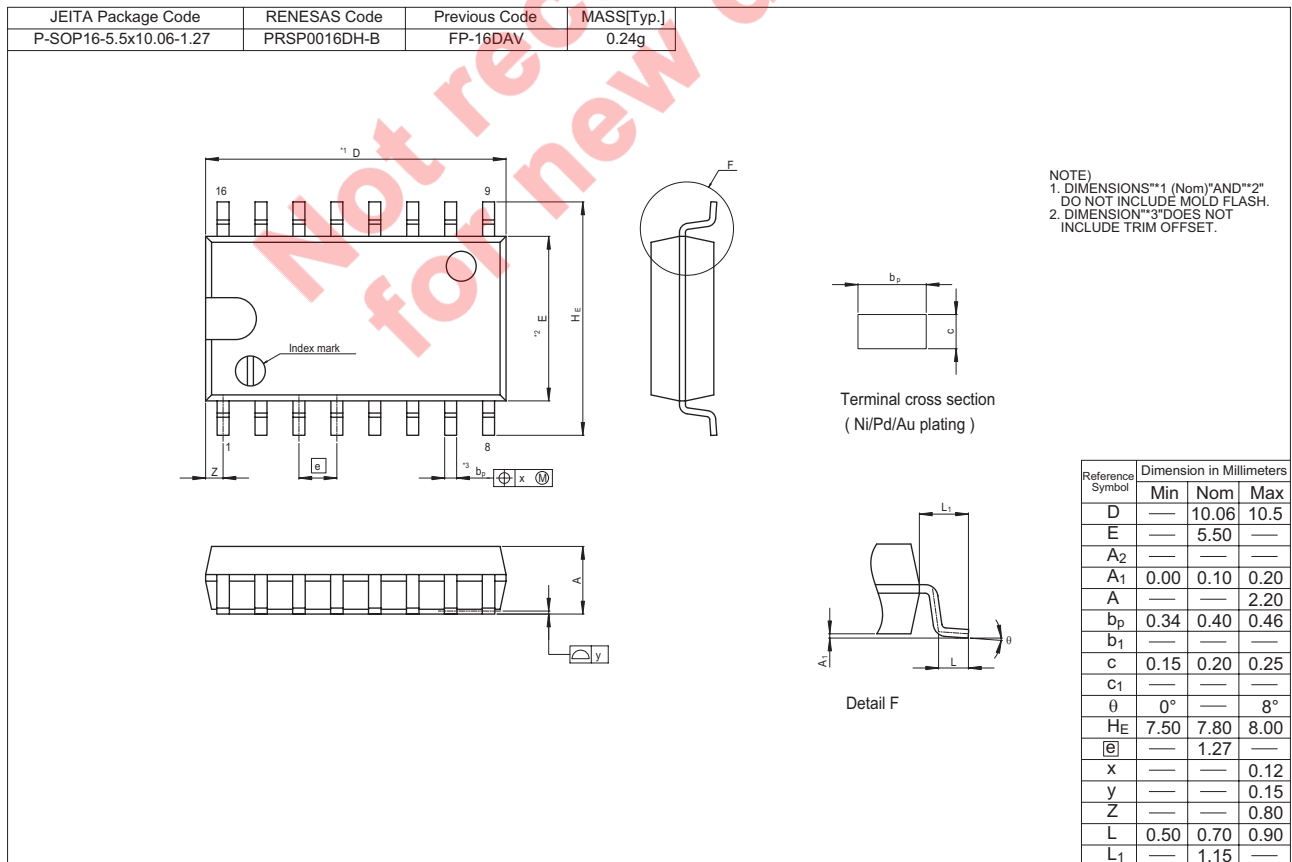
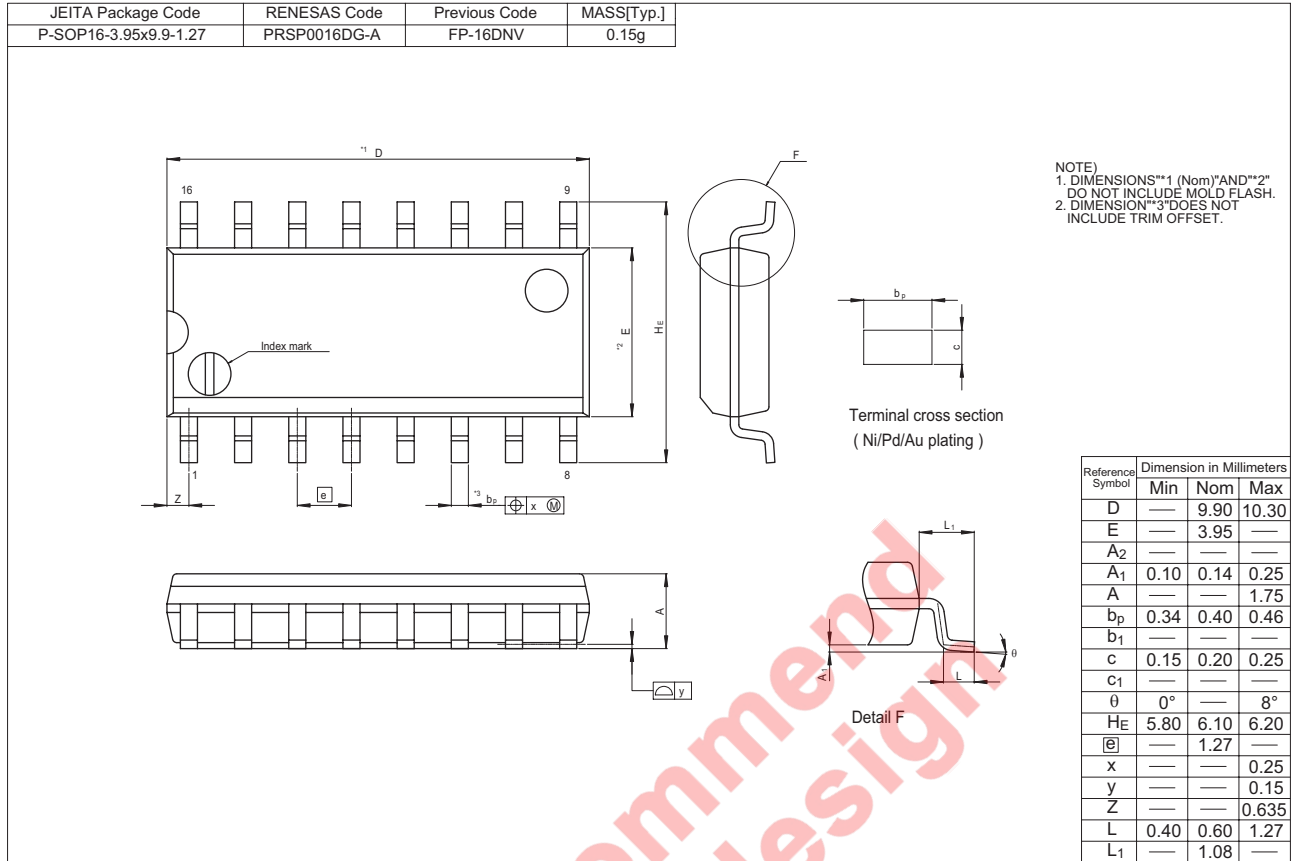
- Notes: 1. Input waveform: PRR \leq 1 MHz, $Z_o = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns
 2. The output are measured one at a time with one transition per measurement.

• Waveform – 5



- Notes: 1. Input waveform: PRR \leq 1 MHz, $Z_o = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns
 2. The output are measured one at a time with one transition per measurement.

Package Dimensions



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