To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74LS122

Retriggerable Monostable Multivibrator (with Clear)

REJ03D0428–0200
Rev.2.00
Feb.18.2005

This d-c triggered multivibrator features output pulse width control by three method. The basic pulse time is programmed by selection of external resistance and capacitance values. The HD74LS122 has internal timing resistor that allows the circuit to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level -active (A) or high-level active (B) inputs or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear. This device is provided enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 mV/ns.

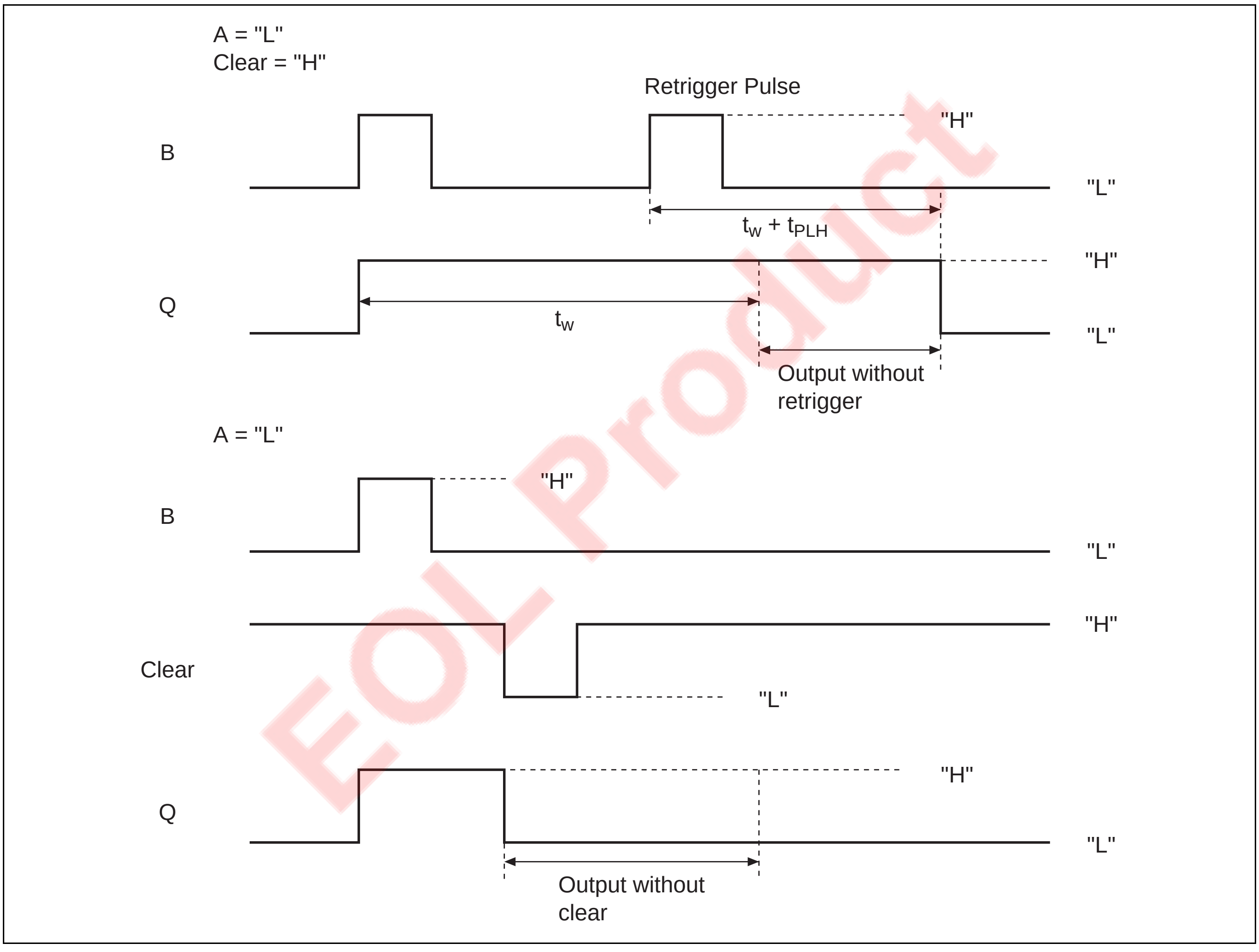


Figure 1 Typical Input / Output Pulse

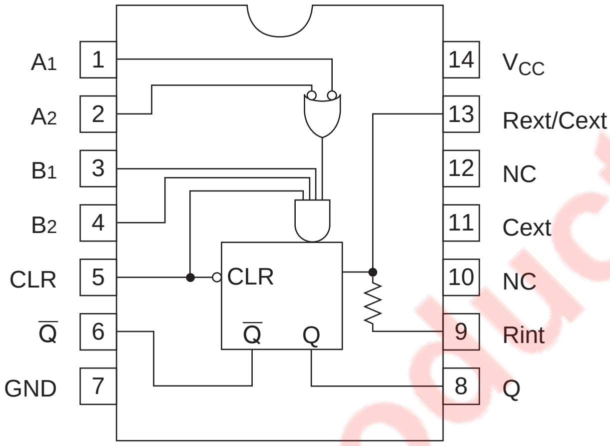
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS122P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS122FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

Function Table

Inputs					Outputs	
Clear	A_1	A_2	B_1	B_2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⊓	⊔
H	L	X	H	↑	⊓	⊔
H	X	L	↑	H	⊓	⊔
H	X	L	H	↑	⊓	⊔
H	H	↓	H	H	⊓	⊔
H	↓	↓	H	H	⊓	⊔
H	↓	H	H	H	⊓	⊔
↑	L	X	H	H	⊓	⊔
↑	X	L	H	H	⊓	⊔

Notes: H; high level, L; low level, X; irrelevant
↑; transition from low to high level
↓; transition from high to low level
⊓; one high-level pulse
⊔; one low-level pulse

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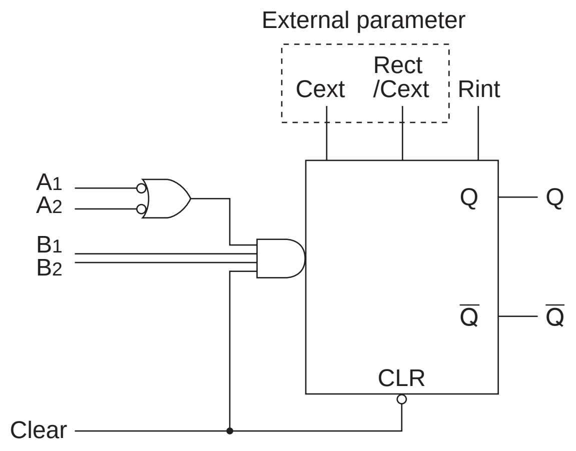
Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	–400	µA
	I_{OL}	—	—	8	mA
Operating temperature	Topr	–20	25	75	°C
Input pulse width	t_w	40	—	—	ns
External timing resistance	R_{ext}	5	—	260	kΩ
External capacitance	C_{ext}	Non restriction			
Wiring capacitance at Rext/Cext terminal	R_{ext}/C_{ext}	—	—	50	pF

Electrical Characteristics

(Ta = –20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V_{IH}	2.0	—	—	V	
	V_{IL}	—	—	0.8	V	
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
	V_{OL}	—	—	0.4	V	I_{OL} = 4 mA; V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
		—	—	0.5		I_{OL} = 8 mA; V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
Input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
Short-circuit output current	I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current**	I_{CC}	—	6	11	mA	V_{CC} = 5.25 V
Input clamp voltage	V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

* V_{CC} = 5 V, Ta = 25°C

** With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

Note: To measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q, ground R_{ext} / C_{ext}, apply 2 V to B and clear, and pulse A from 2 V to 0 V.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Propagation delay time	t_{PLH}	A	Q	—	23	33	ns	C_{ext} = 0, R_{ext} = 5 kΩ, C_L = 15 pF, R_L = 2 kΩ
	t_{PHL}		$\overline{Q}$	—	32	45		
	t_{PLH}	B	Q	—	23	44		
	t_{PHL}		$\overline{Q}$	—	34	56		
	t_{PLH}	Clear	Q	—	20	27		
	t_{PHL}		$\overline{Q}$	—	28	45		
Output pulse width	$t_{(out)min}$	A or B	Q	—	116	200	µs	C_{ext} = 1000 pF, R_{ext} = 10 kΩ, C_L = 15 pF, R_L = 2 kΩ
	$t_{(out)}$		Q	4	4.5	5		

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Typical Application Data for HD74LS122

For pulse widths when $C_{ext} \le 1000$ pF, See Figure 3.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as: $t_{w(out)} = K \bullet R_{ext} \bullet C_{ext}$; See Figure 4.

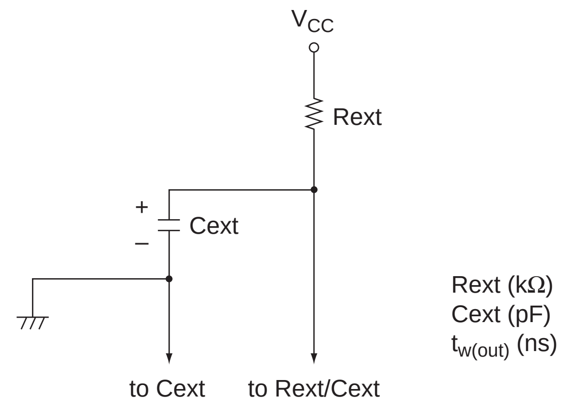


Figure 2 Timing Component Connections

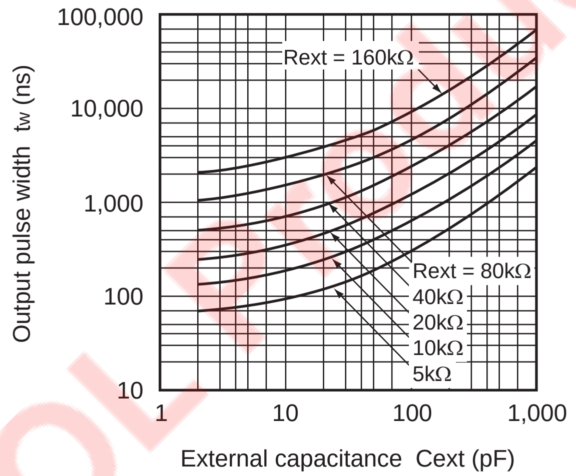


Figure 3 Typical Output Pulse Width (Cext ≤ 1000 pF)

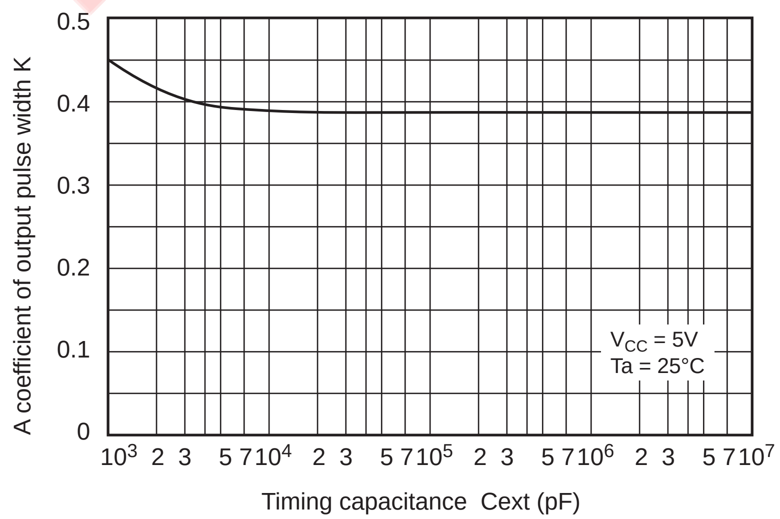
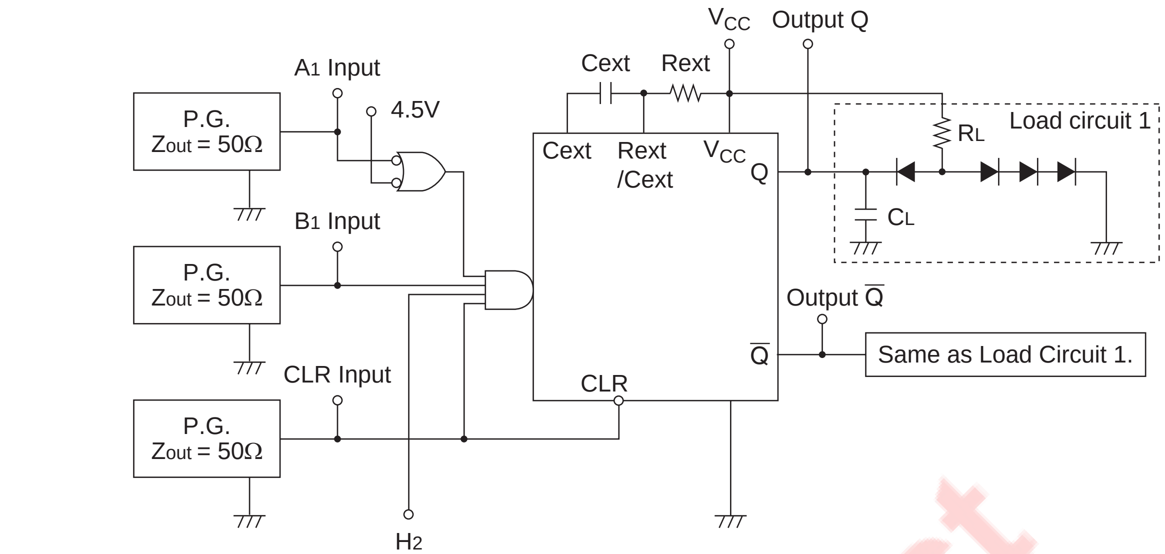


Figure 4 C_{ext} vs. K (C_{ext} > 1000 pF)

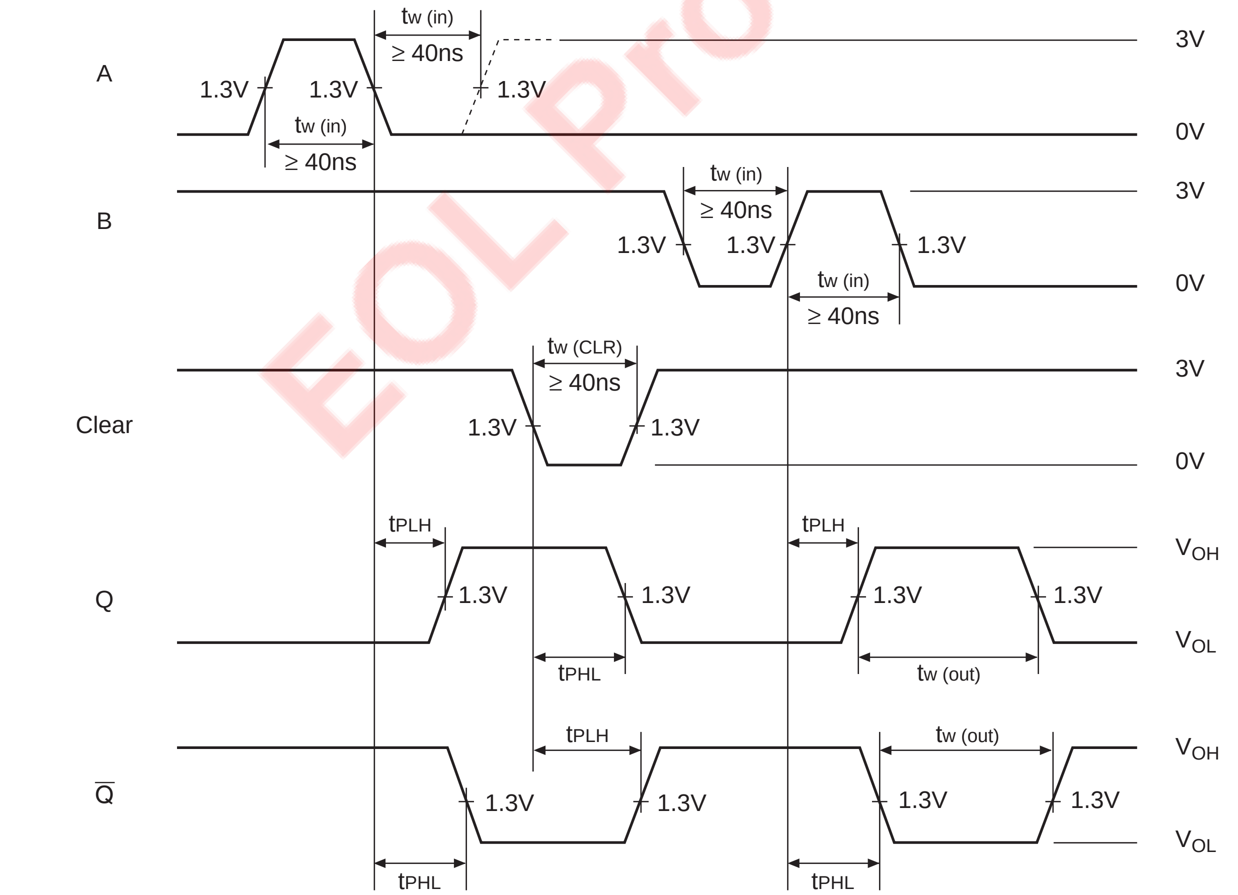
Testing Method

Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

Waveform



Note: Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns.

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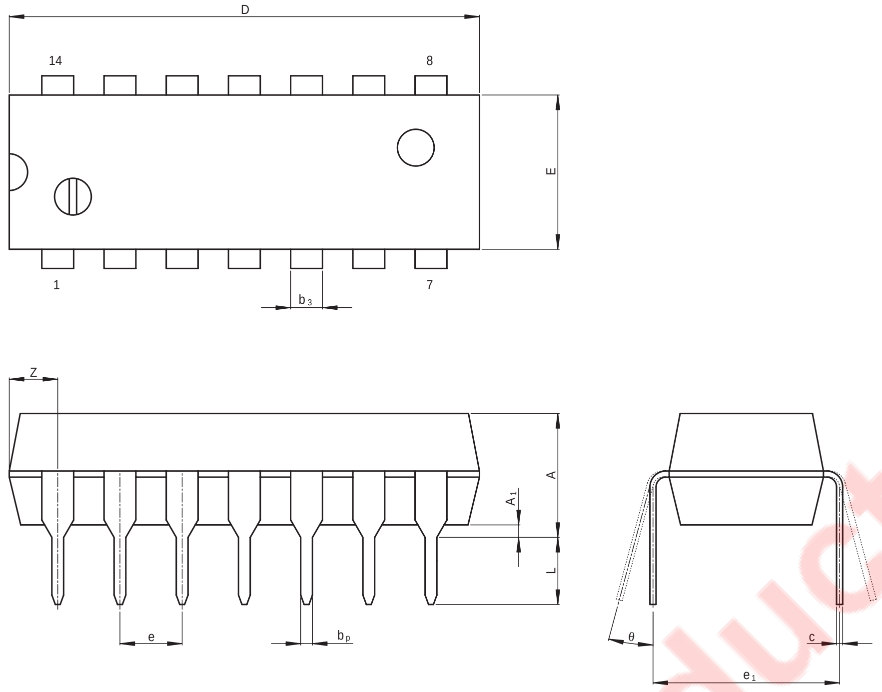
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.3x19.2-2.54	PRDP0014AB-B	DP-14AV	0.97g

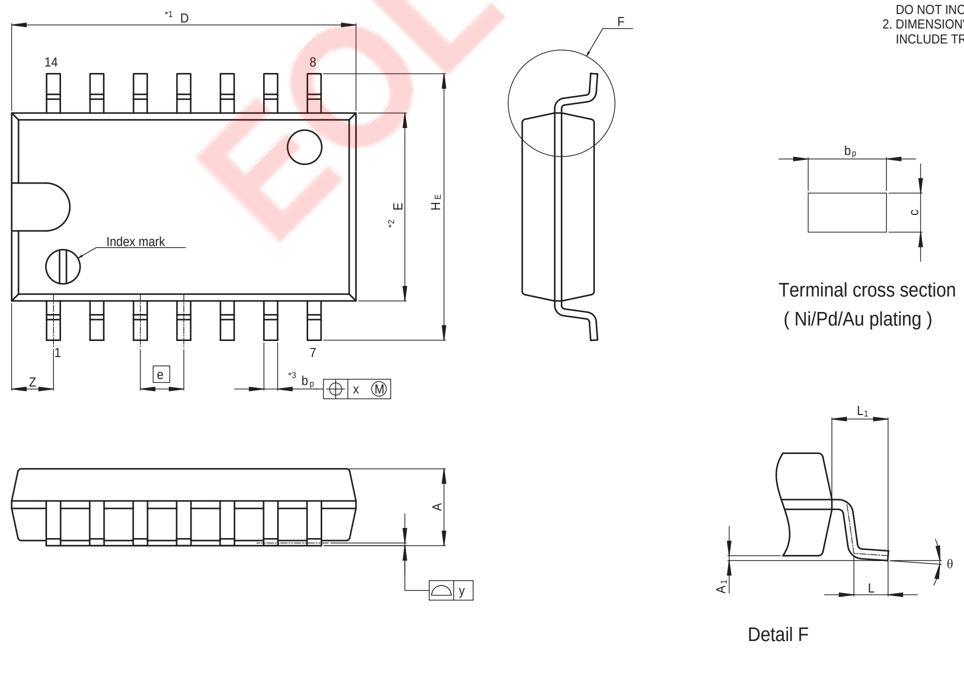


(Ni/Pd/Au plating)

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A_1	0.51	——	——
b_p	0.40	0.48	0.56
b_3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	2.39
L	2.54	——	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP14-5.5x10.06-1.27	PRSP0014DF-B	FP-14DAV	0.23g

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A_2	——	——	——
A_1	0.00	0.10	0.20
A	——	——	2.20
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.15	0.20	0.25
c_1	——	——	——
θ	0°	——	8°
H_E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	1.42
L	0.50	0.70	0.90
L_1	——	1.15	——

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