To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74LS162A

Synchronous Decade Counter (synchronous clear)

REJ03D0446–0300
Rev.3.00
Jul.15.2005

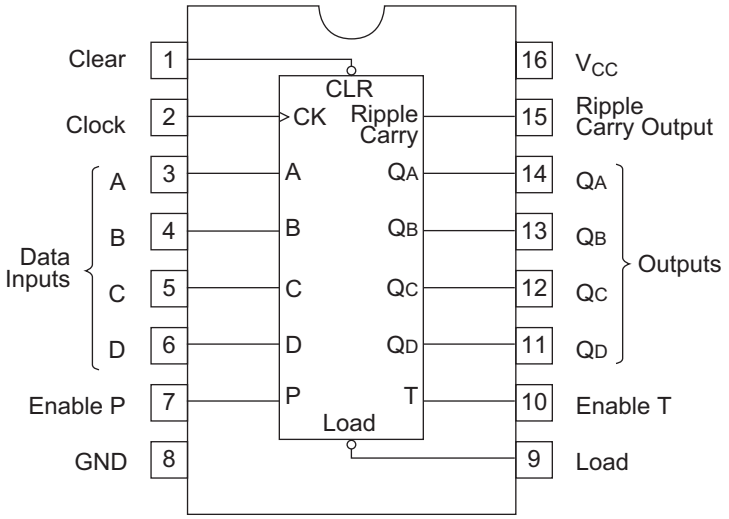
This synchronous decade counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs changes coincident with each other when so instructed by the count-enable inputs and internal gating. This mode is operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform. This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to LLLL. Low-to-high transitions at the clear input should be avoided when the clock is low if the enable and load inputs are high at or before the transition. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional getting. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

Features

- Ordering Information

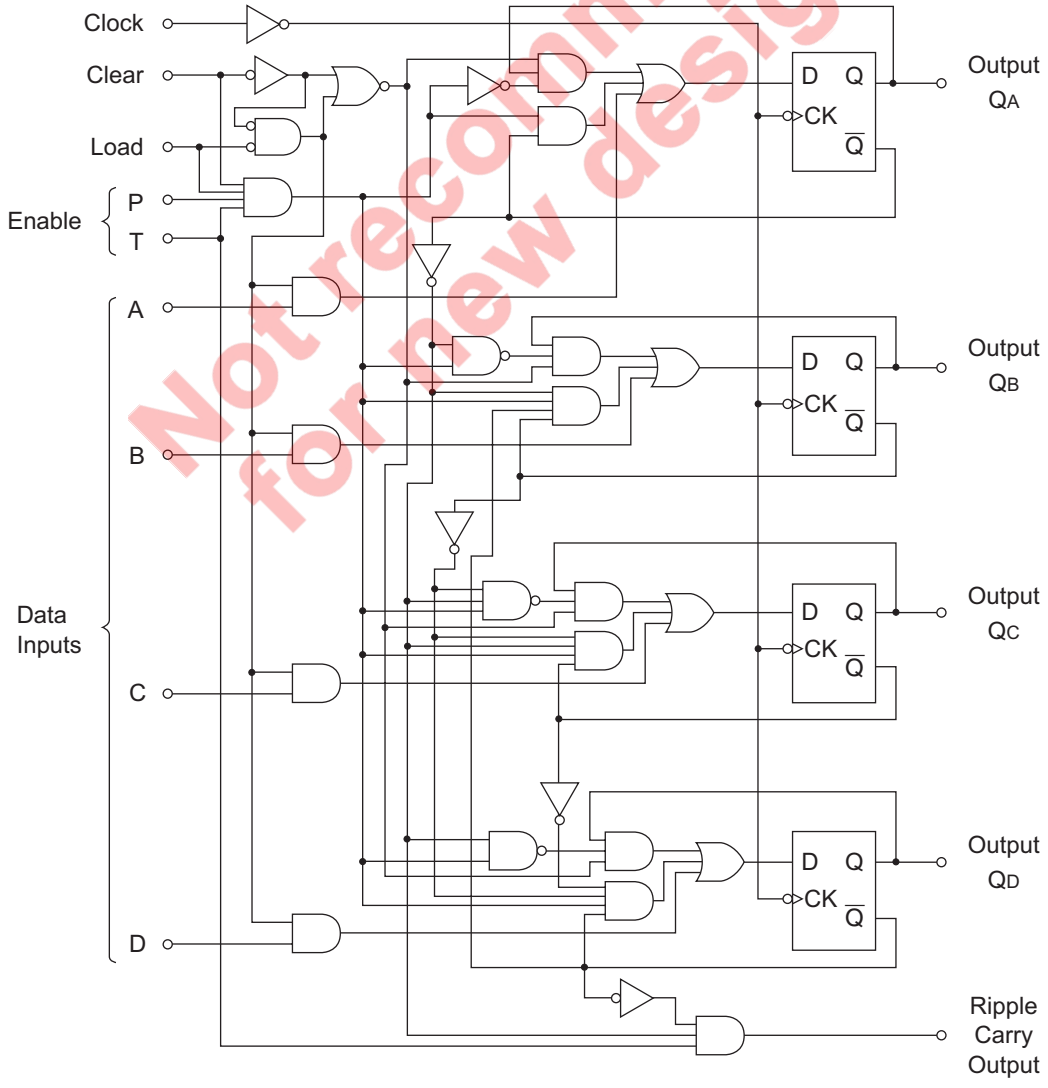
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS162AFPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Pin Arrangement



(Top view)

Block Diagram



Absolute Maximum Ratings

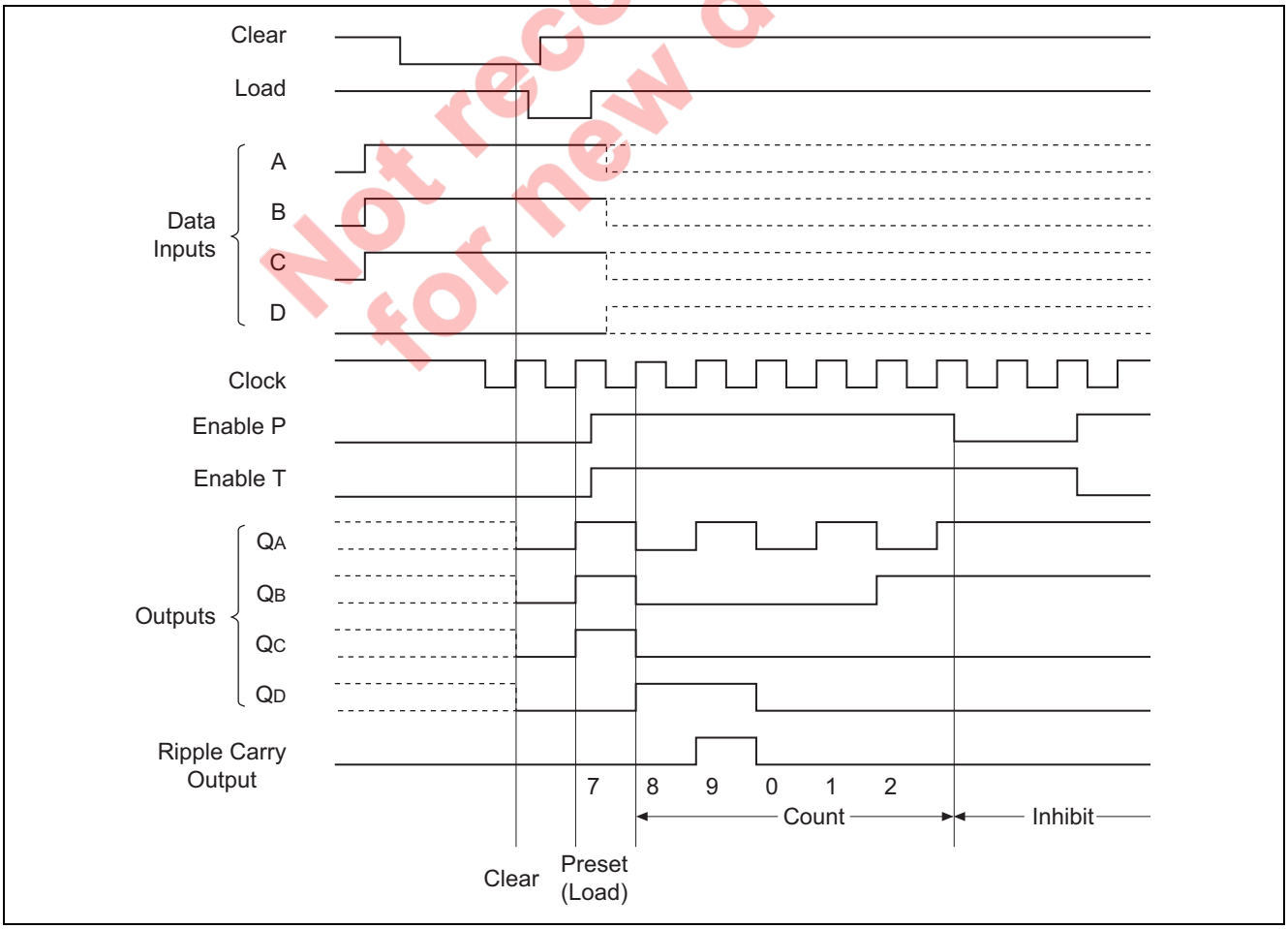
Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		Topr	–20	25	75	°C
Clock frequency		f_{clock}	0	—	25	MHz
Clock pulse width		$t_{w\ (clock)}$	25	—	—	ns
Clear pulse width		$t_{w\ (clear)}$	20	—	—	ns
Setup time	A, B, C, D	t_{su}	20	—	—	ns
	Enable P, T		20	—	—	ns
	Load		20	—	—	ns
	Clear		20	—	—	ns
Hold time		t_h	3	—	—	ns

Typical Clear, Preset, and Inhibit Sequence



Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V_{IH}	2.0	—	—	V	
		V_{IL}	—	—	0.8	V	
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA
		V_{OL}	—	—	0.4	V	I_{OL} = 4 mA, V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
			—	—	0.5		I_{OL} = 8 mA
Input current	Data, Enable P	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V
	Load, Clock, Enable T		—	—	40		
	Clear		—	—	40		
	Data, Enable P	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	Load, Clock, Enable T		—	—	–0.8		
	Clear		—		–0.8		
	Data, Enable P	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
	Load, Clock, Enable T		—	—	0.2		
	Clear		—	—	0.2		
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current**		I_{CCH}	—	18	31	mA	V_{CC} = 5.25 V
		I_{CCL}	—	19	32	mA	V_{CC} = 5.25 V
Input clamp voltage		V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

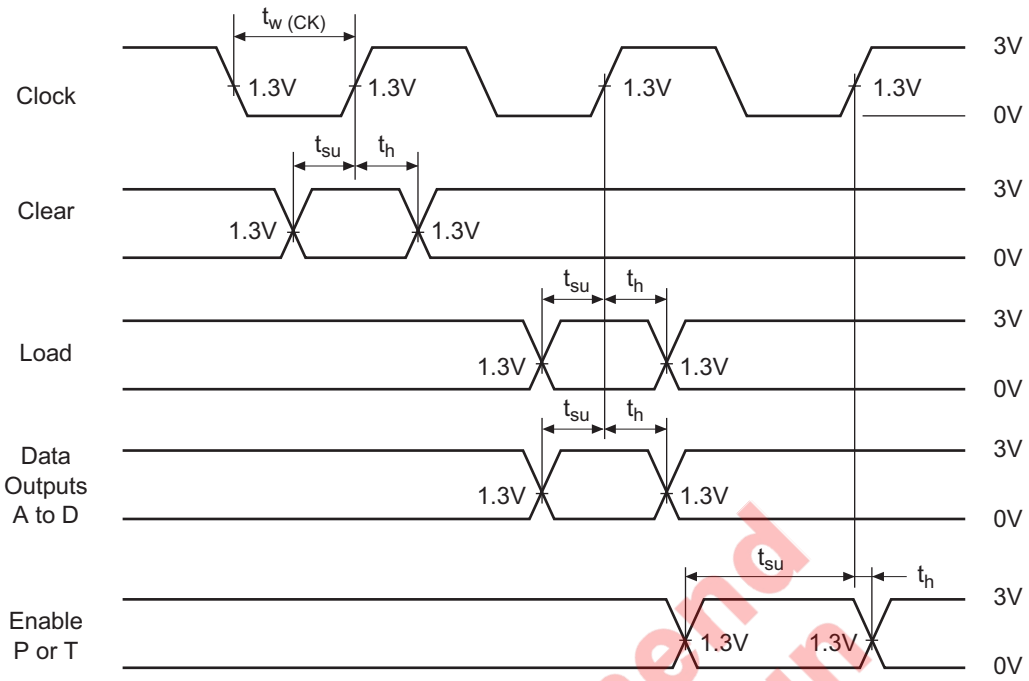
** I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

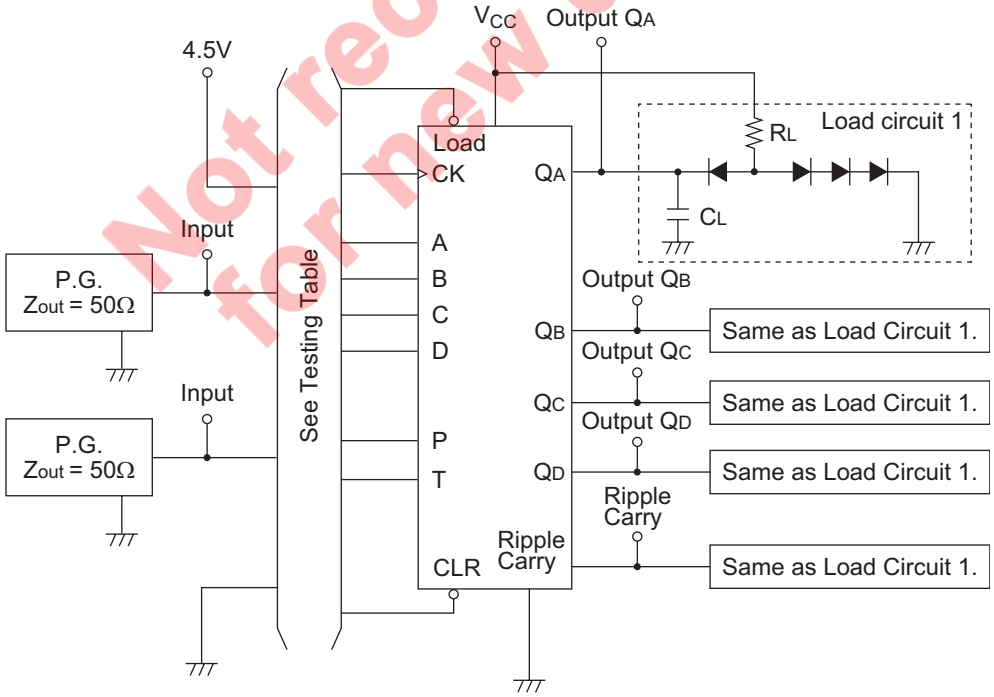
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}	Clock	Q_A to Q_D	25	32	—	MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PLH}	Clock	Ripple Carry	—	20	35	ns	
	t_{PHL}			—	18	35	ns	
	t_{PLH}	Clock (Load = “H”)	Q_A to Q_D	—	13	24	ns	
	t_{PHL}			—	18	27	ns	
	t_{PLH}	Clock (Load = “L”)	Q_A to Q_D	—	13	24	ns	
	t_{PHL}			—	18	27	ns	
	t_{PLH}	Enable T	Ripple Carry	—	9	14	ns	
	t_{PHL}			—	9	14	ns	
	t_{PHL}	Clear	Q_A to Q_D	—	20	28	ns	

Timing Method



Testing Method

Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

Testing Table

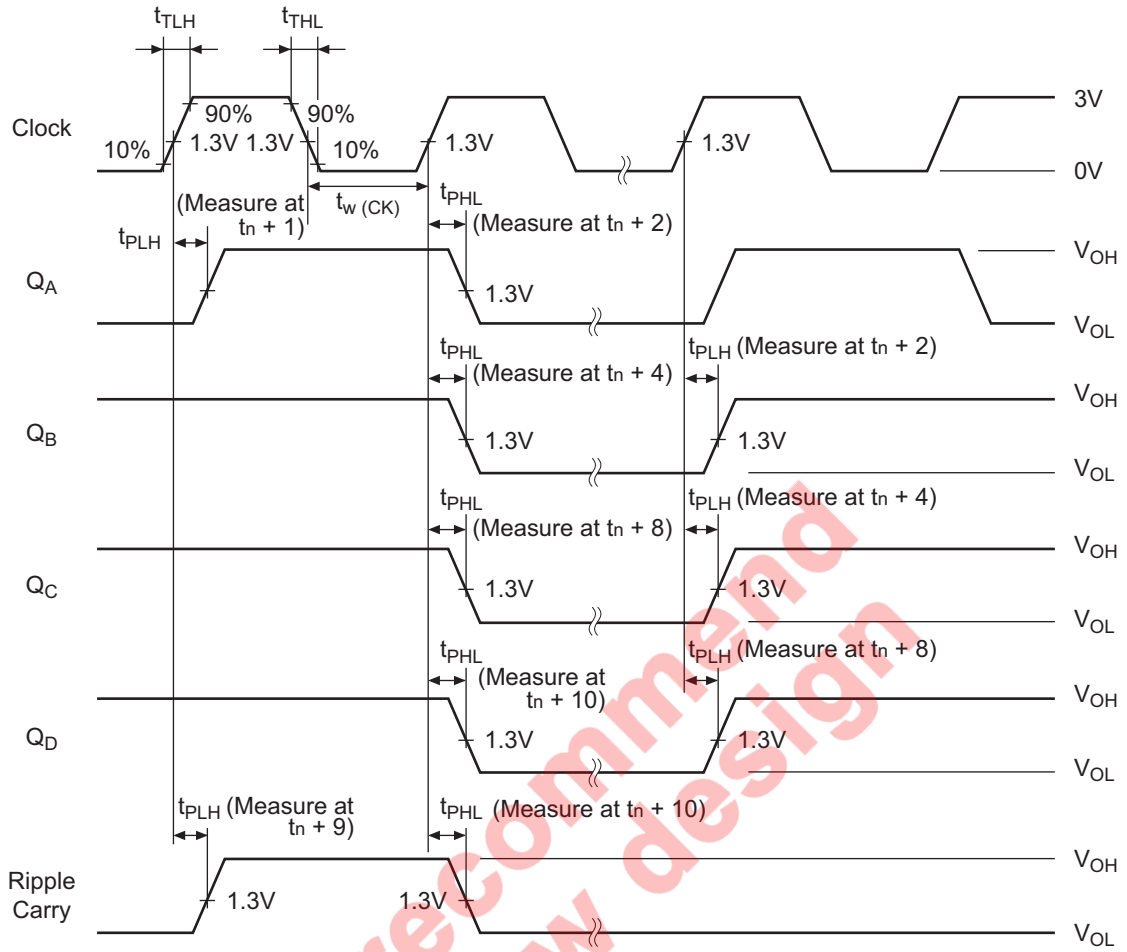
Item	From input to output	Inputs								
		Clear	Load	Enable		Clock	Data			
				P	T		A	B	C	D
f_{max}		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
t_{PLH} t_{PHL}	CK → Ripply Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND
	CK → Q	4.5V	GND	GND	GND	IN	IN*	IN*	IN*	IN*
	Enable T → Ripple Carry	4.5V	GND	4.5V	IN	IN**	4.5V	GND	GND	4.5V
	CLR → Q	IN	GND	GND	GND	IN**	4.5V	4.5V	4.5V	4.5V

Notes: *. Measuring outputs correspond to this condition, each outputs (Q_A, Q_B, Q_C, and Q_D) must not be over the following rate, “H”, “L”, “L”, and “H”.
**. For initialized

Item	From input to output	Outputs				
		Q_A	Q_B	Q_C	Q_D	Ripple Carry
f_{max}		OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CK→Ripple Carry	—	—	—	—	OUT
	CK→Q	OUT	OUT	OUT	OUT	—
	CK→Q	OUT	OUT	OUT	OUT	—
	Enable T→Ripple Carry	—	—	—	—	OUT
	CLR→Q	OUT	OUT	OUT	OUT	—

Waveforms 1

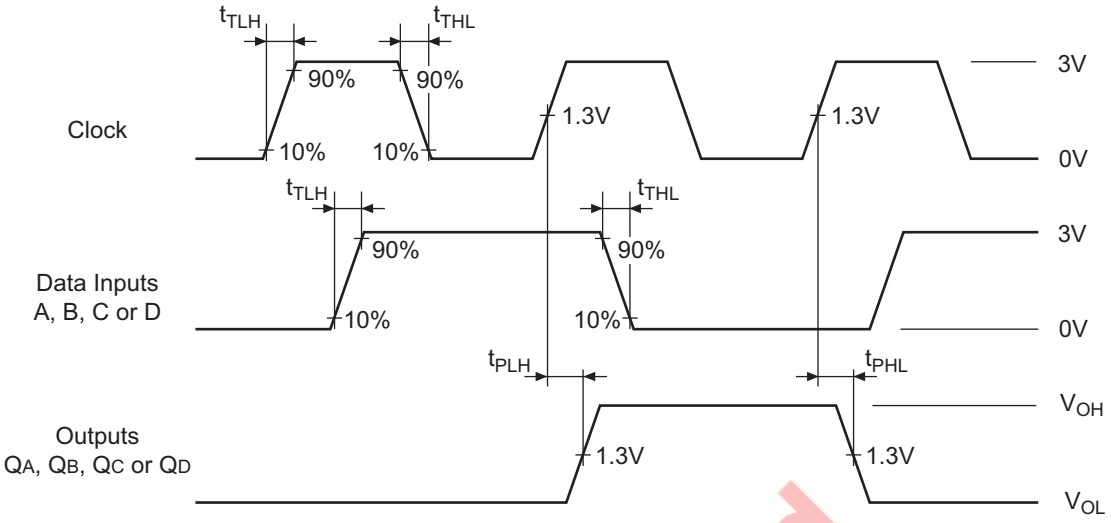
f_{max}, t_{PLH}, t_{PHL}, (Clock→Q, Ripple Carry)



Note: Clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle 50%
and : f_{max} $t_{TLH} = t_{THL} \leq 2.5$ ns.
t_n is reference bit time when all outputs are low.

Waveforms 2

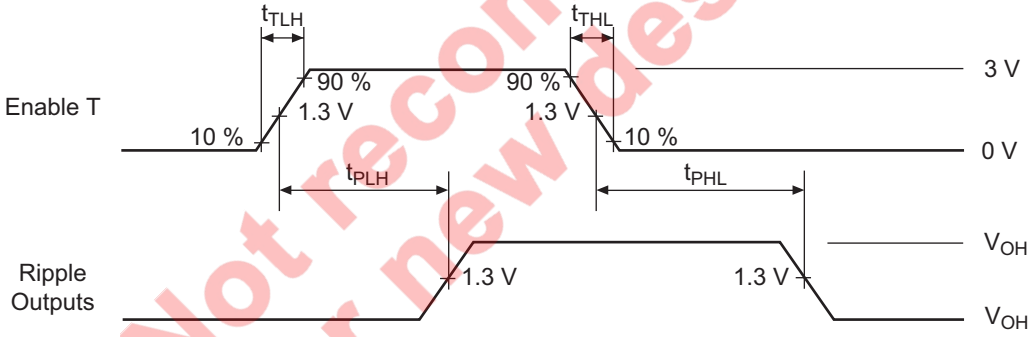
t_{PLH}, t_{PHL}, (Clock→Q)



Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, Clock input: PRR = 1 MHz, duty cycle 50%, Data input: PRR = 500 kHz, duty cycle 50%

Waveforms 3

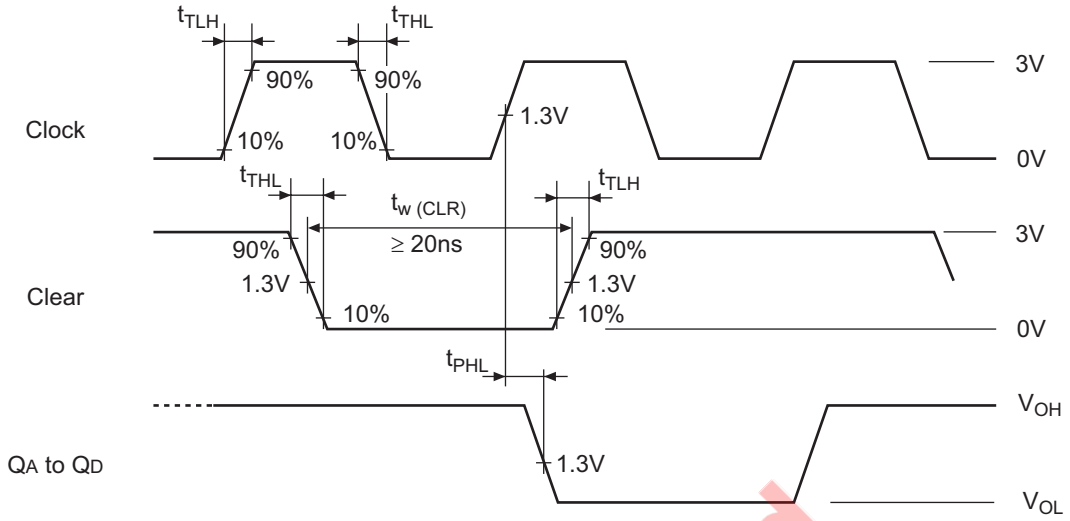
t_{PLH}, t_{PHL}, (Enable T→Ripple Carry)



Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz

Waveforms 4

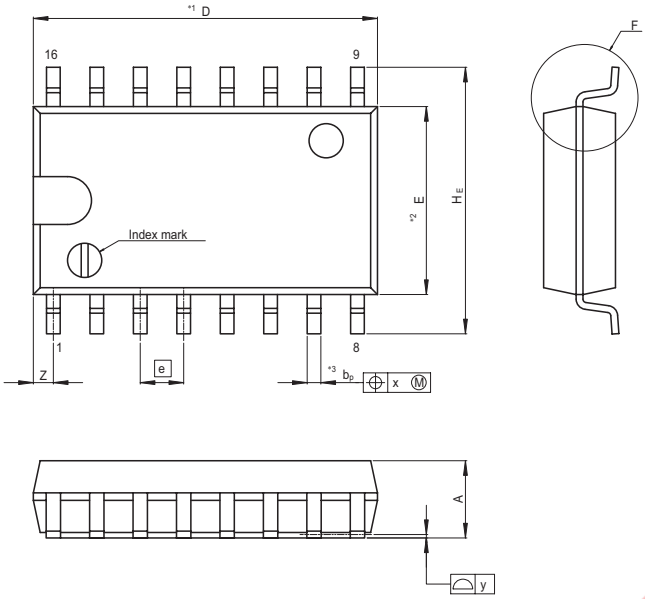
t_{PHL}, (Clear→Q)



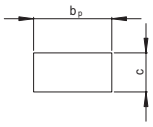
Note: Input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns

Package Dimensions

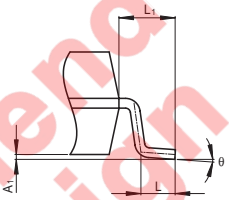
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A_2	——	——	——
A_1	0.00	0.10	0.20
A	——	——	2.20
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.15	0.20	0.25
c_1	——	——	——
θ	0°	——	8°
H_E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L_1	——	1.15	——

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