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Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS HD74LS375 Quadruple Bistable Latches

> REJ03D0484-0200 Rev.2.00 Feb.18.2005

The HD74LS375 bistable latch is electrically and functionally identical to the HD74LS75, respectively. Only the arrangement of the terminals has been changed in the HD74LS375. This latch is ideally suited for use as temporary storage for binary information between processing units and input / output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable goes high.

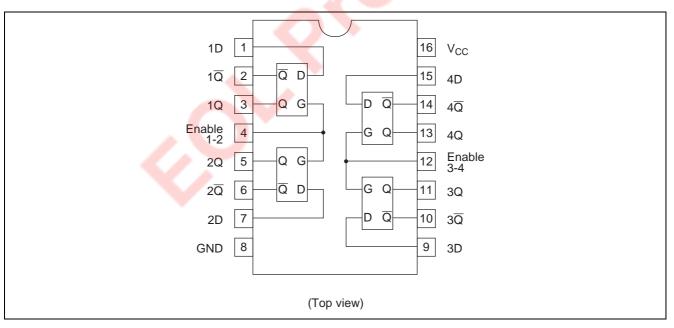
Features

• Ordering Information

| Part Name | Package Type | Package Code (Previous Code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|---------------|--------------------|---------------------------------|-------------------------|-----------------------------------|
| HD74LS375P | DILP-16 pin | PRDP0016AE-B (DP-16FV) | P | — |
| HD74LS375FPEL | SOP-16 pin (JEITA) | PRSP0016DH-B (FP-16DAV) | FP | EL (2,000 pcs/reel) |

Note: Please consult the sales office for the above package availability.

Pin Arrangement





Function Table

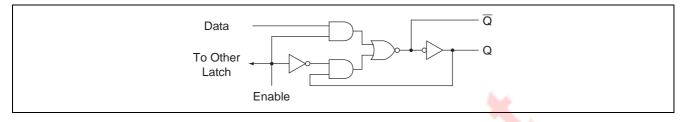
| Inp | uts | Outputs | | | |
|-----|-----|---------|------------------|--|--|
| D | G | Q | ā | | |
| L | Н | L | н | | |
| Н | Н | Н | L | | |
| X | L | Q_0 | \overline{Q}_0 | | |

Notes: H; high level, L; low level, X; irrelevant

 Q_0 ; level of Q before the indicated steady state input conditions were established

 \overline{Q}_0 ; complement of Q_0 or level of \overline{Q} before the indicated steady state input conditions were established

Block Diagram (1/4)



Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit |
|---------------------|-----------------|-------------|------|
| Supply voltage | V _{CC} | 7 | V |
| Input voltage | V _{IN} | 7 | V |
| Power dissipation | PT | 400 | mW |
| Storage temperature | Tstg | -65 to +150 | °C |

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

| ltem | Symbol | Min | Тур | Max | Unit |
|--------------------------|-----------------|------|------|------|------|
| Supply voltage | V _{cc} | 4.75 | 5.00 | 5.25 | V |
| Output current | I _{OH} | — | — | -400 | μΑ |
| Output current | I _{OL} | — | — | 8 | mA |
| Operating temperature | Topr | -20 | 25 | 75 | °C |
| Enable input pulse width | t _w | 20 | — | — | ns |
| Setup time | t _{su} | 20 | _ | | ns |
| Hold time | t _h | 5 | _ | _ | ns |



Electrical Characteristics

| Item | Symbol | min. | typ.* | max. | Unit | Condition | | | |
|------------------------------|-----------------|------|-------|------|------|--|--|--|--|
| Input voltage | V _{IH} | 2.0 | _ | _ | V | | | | |
| Input voltage | V _{IL} | | | 0.8 | V | | | | |
| Output voltogo | V _{он} | 2.7 | | | V | $\label{eq:VCC} \begin{split} V_{CC} &= 4.75 \ \text{V}, \ V_{\text{IH}} = 2 \ \text{V}, \ V_{\text{IL}} = 0.8 \ \text{V}, \\ I_{\text{OH}} &= -400 \ \mu\text{A} \end{split}$ | | | |
| Output voltage | Va | _ | | 0.4 | V | - | V _{CC} = 4.75 V, | | |
| | V _{OL} | _ | | 0.5 | v | $I_{OL} = 8 \text{ mA}$ | $V_{IH} = 2 V, V_{IL} = 0.8 V$ | | |
| | I _{IH} | _ | | 20 | μA | D | $V_{\rm CC} = 5.25 \text{ V}, \text{ V}_{\rm I} = 2.7 \text{ V}$ | | |
| | | _ | | 80 | | G V _{CC} = | | | |
| Input current | I _{IL} | _ | | -0.4 | mA | D | $V_{\rm CC} = 5.25 \text{ V}, \text{ V}_{\rm I} = 0.4 \text{ V}$ | | |
| input current | | | | -1.6 | ШA | G V _{CC} = | 5.25 V, V ₁ = 0.4 V | | |
| | I | | | 0.1 | mA | D | = 5.25 V, V ₁ = 7 V | | |
| | | | | 0.4 | ШA | G V _{CC} = | 5.25 V, V = 7 V | | |
| Short-circuit output current | los | -20 | — | -100 | mA | V _{CC} = 5.25 V | | | |
| Supply current** | Icc | _ | 6.3 | 12 | mA | V _{CC} = 5.25 V | | | |
| Input clamp voltage | VIK | _ | _ | -1.5 | V | $V_{CC} = 4.75 \text{ V}, \text{ I}_{IN} = -18 \text{ mA}$ | | | |

Notes: * $V_{CC} = 5 V$, Ta = 25°C

 ** I_{CC} is measured with all outputs open and all inputs grounded.

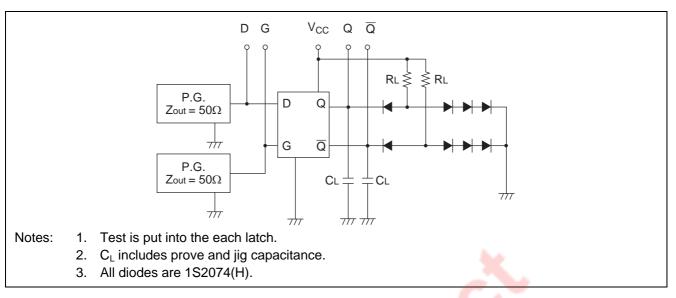
Switching Characteristics

| | | | | | | | $(V_{\rm CC}=5)$ | V, Ta = 25° C) |
|------------------------|------------------|--------|--------|------|------|------|------------------|---|
| ltem | Symbol | Inputs | Output | min. | typ. | max. | Unit | Condition |
| | t _{PLH} | D | Q | - | 15 | 27 | - ns | |
| | t _{PHL} | | | - | 9 | 17 | | $C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega$ |
| | t _{PLH} | D | Q | _ | 12 | 20 | | |
| Propagation delay time | t _{PHL} | | | — | 7 | 15 | | |
| Fropagation delay time | t _{PLH} | G | Q Q | — | 15 | 27 | | |
| | t _{PHL} | | | — | 14 | 25 | | |
| | t _{PLH} | G | | _ | 16 | 30 | | |
| | t _{PHL} | | | — | 7 | 15 | | |
| | | | | | | | | |

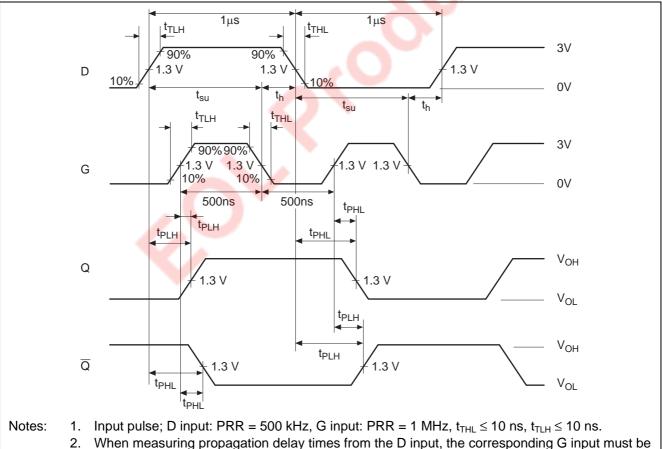


Testing Method

Test Circuit

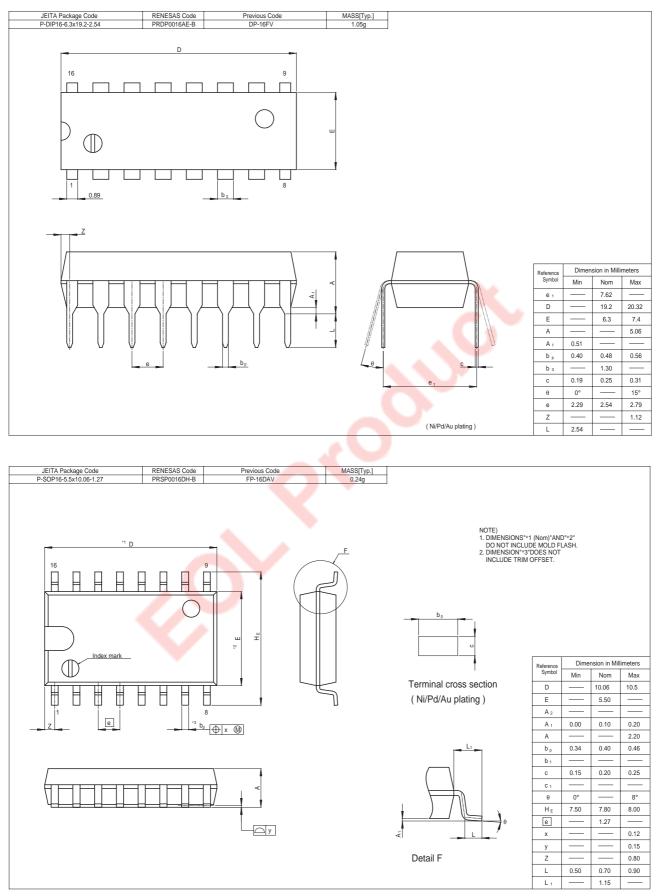


Waveform



held high.

Package Dimensions





Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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