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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74LS77

4-bit Bistable Latches

REJ03D0418-0300 Rev.3.00 Jul.22.2005

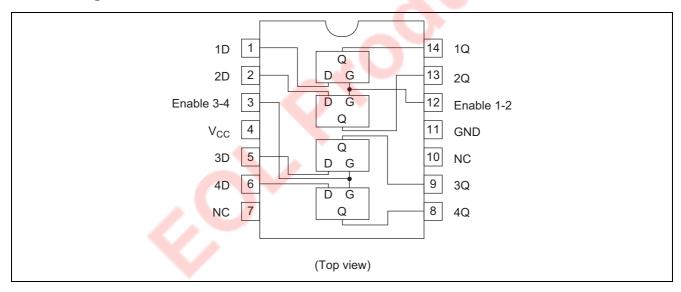
The HD74LS77 is ideally suited for use as temporary storage for binary information between processing units and input / output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

Features

• Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS77FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)

Pin Arrangement

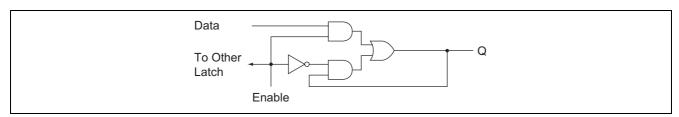


Function Table

Inp	Outputs	
D	G	Q
L	Н	L
Н	Н	Н
X	L	Q_0

H; high level, L; low level, X; irrelevant

Block Diagram (1/4)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	7	V
Input voltage	V _{IN}	7	V
Power dissipation	P _T	400	mW
Storage temperature	Tstg	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

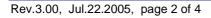
Item	Symbol	Min	Тур	Max	Unit	
Supply voltage	V _{CC}	4.75	5.00	5.25	V	
Output current	I _{OH}	_		-400	μΑ	
Output current	I _{OL}	_		8	mA	
Operating temperature	Topr	-20	25	75	°C	
Pulse width	t _w	20	_	_	ns	
Setup time	t _{su}	20	_	_	ns	
Hold time	t _h	5	_	_	ns	

Electrical Characteristics

 $(Ta = -20 \text{ to } +75 \text{ }^{\circ}\text{C})$

		1	_		Т	Т	(1a = 20 to 175 C)	
Item		Symbol	min.	typ.*	max.	Unit	Condition	
Innut valtage		V _{IH}	2.0	_	_	V		
Input voltage		VIL	7	_	0.8	V		
0 1 1 1		V _{OH}	2.7	_	_	V	$V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V},$ $I_{OH} = -400 \mu\text{A}$	
Output voltage		V _{OL}	_	_	0.4	V	$I_{OL} = 4 \text{ mA}$ $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V},$	
		VOL	_	_	0.5	V	$I_{OL} = 8 \text{ mA}$ $V_{IL} = 0.8 \text{ V}$	
D		I _{IH}	_	_	20		V _{CC} = 5.25 V, V _I = 2.7 V	
	G	I III	_	_	80	μΑ	VCC - 3.23 V, VI - 2.7 V	
Input current	D	I	_	_	-0.4	mA	V _{CC} = 5.25 V, V _I = 0.4 V	
Input current	G	l _{IL}	_	_	-1.6	IIIA	V _{CC} = 5.25 V, V = 0.4 V	
	D	l _l	_	_	0.1	mA	V _{CC} = 5.25 V, V _I = 7 V	
G		11	_	_	0.4	IIIA	$V_{CC} = 5.25 \text{ V}, \text{ V} = 7 \text{ V}$	
Short-circuit output		I _{OS}	-20		-100	mA	V _{CC} = 5.25 V	
current		ios	-20		-100	шА	VCC = 3.23 V	
Supply current	**	I _{CC}		6.9	13	mA	V _{CC} = 5.25 V	
Input clamp vol	tage	V _{IK}	_	_	-1.5	V	$V_{CC} = 4.75 \text{ V}, I_{IN} = -18 \text{ mA}$	

Notes: ${}^*V_{CC} = 5 V$, $Ta = 25 {}^\circ C$



 $^{^{\}star\star}$ I_{CC} is measured with all outputs open and all inputs grounded.

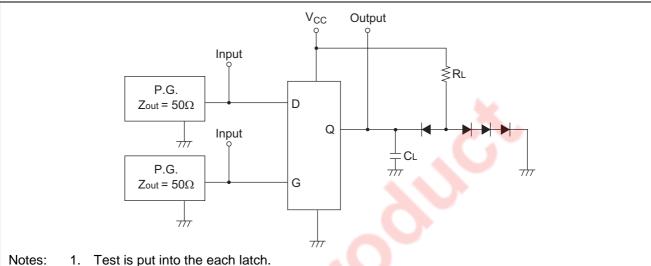
Switching Characteristics

(XI _	5 1	7 7	Ta —	250	\sim
$(V_{CC} =$	י כ	ν. ι	a =	23 '	しり

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Propagation delay time	t _{PLH}	7	Q		11	19	- ns	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega$
	t _{PHL}	ט			9	17		
	t _{PLH}	G	0	_	10	18		
	t _{PHL}	9	α		10	18		

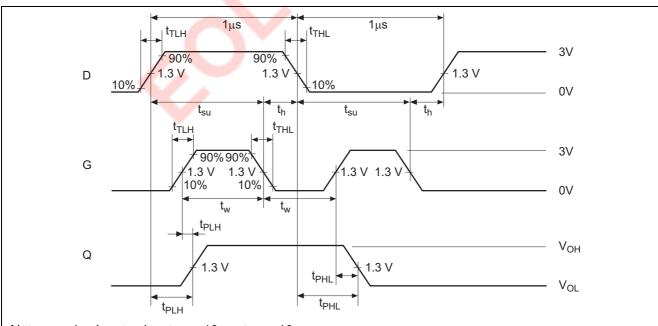
Testing Method

Test Circuit



- Test is put into the each latch.
- C_L includes probe and jig capacitance.
- All diodes are 1S2074(H).

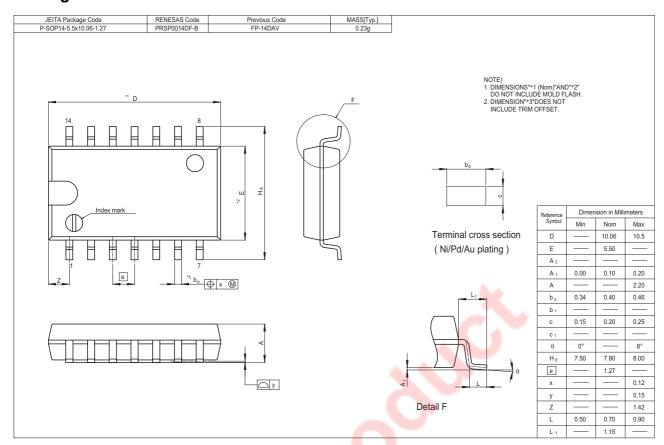
Waveform



Notes:

- Input pulse; $t_{TLH} \le 10$ ns, $t_{THL} \le 10$ ns.
- When measuring propagation delay times from the D input, the corresponding G input must be held high.

Package Dimensions



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