To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74LS83A

4-bit Binary Full Adder (with Fast Carry)

REJ03D0420–0200
Rev.2.00
Feb.18.2005

This improved full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. This adder features full internal look ahead across all four bit generating the carry term in ten nanoseconds typically. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

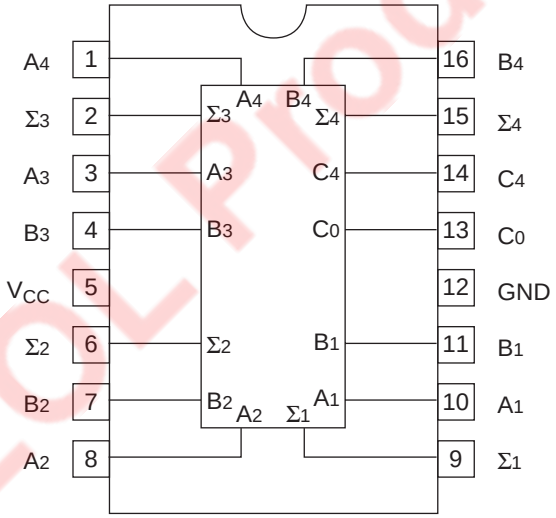
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS83AP	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—

Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

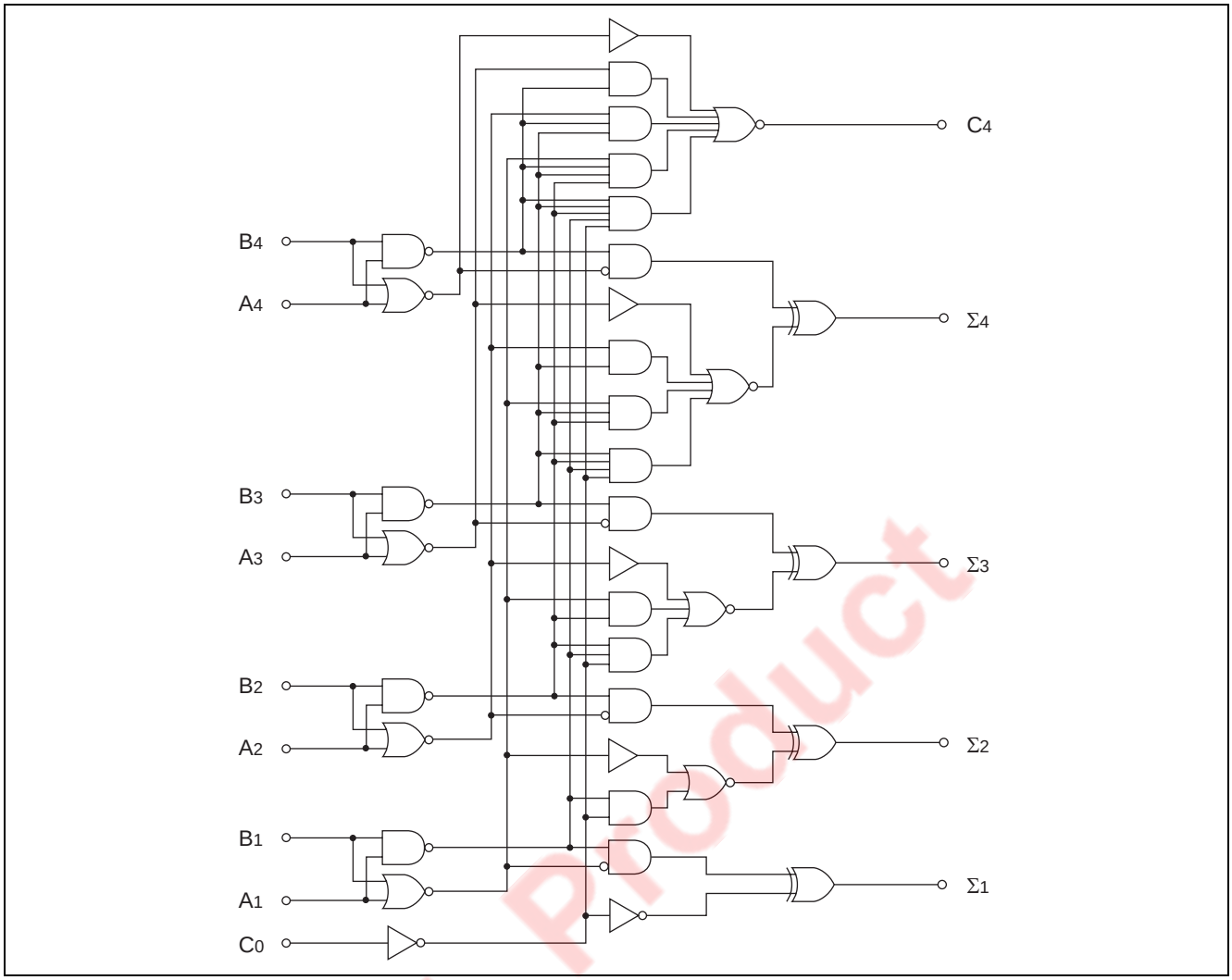
Function Table

Input				Output					
				When C_0 = L			When C_0 = H		
				When C_2 = L			When C_2 = H		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H; high level, L; low level, X; irrelevant

Note: Input conditions at A_1, B_1, A_2, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2 and the value of the internal carry C_2. The value at C_2, A_3, B_3, A_4, and B_4 are than used to determine outputs Σ_3, Σ_4 and C_4.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	–400	µA
	I_{OL}	—	—	8	mA
Operating temperature	Topr	–20	25	75	°C

Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage		V_{IH}	2.0	—	—	V		
		V_{IL}	—	—	0.8	V		
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA	
		V_{OL}	—	—	0.4	V	I_{OL} = 4 mA	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
			—	—	0.5		I_{OL} = 8 mA	
Input current	except C_0	I_{IH}	—	—	40	µA	V_{CC} = 5.25 V, V_I = 2.7 V	
	C_0		—	—	20			
	except C_0	I_{IL}	—	—	–0.8	mA	V_{CC} = 5.25 V, V_I = 0.4 V	
	C_0		—	—	–0.4			
	except C_0	I_I	—	—	0.2	mA	V_{CC} = 5.25 V, V_I = 7 V	
	C_0		—	—	0.1			
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V	
Supply current		I_{CC}	—	22	39	mA	All inputs = 0 V	V_{CC} = 5.25 V
			—	19	34		B input = 0.8 V, Other inputs 4.5 V	
			—	19	34		All inputs = 4.5 V	
Input clamp voltage		V_{IR}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA	

Note: * V_{CC} = 5 V, Ta = 25°C

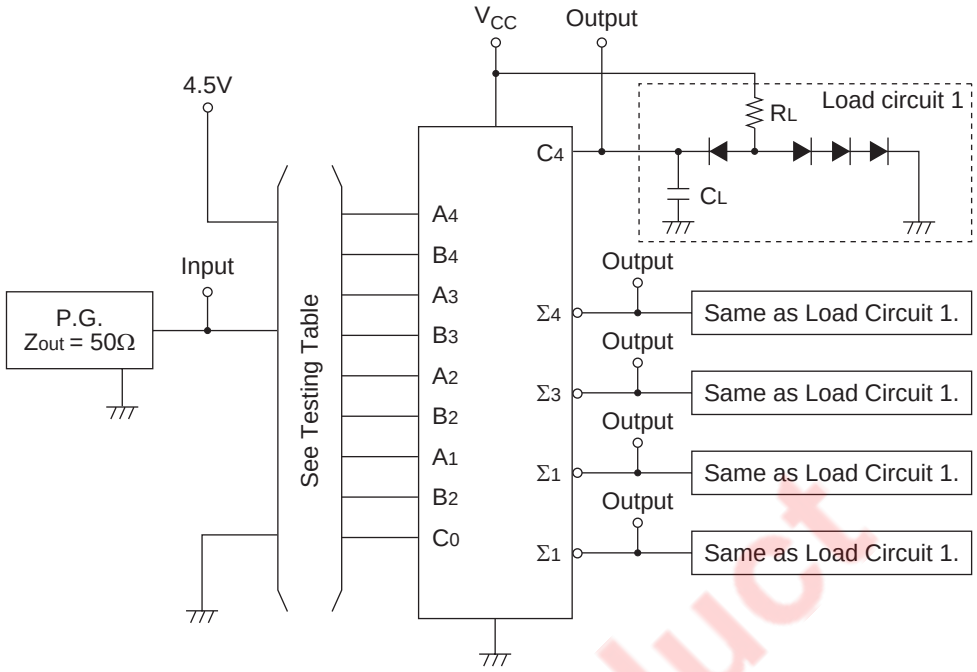
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Propagation delay time	t_{PLH}	C_O	Σ_1	—	16	24	ns	C_L = 15 pF, R_L = 2 kΩ
	t_{PHL}			—	15	24		
	t_{PLH}	A_i, B_i	Σ_1	—	15	24		
	t_{PHL}			—	15	24		
	t_{PLH}	C_O	C_4	—	11	17		
	t_{PHL}			—	15	22		
	t_{PLH}	A_i, B_i	C_4	—	11	17		
	t_{PHL}			—	12	17		

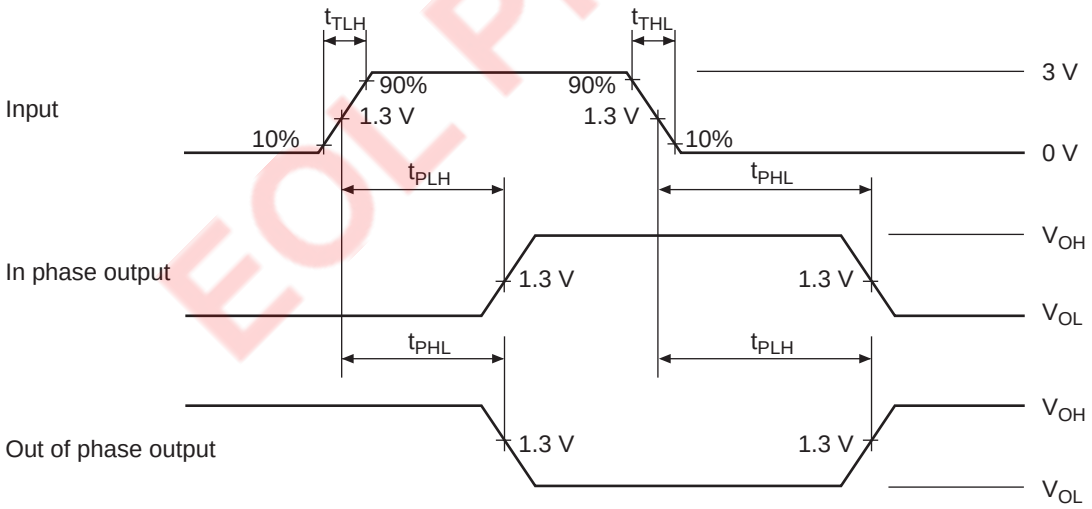
Testing Method

Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

Waveform



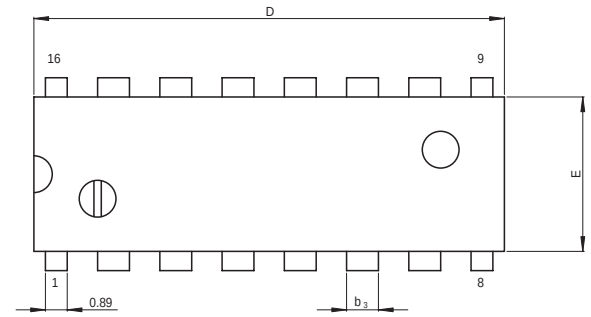
Note: Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50%

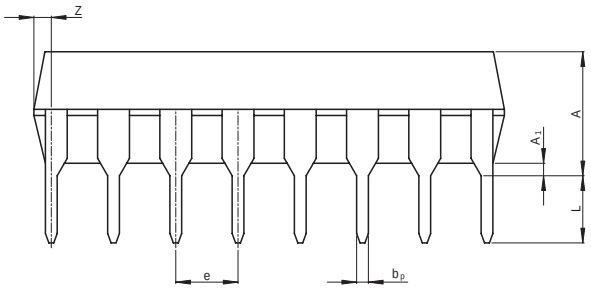
Testing Table

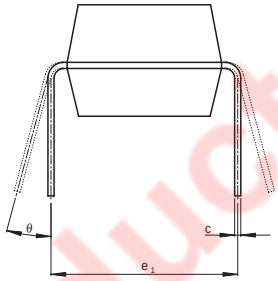
Item	From input to output	Input									Output				
		B_4	A_4	B_3	A_3	B_2	A_2	B_1	A_1	C_0	C_4	Σ_4	Σ_3	Σ_2	Σ_1
t_{PLH} t_{PHL}	$C_O \rightarrow \Sigma_i$ or C_4	GND	GND	GND	GND	GND	GND	GND	GND	IN	—	—	—	—	OUT
		GND	GND	GND	4.5 v	GND	4.5 v	GND	4.5 v	IN	OUT	OUT	OUT	OUT	OUT
	A_i or B_i $\rightarrow \Sigma_i$ or C_4	GND	GND	GND	GND	GND	GND	GND IN	IN GND	GND	—	—	—	—	OUT
		GND	GND	GND	GND	GND IN	IN GND	GND	GND	GND	—	—	—	OUT	—
		GND	GND	GND IN	IN GND	GND	GND	GND	GND	GND	—	—	OUT	—	—
		GND IN	IN GND	GND	GND	GND	GND	GND	GND	GND	—	OUT	—	—	—
		GND	GND	GND	GND	GND	GND	4.5 v IN	IN 4.5 v	GND	—	—	—	OUT	OUT
		GND	GND	GND	GND	4.5 v IN	IN 4.5 v	GND	GND	GND	—	—	OUT	OUT	—
		GND	GND	4.5 v IN	IN 4.5 v	GND	GND	GND	GND	GND	—	OUT	OUT	—	—
		4.5 v IN	IN 4.5 v	GND	GND	GND	GND	GND	GND	GND	OUT	OUT	—	—	—

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g







(Ni/Pd/Au plating)

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A 1	0.51	——	——
b p	0.40	0.48	0.56
b 3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	1.12
L	2.54	——	——

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