To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HD74LVC1G98

Configurable Multiple–Function Gate

REJ03D0013–0400Z
Rev.4.00
Jun. 30, 2004

Description

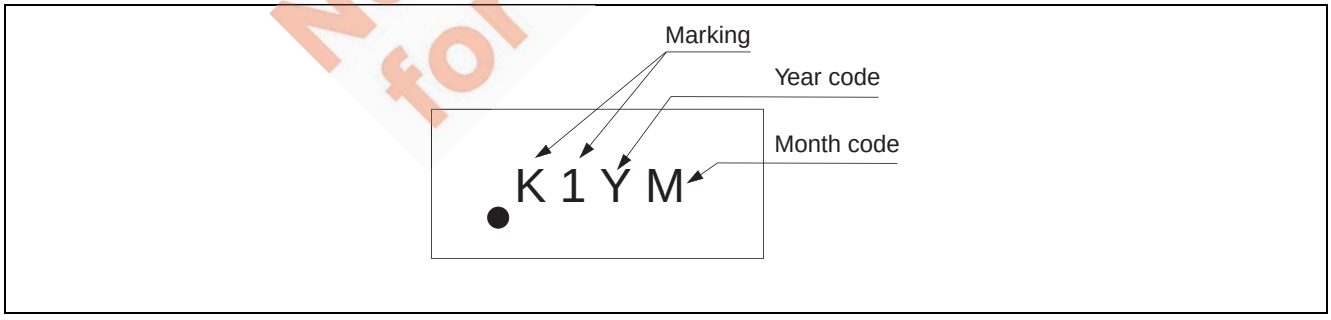
The HD74LVC1G98 has configurable multiple–function gate in a 6-pin package. The Output state is determined by eight patterns of 3–bit input. The user can choose the logic functions AND, NAND, OR, NOR, INVERTER, Non–Inverted Buffer, Data Selector. Low voltage and high-speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

Features

- The basic gate function is lined up as Renesas uni logic series.
- Supply voltage range: 1.65 to 5.5 V
  Operating temperature range: –40 to +85°C
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
  All outputs V_O (Max.) = 5.5 V (@V_{CC} = 0 V)
- Output current: ±4 mA (@V_{CC} = 1.65 V)
  ±8 mA (@V_{CC} = 2.3 V)
  ±24 mA (@V_{CC} = 3.0 V)
  ±32 mA (@V_{CC} = 4.5 V)
- All the logical input has hysteresis voltage for the slow transition.
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVC1G98CPE	WCSP-6 pin	TBS-6V	CP	E (3,000 pcs/reel)
HD74LVC1G98CLE		TBS-6AV	CL	

Article Indication



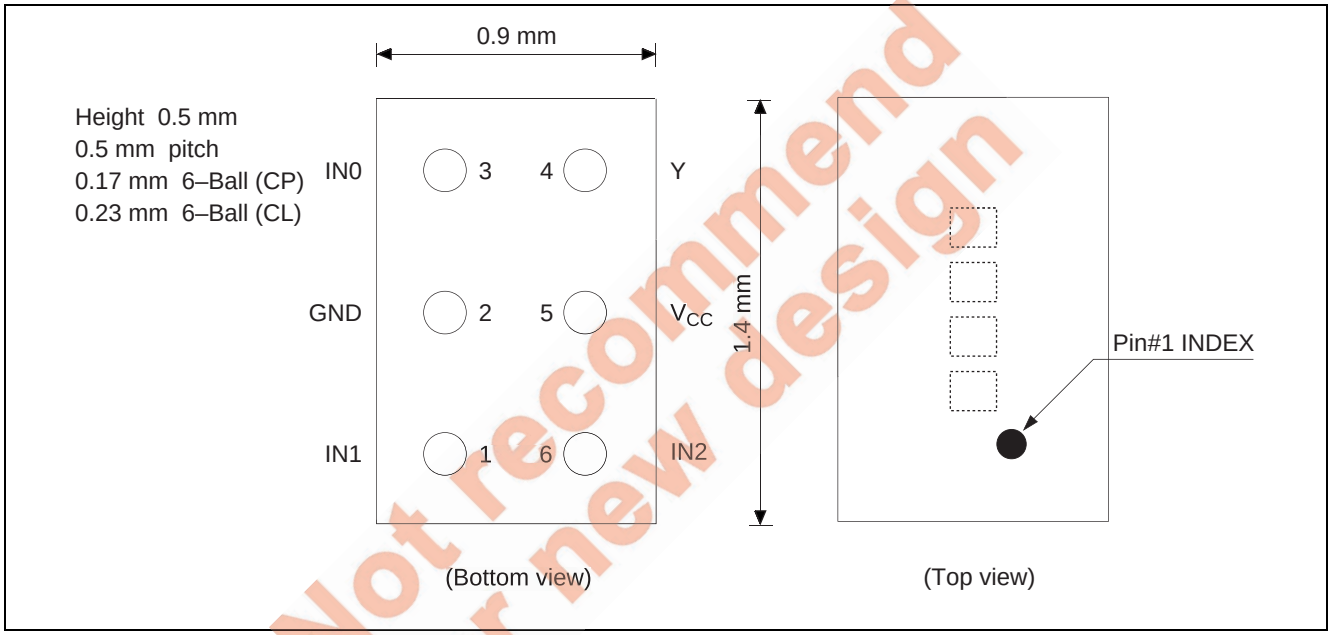
Function Table

Inputs			Output
IN2	IN1	IN0	Y
L	L	L	H
L	L	H	H
L	H	L	L
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

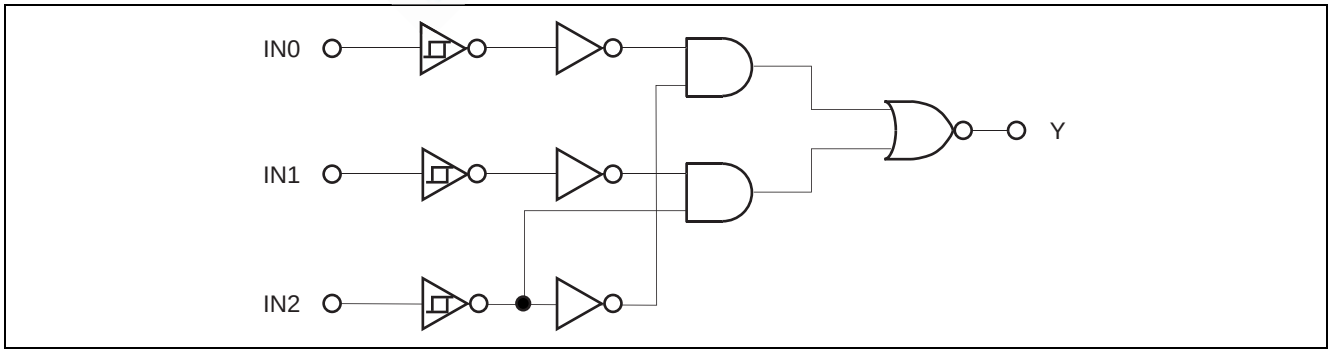
H: High level

L: Low level

Pin Arrangement



Logic Diagram



Function Selection Table

Logic Function	Figure No.
2 to 1 data Selector	1
2–inputs NAND	2
2–inputs NOR with one input inverted	3
2–inputs AND with one input inverted	3
2–inputs NAND with one input inverted	4
2–inputs OR with one input inverted	4
2–inputs NOR	5
Non–Invert Buffer	6
Inverter	7

Logic Configurations

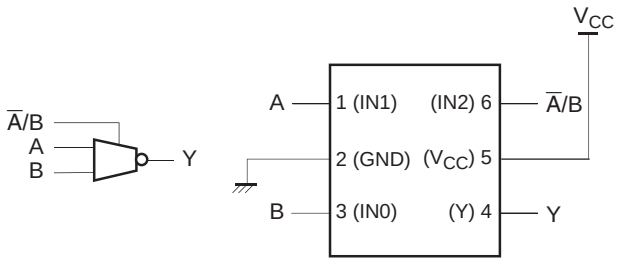


Figure 1. 2 to 1 Data Selector

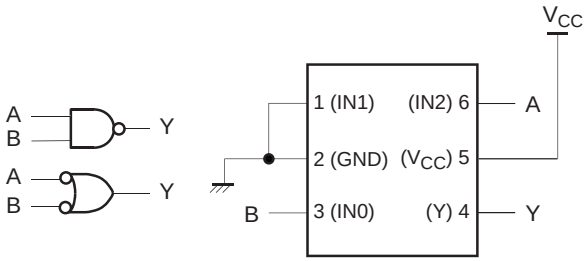


Figure 2. 2–inputs NAND Gate

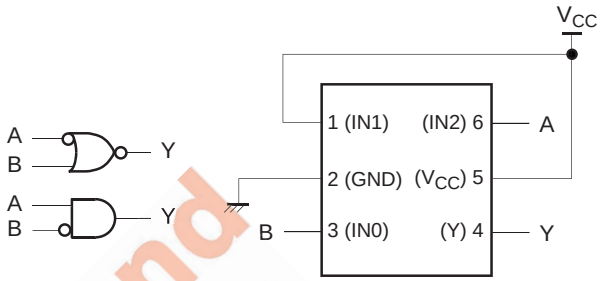


Figure 3. 2–inputs NOR Gate with A input inverted

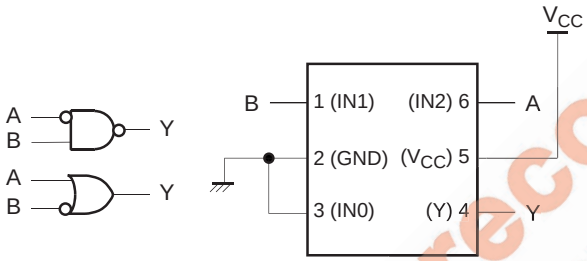


Figure 4. 2–inputs NAND Gate with A input inverted

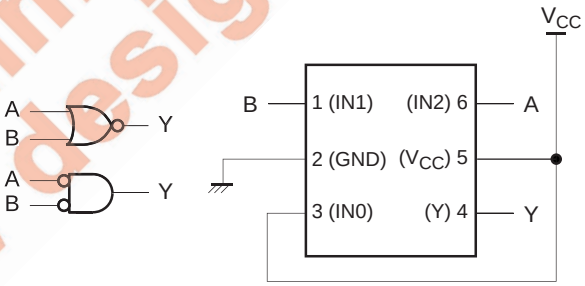


Figure 5. 2–inputs NOR Gate

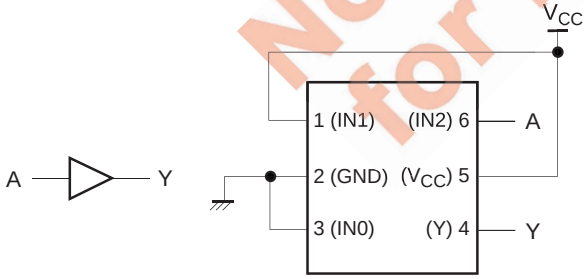


Figure 6. Non–Invert Buffer

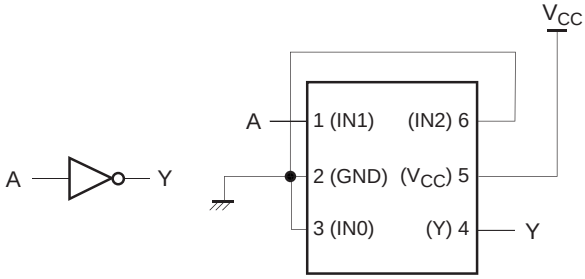


Figure 7. Inverter

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	V_{CC}	–0.5 to 6.5	V	
Input voltage range [*1]	V_I	–0.5 to 6.5	V	
Output voltage range [*1, 2]	V_O	–0.5 to V_{CC} + 0.5	V	Output : H or L
		–0.5 to 6.5		V_{CC} : OFF
Input clamp current	I_{IK}	–50	mA	V_I < 0
Output clamp current	I_{OK}	–50	mA	V_O < 0
Continuous output current	I_O	±50	mA	V_O = 0 to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±100	mA	
Package Thermal impedance	θ_{ja}	143	°C/W	CP
		123		CL
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	1.65	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	
Output current	I_{OL}	—	4	mA	V_{CC} = 1.65 V
		—	8		V_{CC} = 2.3 V
		—	16		V_{CC} = 3.0 V
		—	24		
		—	32		V_{CC} = 4.5 V
	I_{OH}	—	–4		V_{CC} = 1.65 V
		—	–8		V_{CC} = 2.3 V
		—	–16		V_{CC} = 3.0 V
		—	–24		
		—	–32		V_{CC} = 4.5 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	20	ns / V	V_{CC} = 1.65 to 1.95 V, 2.3 to 2.7 V
		0	10		V_{CC} = 3.0 to 3.6 V
		0	5		V_{CC} = 4.5 to 5.5 V
Operating free-air temperature	T_a	–40	85	°C	

Note: Unused or floating inputs must be held high or low.

Electrical Characteristics

Ta = –40 to 85°C

Item	Symbol	V_{CC} (V)	Min	Typ	Max	Unit	Test condition
Threshold voltage	V_T^+	1.8	0.8	—	1.4	V	
		2.5	1.2	—	1.7		
		3.3	1.6	—	2.3		
		5.0	2.3	—	3.0		
	V_T^-	1.8	0.4	—	0.7		
		2.5	0.6	—	1.0		
		3.3	0.9	—	1.4		
		5.0	1.5	—	2.0		
	ΔV_T	1.8	0.4	—	0.7		
		2.5	0.4	—	0.8		
		3.3	0.4	—	0.9		
		5.0	0.4	—	1.0		
Output voltage	V_{OH}	1.65 to 5.5	V_{CC}–0.1	—	—	V	I_{OH} = –100 µA
		1.65	1.2	—	—		I_{OH} = –4 mA
		2.3	1.9	—	—		I_{OH} = –8 mA
		3.0	2.4	—	—		I_{OH} = –16 mA
			2.3	—	—		I_{OH} = –24 mA
		4.5	3.8	—	—		I_{OH} = –32 mA
	V_{OL}	1.65 to 5.5	—	—	0.1		I_{OL} = 100 µA
		1.65	—	—	0.45		I_{OL} = 4 mA
		2.3	—	—	0.3		I_{OL} = 8 mA
		3.0	—	—	0.4		I_{OL} = 16 mA
					0.55		I_{OL} = 24 mA
		4.5	—	—	0.55		I_{OL} = 32 mA
Input current	I_{IN}	0 to 5.5	—	—	±5	µA	V_{IN} = 5.5 V or GND
Quiescent supply current	I_{CC}	5.5	—	—	10	µA	V_{IN} = V_{CC} or GND, I_O = 0
	ΔI_{CC}	3 to 5.5	—	—	500		One input at V_{CC}–0.6 V, Other input at V_{CC} or GND
Output leakage current	I_{OFF}	0	—	—	±10	µA	V_{IN} or V_O = 0 to 5.5 V
Input capacitance	C_{IN}	3.3	—	3.5	—	pF	V_{IN} = V_{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

V_{CC} = 1.8±0.15 V

Item	Symbol	Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Max				
Propagation delay time	t_{PLH} t_{PHL}	3.2	14.4	ns	C_L = 30 pF, R_L = 1.0 kΩ	IN	Y

V_{CC} = 2.5±0.2 V

Item	Symbol	Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Max				
Propagation delay time	t_{PLH} t_{PHL}	2.0	8.3	ns	C_L = 30 pF, R_L = 500 Ω	IN	Y

V_{CC} = 3.3±0.3 V

Item	Symbol	Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Max				
Propagation delay time	t_{PLH} t_{PHL}	1.5	6.3	ns	C_L = 50 pF, R_L = 500 Ω	IN	Y

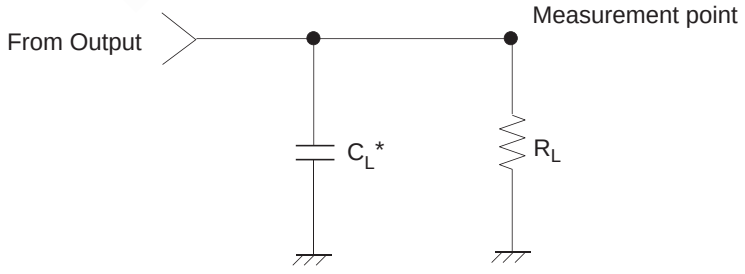
V_{CC} = 5.0±0.5 V

Item	Symbol	Ta = –40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Max				
Propagation delay time	t_{PLH} t_{PHL}	1.1	5.1	ns	C_L = 50 pF, R_L = 500 Ω	IN	Y

Operating Characteristics

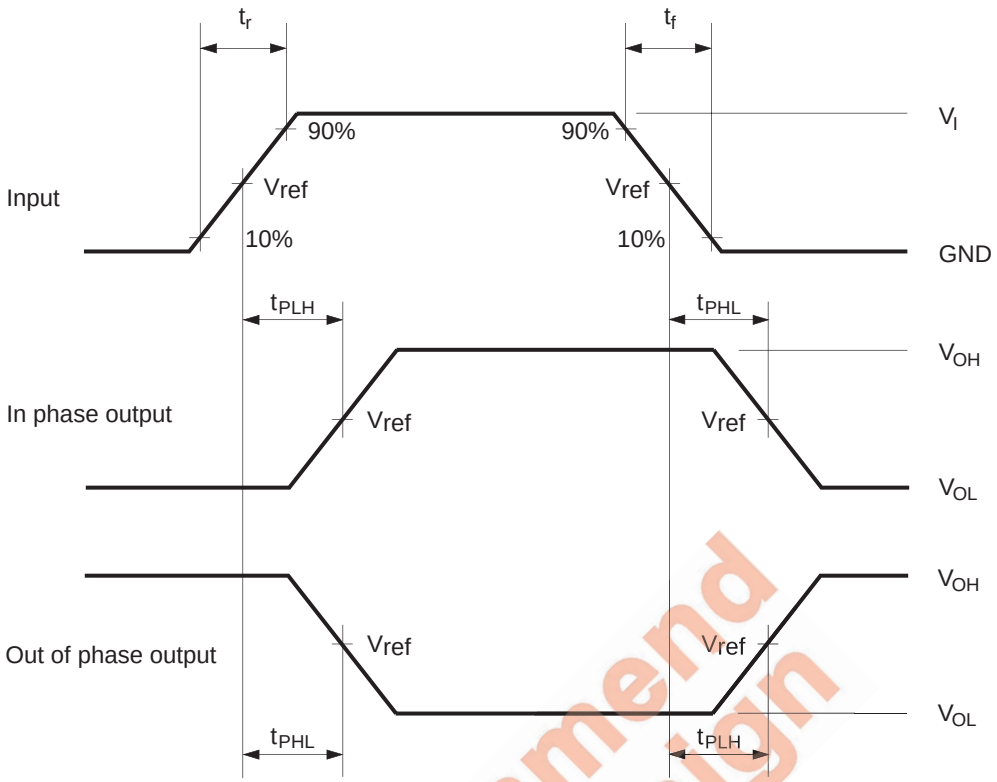
Item	Symbol	V_{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	1.8	—	23	—	pF	f = 10 MHz
		2.5	—	23	—		
		3.3	—	23	—		
		5.0	—	26	—		

Test Circuit



Note: C_L includes probe and jig capacitance.

• **Waveforms**



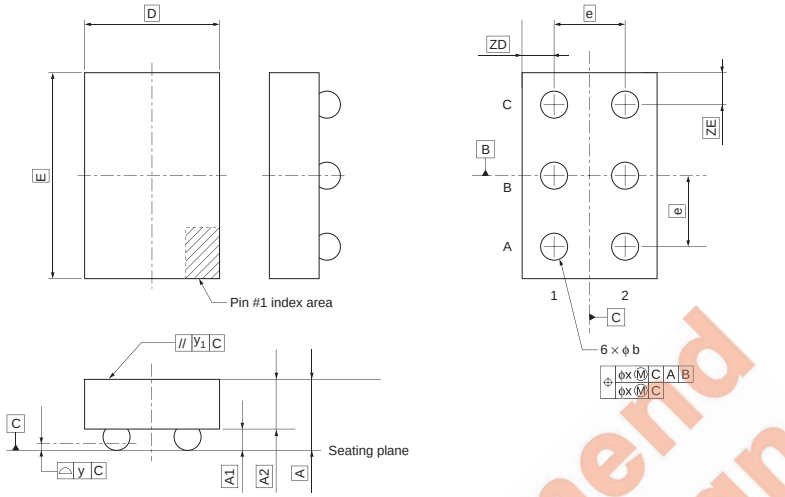
V_{CC} (V)	INPUTS		Vref	C_L	R_L
	V_I	t_r / t_f			
1.8±0.15	V_{CC}	≤ 2 ns	V_{CC} / 2	30 pF	1.0 kΩ
2.5±0.2	V_{CC}	≤ 2 ns	V_{CC} / 2	30 pF	500 Ω
3.3±0.3	3 V	≤ 2.5 ns	1.5 V	50 pF	500 Ω
5.0±0.5	V_{CC}	≤ 2.5 ns	V_{CC} / 2	50 pF	500 Ω

Notes: 1. Input waveform : PRR ≤ 10 MHz, Zo = 50 Ω.
2. The output are measured one at a time with one transition per measurement.

Package Dimensions

TBS-6V

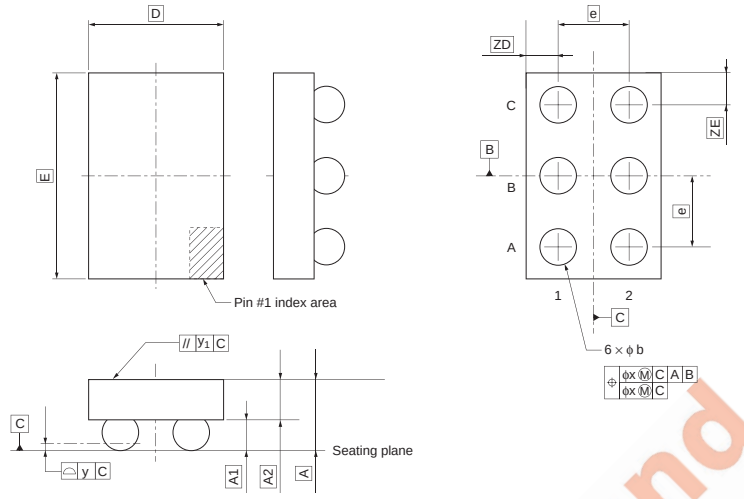
EIAJ Package Code	JEDEC Code	Mass (g)	Lead Material
—	—	0.001	—



Symbol	Dimension in Millimeters		
	Min	Typ	Max
A	———	———	0.50
A_1	0.10	———	0.15
A_2	———	———	0.35
b	0.15	0.17	0.19
D	———	0.90	———
E	———	1.40	———
e	———	0.50	———
x	———	———	0.05
y	———	———	0.05
y_1	———	———	0.20
ZD	———	0.20	———
ZE	———	0.20	———

TBS-6AV

EIAJ Package Code	JEDEC Code	Mass (g)	Lead Material
—	—	0.001	—



*Reference value.

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	———	———	0.50
A_1	0.155	———	0.185
A_2	———	———	(0.315)*
b	0.20	———	0.25
D	———	0.90	———
E	———	1.40	———
e	———	0.50	———
x	———	———	0.05
y	———	———	0.05
y_1	———	———	0.20
ZD	———	0.20	———
ZE	———	0.20	———

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