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RENESAS HD74LVC574A

Octal D-type Flip Flops with 3-state Outputs

REJ03D0361–0400Z (Previous ADE-205-117B (Z)) Rev.4.00 Jul. 29, 2004

Description

The HD74LVC574A has eight edge trigger D type flip flops with three state outputs in a 20 pin package. Data at the D inputs meeting set up requirements are transferred to the Q outputs on positive going transitions of the clock input. When the clock input goes low, data at the D inputs will be retained at the outputs until clock input returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements. Low voltage and high-speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

Features

- $V_{CC} = 2.0 \text{ V}$ to 5.5 V
- All inputs V_{IH} (Max.) = 5.5 V (@V_{CC} = 0 V to 5.5 V)
- All outputs V_{OUT} (Max.) = 5.5 V (@V_{CC} = 0 V or output off state)
- Typical V_{OL} ground bounce < 0.8 V (@V_{CC} = 3.3 V, Ta = 25°C)
- Typical V_{OH} undershoot > 2.0 V (@V_{CC} = 3.3 V, Ta = 25°C)
- High output current $\pm 24 \text{ mA} (@V_{CC} = 3.0 \text{ V to } 5.5 \text{ V})$
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LVC574AFPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD74LVC574ATELL	TSSOP-20 pin	TTP-20DAV	Т	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

Inputs

<u>OC</u>	СК	D	Output Q
L	\uparrow	Н	Н
L	\uparrow	L	L
L	L	Х	Q ₀
Н	Х	Х	Z

H: High level

L: Low level

X: Immaterial

Z: High impedance

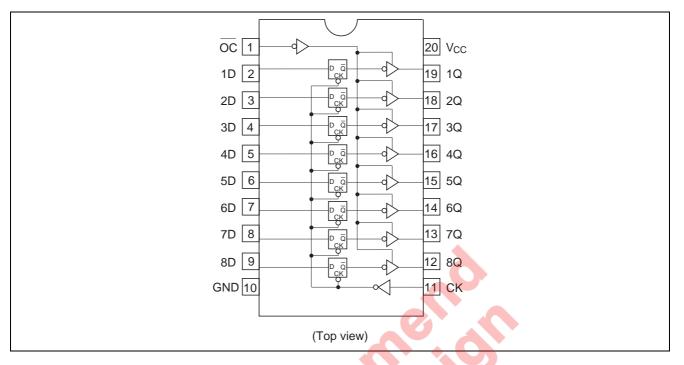
 \uparrow : Low to high transition

Q₀: Level of Q before the indicated steady input conditions were established.



HD74LVC574A

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC}	-0.5 to 6.0	V	
Input diode current	I _{IK}	-50	mA	$V_1 = -0.5 V$
Input voltage	VI	-0.5 to 6.0	V	
Output diode current	I _{OK}	-50	mA	$V_0 = -0.5 V$
		50		$V_{\rm O} = V_{\rm CC} + 0.5 \ V$
Output voltage	Vo	-0.5 to V _{CC} +0.5	V	Output "H" or "L"
	0	-0.5 to 6.0		Output "Z" or V _{CC} :OFF
Output current	lo	±50	mA	
V _{CC} , GND current / pin	I _{CC} or I _{GND}	100	mA	
Storage temperature	Tstg	-65 to +150	°C	

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	Vcc	1.5 to 5.5	V	Data hold
		2.0 to 5.5		At operation
Input / output voltage	VI	0 to 5.5	V	OC, CK, D
	Vo	0 to V _{CC}	V	Output "H" or "L"
		0 to 5.5		Output "Z" or V _{CC} :OFF
Operating temperature	Та	-40 to 85	°C	
Output current	I _{ОН}	-12	mA	$V_{CC} = 2.7 V$
		-24* ²		$V_{CC} = 3.0 \text{ V to } 5.5 \text{ V}$
	I _{OL}	12	mA	$V_{CC} = 2.7 V$
		24 ^{*2}		$V_{CC} = 3.0 \text{ V to } 5.5 \text{ V}$
Input rise / fall time *1	t _r , t _f	10	ns/V	

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

2. Duty cycle $\leq 50\%$

Electrical Characteristics

		Ta = −40 to 85°C						
Item	Symbol	V _{cc} (V)	Min	Max	Unit	Test Conditions		
Input voltage	VIH	2.7 to 3.6	2.0	A	V			
		4.5 to 5.5	V _{cc} ×0.7					
	V _{IL}	2.7 to 3.6	-	0.8	V			
		4.5 to 5.5		V _{CC} ×0.3				
Output voltage	V _{OH}	2.7 to 5.5	V _{cc} -0.2	-	V	I _{OH} = -100 μA		
		2.7	2.2	<u> </u>		$I_{OH} = -12 \text{ mA}$		
		3.0	2.4	Y	_			
		3.0	2.2	_	_	I _{OH} = -24 mA		
		4.5	3.8	—	_			
	V _{OL}	2.7 to 5.5	—	0.2	V	I _{OL} = 100 μA		
		2.7		0.4		I _{OL} = 12 mA		
		3.0	_	0.55		I _{OL} = 24 mA		
	<u> </u>	4.5	_	0.55				
Input current	I _{IN}	0 to 5.5	_	±5.0	μΑ	$V_{IN} = 5.5 \text{ V or GND}$		
Off state output current	I _{OZ}	2.7 to 5.5	—	±5.0	μΑ	$V_{IN} = V_{CC}, GND$		
						$V_{OUT} = 5.5 V \text{ or GND}$		
Output leak current	I _{OFF}	0	_	20	μΑ	$V_{IN} / V_{OUT} = 5.5 V$		
Quiescent supply current	I _{CC}	2.7 to 3.6	_	±10	μΑ	$V_{IN} / V_{OUT} = 3.6 \text{ to } 5.5 \text{ V}$		
		2.7 to 5.5	_	10		$V_{IN} = V_{CC} \text{ or } GND$		
	ΔI_{CC}	3.0 to 3.6	—	500	μΑ	V_{IN} = one input at(V_{CC} -0.6)V,		
						other inputs at V_{CC} or GND		

Switching Characteristics

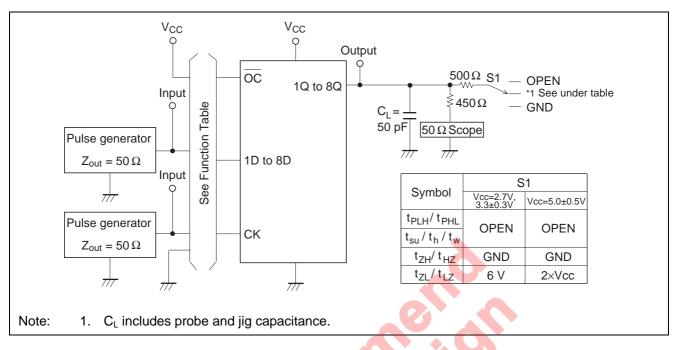
			Ta = −40 to 85°C				From	То
Item	Symbol	V _{cc} (V)	Min	Тур	Max	Unit	(Input)	(Output)
Maximum clock frequency	f _{max}	2.7	80.0	_	_	MHz		
		3.3±0.3	100.0	150.0	_			
		5.0±0.5	125.0	_				
Propagation delay time	t _{PLH}	2.7	_	_	9.5	ns	СК	Q
	t _{PHL}	3.3±0.3	1.5	_	8.5			
		5.0±0.5			7.0			
Output enable time	t _{ZH}	2.7	_	_	9.5	ns	OC	Q
	t _{ZL}	3.3±0.3	1.5		8.5			
		5.0±0.5	_		7.0			
Output disable time	t _{HZ}	2.7	_	_	8.5	ns	OC	Q
	t _{LZ}	3.3±0.3	1.5		7.5			
		5.0±0.5	_		6.5			
Setup time	t _{su}	2.7	2.0	_	_	ns		
		3.3±0.3	2.0	_	_			
		5.0±0.5	2.0	_				
Hold time	t _h	2.7	1.5	_		ns		
		3.3±0.3	1.5		-			
		5.0±0.5	1.5		—			
Pulse width	t _w	2.7	3.3		- 6	ns		
		3.3±0.3	3.3		6			
		5.0±0.5	3.3	- 7				
Between output	t _{OSLH}	2.7			-	ns		
pins skew ^{*1}	t _{OSHL}	3.3±0.3		-	1.0			
		5.0±0.5	—		1.0			
Input capacitance	CIN	2.7	-	3.0	_	pF		
Output capacitance	Co	2.7	-0	15.0	_	pF		

Note: 1. This parameter is characterized but not tested.

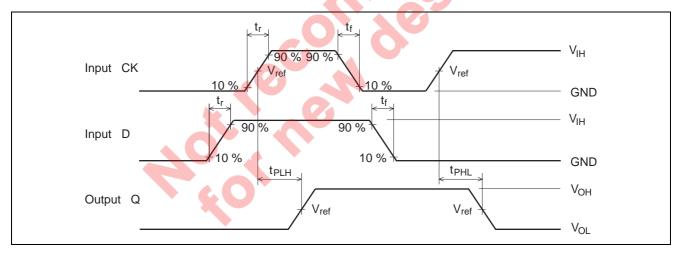
 $tos_{LH} = |t_{PLHm} - t_{PLHn}|, tos_{HL} = |t_{PHLm} - t_{PHLn}|$

HD74LVC574A

Test Circuit

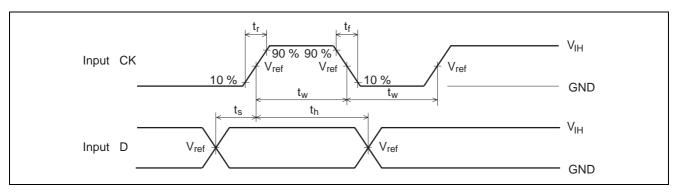


Waveforms - 1

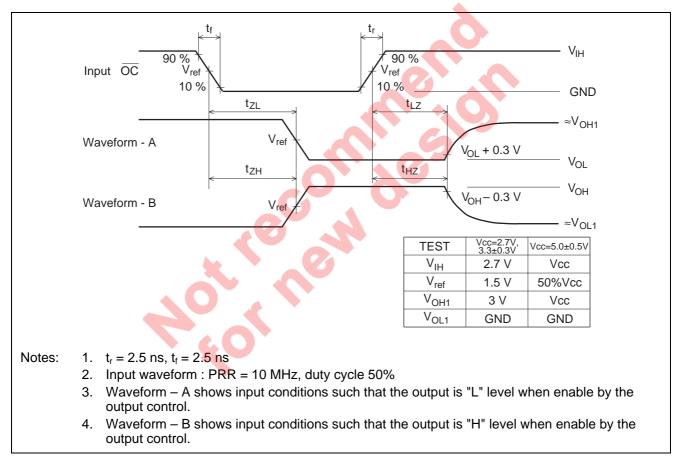


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Waveforms - 2

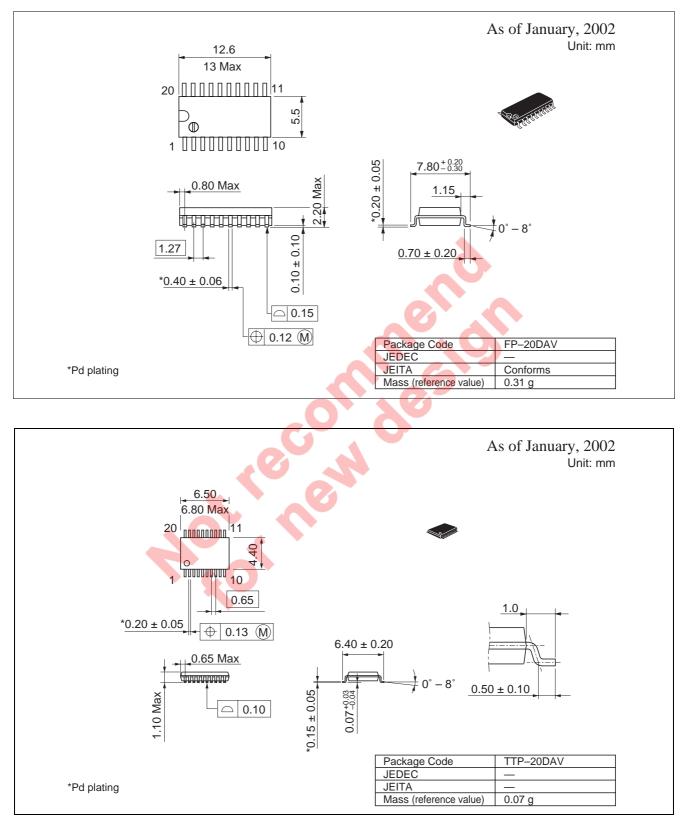


Waveforms - 3





Package Dimensions





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