

## HIP6501A

Triple Linear Power Controller with ACPI Control Interface

FN4749  
 Rev 6.00  
 December 30, 2004

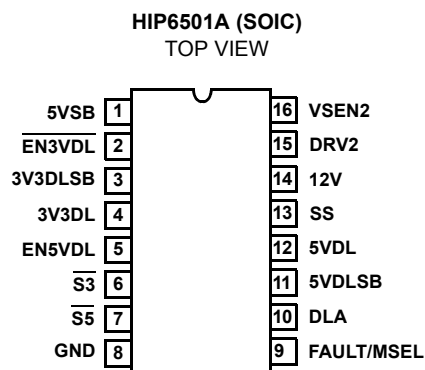
The HIP6501A, paired with either the HIP6020 or HIP6021, simplifies the implementation of ACPI-compliant designs in microprocessor and computer applications. The IC integrates two linear controllers and a low-current pass transistor, as well as the monitoring and control functions into a 16-pin SOIC package. One linear controller generates the 3.3V<sub>DUAL</sub> voltage plane from an ATX power supply's 5VSB output during sleep states (S3, S4/S5), powering the PCI slots through an external pass transistor, as instructed by the status of the 3.3V<sub>DUAL</sub> enable pin. An additional pass transistor is used to switch in the ATX 3.3V output for PCI operation during S0 and S1 (active) operating states. The second linear controller supplies the computer system's 2.5V/3.3V memory power through an external pass transistor in active states. During S3 state, an integrated pass transistor supplies the 2.5V/3.3V sleep-state power. A third controller powers up a 5V<sub>DUAL</sub> plane by switching in the ATX 5V output in active states, or the ATX 5VSB in sleep states.

The HIP6501A's operating mode (active-state outputs or sleep-state outputs) is selectable through two control pins:  $\overline{S3}$  and  $\overline{S5}$ . Further control of the logic governing activation of different power modes is offered through two enabling pins:  $\overline{EN3VDL}$  and  $\overline{EN5VDL}$ . In active states, the 3.3V<sub>DUAL</sub> linear regulator uses an external N-Channel pass MOSFET to connect the output ( $V_{OUT1}$ ) directly to the 3.3V input supplied by an ATX (or equivalent) power supply, while incurring minimal losses. In sleep state, the 3.3V<sub>DUAL</sub> output is supplied from the ATX 5VSB through an NPN transistor, also external to the controller. Active state power delivery for the 2.5/3.3V<sub>MEM</sub> output is done through an external NPN transistor, or an NMOS switch for the 3.3V setting. In sleep states, conduction on this output is transferred to an internal pass transistor. The 5V<sub>DUAL</sub> output is powered through two external MOS transistors. In sleep states, a PMOS (or PNP) transistor conducts the current from the ATX 5VSB output, while in active states, current flow is transferred to an NMOS transistor connected to the ATX 5V output. Similar to the 3.3V<sub>DUAL</sub> output, the operation of the 5V<sub>DUAL</sub> output is dictated not only by the status of the  $\overline{S3}$  and  $\overline{S5}$  pins, but that of the  $\overline{EN5VDL}$  pin as well.

### Features

- Provides 3 ACPI-Controlled Voltages
  - 5V Active/Sleep (5V<sub>DUAL</sub>)
  - 3.3V Active/Sleep (3.3V<sub>DUAL</sub>)
  - 2.5V/3.3V Active/Sleep (2.5V<sub>MEM</sub>)
- Simple Control Design - No Compensation Required
- Excellent Output Voltage Regulation
  - 3.3V<sub>DUAL</sub> Output:  $\pm 2.0\%$  Over Temperature; Sleep States Only
  - 2.5V/3.3V Output:  $\pm 2.0\%$  Over Temperature; Both Operational States (3.3V setting in sleep only)
- Fixed Output Voltages Require No Precision External Resistors
- Small Size
  - Small External Component Count
- Selectable 2.5V<sub>MEM</sub> Output Voltage Via FAULT/MSEL Pin
  - 2.5V for RDRAM Memory
  - 3.3V for SDRAM Memory
- Under-Voltage Monitoring of All Outputs with Centralized FAULT Reporting
- Adjustable Soft-Start Function Eliminates 5VSB Perturbations
- Pb-Free Available (RoHS Compliant)

### Pinout



### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIP6501ACB	0 to 70	16 Ld SOIC	M16.15
HIP6501ACBZ (Note)	0 to 70	16 Ld SOIC (Pb-free)	M16.15
HIP6501AEVAL1	Evaluation Board		

\*Add "-T" suffix to part number for tape and reel packaging.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Block Diagram

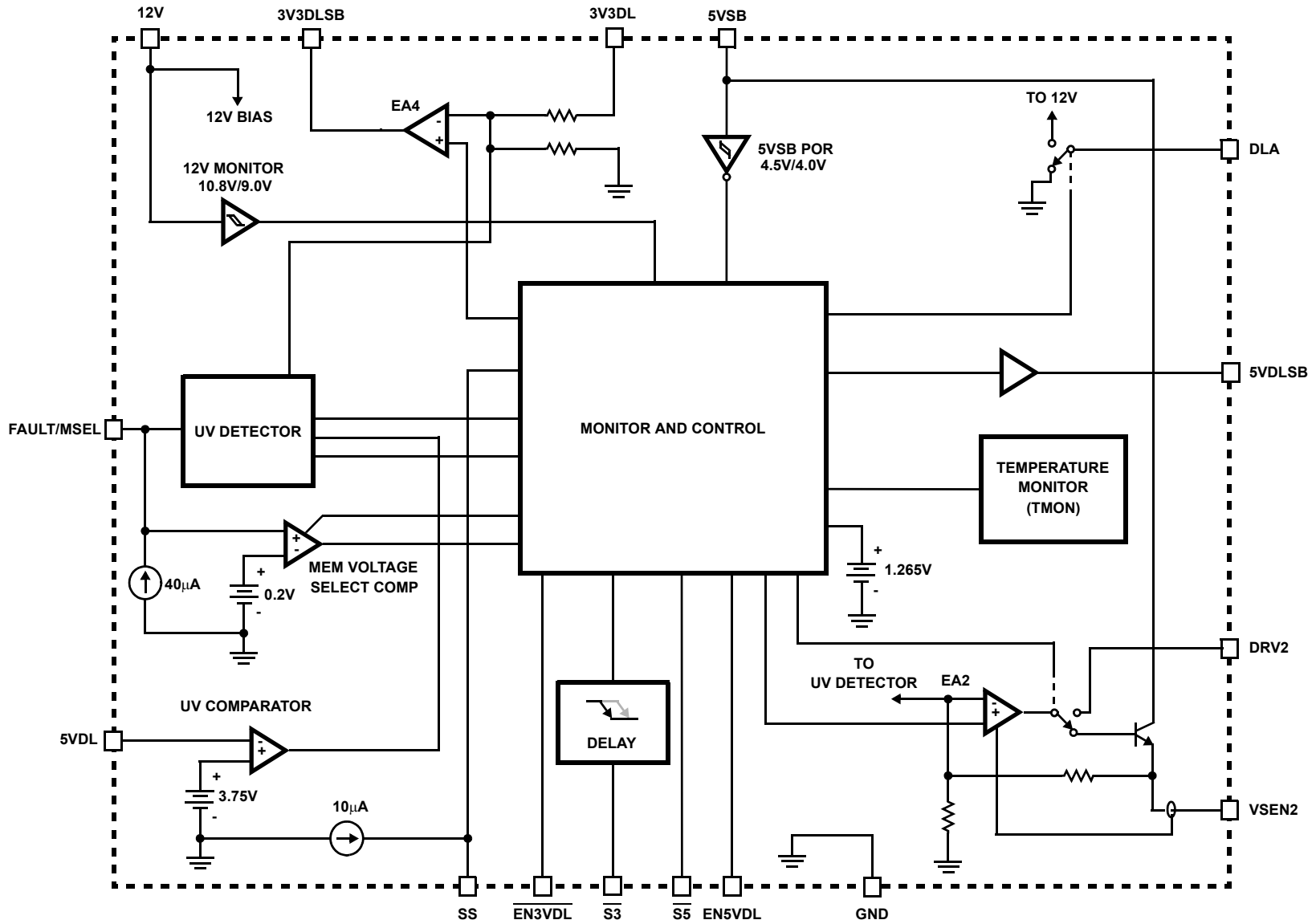


FIGURE 1.

**Simplified Power System Diagram**

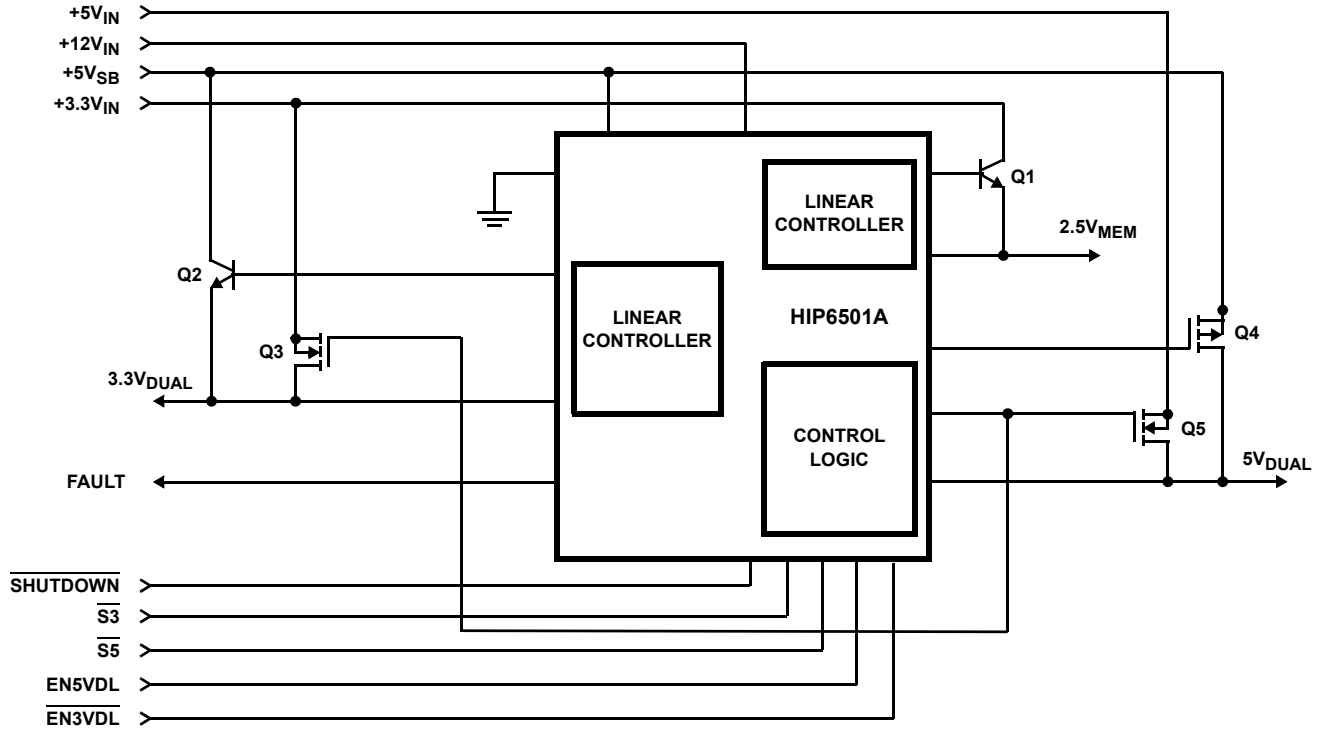


FIGURE 2.

**Typical Application**

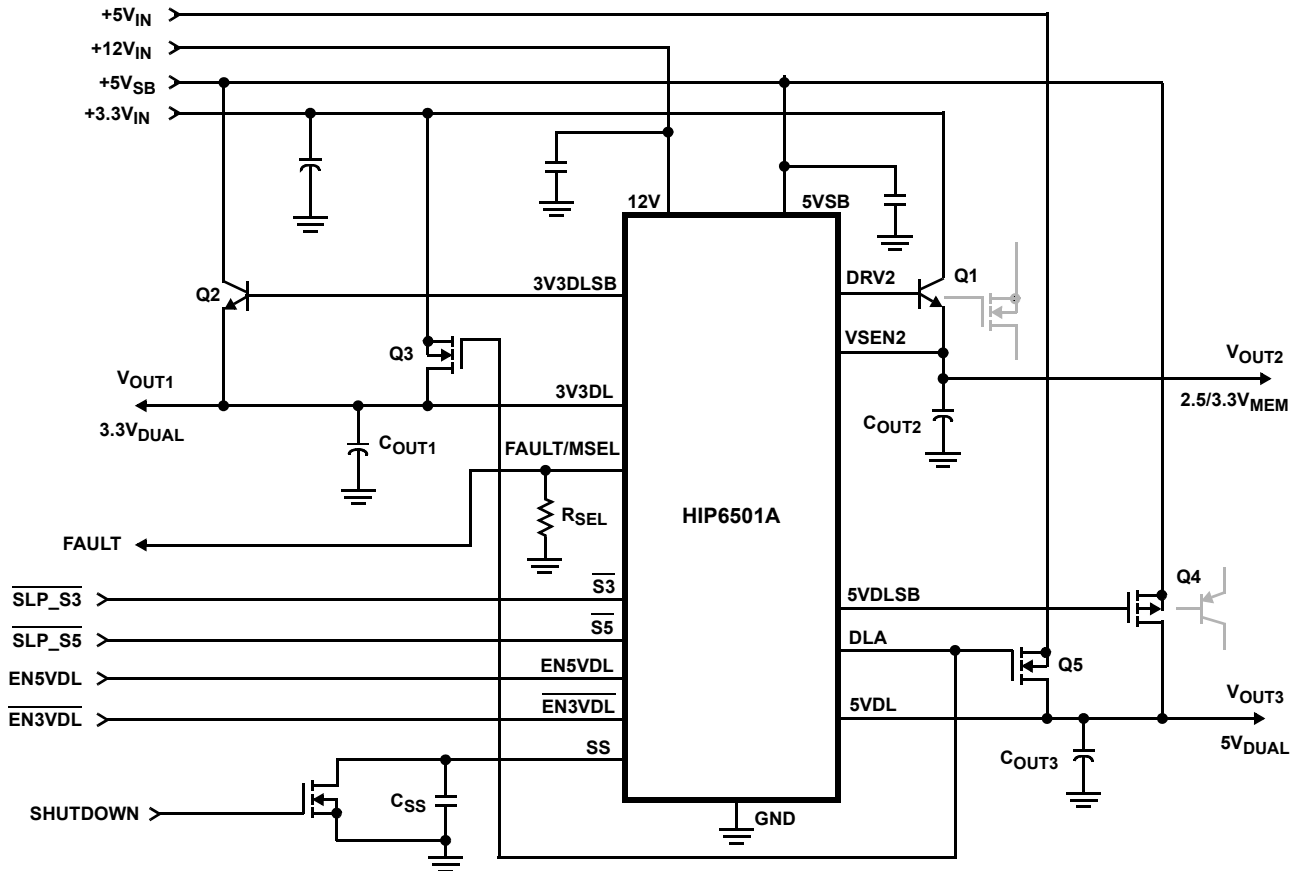


FIGURE 3.

**Absolute Maximum Ratings**

Supply Voltage, $V_{5VSB}$	+7.0V
12V	GND - 0.3V to +14.5V
DLA, DRV2	GND - 0.3V to $V_{12V}$ +0.3V
All Other Pins	GND - 0.3V to 5VSB + 0.3V
ESD Classification	Class 3 [5kV]

**Recommended Operating Conditions**

Supply Voltage, $V_{5VSB}$	+5V $\pm$ 5%
Secondary Bias Voltage, $V_{12V}$	+12V $\pm$ 10%
Digital Inputs, $\overline{V_{S3}}$ , $\overline{V_{S5}}$ , $\overline{V_{EN3VDL}}$ , $\overline{V_{EN5VDL}}$	0 to +5.5V
Ambient Temperature Range	0°C to 70°C
Junction Temperature Range	0°C to 125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

## NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Thermal Information**

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
SOIC Package	100
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (SOIC - Lead Tips Only)

**Electrical Specifications** Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>VCC SUPPLY CURRENT</b>						
Operating Supply Current	$I_{5VSB}$		-	20	-	mA
Shutdown Supply Current	$I_{5VSB(OFF)}$	$V_{SS} = 0.8V$ , $\overline{S3} = 0$ , $\overline{S5} = 0$	-	10	-	mA
<b>POWER-ON RESET, SOFT-START, AND 12V MONITOR</b>						
Rising 5VSB POR Threshold			-	-	4.5	V
5VSB POR Hysteresis			-	0.2	-	V
Rising 12V Threshold			-	-	10.8	V
Soft-Start Current			-	10	-	$\mu$ A
Shutdown Soft-Start Voltage			-	-	0.8	V
<b>2.5V/3.3V LINEAR REGULATOR (<math>V_{OUT2}</math>)</b>						
Regulation			-	-	2.0	%
VSEN2 Nominal Voltage Level	$V_{VSEN2}$	$R_{SEL} = 1k\Omega$	-	2.5	-	V
VSEN2 Nominal Voltage Level	$V_{VSEN2}$	$R_{SEL} = 10k\Omega$	-	3.3	-	V
VSEN2 Under-voltage Rising Threshold			-	75	-	%
VSEN2 Under-voltage Hysteresis			-	6	-	%
VSEN2 Output Current	$I_{VSEN2}$	5VSB = 5V	250	300	-	mA
DRV2 Output Drive Current	$I_{DRV2}$	5VSB = 5V, $R_{SEL} = 1k\Omega$	20	30	-	mA
DRV2 Output Impedance		$R_{SEL} = 10k\Omega$	-	200	-	$\Omega$
<b>3.3VDUAL LINEAR REGULATOR (<math>V_{OUT1}</math>)</b>						
Sleep-Mode Regulation			-	-	2.0	%
3V3DL Nominal Voltage Level	$V_{3V3DL}$		-	3.3	-	V
3V3DL Under-voltage Rising Threshold			-	2.450	-	V
3V3DL Under-voltage Hysteresis			-	200	-	mV
3V3DLSB Output Drive Current	$I_{3V3DLSB}$	5VSB = 5V	5.0	8.5	-	mA
DLA Output Impedance			-	90	-	$\Omega$

**Electrical Specifications** Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3 (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>5VDUAL SWITCH CONTROLLER (V<sub>OUT3</sub>)</b>						
5VDL Under-Voltage Rising Threshold			-	3.750	-	V
5VDL Under-Voltage Hysteresis			-	260	-	mV
5VDLSB Output Drive Current	I <sub>5VDLSB</sub>	5VDLSB = 4V	-20	-	-40	mA
5VDLSB Pull-up Impedance to 5VSB			-	350	-	Ω
<b>TIMING INTERVALS</b>						
Active State Assessment Past 12V Threshold		Note 2	40	50	60	ms
Maximum Allowable $\overline{S3}$ to $\overline{S5}$ Skew			-	200	-	μs
5VSB POR Extension Past Threshold Voltage			-	3.3	-	ms
<b>CONTROL I/O (S3, S5, EN3VDL, EN5VDL, FAULT)</b>						
High Level Threshold			-	-	2.2	V
Low Level Threshold			0.8	-	-	V
$\overline{S3}, \overline{S5}$ Internal Pull-up Impedance to 5VSB			-	70	-	kΩ
FAULT Output Impedance		FAULT = high	-	100	-	Ω
FAULT Under-Voltage Reporting Delay			-	10	-	μs
<b>TEMPERATURE MONITOR</b>						
Fault-Level Threshold		Note 3	125	-	-	°C
Shutdown-Level Threshold		Note 3	-	150	-	°C

## NOTES:

- Guaranteed by Correlation.
- Guaranteed by Design.

**Functional Pin Description****5VSB (Pin 1)**

Provide a 5V bias supply for the IC to this pin by connecting it to the ATX 5VSB output. This pin also provides the base bias current for all the external NPN transistors controlled by the IC. The voltage at this pin is monitored for power-on reset (POR) purposes.

**GND (Pin 8)**

Signal ground for the IC. All voltage levels are measured with respect to this pin.

 **$\overline{S3}$  and  $\overline{S5}$  (Pins 6 and 7)**

These pins switch the IC's operating state from active (S0, S1) to S3 and S4/S5 sleep states. Connect  $\overline{S3}$  to SLP\_S3 and  $\overline{S5}$  to SLP\_S5. These are digital inputs featuring internal 70kΩ (typical) resistor pull-ups to 5VSB. Internal circuitry de-glitches the S3 pin for disturbances. Additional circuitry blocks any illegal state transitions (such as S3 to S4/S5 or vice versa). When entering an S4/S5 sleep state, the  $\overline{S3}$  signal is allowed to go low as far as 200μs (typically) ahead of the S5 signal.

**EN3VDL and EN5VDL (Pins 2 and 5)**

These pins control the logic governing the output behavior in response to S3 and S4/S5 requests. These are digital inputs whose status can only be changed during active states operation or during chip shutdown (SS pin grounded by external open-drain device). The input information is latched-in when entering a sleep state, as well as following 5VSB POR release or exit from shutdown.

**FAULT/MSEL (Pin 9)**

This is a multiplexed function pin allowing the setting of the memory output voltage to either 2.5V or 3.3V (for RDRAM or SDRAM memory systems). The memory voltage setting is latched-in 3ms (typically) after 5VSB POR release. In case of an under-voltage on any of the outputs or an over-temperature event, this pin is used to report the fault condition by being pulled to 5VSB.

**SS (Pin 13)**

Connect a small ceramic capacitor (allowable range: 5nF-0.22μF; 0.1μF recommended) from this pin to GND. The internal Soft-Start (SS) current source along with the external capacitor creates a voltage ramp used to control the ramp-up of the output voltages. Pulling this pin low with an open-drain device shuts down all the outputs as well as

forces the FAULT pin low. The  $C_{SS}$  capacitor is also used to provide a controlled voltage slew rate during active-to-sleep transitions on the  $3.3V_{DUAL}$  and  $2.5/3.3V_{MEM}$  outputs.

### 12V (Pin 14)

Connect this pin to the ATX (or equivalent) 12V output. This pin is used to monitor the status of the power supply as well as provide bias for the NMOS-compatible output drivers.

12V presence at the chip in the absence of bias voltage, or severe 12V brownout during active states (S0, S1) operation can lead to chip misbehavior.

### VSEN2 (Pin 16)

Connect this pin to the memory output ( $V_{OUT2}$ ). In sleep states, this pin is regulated to 2.5V or 3.3V (based on  $R_{SEL}$ ) through an internal pass transistor capable of delivering 300mA (typically). When  $V_{OUT2}$  is programmed to 2.5V, the active-state voltage at this pin is regulated through an external NPN transistor connected at the DRV2 pin. For the 3.3V setting, the ATX 3.3V is passed to this pin through a fully on N-MOS transistor. During all operating states, the voltage at this pin is monitored for under-voltage events.

### DRV2 (Pin 15)

For the 2.5V RDRAM systems, connect this pin to the base of a suitable NPN transistor. This pass transistor regulates the 2.5V output from the ATX 3.3V during active states operation. For 3.3V SDRAM systems connect this pin to the gate of a suitable N-MOS transistor; this transistor is used to switch in the ATX 3.3V output.

### 3V3DL (Pin 4)

Connect this pin to the 3.3V dual output ( $V_{OUT1}$ ). In sleep states, the voltage at this pin is regulated to 3.3V; in active states, ATX 3.3V output is delivered to this node through a fully on N-MOS transistor. During all operating states, this pin is monitored for under-voltage events.

### 3V3DLSB (Pin 3)

Connect this pin to the base of a suitable NPN transistor. In sleep states, this transistor is used to regulate the voltage at the 3V3DL pin to 3.3V.

### DLA (Pin 10)

Connect this pin to the gates of suitable N-MOSFETs, which in active states, are used to switch in the ATX 3.3V and 5V outputs into the  $3.3V_{DUAL}$  and  $5V_{DUAL}$  outputs, respectively.

### 5VDL (Pin 12)

Connect this pin to the  $5V_{DUAL}$  output ( $V_{OUT3}$ ). In either operating state, the voltage at this pin is provided through a fully on MOS transistor. This pin is also monitored for under-voltage events.

### 5VDLSB (Pin 11)

Connect this pin to the gate of a suitable P-MOSFET or bipolar PNP. In sleep states, this transistor is switched on, connecting the ATX 5VSB output to the  $5V_{DUAL}$  regulator output.

## Description

### Operation

The HIP6501A controls 3 output voltages (Refer to Figures 1, 2, and 3). It is designed for microprocessor computer applications with 3.3V, 5V, 5VSB, and 12V outputs from an ATX power supply. The IC is composed of two linear controllers supplying the PCI slots'  $3.3V_{AUX}$  power ( $3.3V_{DUAL}$ ,  $V_{OUT1}$ ) and the 2.5V RDRAM or 3.3V SDRAM memory power ( $2.5/3.3V_{MEM}$ ,  $V_{OUT2}$ ), and a dual switch controller supplying the  $5V_{DUAL}$  voltage ( $V_{OUT3}$ ). In addition, all the control and monitoring functions necessary for complete ACPI implementation are integrated into the HIP6501A.

### Initialization

The HIP6501A automatically initializes upon receipt of input power. The Power-On Reset (POR) function continually monitors the 5VSB input supply voltage, initiating soft-start operation after it exceeds its POR threshold (in either S3 or S4/S5 states). To ensure stabilization of the 5VSB supply before operation is allowed, POR is released 3.3ms (typically) after 5VSB exceeds the POR threshold. The 5VSB POR trip event is also used to lock in the memory voltage setting based on  $R_{SEL}$ .

### Operational Truth Tables

The  $\overline{EN3VDL}$  and  $\overline{EN5VDL}$  pins offer a host of choices in terms of the overall system architecture and supported features. Tables 1-3 describe the truth combinations pertaining to each of the three outputs.

TABLE 1.  $3.3V_{DUAL}$  OUTPUT ( $V_{OUT1}$ ) TRUTH TABLE

$\overline{EN3VDL}$	$\overline{S5}$	$\overline{S3}$	3V3DL	COMMENTS
0	1	1	3.3V	S0, S1 STATES (Active)
0	1	0	3.3V	S3
0	0	1	Note 4	Maintains Previous State
0	0	0	3.3V	S4/S5
1	1	1	3.3V	S0, S1 STATES (Active)
1	1	0	3.3V	S3
1	0	1	Note 4	Maintains Previous State
1	0	0	0V	S4/S5

NOTE:

4. Combination not allowed.

As seen in Table 1,  $\overline{EN3VDL}$  simply controls whether the  $3.3V_{DUAL}$  plane remains powered up during S4/S5 sleep state.

**TABLE 2. 5V<sub>DUAL</sub> OUTPUT (V<sub>OUT3</sub>) TRUTH TABLE**

EN5VDL	$\overline{S5}$	$\overline{S3}$	5VDL	COMMENTS
0	1	1	5V	S0, S1 STATES (Active)
0	1	0	0V	S3
0	0	1	Note 5	Maintains Previous State
0	0	0	0V	S4/S5
1	1	1	5V	S0, S1 STATES (Active)
1	1	0	5V	S3
1	0	1	Note 5	Maintains Previous State
1	0	0	5V	S4/S5

NOTE:

5. Combination not allowed.

Very similarly, Table 2 details the fact that EN5VDL status controls whether the 5V<sub>DUAL</sub> plane supports sleep states.

**TABLE 3. 2.5/3.3V<sub>MEM</sub> OUTPUT (V<sub>OUT2</sub>) TRUTH TABLE**

RSEL	$\overline{S5}$	$\overline{S3}$	2.5/3.3V <sub>MEM</sub>	COMMENTS
1kΩ	1	1	2.5V	S0, S1 STATES (Active)
1kΩ	1	0	2.5V	S3
1kΩ	0	1	Note 6	Maintains Previous State
1kΩ	0	0	0V	S4/S5
10kΩ	1	1	3.3V	S0, S1 STATES (Active)
10kΩ	1	0	3.3V	S3
10kΩ	0	1	Note 6	Maintains Previous State
10kΩ	0	0	0V	S4/S5

NOTE:

6. Combination not allowed.

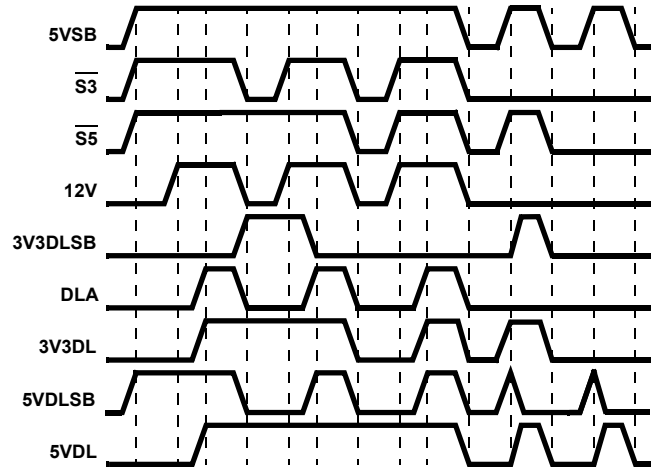
As seen in Table 3, 2.5/3.3V<sub>MEM</sub> output is maintained in S3 (Suspend-To-RAM), but not in S4/S5 state. The dual-voltage support accommodates both SDRAM as well as RDRAM type memories.

Additionally, the internal circuitry does not allow the transition from an S3 (suspend to RAM) state to an S4/S5 (suspend to disk/soft off) state or vice versa. The only 'legal' transitions are from an active state (S0, S1) to a sleep state (S3, S4/S5) and vice versa.

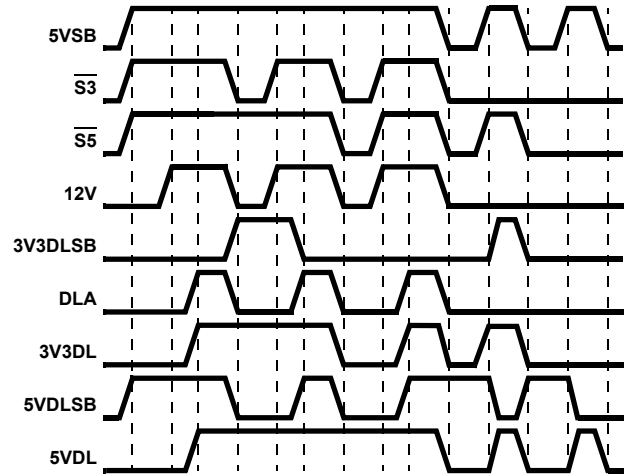
**Functional Timing Diagrams**

Figures 4-8 are timing diagrams, detailing the power up/down sequences of all three outputs in response to the status of the enable (EN3VDL, EN5VDL) and sleep-state pins ( $\overline{S3}$ ,  $\overline{S5}$ ), as well as the status of the ATX supply.

The status of the  $\overline{EN3VDL}$  and EN5VDL pins can only be changed while in active (S0, S1) states, when the bias supply (5VSB pin) is below POR level, or during chip shutdown (SS pin shorted to GND); a status change of these two pins while in a sleep state is ignored.



**FIGURE 4. 3V<sub>DUAL</sub> AND 5V<sub>DUAL</sub> TIMING DIAGRAM FOR EN3VDL = 1, EN5VDL = 1**



**FIGURE 5. 3V<sub>DUAL</sub> AND 5V<sub>DUAL</sub> TIMING DIAGRAM FOR EN3VDL = 1, EN5VDL = 0**

Not shown in these diagrams is the de-glitching feature used to protect against false sleep state tripping. Once the status of the  $\overline{S3}$  pin changes, an internal timer is activated. If at the end of the timeout period (typically 200μs) the input pins present a valid state change request, then the controller transitions to the new configuration. Otherwise, the previously attained valid state is maintained until valid control signals are received from the system. This particular feature is useful in noisy computer environments if the control signals have to travel over significant distances.

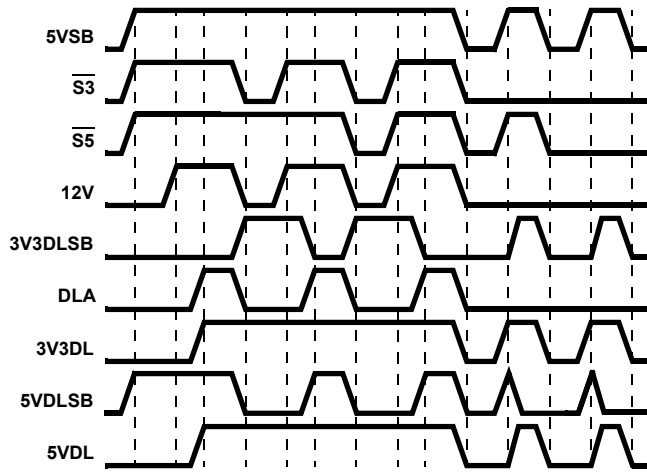


FIGURE 6. 3VDUAL AND 5VDUAL TIMING DIAGRAM FOR EN3VDL = 0, EN5VDL = 1

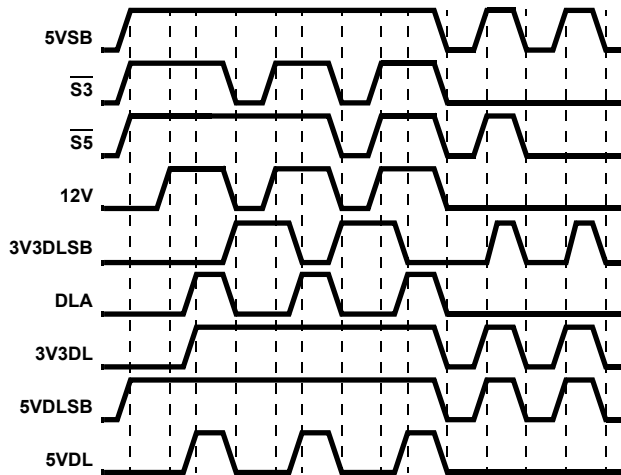


FIGURE 7. 3VDUAL AND 5VDUAL TIMING DIAGRAM FOR EN3VDL = 0, EN5VDL = 0

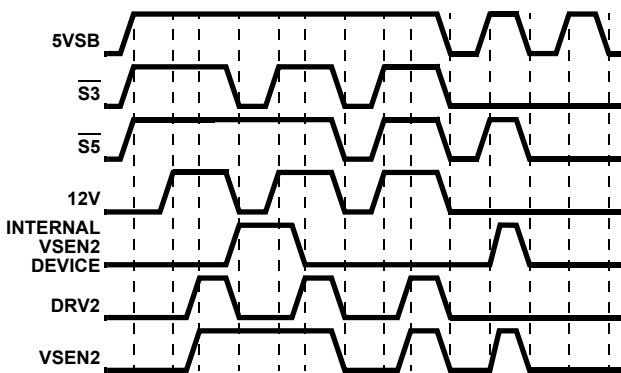


FIGURE 8. 2.5V/3.3VMEM TIMING DIAGRAM

## Soft-Start Circuit

### Soft-Start into Sleep States (S3, S4/S5)

The 5VSB POR function initiates the soft-start sequence. An internal 10µA current source charges an external capacitor to 5V. The error amplifiers reference inputs are clamped to a level proportional to the SS (Soft-Start) pin voltage. As the SS pin voltage slews from about 1.25V to 2.5V, the input clamp allows a rapid and controlled output voltage rise.

Figure 9 shows the soft-start sequence for the typical application start-up in a sleep state with all output voltages enabled. At time T0 5V<sub>SB</sub> (bias) is applied to the circuit. At time T1, 5V<sub>SB</sub> surpasses POR level, and an internal fast charge circuit quickly raises the SS capacitor voltage to approximately 1V. At this point, the 10µA current source continues the charging up to T2, where a voltage of 1.25V (typically) is reached and an internal clamp limits further charging. Clamping of the soft-start voltage (T2 to T3 interval) should only be noticed with capacitors smaller than 0.1µF; soft-start capacitors of 0.1µF and above should present a soft-start ramp void of this plateau. At time T3, 3ms (typically) past the 5V<sub>SB</sub> POR (T1), the memory output voltage selection is latched in and the charging of the soft-start capacitor resumes, using the 10µA current source. At this point, the error amplifiers' reference inputs are starting their transitions, causing the output voltages to ramp up proportionally. The ramping continues until time T4 when all the voltages reach the set value. At time T5, when the soft-start capacitor value reaches approximately 2.8V, the under-voltage monitoring circuits are activated and the soft-start capacitor is quickly discharged down to the value attained at time T2 (approximately 1.25V).

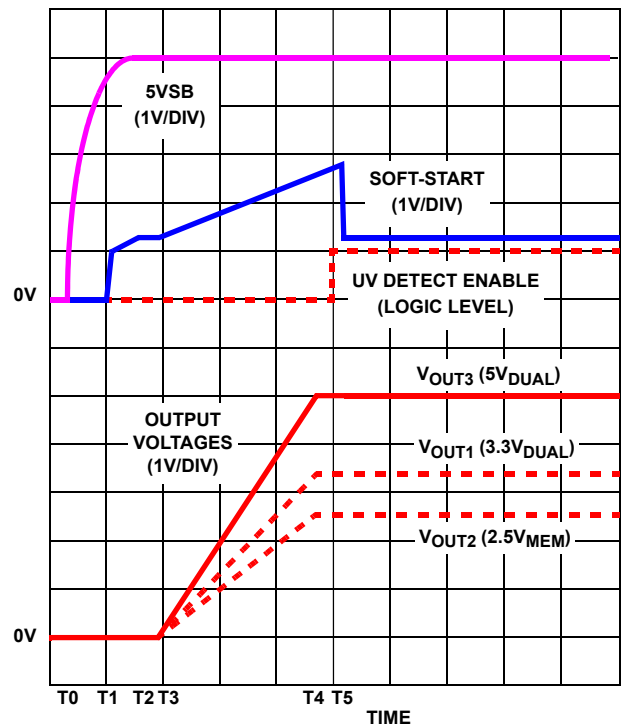


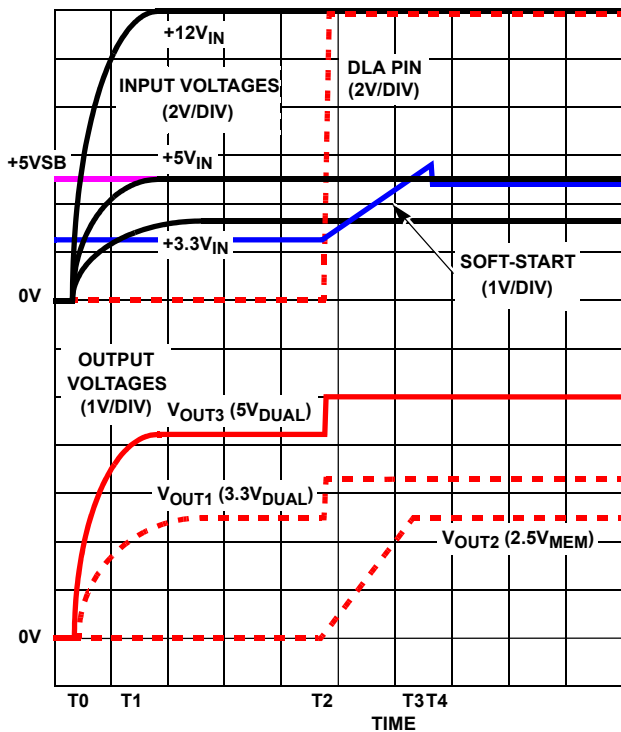
FIGURE 9. SOFT-START INTERVAL IN A SLEEP STATE (ALL OUTPUTS ENABLED)



**Soft-Start into Active States (S0, S1)**

If both  $\overline{S3}$  and  $\overline{S5}$  are logic high at the time the 5VSB is applied, the HIP6501A will assume an active state and keep off the controlled external transistors until about 50ms after the ATX's 12V output (sensed at the 12V pin) exceeds the set threshold (typically 10.8V). This timeout feature is necessary in order to ensure the main ATX outputs are stabilized. The timeout also assures smooth transitions from sleep into active when sleep states are being supported.

During sleep to active state transitions from conditions where the outputs are initially 0V (such as S4/S5 to S0 transition with  $\overline{EN3VDL} = 1$  and  $\overline{EN5VDL} = 0$ , or simple power-up sequence directly into active state), the 3V<sub>DUAL</sub> and 5V<sub>DUAL</sub> outputs go through a quasi soft-start by being pulled high through the body diodes of the N-channel MOSFETs connected between these outputs and the 3.3V and 5V ATX outputs, respectively. Figure 10 shows this start-up scenario.



**FIGURE 10. SOFT-START INTERVAL IN AN ACTIVE STATE**

5V<sub>SB</sub> is already present when the main ATX outputs are turned on at time T0. Similarly, the soft-start capacitor has already been charged up to 1.25V and the clamp is active, awaiting for the 12V POR timer to expire. As a result of 3.3V<sub>IN</sub> and 5V<sub>IN</sub> ramping up, the 3.3V<sub>DUAL</sub> and 5V<sub>DUAL</sub> output capacitors charge up through the body diodes of Q3 and Q5, respectively (see Figure 3). At time T1, the 12V ATX output exceeds the HIP6501A's 12V under-voltage threshold, and the internal 50ms (typical) timer is initiated. At T2 the time-out initiates a soft-start, and the memory output is ramped-up, reaching regulation limits at time T3.

Simultaneous with the memory voltage ramp-up, the DLA pin is pulled high (to 12V), turning on Q3 and Q5, and bringing the 3.3V<sub>DUAL</sub> and 5V<sub>DUAL</sub> outputs in regulation at time T2. At time T4, when the soft-start voltage reaches approximately 2.8V, the under-voltage monitoring circuits are enabled and the soft-start capacitor is quickly discharged to approximately 2.45V.

Requests to go into a sleep state during an active state soft-start ramp-up result in a chip reset, followed by a new soft-start sequence into the desired state.

**Fault Protection**

All the outputs are monitored against under-voltage events. A severe over-current caused by a failed load on any of the outputs, would, in turn, cause that specific output to suddenly drop. If any of the output voltages drop below 69% of their set value, such event is reported by having the FAULT/MSEL pin pulled to 5V. Additionally, the 2.5/3.3V memory regulator is internally current limited while in a sleep state. Exceeding the maximum current rating of this output in a sleep state can lead to output voltage drooping. If excessive, this droop can ultimately trip the under-voltage detector and send a FAULT signal to the computer system. However, a FAULT condition will only set off the FAULT flag, and it will not shut off or latch off any part of the circuit. If shutdown or latch off of the circuit is desired, this can be achieved by externally pulling or latching the SS pin low. Pulling the SS pin low will also force the FAULT pin to go low.

Under-voltage sensing is disabled on all disabled outputs and during soft-start ramp-up intervals. SS voltage reaching the 2.8V threshold signals activation of the under-voltage monitor.

Another condition that could set off the FAULT flag is chip over-temperature. If the HIP6501A reaches an internal temperature of 125°C (minimum), the FAULT flag is set (FAULT/MSEL pulled high), but the chip continues to operate until the temperature reaches 150°C (typical), when unconditional latched shutdown of all outputs takes place. The thermal latch can be reset only by cycling the 5V<sub>SB</sub> off, and then on.

**Output Voltages**

The output voltages are internally set and do not require any external components. Selection of the memory voltage is done by means of an external resistor connected between the FAULT/MSEL pin and ground. An internal 40µA (typical) current source creates a voltage drop across this resistor. During every 5V<sub>SB</sub> trip above POR level, this voltage is compared with an internal reference (200mV typically). Based on this comparison, the output voltage is set at either 2.5V (R<sub>SEL</sub> = 1kΩ), or 3.3V (R<sub>SEL</sub> = 10kΩ). It is very important that no capacitor is connected to the FAULT/MSEL pin; the presence of a capacitive element at this pin can lead to false memory voltage selection. See Figure 11 for details.

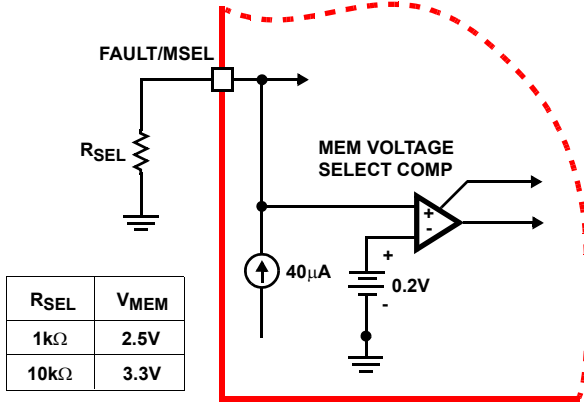


FIGURE 11. 2.5/3.3V<sub>MEM</sub> OUTPUT VOLTAGE SELECTION CIRCUITRY DETAILS

**Application Guidelines**

**Soft-Start Interval**

The 5VSB output of a typical ATX supply is capable of 725mA. During power-up in a sleep state, it needs to provide sufficient current to charge up all the output capacitors and simultaneously provide some amount of current to the output loads. Drawing excessive amounts of current from the 5VSB output of the ATX can lead to voltage collapse and induce a pattern of consecutive restarts with unknown effects on the system's behavior or health.

The built-in soft-start circuitry allows tight control of the slew-up speed of the output voltages controlled by the HIP6501A, thus enabling power-ups free of supply drop-off events. Since the outputs are ramped up in a linear fashion, the current dedicated to charging the output capacitors can be calculated with the following formula:

$$I_{COUT} = \frac{I_{SS}}{C_{SS} \times V_{BG}} \times \sum(C_{OUT} \times V_{OUT}), \text{ where}$$

I<sub>SS</sub> - soft-start current (typically 10µA)

C<sub>SS</sub> - soft-start capacitor

V<sub>BG</sub> - bandgap voltage (typically 1.26V)

∑(C<sub>OUT</sub> × V<sub>OUT</sub>) - sum of the products between the capacitance and the voltage of an output.

Due to the various system timing events, it is recommended that the soft-start interval not be set to exceed 30ms. Additionally, the recommended soft-start capacitor range spans from 5nF up to 0.22µF (0.1µF recommended).

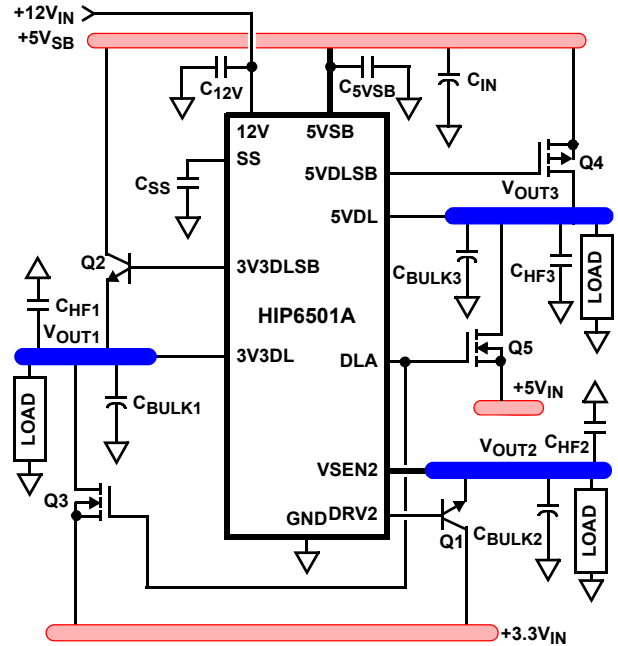
**Shutdown**

In case of a FAULT condition that might endanger the computer system, or at any other time, the HIP6501A can be shut down by pulling the SS pin below the specified shutdown level (typically 0.8V) with an open drain or open collector device capable of sinking a minimum of 2mA. Pulling the SS pin low effectively shuts down all the pass elements. Upon release of the SS pin, the HIP6501A

undergoes a new soft-start cycle and resumes normal operation in accordance to the ATX supply and control pins status.

**Layout Considerations**

The typical application employing a HIP6501A is a fairly straight-forward implementation. Similar to any other linear regulators, attention has to be paid to a few potentially sensitive small signal components, such as those connected to high-impedance nodes or those supplying critical by-pass currents.



- KEY
- ISLAND ON POWER PLANE LAYER
- ISLAND ON CIRCUIT/POWER PLANE LAYER
- VIA CONNECTION TO GROUND PLANE

FIGURE 12. PRINTED CIRCUIT BOARD ISLANDS

The power components (pass transistors) and the controller IC should be placed first. The controller should be placed in a central position on the motherboard, closer to the memory load if possible. Ensure the VSEN2 connection is properly sized to carry 200mA without significant resistive losses. The pass transistors should be placed on pads capable of heatsinking, matching the device's power dissipation. Where applicable, multiple via connections to a large internal plane can significantly lower localized device temperature rise.

Placement of the decoupling and bulk capacitors should follow a placement reflecting their purpose. As such, the high-frequency decoupling capacitors (C<sub>H<sub>F</sub></sub>) should be placed as close as possible to the load they are decoupling; the ones decoupling the controller (C<sub>12V</sub>, C<sub>5VSB</sub>) close to the controller pins, the ones decoupling the load close to the load connector or the load itself (if embedded). The bulk

capacitance (aluminum electrolytics or tantalum capacitors) placement is not as critical as the high-frequency capacitor placement, but having these capacitors close to the load they serve is preferable.

The only critical small signal component is the soft-start capacitor,  $C_{SS}$ . Locate this component close to SS pin of the control IC and connect to ground through a via placed close to the capacitor's ground pad. Minimize any leakage current paths from SS node, since the internal current source is only 10 $\mu$ A.

A multi-layer printed circuit board is recommended. Figure 12 shows the connections of most of the components in the converter. Note that the individual capacitors each could represent numerous physical capacitors. Dedicate one solid layer for a ground plane and make all critical component ground connections through vias placed as close to the component as possible. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Ideally, the power plane should support both the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers to create power islands connecting the filtering components (output capacitors) and the loads. Use the remaining printed circuit layers for small signal wiring.

## Component Selection Guidelines

### Output Capacitors Selection

The output capacitors for all outputs should be selected to allow the output voltage to meet the dynamic regulation requirements of active state operation (S0, S1). The load transient for the various microprocessor system's components may require high quality capacitors to supply the high slew rate (di/dt) current demands. Thus, it is recommended that capacitors  $C_{OUT1}$  and  $C_{OUT2}$  should be selected for transient load regulation.

Also, during the transition between active and sleep states, there is a short interval of time during which none of the power pass elements are conducting - during this time the output capacitors have to supply all the output current. The output voltage drop during this brief period of time can be approximated with the following formula:

$$\Delta V_{OUT} = I_{OUT} \times \left( ESR_{OUT} + \frac{t_t}{C_{OUT}} \right), \text{ where}$$

$\Delta V_{OUT}$  - output voltage drop

$ESR_{OUT}$  - output capacitor bank ESR

$I_{OUT}$  - output current during transition

$C_{OUT}$  - output capacitor bank capacitance

$t_t$  - active-to-sleep or sleep-to-active transition time (10 $\mu$ s typical)

Since the output voltage drop is heavily dependent on the ESR (equivalent series resistance) of the output capacitor bank, the capacitors should be chosen to maintain the output voltage above the lowest allowable regulation level.

### Input Capacitors Selection

The input capacitors for an HIP6501A application must have sufficiently low ESR so that the input voltage does not dip excessively when energy is transferred to the output capacitors. If the ATX supply does not meet the specifications, certain imbalances between the ATX's outputs and the HIP6501A's regulation levels could result in a brisk transfer of energy from the input capacitors to the supplied outputs. When transiting from active to sleep states, this phenomena could result in the 5VSB voltage dropping below the POR level (typically 4.3V) and temporarily disabling the HIP6501A. The solution to this potential problem is to use larger input capacitors (on 5VSB) with a lower total combined ESR.

### Transistor Selection/Considerations

The HIP6501A typically requires one P-Channel and two N-Channel power MOSFETs and two bipolar NPN transistors.

One general requirement for selection of transistors for all the linear regulators/switching elements is package selection for efficient removal of heat. The power dissipated in a linear regulator/switching element is:

$$P_{LINEAR} = I_O \times (V_{IN} - V_{OUT})$$

Select a package and heatsink that maintains the junction temperature below the rating with the maximum expected ambient temperature.

#### Q1

The active element on the 2.5V/3.3V<sub>MEM</sub> output has different requirements for each of the two voltage settings. In 2.5V systems utilizing RDRAM (or voltage-compatible) memory, Q1 must be a bipolar NPN capable of conducting the maximum required output current and it must have a minimum current gain ( $h_{fe}$ ) of 100-150 at this current and 0.7V  $V_{CE}$ . In such systems, the 2.5V output is regulated from the ATX 3.3V output while in an active state. In 3.3V systems (SDRAM or compatible) Q1 must be an N-Channel MOSFET, since the MOSFET serves as a switch during active states (S0, S1). The main criteria for the selection of this transistor is output voltage budgeting. The maximum  $r_{DS(ON)}$  allowed at highest junction temperature can be expressed with the following equation:

$$r_{DS(ON) MAX} = \frac{V_{IN MIN} - V_{OUT MIN}}{I_{OUT MAX}}, \text{ where}$$

$V_{IN MIN}$  - minimum input voltage

$V_{OUT MIN}$  - minimum output voltage allowed

$I_{OUT MAX}$  - maximum output current

The gate bias available for this MOSFET is approximately 8V.

**Q4**

If a P-Channel MOSFET is used to switch the 5VSB output of the ATX supply into the 5V<sub>DUAL</sub> output during S3 and S4/S5 states (as dictated by EN5VDL status), then, similar to the situation where Q1 is a MOSFET, the selection criteria of this device is also proper voltage budgeting. The maximum  $r_{DS(ON)}$ , however, has to be achieved with only 4.5V of  $V_{GS}$ , so a logic level MOSFET needs to be selected. If a PNP device is chosen to perform this function, it has to have a low saturation voltage while providing the maximum sleep-state current and have a current gain sufficiently high to be saturated using the minimum drive current (typically 20mA; 4mA during soft-start).

**Q3, Q5**

The two N-Channel MOSFETs are used to switch the 3.3V and 5V inputs provided by the ATX supply into the 3.3VDUAL and 5VDUAL outputs, respectively, while in active (S0, S1) states. Similar  $r_{DS(ON)}$  criteria apply in these cases as well, unlike the PMOS, however, these NMOS transistors get the benefit of an increased  $V_{GS}$  drive (approximately 8V and 7V, respectively).

**Q2**

The NPN transistor used as sleep-state pass element on the 3.3VDUAL output must have a minimum current gain of 100 at  $V_{CE} = 1.5V$ , and  $I_{CE} = 500mA$  throughout the in-circuit operating temperature range.

### HIP6501A Application Circuit

Figure 13 shows an application circuit of an ACPI-compliant power management system for a microprocessor computer system. The power supply provides the PCI 3.3V<sub>DUAL</sub> voltage (V<sub>OUT1</sub>), the RDRAM 2.5V<sub>MEM</sub> memory voltage (V<sub>OUT2</sub>), and the 5V<sub>DUAL</sub> voltage (V<sub>OUT3</sub>) from +3.3V, +5V, +5V<sub>SB</sub>, and +12VDC ATX supply outputs. For systems

employing SDRAM memory, replace R1 with 10kΩ and Q1 with an HUF76113SK8. Q4 can also be a PNP, such as an MMBT2907AL. For detailed information on the circuit, including a Bill-of-Materials and circuit board description, see Application Note AN9846.

See Intersil's web site [www.intersil.com](http://www.intersil.com) for the latest information.

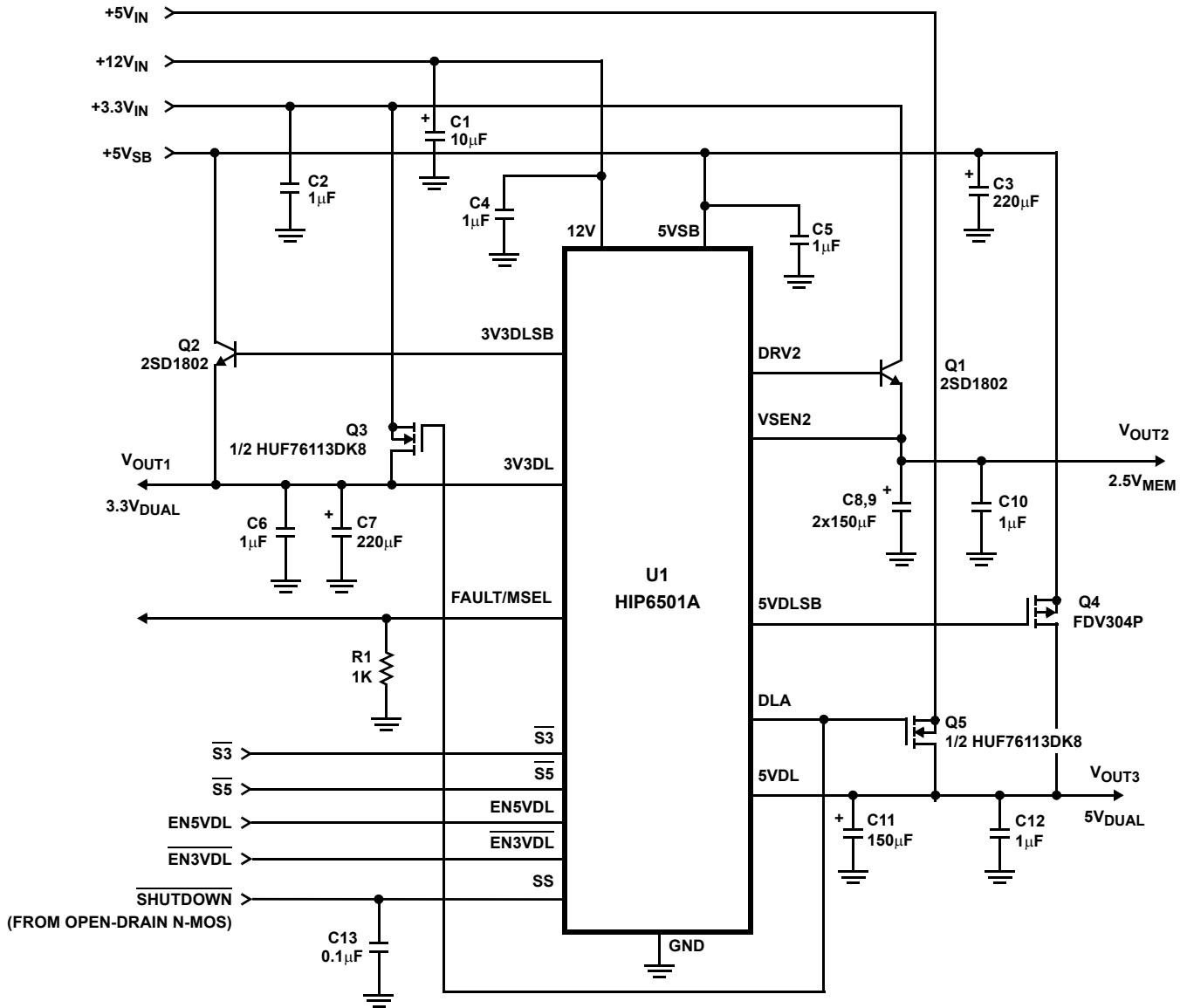
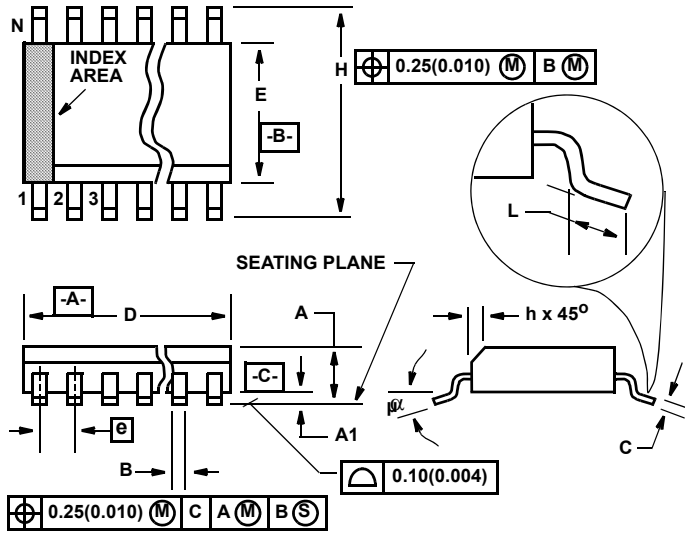


FIGURE 13. TYPICAL HIP6501A APPLICATION CIRCUIT

**Small Outline Plastic Packages (SOIC)**



**M16.15 (JEDEC MS-012-AC ISSUE C)  
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
B	0.014	0.019	0.35	0.49	9
C	0.007	0.010	0.19	0.25	-
D	0.386	0.394	9.80	10.00	3
E	0.150	0.157	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.228	0.244	5.80	6.20	-
h	0.010	0.020	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
$\alpha$	0°	8°	0°	8°	-

Rev. 1 02/02

**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

© Copyright Intersil Americas LLC 2000-2004. All Rights Reserved.  
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see [www.intersil.com/en/products.html](http://www.intersil.com/en/products.html)

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at [www.intersil.com/en/support/qualandreliability.html](http://www.intersil.com/en/support/qualandreliability.html)

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)