HS-303CEH

Radiation Hardened BiCMOS Dual SPDT Analog Switch

The HS-303CEH is an analog switch and a monolithic device that is fabricated using the Renesas dielectrically isolated Radiation Hardened Silicon Gate (RSG) process technology to ensure latch-up free operation. The HS-303CEH is pinout compatible and functionally equivalent to the HS-303RH. The HS-303CEH offers low-resistance switching performance for analog voltages up to the supply rails. ON-resistance is low and stays reasonably constant across the full range of operating voltage and current. ON-resistance also stays reasonably constant when exposed to radiation.
Break-before-make switching is controlled by 5V digital inputs. The HS-303CEH can operate with ±15V rails.

Specifications

See SMD 5962-95813 for detailed electrical specifications.

Related Literature

For a full list of related documents, visit our website:

- HS-303CH device page

Features

- QML, per MIL-PRF-38535
- No latch-up, dielectrically isolated device islands
- Pinout and functionally compatible with the HS-303RH series of analog switches
- Analog signal range equal to the supply voltage range
- Low leakage: 150nA (max, post-rad)
- Low r_{ON}: 60Ω (max, post-rad)
- Low standby supply current: ±150µA (max, post-rad)
- Radiation assurance
  - High dose rate (50 to 300rad(Si)/s): 100krad(Si)
  - Low dose rate (0.01rad(Si)/s): 50krad(Si) (Note 1)
- Single event effects
  - For LET = 60MeV·cm^2/mg at 60° incident angle, <150pC charge transferred to the output of an off switch (based on SOI design calculations)

Note:
1. Product capability established by initial characterization. The EH version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate.

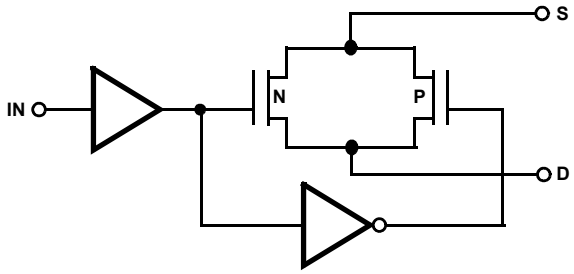


Figure 1. Logic Circuit

Table 1. Truth Table

Logic	SW1 and SW2	SW3 and SW4
0	OFF	ON
1	ON	OFF

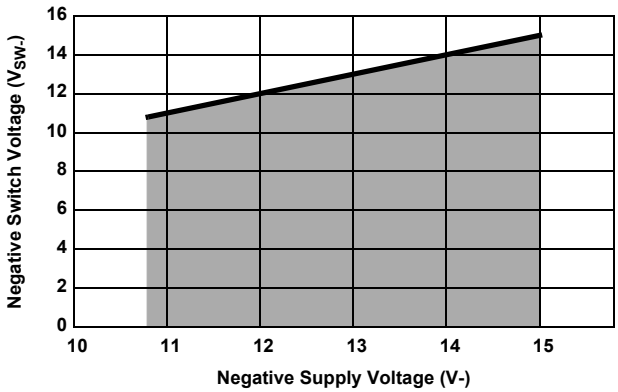
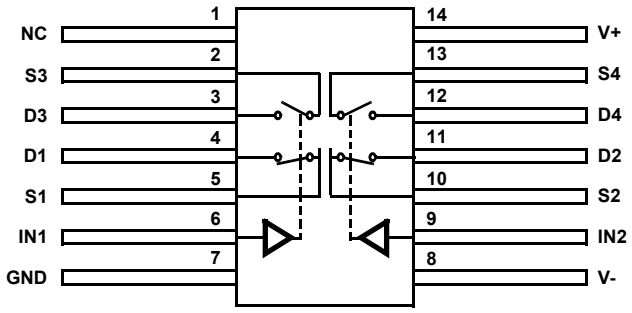


Figure 2. Recommended Operating Area in Grey

1. Overview

1.1 Pin Configuration

14 Ld Flatpack
Top View



1.2 Pin Descriptions

Pin Number	Pin Name	Pin Description
1	NC	Not electrically connected
2	S3	Analog switch: source connection
3	D3	Analog switch: drain connection
4	D1	Analog switch: drain connection
5	S1	Analog switch: source connection
6	IN1	Digital control input for SW1 and SW3
7	GND	Ground
8	V-	Negative power supply
9	IN2	Digital control input for SW2 and SW4
10	S2	Analog switch: source connection
11	D2	Analog switch: drain connection
12	D4	Analog switch: drain connection
13	S4	Analog switch: source connection
14	V+	Positive power supply

1.3 Ordering Information

Ordering SMD Number (Note 3)	Part Number (Note 2)	Temp. Range (°C)	Package (RoHS Compliant)	Pkg. Dwg. #
5962R9581308VXC	HS9-303CEH-Q	-55 to +125	14 Ld Flatpack	K14.A
5962R9581308V9A	HS0-303CEH-Q	-55 to +125	Die	N/A
N/A	HS9-303CEH/PROTO (Note 4)	-55 to +125	14 Ld Flatpack	K14.A
N/A	HS0-303CEH/SAMPLE (Note 4)	-55 to +125	Die	N/A

Notes:

2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in this table must be used when ordering.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening across the temperature range to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because there is no radiation assurance testing and they are not DLA qualified devices.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Voltage Between V+ and V- Terminals		35	V
$\pm V_{SUPPLY}$ to Ground (V+, V-)		±17.5	V
Analog Input Voltage			
$(+V_S)$		$+V_{SUPPLY}$ + 1.5	V
$(-V_S)$		$-V_{SUPPLY}$ - 1.5	V
Digital Input Voltage			
$(+V_A)$		$+V_{SUPPLY}$ + 4	V
$(-V_A)$		$-V_{SUPPLY}$ - 4	V
Peak Current (S or D), (Pulse at 1ms, 10% Duty Cycle Max)		40	mA
Continuous Current		10	mA
ESD Rating	**Value**		**Unit**
Human Body Model	2		kV
Machine Model	200		V
Charged Device Model	1		kV

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Flatpack Package (Notes 5, 6)	105	17

Notes:

5. θ_{JA} is measured in free air with the component mounted on a low-effective thermal conductivity test board in free air. See TB379.
6. For θ_{JC}, the “case temp” location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Package Power Dissipation at 125°C for Flatpack Package		0.48	W/°C
Junction Temperature (T_J)		+175	°C
Storage Temperature Range	-65	+150	°C
Lead Temperature (Soldering, 10s)		+300	°C

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Operating Temperature Range	-55	+125	°C
Operating Supply Voltage Range ($\pm V_{SUPPLY}$)		±15	V
Analog Input Voltage (V_S)		$\pm V_{SUPPLY}$	V
Logic Low Level (V_{AL})	0	0.8	V
Logic High Level (V_{AH})	4.0	$+V_{SUPPLY}$	V

2.4 Electrical Specifications

V_{SUPPLY} = ±15V unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ	Max (Note 9)	Unit
"Switch On" Resistance	$+r_{DS(ON)}$	V_D = 10V, I_S = -10mA		35	**75**	Ω
"Switch On" Resistance	$-r_{DS(ON)}$	V_D = -10V, I_S = 10mA		35	**75**	Ω
Leakage Current into Source of an "OFF" Switch	$+I_{S(OFF)}$	V_S = +14V, V_D = -14V	**-150**	0.05	**150**	nA
		V_S = +15V, V_D = -15V	**-20**		**20**	µA
Leakage Current into Source of an "OFF" Switch	$-I_{S(OFF)}$	V_S = -14V, V_D = +14V	**-150**	0.5	**150**	nA
		V_S = -15V, V_D = +15V	**-20**		**20**	µA
Leakage Current into Drain of an "OFF" Switch	$+I_{D(OFF)}$	V_S = +14V, V_D = -14V	**-150**	0.05	**150**	nA
		V_S = +15V, V_D = -15V	**-20**		**20**	µA
Leakage Current into Drain of an "OFF" Switch	$-I_{D(OFF)}$	V_S = -14V, V_D = +14V	**-150**	0.5	**150**	nA
		V_S = -15V, V_D = +15V	**-20**		**20**	µA
Leakage Current from an "ON" Driver into the Switch (Drain and Source)	$+I_{D(ON)}$	V_S = +14V, V_D = +14V	**-100**	-0.1	**100**	nA
Leakage Current from an "ON" Driver into the Switch (Drain and Source)	$-I_{D(ON)}$	V_S = -14V, V_D = -14V	**-100**	0.01	**100**	nA
Low Level Input Address Current	I_{AL}	All Channels V_A = 0.8V	**-1000**	0.03	**1000**	nA
High Level Input Address Current	I_{AH}	All Channels V_A = 4.0V	**-1000**	0.03	**1000**	nA
Positive Supply Current	I+	All Channels V_A = 0.8V		45	**150**	µA
		V_{A1} = 0V, V_{A2} = 4V V_{A1} = 4V, V_{A2} = 0V		0.15	**0.6**	mA
Negative Supply Current	I-	All Channels V_A = 0.8V		-0.1	**-100**	µA
		V_{A1} = 0V, V_{A2} = 4V V_{A1} = 4V, V_{A2} = 0V		-0.1	**-100**	µA
Switch Input Capacitance	CIS(OFF)	From Source to GND (Notes 7, 8)			**28**	pF
Driver Input Capacitance	CC1	V_A = 0V (Notes 7, 8)			**10**	pF
Driver Input Capacitance	CC2	V_A = 15V (Notes 7, 8)			**10**	pF
Switch Output	COS	Measured Drain to GND (Notes 7, 8)			**28**	pF
Off Isolation	V_{ISO}	V_{GEN} = $1V_{p-p}$, f = 1MHz (Notes 7, 8)	**40**			dB
Cross Talk	V_{CR}	V_{GEN} = $1V_{p-p}$, f = 1MHz (Notes 7, 8)	**40**			dB
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 0.01µF (Notes 7, 8)			**15**	mV
Break-before-make Time Delay	t_{OPEN}	R_L = 300Ω, V_S = 3V, V_{AH} = 5V, V_{AL} = 0V	**10**	50	**300**	ns
Switch Turn "ON" Time	t_{ON}	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V		250	**500**	ns
Switch Turn "OFF" Time	t_{OFF}	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V		200	**450**	ns

Notes:

7. Limits established by characterization and are not production tested.
8. V_{AL} = 0V and V_{AH} = 4V.
9. Parameters with Min and/or Max limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

2.5 Post Radiation Characteristics (Test Rate 50rad(Si)/s to 300rad(Si)/s

V_{SUPPLY} = ±15V unless otherwise specified. This data is typical test data post radiation exposure at a rate of 50 to 300rad(Si)/s. This data shows typical parameter shifts due to total ionizing dose (high dose radiation) T_A= +25°C.

Symbol	Parameter	Test Conditions	0k	100k	Unit
$+r_{DS(ON)}$	“Switch On” Resistance	V_D = 10V, I_S = -10mA	34	35	Ω
$-r_{DS(ON)}$	“Switch On” Resistance	V_D = -10V, I_S = 10mA	28	29	Ω
$+I_{S(OFF)}$	Leakage Current into Source of an “OFF” Switch	V_S = +14V, V_D = -14V	-0.20	-0.31	nA
		V_S = +15V, V_D = -15V	-0.003	-0.47	µA
$-I_{S(OFF)}$	Leakage Current into Source of an “OFF” Switch	V_S = -14V, V_D = +14V	0.30	0.84	nA
		V_S = -15V, V_D = +15V	0.001	0.02	µA
$+I_{D(OFF)}$	Leakage Current into Drain of an “OFF” Switch	V_S = +14V, V_D = -14V	-1.20	-0.90	nA
		V_S = +15V, V_D = -15V	-0.001	-0.001	µA
$-I_{D(OFF)}$	Leakage Current into Drain of an “OFF” Switch	V_S = -14V, V_D = +14V	0.31	0.90	nA
		V_S = -15V, V_D = +15V	0.0003	0.001	µA
$+I_{D(ON)}$	Leakage Current from an “ON” Driver into the Switch (Drain and Source)	V_S = +14V, V_D = +14V	-0.2	-0.55	nA
$-I_{D(ON)}$	Leakage Current from an “ON” Driver into the Switch (Drain and Source)	V_S = -14V, V_D = -14V	0.15	0.28	nA
I_{AL}	Low Level Input Address Current	All channels V_A = 0.8V	0.35	0.25	nA
I_{AH}	High Level Input Address Current	All channels V_A = 4.0V	1.98	1.47	nA
I+	Positive Supply Current	All channels V_A = 0.8V	55	53	µA
		V_{A1} = 0V, V_{A2} = 4V V_{A1} = 4V, V_{A2} = 0V	167.2	113.7	µA
I-	Negative Supply Current	All channels V_A = 0.8V	-0.01	-0.01	µA
		V_{A1} = 0V, V_{A2} = 4V V_{A1} = 4V, V_{A2} = 0V	-0.01	-0.02	µA
t_{OPEN}	Break-before-make Time Delay	R_L = 300Ω, V_S = 3V, V_{AH} = 5V, V_{AL} = 0V	42	47	ns
t_{ON}	Switch Turn “ON” Time	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V	224	213	ns
t_{OFF}	Switch Turn “OFF” Time	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V	192	173	ns

2.6 Post Radiation Characteristics (Test Rate <10mrad(Si)/s

V_{SUPPLY} = ±15V unless otherwise specified. This data is typical test data post radiation exposure at a rate of <10mrad(Si)/s. This data shows typical parameter shifts due to total ionizing dose (low dose radiation). T_A= +25°C.

Parameter	Symbol	Test Conditions	0k	25k	50k	75k	100k	Unit
“Switch On” Resistance	$+r_{DS(ON)}$	V_D = 10V, I_S = -10mA	33.57	34.39	34.37	34.75	34.65	Ω
“Switch On” Resistance	$-r_{DS(ON)}$	V_D = -10V, I_S = 10mA	27.56	28.37	28.48	28.92	28.77	Ω
Leakage Current into Source of an “OFF” Switch	$+I_{S(OFF)}$	V_S = +14V, V_D = -14V	-0.30	-0.26	-0.36	-0.55	-0.47	nA
		V_S = +15V, V_D = -15V	-0.006	-0.002	-0.002	-0.003	-0.002	µA
Leakage Current into Source of an “OFF” Switch	$-I_{S(OFF)}$	V_S = -14V, V_D = +14V	0.32	0.45	0.75	1.05	0.94	nA
		V_S = -15V, V_D = +15V	0.004	0.003	0.003	0.003	0.002	µA
Leakage Current into Drain of an “OFF” Switch	$+I_{D(OFF)}$	V_S = +14V, V_D = -14V	-0.36	-0.22	-0.25	-0.46	-0.40	nA
		V_S = +15V, V_D = -15V	-0.001	-0.001	-0.001	-0.001	-0.002	µA
Leakage Current into Drain of an “OFF” Switch	$-I_{D(OFF)}$	V_S = -14V, V_D = +14V	0.34	0.43	0.69	1.02	0.92	nA
		V_S = -15V, V_D = +15V	0.0004	0.0008	0.0011	0.0014	0.0018	µA

V_{SUPPLY} = ±15V unless otherwise specified. This data is typical test data post radiation exposure at a rate of <10mrad(Si)/s. This data shows typical parameter shifts due to total ionizing dose (low dose radiation). T_A= +25°C. **(Continued)**

Parameter	Symbol	Test Conditions	0k	25k	50k	75k	100k	Unit
Leakage Current from an “ON” Driver into the Switch (Drain and Source)	$+I_{D(ON)}$	V_S = +14V, V_D = +14V	-0.25	-0.26	-0.36	-0.55	-0.65	nA
Leakage Current from an “ON” Driver into the Switch (Drain and Source)	$-I_{D(ON)}$	V_S = -14V, V_D = -14V	0.17	0.15	0.26	0.45	0.40	nA
Low Level Input Address Current	I_{AL}	All channels V_A = 0.8V	0.19	0.30	0.23	0.71	0.48	nA
High Level Input Address Current	I_{AH}	All channels V_A = 4.0V	1.72	0.87	0.83	0.28	1.31	nA
Positive Supply Current	I+	All channels V_A = 0.8V	54	51	50	49	50	µA
		V_{A1} = 0V, V_{A2} = 4V V_{A1} = 4V, V_{A2} = 0V	185	146	129	116	106	µA
Negative Supply Current	I-	All channels V_A = 0.8V	-0.011	-0.015	-0.011	-0.019	-0.022	µA
		V_{A1} = 0V, V_{A2} = 4V V_{A1} = 4V, V_{A2} = 0V	-0.013	-0.016	-0.017	-0.019	-0.014	µA
Break-before-make Time Delay	t_{OPEN}	R_L = 300Ω, V_S = 3V, V_{AH} = 5V, V_{AL} = 0V	42.58	50.84	55.63	56.74	58.06	ns
Switch Turn “ON” Time	t_{ON}	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V	221.03	229.24	240.85	249.79	256.37	ns
Switch Turn “OFF” Time	t_{OFF}	R_L = 300Ω, V_S = 3V, V_{AH} = 4V, V_{AL} = 0V	188.62	184.65	182.27	184.06	182.45	ns

3. Test Circuits

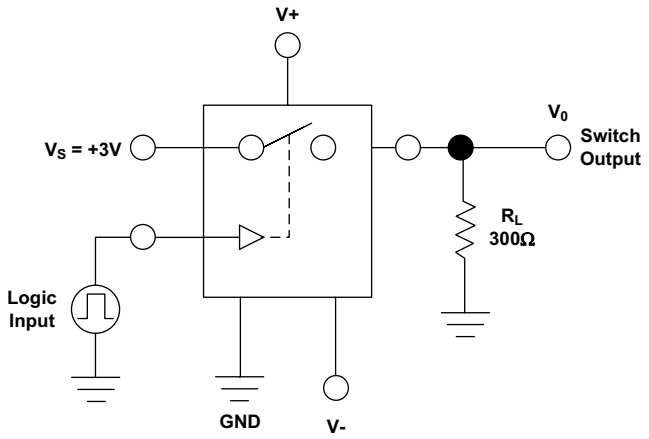


Figure 3. Switching Test Circuit

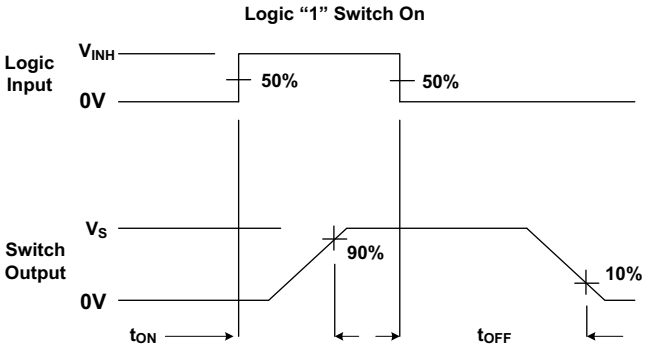


Figure 4. Switching Test Circuit Waveform

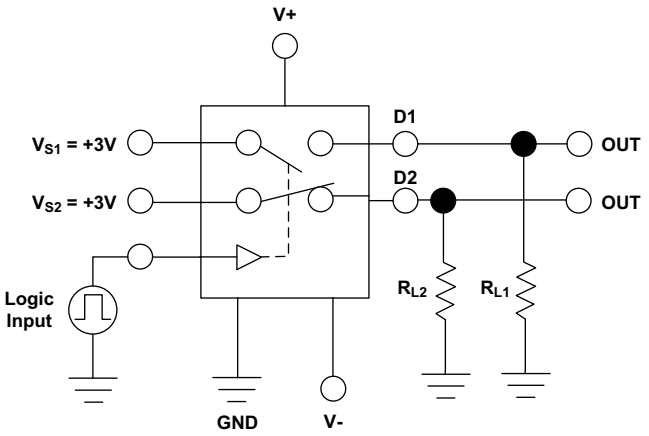


Figure 5. Break-Before-Make Test Circuit

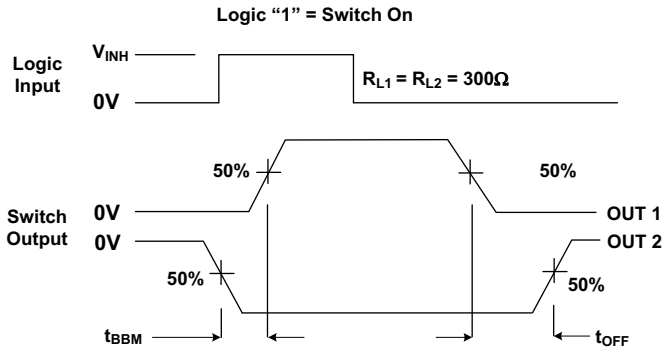


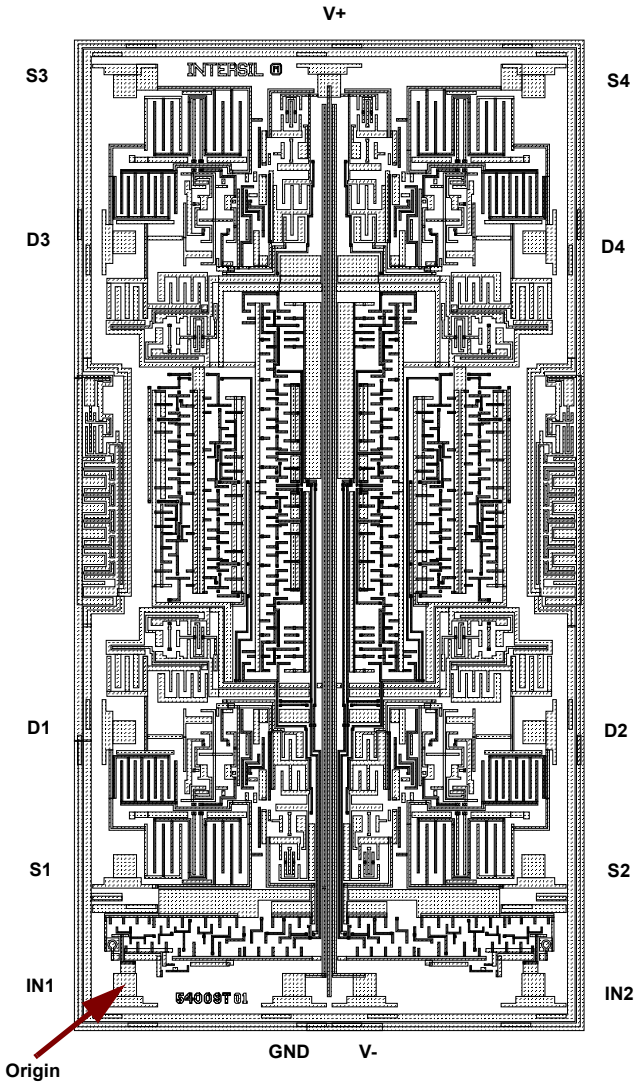
Figure 6. Break-Before-Make Test Circuit Waveforms

4. Die Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimensions	2815µm x 5325µm (106 milsx205 mils) Thickness: 483µm ±25.4µm (19 mils ±1 mil)
Interface Materials	
Glassivation	Type: PSG (Phosphorous Silicon Glass) Thickness: 8.0kÅ ±1.0kÅ
Top Metallization	Type: AlSiCu Thickness: 16.0kÅ ±2kÅ
Backside Finish	Silicon
Substrate	Radiation Hardened Silicon Gate, Dielectric Isolation
Assembly Information	
Substrate Potential	Unbiased (DI)
Additional Information	
Worst Case Current Density	$<2.0 \times 10^5$ A/cm^2
Transistor Count	348
Package Lid Potential	Floating

5. Metallization Mask Layout



5.1 Layout Characteristics

Step and Repeat: 2815µm x 5325µm

Table 3. Layout X-Y Coordinates

Pad Name	X (µm)	Y (µm)	DX (µm)	DY (µm)
S3	0	4672.5	109	109
D3	-4.5	3861	109	109
D1	-4.5	1314	109	109
S1	0	617.5	109	109
IN1	0	0	109	109
GND	878	0	109	109
V-	1246	0	109	109
IN2	2124	0	109	109
S2	2124	617.5	109	109
D2	2128.5	1314	109	109
D4	2128.5	3861	109	109

Table 3. Layout X-Y Coordinates (Continued)

Pad Name	X (µm)	Y (µm)	DX (µm)	DY (µm)
S4	2124	4672	109	109
V+	1062	4675	109	109

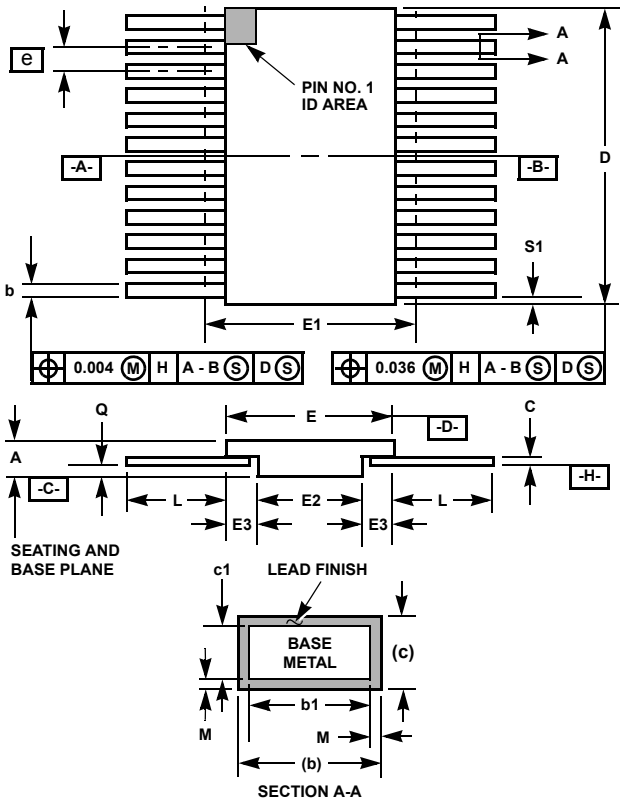
Note: "Origin" as labeled in the Metallization Mask layout is the centroid of the pad labeled "IN1".

6. Revision History

Date	Revision	Change
Jun.17.19	FN8399.4	Applied new template. Updated single event effects description on page 1. Added related literature section on page 1. Added note 4 on page 3. Updated links. Removed About Intersil section.
Mar.4.15	FN8399.3	On page 7, changed the transistor count from “216” to “348”. In Table 3 on page 10, updated 2 pad names to match the “Metallization Mask Layout”: - Changed from “VEE” to “V-” and from “VCC” to “V+”.
Dec.19.13	FN8399.2	Added ESD ratings to Abs Max Table on page 3
Apr.5.13	FN8399.1	Title on page 1 changed CMOS to BiCMOS Continuous Current in Absolute Maximum Ratings on page 3: changed from 30mA to 10mA “V_{SUPPLY} = ±15V unless otherwise specified. This data is typical test data post radiation exposure at a rate of 50 to 300rad(Si)/s. This data shows typical parameter shifts due to total ionizing dose (high dose radiation) T_A= +25°C.” on page 6 changed unit in positive supply current from mA to µA. Updated throughout 300krad to 100krad. Updated Ordering Information on page 2 Updated Electrical Spec Table MIN and MAX values for Leakage Current in Source and Drain for ±15V from ±5 to ±20 Updated in Post Radiation Characteristics Typical values on page 4 for Positive Supply Current for VA1, VA2 from 107.1 to 113.7 and Negative Supply Current for VA1, VA2 from -0.01 to -0.02 Added 100k column to Post Radiation Characteristics table on page 5 Removed negative symbol under 75k column IAL, IAH from 0.71, 0.28 and added negative symbol in I- to 0.019 in VA1, VA2 Removed the words exposed pad from Tjc note. Updated numbers in Table 2 in X(µm) column. Added Note to Table 2.
December 21, 2012	FN8399.0	Initial Release

7. Package Outline Drawing

For the most recent package outline drawing, see K14.A.



K14.A MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B)
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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