HSP48212

Digital Video Mixer

FN3627
Rev 2.00
May 1999

The Intersil HSP48212 is a 68 pin Digital Video Mixer IC intended for use in multimedia and medical imaging applications.

The HSP48212 allows the user to mix two video sources based on a programmable weighting factor. After weighting the input data signals, the Video Mixer simply adds the two weighted signals mathematically. This results in the mixed output, which is a weighted sum of the two sources.

The input and output interfaces are synchronous with respect to the input clock, simplifying the user interface requirements.

Input Data (DINA, DINB), Mix Factor (M) and control signals (RND, TCB) may be delayed relative to each other in order to compensate for any misalignment that may have occurred prior to entering the HSP48212. Each input's delay may be independently programmed up to seven clock cycles.

The output data may be rounded to 8, 10, 12, or 13-bits. The enabling of data onto the output data bus is under the user's control via an output enable signal ($\overline{OE}$).

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP48212VC-40	0 to 70	64 Ld MQFP	Q64.14x14
HSP48212JC-40	0 to 70	68 Ld PLCC	N68.95

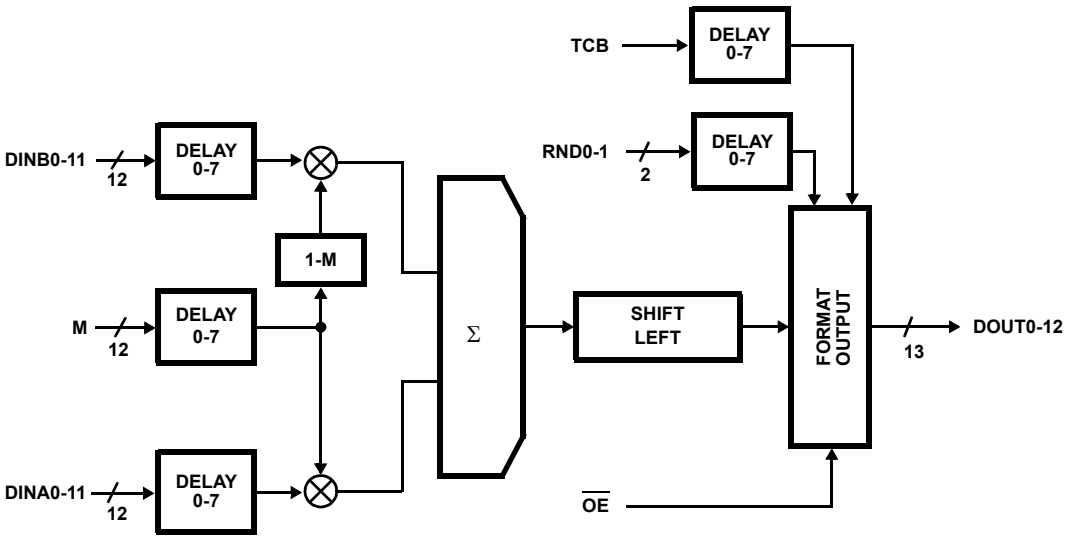
Features

- 12-Bit Pixel Data
- Two's Complement or Unsigned Data
- 12-Bit Mix Factor
- 13-Bit Signed or Unsigned Three State Output
- Overflow Detection and Output Saturation
- Rounding to 8, 10, 12, or 13-Bits
- Input and Output Pixel Data Synchronous to Clock
- Programmable Pipeline Delay of up to 7 Clock Cycles for Control of Misaligned Input Data
- TTL Compatible Inputs/Outputs
- DC to 40MHz Clock Rate

Applications

- Video Summing (Frame Addition)
- Video Mixing
- Fade In/Out
- Video Switching
- High Speed Multiplying

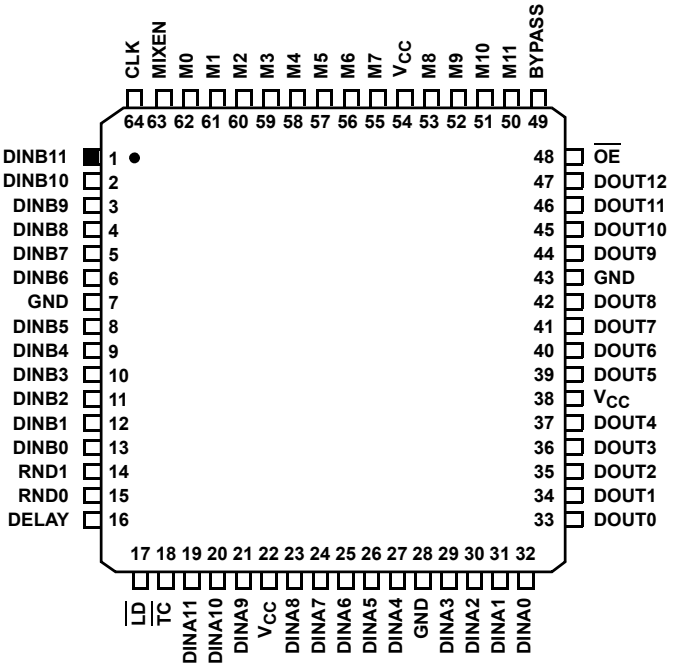
Block Diagram



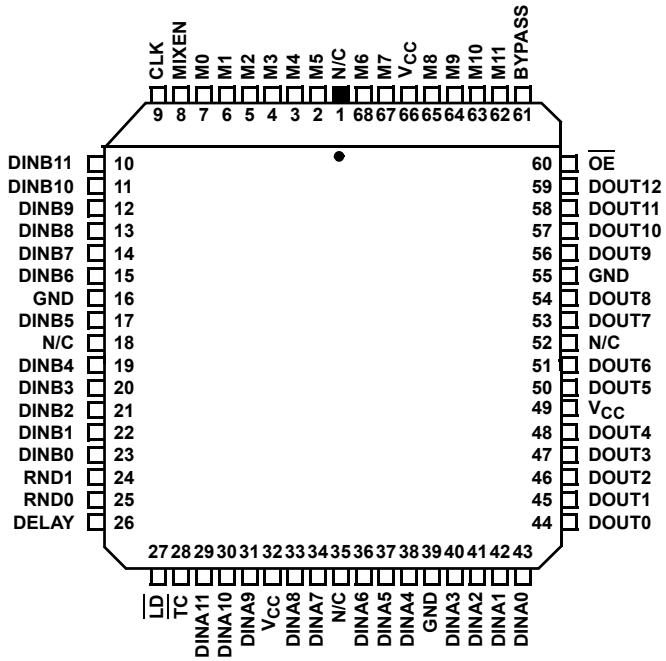
DOUT = 2 x [DINA x M + DINB x (1-M)]

Pinouts

64 LEAD MQFP
TOP VIEW



68 PIN PLCC
TOP VIEW



Pin Descriptions

NAME	PLCC PIN	TYPE	DESCRIPTION
CLK	9	I	Clock Input. All signal pins are synchronous with respect to this clock except $\overline{LD}$, DEL, $\overline{OE}$, and BYPASS.
DINA0-11	29-31 33-34 36-38 40-43	I	Input Data Bus. Provides data to the Mixer from one video source. Synchronous to the rising edge of CLK.
DINB0-11	10-15, 17 19-23	I	Input Data Bus. Provides data to the Mixer from one video source. Synchronous to the rising edge of CLK.
M0-11	62-65 67-68 2-7	I	Mix Input Bus. The range of M is from 0 to 1. The number format is unsigned, with one bit position to the left of the binary point. If a value greater than 1 is placed on this bus, the internal circuitry will saturate M to 1, i.e, anytime the MSB is 1, the internal value defaults to 1.00000000000; synchronous to the rising edge of CLK.
$\overline{TC}$	28	I	Specifies the number format of the input data busses DINA and DINB. 1 = unsigned, 0 = 2's complement. The signal has the same number of latency stages as the incoming data. Therefore, the number format affects the incoming data but not the data in the internal pipeline stages. Synchronous to the rising edge of CLK.
RND0-1	24-25	I	Specifies the number of significant bits on the output bus. 00 = 8-bit, 01 = 10-bit, 10 = 12-bit, 11 = 13-bit. Rounding is performed by adding a binary 1 to the bit position to the right of the desired LSB. The remaining bits are forced to zero. These control signals have the same number of latency stages as the incoming data. Therefore, the output round format does not take effect until the current data has propagated to the output. Synchronous to the rising edge of CLK.
MIXEN	8	I	Mix Enable. This pin is used to disable the clock signal which samples the Mix input. When MIXEN = 1, the M0-11 bus is sampled by the rising edge of CLK. When MIXEN = 0, the M0-11 bus is ignored and the previously stored value of M0-11 is used. Synchronous to the rising edge of CLK.
$\overline{LD}$	27	I	Asynchronous Load Pin. $\overline{LD}$ is used to load the delay control registers. The delay control word is loaded serially from LSB to MSB. This signal drives the clock input to a 15-bit serial shift register. Each $\overline{LD}$ cycle, the data is transferred through the register bank on the rising edge of $\overline{LD}$ In order to load the delay control word, the user must supply exactly 15 $\overline{LD}$ pulses.
DEL	26	I	Delay Input. This is the serial input data that is sampled by the rising edge of $\overline{LD}$. It is the input to the first stage of the 15-bit serial shift register which contains the delay control word. Synchronous to the rising edge of $\overline{LD}$.
BYPASS	61	I	Allows user to disable (bypass) the $\overline{LD}$ interface and use the default delay paths. When BYPASS = 1, the delay control word is forced to all 0's and no extra delays are included in the paths. When BYPASS = 0, the delay control word must be initialized using the $\overline{LD}$/DEL interface in order for the chip to give predictable results. This pin is asynchronous and is not intended to change states during operation.
DOUT0-12	59-56 54-53 51-50 48-44	O	Output Data Bus. The data on this bus reflects the results of the equation: 2x[AxM + Bx(1-M)]. The number format of the output is either 2's complement or unsigned depending on the value of the $\overline{TC}$ signal during data input. The representation of DOUT is also dependent on the value sampled on RND0-1 during data input. (See RND0-1 and $\overline{TC}$ pin description).
$\overline{OE}$	60	I	Output Enable. Asynchronous input which takes effect immediately following a transition. When $\overline{OE}$ = 0 the DOUT bus is driving, when $\overline{OE}$ = 1 the DOUT bus is not driven (floating).
V_{CC}	32, 49, 66	I	5V power supply. There are 3 V_{CC} pads.
GND	16, 39, 55	I	0V power supply. There are 3 GND pads.

Functional Block Diagram

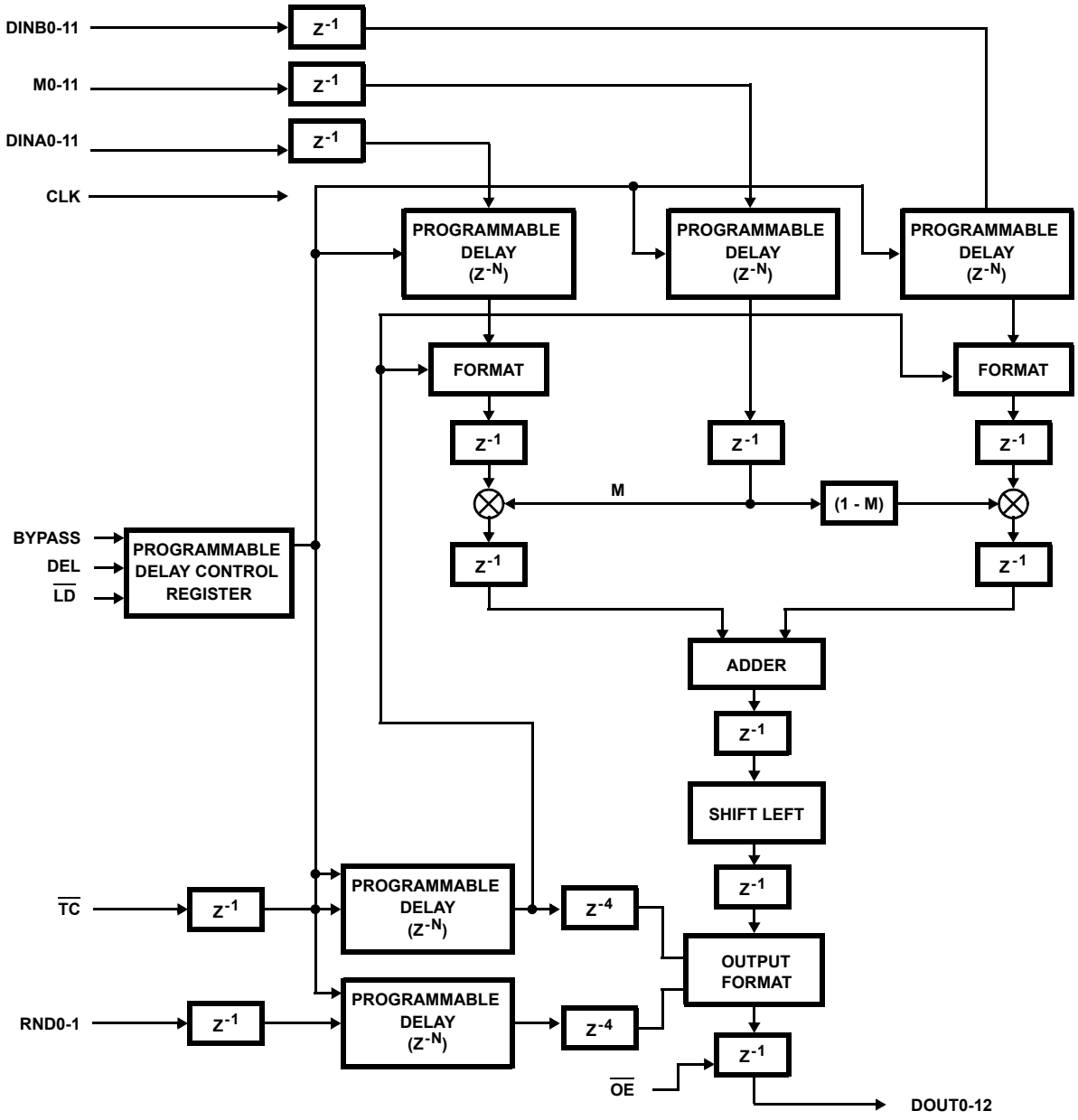


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Functional Description

The Digital Video Mixer is intended for use in professional video, multimedia and medical imaging applications. The HSP48212 allows the user to mix two video sources based on a programmable weighting factor. After weighting the input data signals, the Video Mixer simply adds the two weighted signals mathematically. This results in the mixed output, which is a weighted sum of the two sources. The fundamental equation implemented by this architecture is:

$$DOUT = 2 \times [DINA \times M + DINB \times (1 - M)] \quad \text{(EQ. 1)}$$

where DINA and DINB are the two video sources (pixels) and M is the weighting (Mix) factor. As expressed by this equation, the output DOUT is a weighted average of the incoming pixels. For instance, when M is set to 0 the DINB input source is passed to the output, and when M is set to 1 the DINA input is passed to the output, and when M is set to 0.5 the output is the sum of the two sources DINA and DINB. The user can therefore vary the mix factor to apply different weights to each of the inputs DINA, DINB. This allows functions such as fading in, fading out, fading between images, graphics overlays, and keying. The multiplication factor of 2 as seen in (EQ. 1) is accomplished through a 1-bit shift left (See Figure 1). This shifter is not programmable and cannot be accessed by the user.

The Functional Block Diagram is shown in Figure 1. It can be seen that (EQ. 1) is directly implemented by this architecture. The architecture has a 6 stage inherent latency. This architecture is extremely flexible in that it allows the user to account for misaligned input data by independently programming up to seven additional delay stages for DINA0-11, DINB0-11, and M0-11, as well as for the format control signals $\overline{TC}$ and RND0-1. The programmable delay registers are controlled by the signals DEL, $\overline{LD}$, and BYPASS.

The HSP48212 input interface is primarily synchronous to the rising edge of CLK with the exception of the programmable delay control signals DEL, $\overline{LD}$, and BYPASS. The output data bus DOUT0-12 is registered synchronous to the rising edge of CLK and may also be controlled via the asynchronous output enable signal $\overline{OE}$. The input data, DINA0-11 and DINB0-11, as well as the mix factor M0-11 have 12-bit precision. The output data DOUT0-12 has 13-bit precision to allow for 1-bit of growth.

The signals $\overline{TC}$ and RND0-1 control the format of the input and output data. $\overline{TC}$ allows DINA0-11 and DINB 0-11 to be either two's complement or unsigned (Note: DINA0-11 and DINB0-11 must have the same format, i.e., no mixed mode). The output data DOUT0-12 can be rounded to 8, 10, 12, or 13-bits as determined by the control signals RND0-1.

Input Data Format

DINA0-11 and DINB0-11 represent two digital video sources (pixels). Each input bus has 12-bits of precision. They may be represented in two's complement form ($\overline{TC}$ = 0) or in unsigned form ($\overline{TC}$ = 1). It is important to note that DINA0-11 and DINB0-11 must be represented in the same format (i.e., no mixed mode operation is allowed).

M0-11 supplies the weighting (Mix) factor and has 12-bits of precision. M0-11 must be represented in unsigned format and may range from 0 to 1. If a value greater than 1 is placed on the bus, the internal circuitry will saturate M0-11 to 1.00000000000.

DINA0-11, DINB0-11, and M0-11 are synchronously registered on the rising edge of CLK.

The signal MIXEN allows the user to disable the internal clock signal which samples the M0-11 input bus. When MIXEN = 0, the M0-11 bus is ignored and the previously sampled M0-11 value is used. When MIXEN = 1, the M0-11 bus is sampled on the rising edge of CLK.

Programmable Delay

The input data (DINA0-11, DINB0-11), mix factor (M0-11), and control signals (RND0-1, $\overline{TC}$), may be delayed relative to each other in order to compensate for any misalignment that may have occurred prior to entering the HSP48212. Each input's delay may be independently programmed for up to seven delays. In other words, the user can program a different number of pipeline delays for each input. This programmed delay is in addition to the inherent 6 stage delay required by the architecture.

As shown in Figures 2 and 3, the programmable delay information is loaded using the signals $\overline{LD}$ and DEL. $\overline{LD}$ is the asynchronous load pin used to clock in the delay control word. The delay control word is clocked into a 15-bit serial shift register on the rising edge of $\overline{LD}$ (i.e., DEL is synchronous to $\overline{LD}$). The delay control word data is supplied by the DEL signal beginning with the least significant bit and continuing until the most significant bit has been clocked in. On each $\overline{LD}$ cycle the DEL data input is transferred through the register bank. The user must supply exactly 15 $\overline{LD}$ pulses; if the shift register is clocked more than 15 times, only the most recent 15 data inputs will be stored.

As previously stated, the length of the control word is 15-bits: 3-bits are allocated for each of the 5 inputs, DINA0-11, DINB0-11, M0-11, RND0-1, and $\overline{TC}$. Each 3-bits of the control word allow the user to specify from 0 to 7 additional delay stages by programming the binary equivalent of the desired delay into the appropriate bit position of the delay control word register (e.g., 000 for 0 delays, 001 for 1 delay, ..., 111 for 7 delays).

TABLE 1.

INPUT SIGNAL	CONTROL WORD BIT POSITION
RND0-1	12-14
$\overline{TC}$	9-11
M0-11	6-8y
DINB0-11	3-5
DINA0-11	0-2

The BYPASS control signal enables the programmable delay registers to be bypassed. When BYPASS is high, the delay control word is forced to all 0's and no additional delays are included in any of the input paths. However, when BYPASS is low, the $\overline{LD}$/DEL serial delay control word interface is active and the delay control word must be initialized in order to achieve any meaningful results.

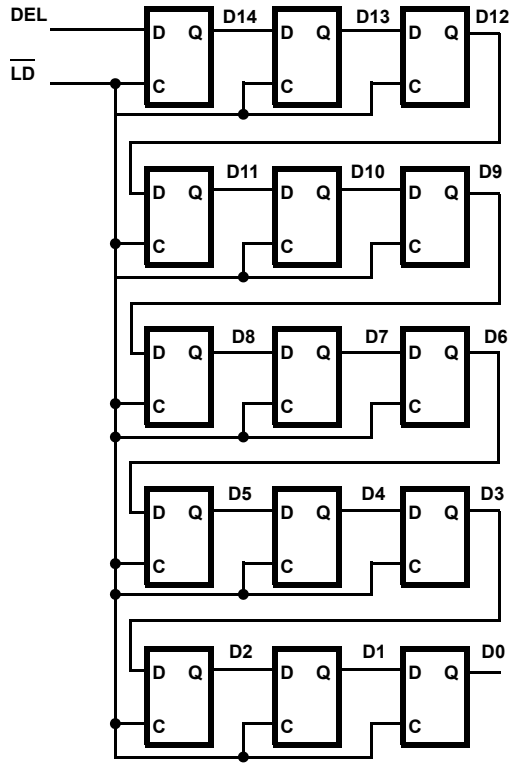


FIGURE 2. DELAY CONTROL WORD SHIFT REGISTER

Format Control Signals

The control signals $\overline{TC}$ and RND0-1 are used to specify the input data representation and the output data representation respectively. $\overline{TC}$ and RND0-1 are synchronous to CLK, which allows them to be changed on a cycle by cycle basis if needed. The control signals are designed to match the latency of the data paths. When the control inputs change, the new configuration will effect the current input data and will not effect the data in the pipeline stages. For example, if the rounding selection is changed from 8-bit rounding to 10-bit rounding on a given cycle, the output will remain in an 8-bit representation while the new data is propagating through the circuit. When the results of the new data are available at the output, the number format will change to 10-bits.

The RND0-1 control signals determine the number of significant bits on the output bus DOUT0-12. The output data may be rounded to 8, 10, 12, or 13-bits. The rounding operation is performed by adding a binary 1 to the bit position right of the desired LSB and forcing the undesired bits to 0. For example, in 8-bit rounding, a 1 is added to the 9th bit to the right of the MSB (DOUT4), and DOUT0-4 are forced to 0 (i.e., DOUT0-12 = XXXXXXXX00000).

Output Control

DOUT0-12 is the output data bus which represents the weighted average of the incoming pixel data as indicated by (EQ. 2):

$$DOUT = 2 \times [(DINA \times M) + (DINB \times (1 - M))] \quad \text{(EQ. 2)}$$

The output data will be represented in either two's complement format or in unsigned format depending on the value of the $\overline{TC}$ signal when the input data (DINA0-11 and DINB0-11) is sampled by CLK. Similarly, the output representation of DOUT0-12 is also dependent on the value of RND0-1 during sampling of the input data.

The output data DOUT0-12 is registered at the output of the HSP48212 on the rising edge of CLK. The output data may be accessed through the activation of the signal $\overline{OE}$. $\overline{OE}$ is an asynchronous input which, when low, causes the DOUT0-12 bus to drive; when $\overline{OE}$ is high, the DOUT0-12 bus is not driven (floating).

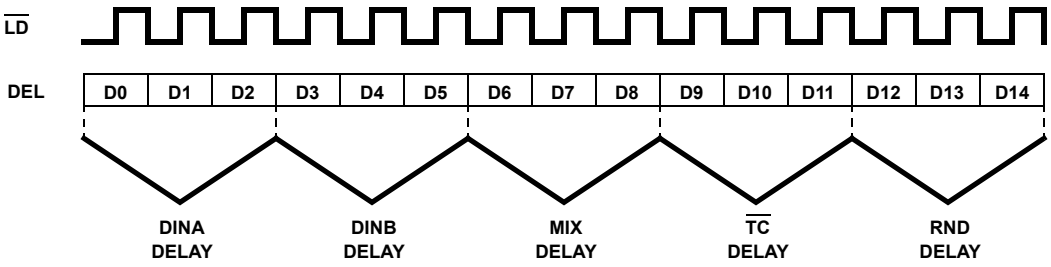


FIGURE 3. DELAY CONTROL WORD TIMING DIAGRAM

Absolute Maximum Ratings

Supply Voltage 8.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
Storage Temperature Range . . . . . -65^oC to 150^oC
Junction Temperature . . . . . 150^oC
Lead Temperature (Soldering 10s) . . . . . 300^oC
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PLCC Package	48
MQFP Package	55

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Operating Conditions

Operating Voltage Range, Commercial . . . . . 5V ±5%
Supply Voltage Range (Typical) . . . . . 0^oC to 70

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = Max, CLK Frequency 40MHz, (Notes 3, 4)	-	170	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = Max, Outputs Not Loaded	-	500	µA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC}	-10	10	µA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-10	10	µA
Logical One Input Voltage	V_{IH}	V_{CC} = Max	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min	-	0.8	V
Logical One Output Voltage	V_{OH}	I_{OH} = -400µA, V_{CC} = Min	2.6	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 2mA, V_{CC} = Min	-	0.4	V
Clock Input High	V_{IHC}	V_{CC} = Max	3.0	-	V
Clock input Low	V_{ILC}	V_{CC} = Min	-	0.8	V
Input Capacitance	C_{IN}	CLK Frequency 1MHz, all measurements referenced to GND. $T_A = 25^oC$, Note 2	-	10	pF
Output Capacitance	C_{OUT}		-	10	pF

NOTES:

2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.
3. Power Supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 4.25mA/MHz.
4. Output load per test load circuit and C_L = 40pF.

AC Electrical Specifications

PARAMETER	SYMBOL	40MHz		UNITS
		MIN	MAX	
CLK Period	T_{CP}	25	-	ns
CLK High	T_{CH}	10	-	ns
CLK Low	T_{CL}	10	-	ns
$\overline{LD}$ Period	T_{LP}	25	-	ns
$\overline{LD}$ High	T_{LH}	10	-	ns
$\overline{LD}$ Low	T_{LL}	10	-	ns
Data Setup Time to CLK High	T_{DS}	10		ns
Data Hold Time from CLK High	t_{DH}	0	-	ns

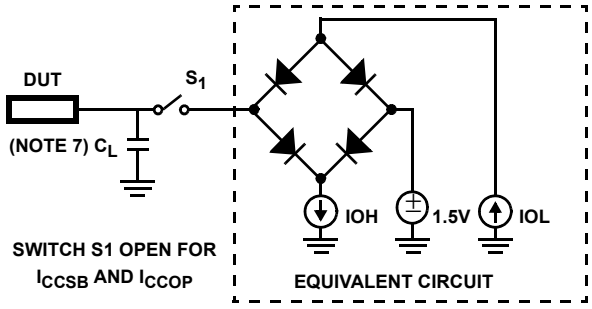
AC Electrical Specifications (Continued)

PARAMETER	SYMBOL	40MHz		UNITS
		MIN	MAX	
MIX Data Setup Time to CLK High	t_{MS}	10	-	ns
MIX Data Hold Time From CLK High	t_{MH}	0	-	ns
Control Data Setup Time to CLK High	t_{CS}	10	-	ns
Control Data Hold Time From CLK High	t_{CH}	0	-	ns
DEL Setup to $\overline{LD}$ High	t_{DLS}	12	-	ns
DEL Hold from $\overline{LD}$ High	t_{DLH}	0	-	ns
CLK to Output Data Delay	t_{OUT}	-	13	ns
Output Enable Time	t_{OE}	-	13	ns
Output Disable Time	t_{OD}	-	13	ns, Note 6
Output Rise/Fall Time	t_{RF}	-	5	ns. Note 6

NOTES:

5. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -400µA. Input reference level CLK = 2.0V. Input reference level for all other inputs is 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V, V_{ILC} = 0V.
6. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or Design changes.

AC Test Load Circuit



NOTE:

7. Test Head Capacitance.

Waveforms

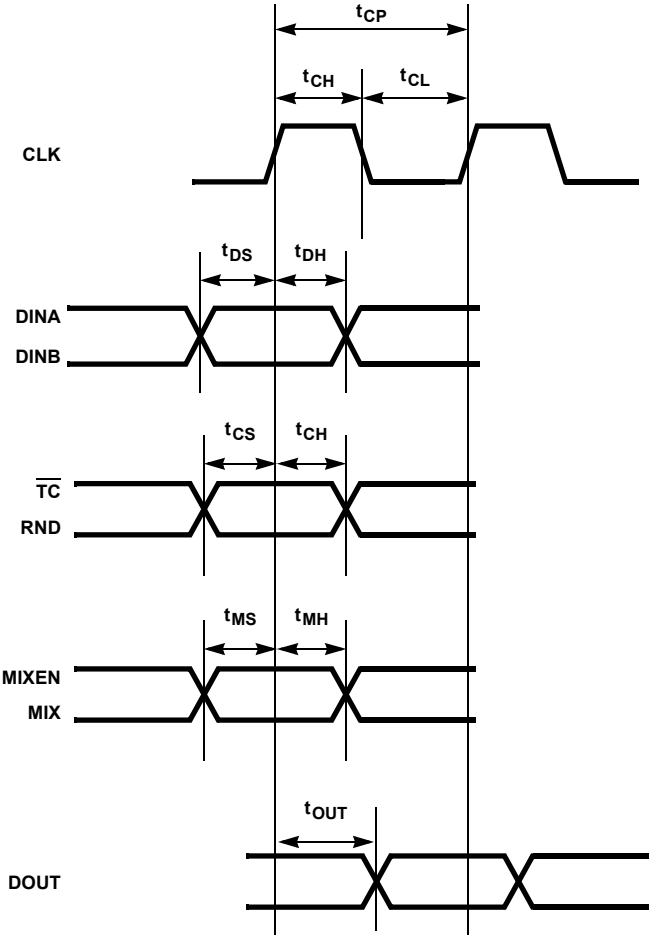


FIGURE 4. SYNCHRONOUS TIMING

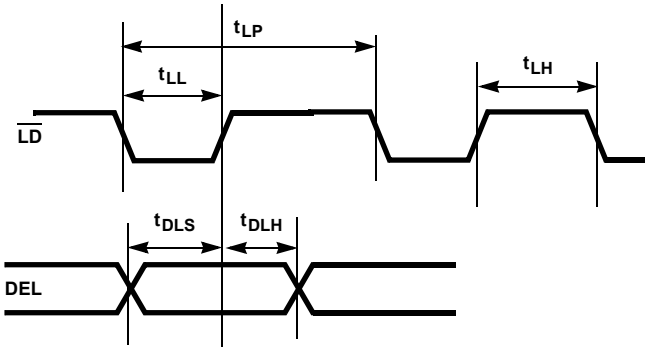


FIGURE 5. ASYNCHRONOUS TIMING

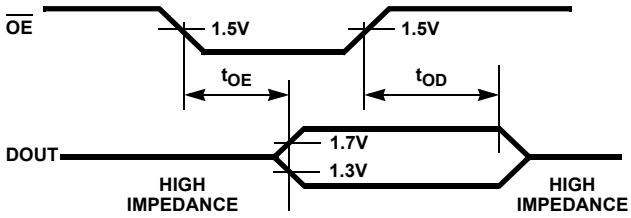


FIGURE 6. OUTPUT ENABLE, DISABLE TIMING

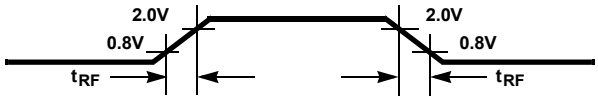


FIGURE 7. OUTPUT RISE AND FALLTIMES