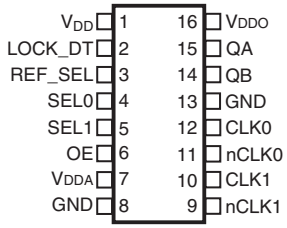
General Description

The ICS840272I is a PLL-based Frequency Translator intended for use in Synchronous Ethernet applications. This high performance device is optimized to generate 25MHz and 8kHz LVCMOS clock outputs. The ICS840272I accepts the following differential or single-ended input signals: 161.1328125MHz (10GbE Mode), 156.25MHz (1GbE Mode), or 125MHz (Recovered clock from 10/100/1000BaseT Ethernet PHY). The extended temperature range supports telecommunication and networking end equipment requirements.

Features

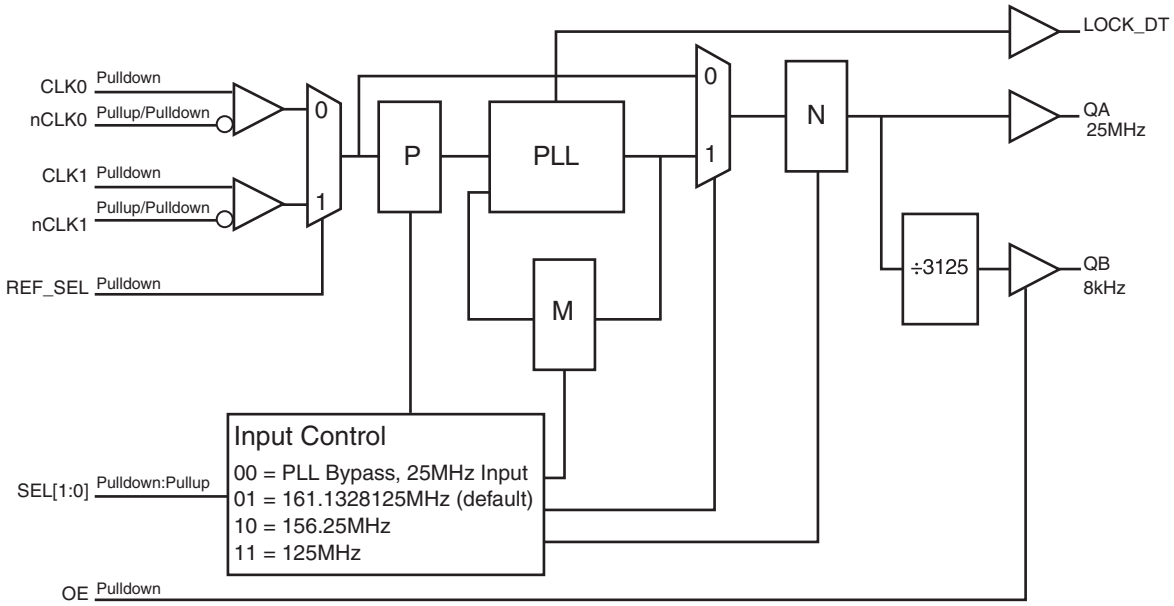
- Two single-ended outputs (LVCMOS or LVTTL levels), output impedance: 17Ω
- Single-ended lock detect output (LVCMOS or LVTTL levels)
- Two selectable differential clock inputs
- Differential input pair (CLKx, nCLKx) accepts LVPECL, LVDS, LVHSTL, SSTL, HCSL input levels
- Internal resistor bias on nCLK pin allows the user to drive CLK input with external single-ended (LVCMOS/ LVTTL) input levels
- Selectable input frequencies: 161.1328MHz, 156.25MHz or 125MHz
- Output frequency: 25MHz, 8kHz
- Full 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging

Pin Assignment



ICS840272I
16-Lead TSSOP
4.40mm x 5.0mm x 0.925mm package body
G Package
Top View

Block Diagram



Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DD}	Power		Core supply pin.
2	LOCK_DT	Output		Lock detect. Logic HIGH when PLL is locked.
3	REF_SEL	Input	Pulldown	Selects the input reference clock. When LOW, selects CLK0, nCLK0. When HIGH, selects CLK1, nCLK1. LVCMOS/LVTTL interface levels.
4	SEL0	Input	Pullup	Selects the input reference frequency and the PLL bypass mode. See *Table 3A*. LVCMOS/LVTTL interface levels.
5	SEL1	Input	Pulldown	Selects the input reference frequency and the PLL bypass mode. See *Table 3A*. LVCMOS/LVTTL interface levels.
6	OE	Input	Pulldown	8kHz output enable pin. When LOW, QB is disabled. When HIGH, QB is enabled. LVCMOS/LVTTL interface levels. See *Table 3B*.
7	V_{DDA}	Power		Analog supply pin.
8	GND	Power		Power supply ground.
9	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to $V_{DD}/2$.
10	CLK1	Input	Pulldown	Non-inverting differential clock input.
11	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to $V_{DD}/2$.
12	CLK0	Input	Pulldown	Non-inverting differential clock input.
13	GND	Power		Power supply ground.
14	QB	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
15	QA	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
16	V_{DDO}	Power		Output supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See *Table 2*, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DDO} = 3.465V		17		Ω

Function Tables

Table 3A. SEL[1:0] Function Table

Inputs			Function	Output (MHz)
SEL1	**SEL0**	**CLKx, nCLKx (MHz)**	**Mode**	**QA**
0	0	25	PLL Bypass	25
0 (default)	1 (default)	161.1328125	PLL Enabled	25
1	0	156.25	PLL Enabled	25
1	1	125	PLL Enabled	25

Table 3B. OE Function Table

Control Input	Function
OE	**QB Output**
0 (default)	Disabled (High impedance)
1	Enabled

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVCMOS)	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	81.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.11	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				57	mA
I_{DDA}	Analog Supply Current				11	mA
I_{DDO}	Output Supply Current				5	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		0.8	V
I_{IH}	Input High Current	OE, SEL1, REF_SEL	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		SEL0	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	OE, SEL1, REF_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		SEL0	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage		I_{OH} = -12mA	2.6			V
V_{OL}	Output Low Voltage		I_{OL} = 12mA			0.5	V

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK[0:1], nCLK[0:1]	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK[0:1]	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK[0:1]	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

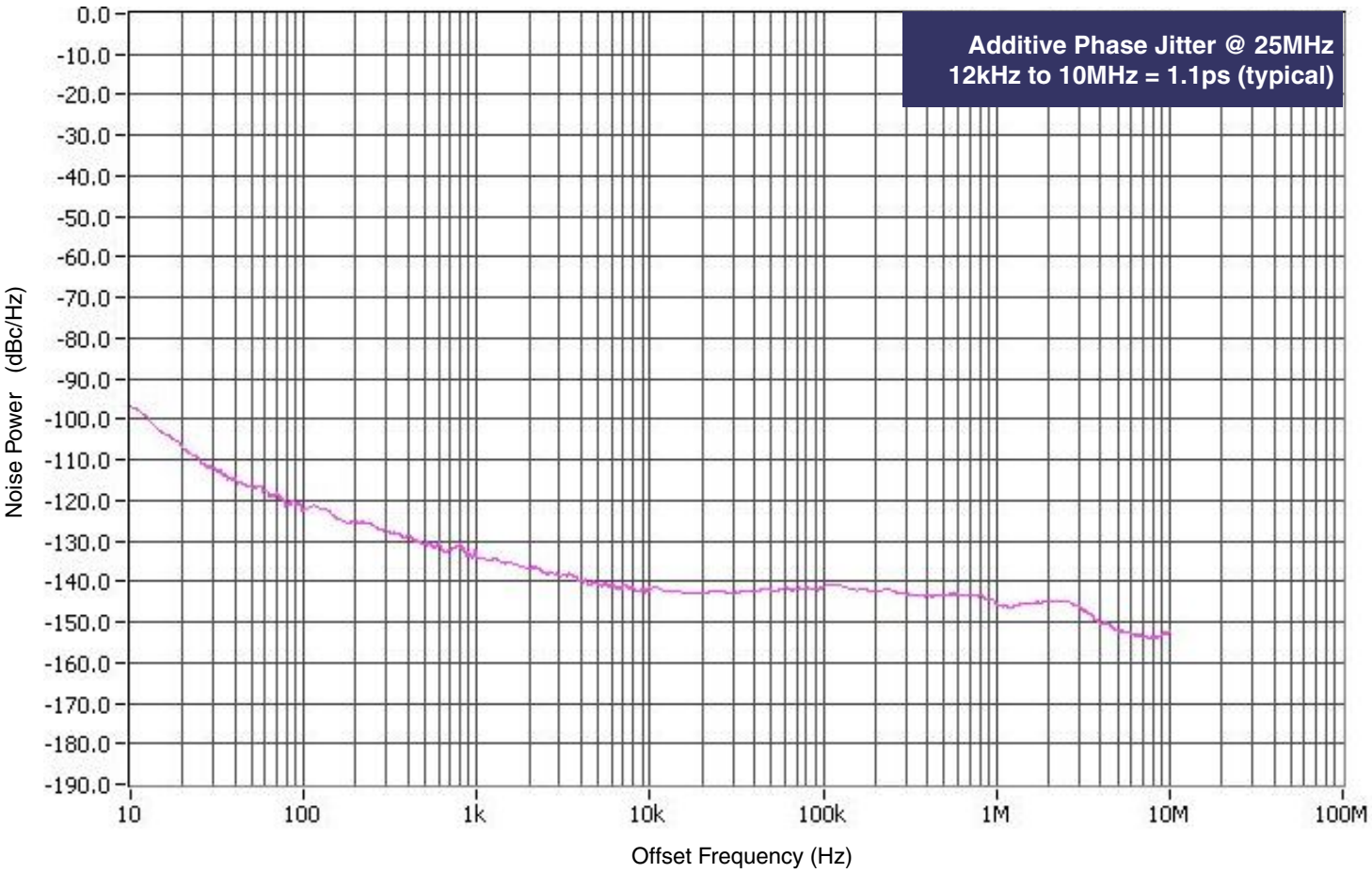
AC Electrical Characteristics

Table 5. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

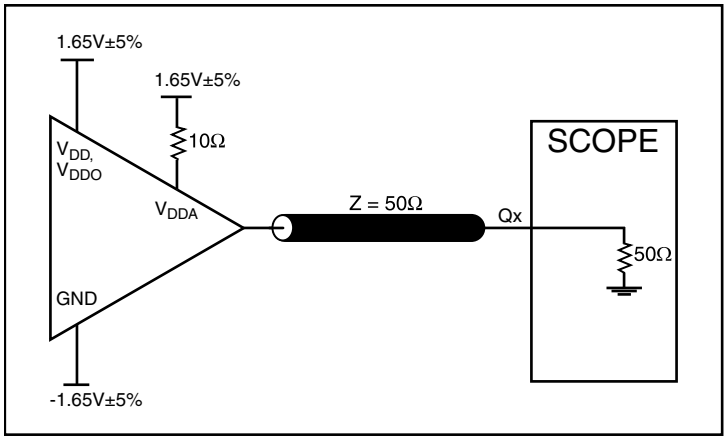
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QA			25		MHz
		QB			8		kHz
$t_{jit}(Ø)$	RMS Phase Jitter (Random); NOTE 1	QA	25MHz, Integration Range: 12kHz – 10MHz		1.1		ps
$t_{jit}(cc)$	Cycle-to-Cycle Jitter	QA	25MHz			37	ps
t_R / t_F	Output Rise/Fall Time	QA	20% to 80%	450		1100	ps
		QB	20% to 80%	450		1100	ps
odc	Output Duty Cycle	QA		47		53	%
		QB		47		53	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Refer to Phase Noise plot.

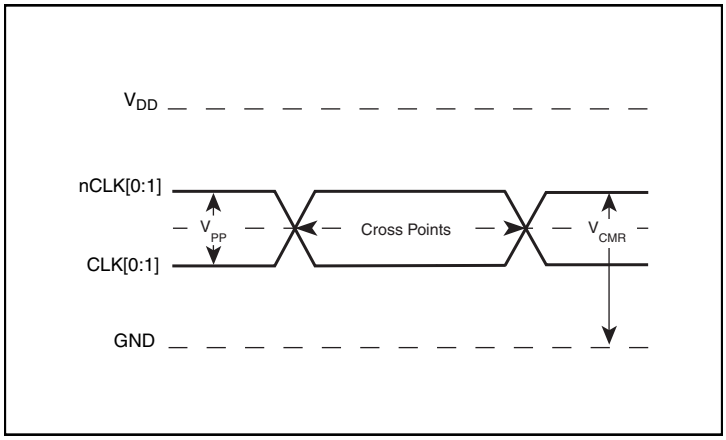
Typical Phase Noise at 25MHz



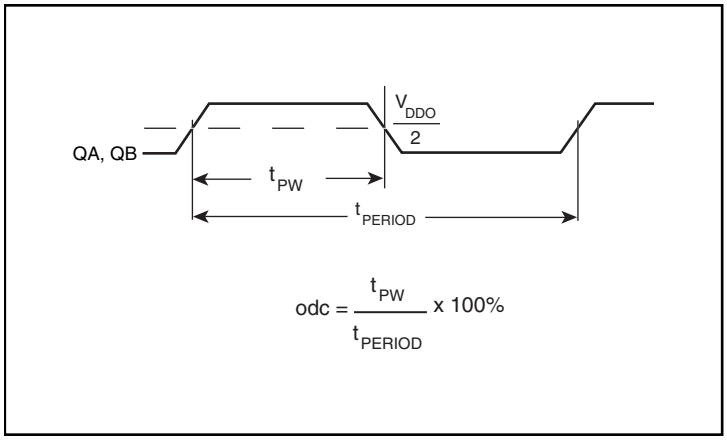
Parameter Measurement Information



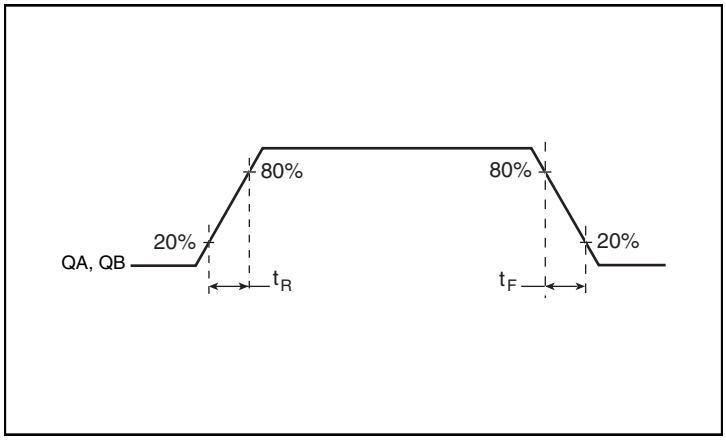
LVCMOS Output Load AC Test Circuit



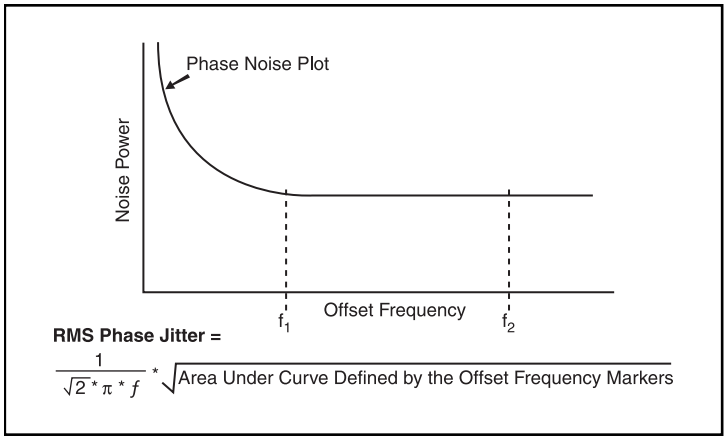
Differential Input Level



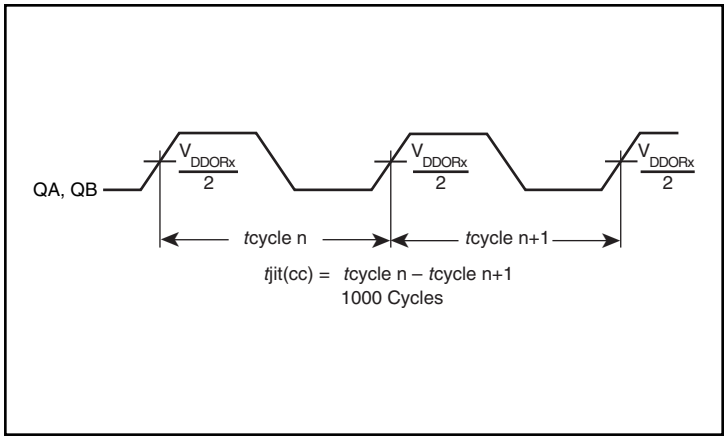
Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time



RMS Phase Jitter



Cycle-to-Cycle Jitter

Applications Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS840272I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{DD,}$ V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

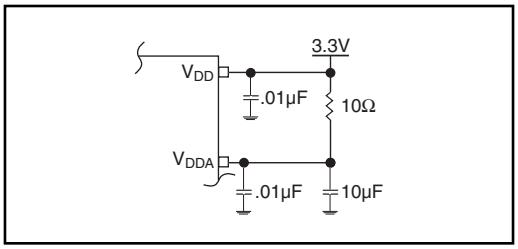


Figure 1. Power Supply Filtering

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Suggested edge rate faster than 1V/ns. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

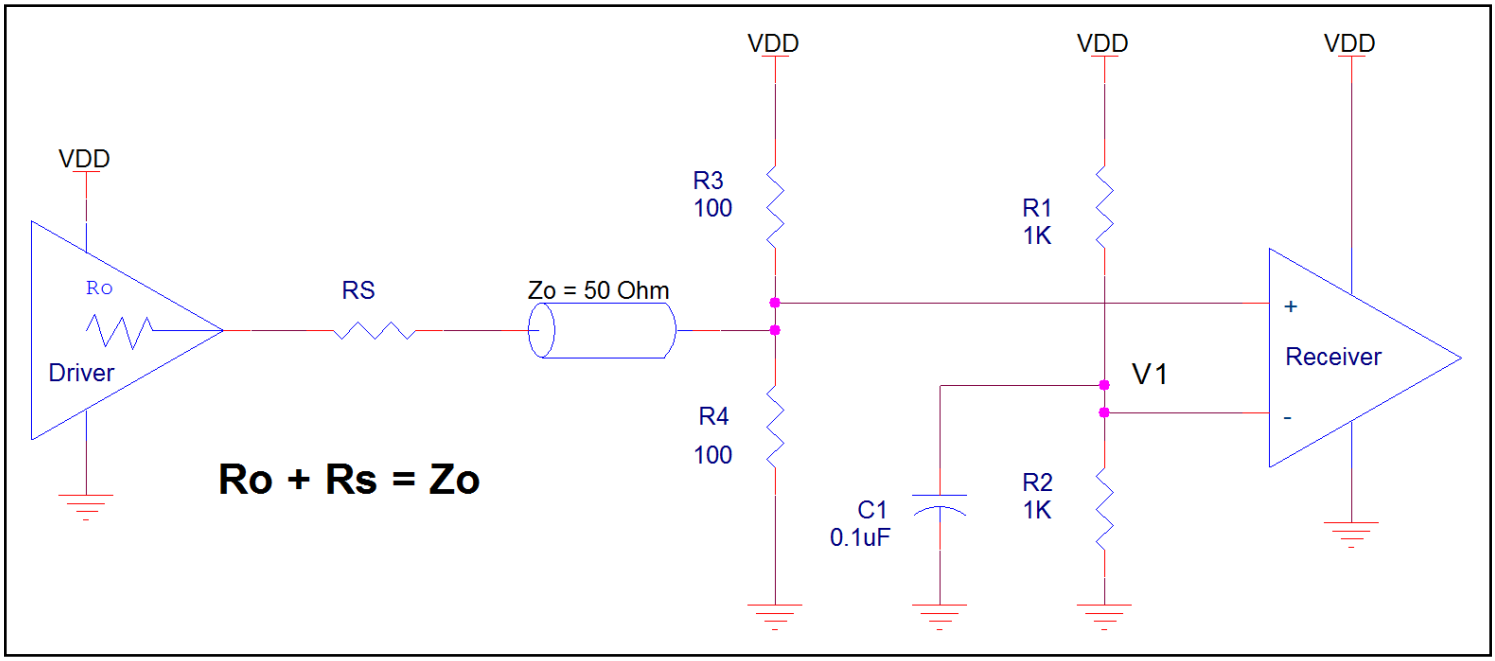


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figure 3A* to *Figure 3F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 3A*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

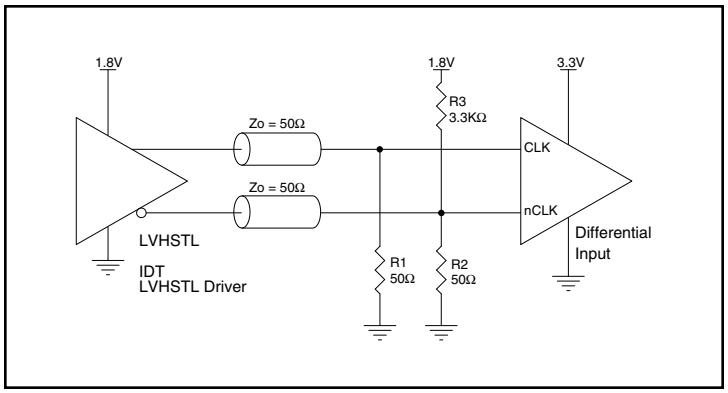


Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

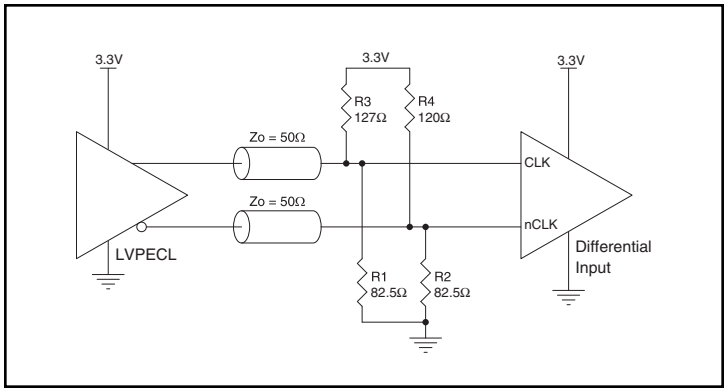


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

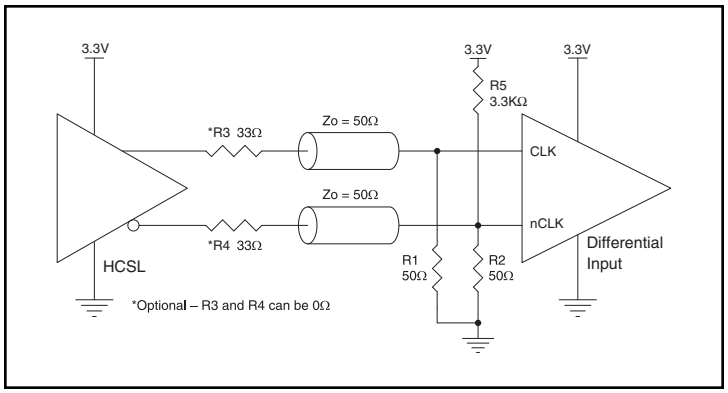


Figure 3C. CLK/nCLK Input Driven by a 3.3V HCSL Driver

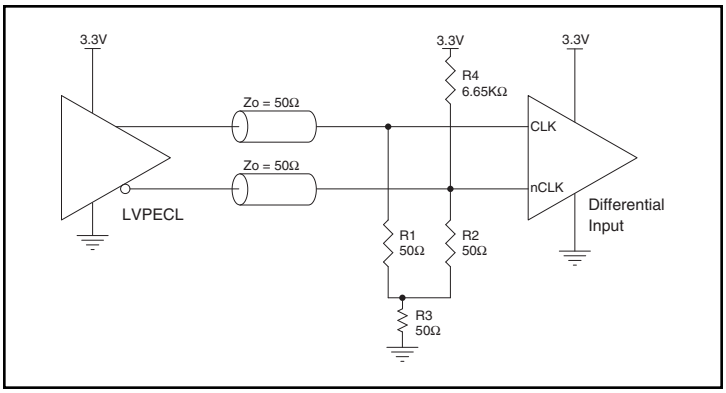


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

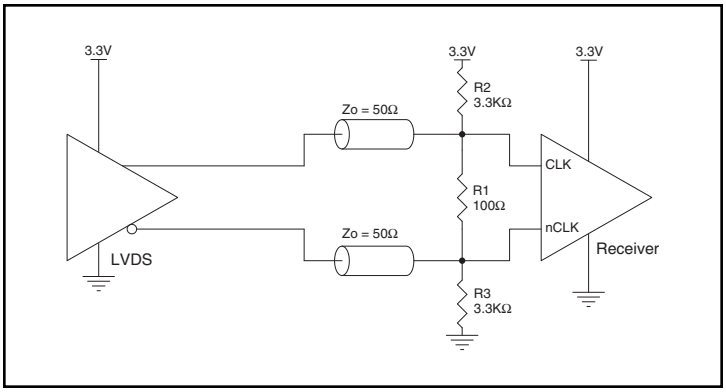


Figure 3E. CLK/nCLK Input Driven by a 3.3V LVDS Driver

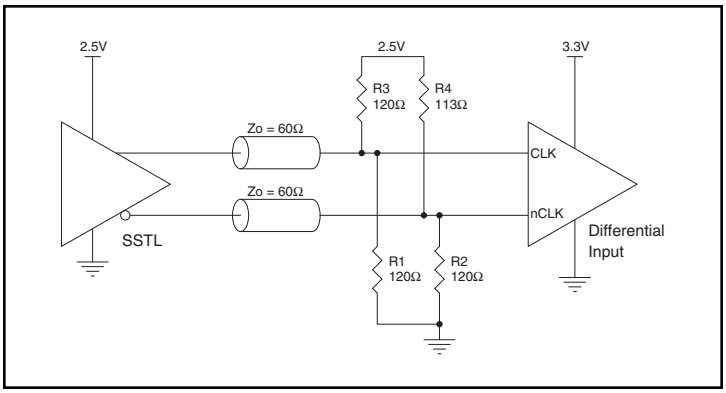


Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

Schematic Example

Figure 4 (next page) shows an example ICS840272I application which focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

The ICS840272I requires a variation on each of the standard LVDS and LVPECL termination networks for the input clocks. These variations introduce an input offset that ensures the LOCK_DT output stays at a stable logic low value when the input clock is either stopped or tri-stated. Notice in particular the nonstandard value of R4 in the LVPECL termination and the addition of R11 and R12 in the LVDS termination. Use these same terminations for AC coupling.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS840272I provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 10 ohm VCCA resistor and the 0.1uf capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Pull up and pull down resistors to set configuration pins can all be placed on the pcb side opposite the device side to free up device side area if necessary.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

For additional layout recommendations and guidelines, contact clocks@idt.com.

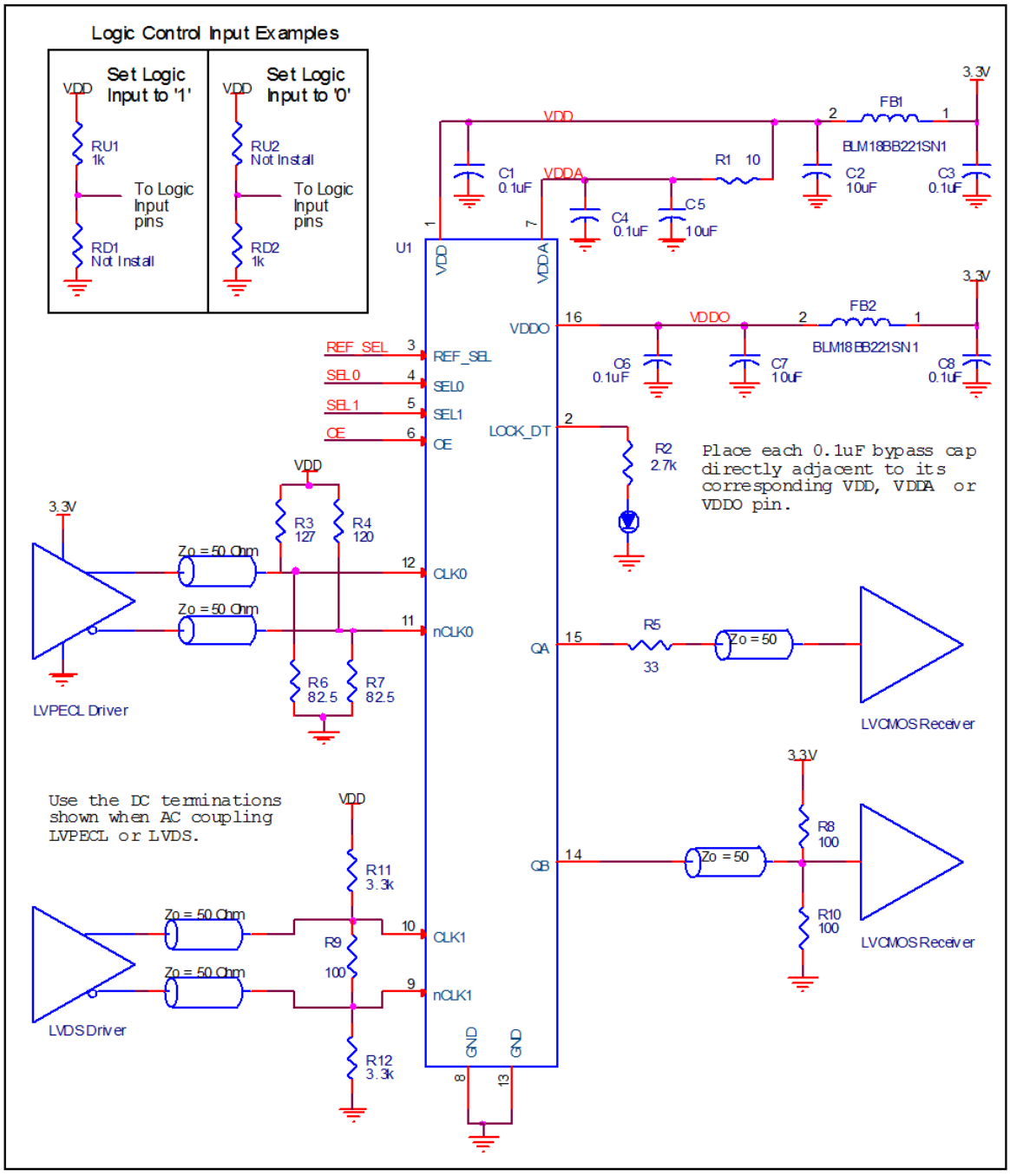


Figure 4. ICS840272I Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS840272I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS840272I is the sum of the core power plus the analog power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD} + I_{DDA} + I_{DDO})$ = 3.465V *(57mA + 11mA + 5mA) = **252.9mW**
- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD\_MAX} / [2 * (50Ω + R_{OUT})]$ = 3.465V / [2 * (50Ω + 17Ω)] = **25.86mA**
- Total Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 17Ω * (25.86mA)^2 = **11.4mW per output**
  Total Power (R_{OUT}) = 11.4mW * 2 = 22.8mW

Total Power Dissipation

- **Total Power**
  = Power $(core)_{MAX}$ + Total Power (R_{OUT})
  = 252.9mW + 22.8mW
  = 275.7mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 81.2°C/W per *Table 6* below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.276W *81.2°C/W = 107.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16-Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.2°C/W	73.9°C/W	70.2°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16-Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.2°C/W	73.9°C/W	70.2°C/W

Transistor Count

The transistor count for ICS840272I: 3326

Package Outline and Package Dimensions

Package Outline - G Suffix for 16-Lead TSSOP

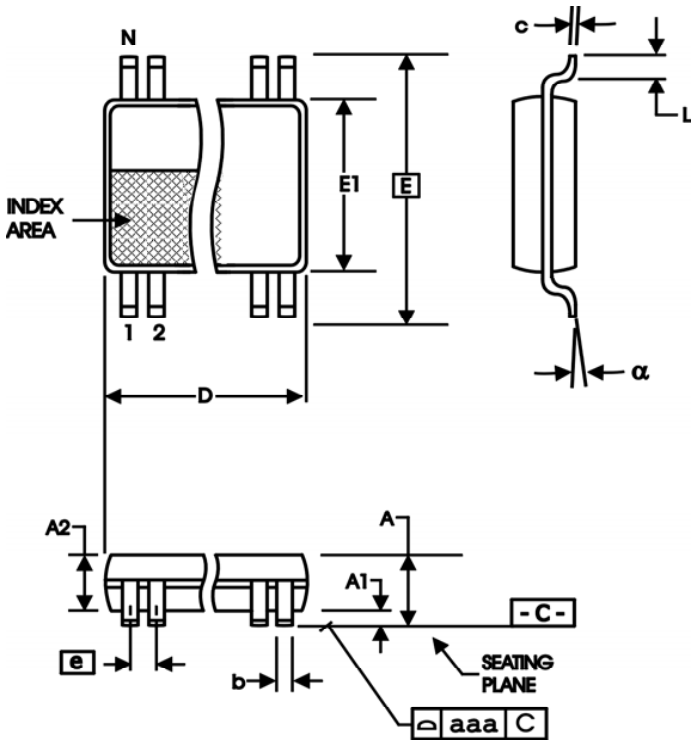


Table 8. Package Dimensions for 16-Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840272AGILF	40272AIL	“Lead-Free” 16-Lead TSSOP	Tube	-40°C to 85°C
840272AGILFT	40272AIL	“Lead-Free” 16-Lead TSSOP	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		10 11-12	Updated Differential Clock Input Interface drawings. Updated schematic and schematic text.	6/19/2014

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