GENERAL DESCRIPTION

The 841S012DI is an optimized PCIe, sRIO and Gigabit Ethernet Frequency Synthesizer and a member of high performance clock solutions from IDT. The 841S012DI uses a 25MHz parallel resonant crystal to generate 33.33MHz - 200MHz clock signals, replacing multiple oscillators and fanout buffer solutions. The device supports ±0.25% center-spread, and -0.5% down-spread clocking with two spread select pins (SSC[1:0]). The VCO operates at a frequency of 2GHz. The device has three output banks: Bank A with two 100MHz – 250MHz HCSL outputs; Bank B with seven 33.33MHz – 200MHz LVCMOS/ LVTTL outputs; and Bank C with one 33.33MHz – 200MHz LVCMOS/LVTTL output.

All Banks A, B and C have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The low jitter characteristic of the 841S012DI makes it an ideal clock source for PCIe, sRIO and Gigabit Ethernet applications. Designed for networking and industrial applications, the 841S012DI can also drive the high-speed clock inputs of communication processors, DSPs, switches and bridges.

FEATURES

- Two 0.7V differential HCSL outputs (Bank A), configurable for PCIe (100MHz or 250MHz) and sRIO (100MHz or 125MHz) clock signals

  Eight LVCMOS/LVTTL outputs (Banks B/C), 18Ω typical output impedance

  Two REF_OUT LVCMOS/LVTTL clock outputs, 23Ω typical output impedance

- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or one LVCMOS/LVTTL single-ended reference clock input

- Supports the following output frequencies:
  HCSL Bank A: 100MHz, 125MHz, 200MHz and 250MHz
  LVCMOS/LVTTL Bank B/C: 33.33MHz, 50MHz, 66.67MHz, 100MHz, 125MHz, 133.33MHz, 166.67MHz and 200MHz

- VCO: 2GHz

- Spread spectrum clock: ±0.25% center-spread (typical) and -0.6% down-spread (typical)

- PLL bypass and output enable

- RMS period jitter: 10ps (typical), QAx/nQAx outputs

- Full 3.3V supply mode

- -40°C to 85°C ambient operating temperature

- Available in lead-free (RoHS 6) package

PIN ASSIGNMENT

Top pins (56–43): V_DDOB, QB6, GND, QB5, V_DDOB, QB4, GND, QB3, V_DDOB, QB2, GND, QB1, QB0, V_DDOB

Left pins (1–14):
1 V_DD_REFOUT
2 REF_OUT0
3 REF_OUT1
4 GND
5 GND
6 REF_IN
7 V_DD
8 REF_SEL
9 XTAL_IN
10 XTAL_OUT
11 BYPASS
12 REF_OE
13 nMR
14 V_DD

Right pins (42–29):
42 V_DDOC
41 QC
40 GND
39 QBC_OE
38 V_DDA
37 V_DDA
36 GND
35 GND
34 IREF
33 QA0
32 nQA0
31 QA1
30 nQA1
29 V_DD

ICS841S012DI
56-Lead VFQFN
8mm x 8mm x 0.925mm package body
K Package
Top View

Bottom pins (15–28): GND, SSC1, SSC0, F_SELB2, F_SELB1, F_SELB0, F_SELC2, F_SELC1, F_SELC0, F_SELA1, F_SELA0, QA_OE, GND, V_DD

BLOCK DIAGRAM

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DD_REFOUT}	Power		Output supply pin for REF_OUT.
7, 14, 28, 29	V_{DD}	Power		Core supply pins.
2, 3	REF_OUT0, REF_OUT1	Output		Single-ended LVCMOS/LVTTL reference clock outputs. 23Ω typical output impedance.
4, 5, 15, 27, 35, 36, 40, 46, 50, 54	GND	Power		Power supply ground.
6	REF_IN	Input	Pulldown	Single-ended LVCMOS/LVTTL reference clock input.
8	REF_SEL	Input	Pulldown	Reference select pin. When HIGH selects REF_IN. When LOW, selects crystal. LVCMOS/LVTTL interface levels. See Table 3E.
9, 10	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input. External tuning capacitor must be used for proper operation.
11	BYPASS	Input	Pulldown	When HIGH bypasses PLL. When LOW, selects PLL. LVCMOS/LVTTL interface levels. See Table 3J.
12	REF_OE	Input	Pulldown	Active HIGH REF_OUT enables/disables pin. LVCMOS/LVTTL interface levels. See Table 3H.
13	nMR	Input	Pullup	Active LOW Master Reset. When logic LOW, the internal dividers are reset and the outputs are in high impedance (HI-Z). When logic HIGH, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels. See Table 3I.
16, 17	SSC1, SSC0	Input	Pullup	SSC control pin. LVCMOS/LVTTL interface levels. See Table 3D.
18, 19, 20	F_SELB2, F_SELB1, F_SELB0	Input	Pulldown	Frequency select pins for QBx outputs. See Table 3B. LVCMOS/LVTTL interface levels.
21, 22, 23	F_SELC2, F_SELC1, F_SELC0	Input	Pulldown	Frequency select pins for QC output. See Table 3C. LVCMOS/LVTTL interface levels.
24, 25	F_SELA1, F_SELA0	Input	Pulldown	Frequency select pins for QAx/nQAx outputs. See Table 3A. LVCMOS/LVTTL interface levels.
26	QA_OE	Input	Pullup	Output enable pin for Bank A outputs. See Table 3F. LVCMOS/LVTTL interface levels.
30, 31 32, 33	nQA1, QA1 nQA0, QA0	Output		Differential Bank A clock outputs. HCSL interface levels.
34	IREF	Output		External fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode QAx/nQAx clock outputs.
37, 38	V_{DDA}	Power		Analog supply pin.
39	QBC_OE	Input	Pullup	Output enable pin for Bank B and Bank C outputs. LVCMOS/LVTTL Interface levels. See Table 3G.
41	QC	Output		Single-ended Bank C clock output. LVCMOS/LVTTL interface levels. 18Ω typical output impedance.
42	V_{DDOC}	Power		Output supply pin for QC LVCMOS output.
43, 48, 52, 56	V_{DDOB}	Power		Output supply pins for QBx LVCMOS outputs.
44, 45, 47, 49, 51, 53, 55	QB0, QB1, QB2, QB3, QB4, QB5, QB6	Output		Single-ended Bank B clock outputs. LVCMOS/LVTTL interface levels. 18Ω typical output impedance.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				4		pF
C_{PD}	Power Dissipation Capacitance	QB[0:6], QC	V_{DD}, V_{DD_REFOUT}, V_{DDOB}, V_{DDOC} = 3.465V		19		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	QB[0:6], QC			18		Ω
		REF_OUT[1:0]			23		Ω

TABLE 3A. F_SELA FREQUENCY SELECT FUNCTION TABLE

Inputs				Output Frequency (25MHz Ref.)
F_SELA1	F_SELA0	M Divider Value	NA Divider Value	QA[0:1]/nQA[0:1] (MHz)
L	L	80	20	100 (default)
L	H	80	16	125
H	L	80	10	200
H	H	80	8	250

TABLE 3B. F_SELB FREQUENCY SELECT FUNCTION TABLE

Inputs					Output Frequency (25MHz Ref.)
F_SELB2	F_SELB1	F_SELB0	M Divider Value	NB Divider Value	QB[0:6] (MHz)
L	L	L	80	60	33.33 (default)
L	L	H	80	40	50
L	H	L	80	30	66.67
L	H	H	80	20	100
H	L	L	80	16	125
H	L	H	80	15	133.33
H	H	L	80	12	166.67
H	H	H	80	10	200

TABLE 3C. F_SELC FREQUENCY SELECT FUNCTION TABLE

Inputs					Output Frequency (25MHz Ref.)
F_SELC2	F_SELC1	F_SELC0	M Divider Value	NC Divider Value	QC (MHz)
L	L	L	80	60	33.33 (default)
L	L	H	80	40	50
L	H	L	80	30	66.67
L	H	H	80	20	100
H	L	L	80	16	125
H	L	H	80	15	133.33
H	H	L	80	12	166.67
H	H	H	80	10	200

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TABLE 3D. SSC FUNCTION TABLE

Input		
SSC1	SSC0	Mode
0	0	0 to -0.5% Down-spread
0	1	±0.25% Center-spread
1	0	±0.25% Center-spread
1	1	SSC Off (default)

TABLE 3E. REF_SEL FUNCTION TABLE

Input	
REF_SEL	Input Reference
0	XTAL
1	REF_IN

TABLE 3F. QA_OE FUNCTION TABLE

Input	
QA_OE	Function
0	QA[0:1]/nQA[0:1] disabled (High-Impedance)
1(default)	QA[0:1]/nQA[0:1] enabled

TABLE 3G. QBC_OE FUNCTION TABLE

Input	
QBC_OE	Function
0	QB[0:6] and QC disabled (High-Impedance)
1 (default)	QB[0:6] and QC enabled

TABLE 3H. REF_OE FUNCTION TABLE

Input	
REF_OE	Function
0 (default)	REF_OUT[0:1] disabled (High-Impedance
1	REF_OUT[0:1] enabled

TABLE 3I. nMR FUNCTION TABLE

Input	
nMR	Function
0	Device reset, output divider disabled (High-Impedance)
1 (default)	Output enabled

NOTE: This device requires a reset signal after power-up to function properly.

TABLE 3J. BYPASS FUNCTION TABLE

Input	
BYPASS	Function
0 (default)	PLL
1	Bypass (reference ÷N)

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} 4.6V

Inputs, V_I .... -0.5V to V_{DD} + 0.5 V

Outputs, V_O .... -0.5V to V_{DDO} + 0.5V

Package Thermal Impedance, θ_{JA} ...... 31.4°C/W (0 mps)

Storage Temperature, T_{STG} ...... -65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DD\_REFOUT} = V_{DDOB} = V_{DDOC} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.20	3.3	V_{DD}	V
$V_{DDOB,}$ V_{DDOC}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	HCSL Loaded, LVCMOS No Load			300	mA
I_{DDA}	Analog Supply Current				20	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DD\_REFOUT} = V_{DDOB} = V_{DDOC} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	QA_OE, QBC_OE, nMR, SSC0, SSC1,	$V_{DD} = V_{IN} = 3.465V$			10	µA
		F_SELA[0:1], F_SELB[0:2]. F_SELC[0:2], REF_OE, BYPASS, REF_IN, REF_SEL	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	QA_OE, QBC_OE, nMR, SSC0, SSC1,	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
		F_SELA[0:1], F_SELB[0:2]. F_SELC[0:2], REF_OE, BYPASS, REF_IN, REF_SEL	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-10			µA
V_{OH}	Output High Voltage		$V_{DDOB,}$ $V_{DDOC} = I_{OH} = -2mA$	2.6			V
V_{OL}	Output Low Voltage		$V_{DDOB,}$ $V_{DDOC} = I_{OL} = 2mA$			0.5	V

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				100	µW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DD\_REFOUT} = V_{DDOB} = V_{DDOC} = 3.3V\pm5\%$, $T_A = -40°C$ TO $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QB[0:6]		33.33		200	MHz
		QA[0:1]/nQA[0:1]		100		250	MHz
		QC		33.33		200	MHz
tsk(b)	Bank Skew; NOTE 1, 2	QB[0:6]				50	ps
		QA[0:1]/nQA[0:1]				50	ps
tsk(o)	Output Skew; NOTE 1, 3		across Banks B and C (at Same Frequency)			160	ps
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 1	QA[0:1]/nQA[0:1]	All Outputs at Same Frequency			65	ps
tjit(per)	RMS Period Jitter	QA[0:1]/nQA[0:1]	REF_OE = 0, All Outputs at Same Frequency			10	ps
		QB[0:6]				20	ps
		QC				20	ps
F_M	SSC Modulation Frequency	Banks A, B, C		29		33.33	kHz
V_{HIGH}	Voltage High; NOTE 4, 5			580		1200	mV
V_{LOW}	Voltage Low; NOTE 4, 6			-150			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 4, 7, 8			200		600	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 4, 7, 9					200	mV
t_R / t_F	Output Rise/Fall Time	Bank A	±150mV from crosspoint	25		100	ps
		Banks B, C	20% - 80%	0.4		1.3	ns
odc	Output Duty Cycle	Bank A		45		55	%
		Banks B, C		42		58	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 2: Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDOB, C}/2$.

NOTE 4: Measurement taken from single-ended waveform.

NOTE 5: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 6: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 7: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx. See Parameter Measurement Information Section.

NOTE 8: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.

NOTE 9: Defined as the total variation of all crossing voltage of rising Qx and falling nQx. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.

PARAMETER MEASUREMENT INFORMATION
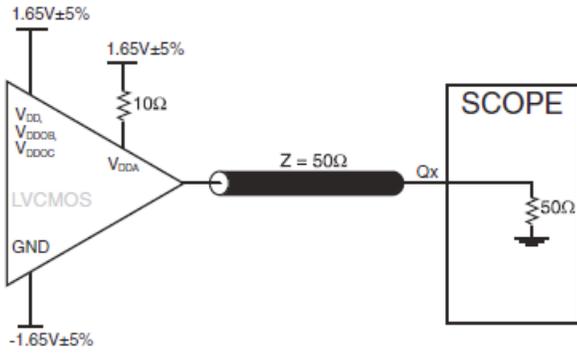

3.3V CORE/3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT

3.3V CORE/3.3V HCSL OUTPUT LOAD AC TEST CIRCUIT

1σ contains 68.26% of all measurements
2σ contains 95.4% of all measurements
3σ contains 99.73% of all measurements
4σ contains 99.99366% of all measurements
6σ contains (100-1.973x10⁻⁷)% of all measurements
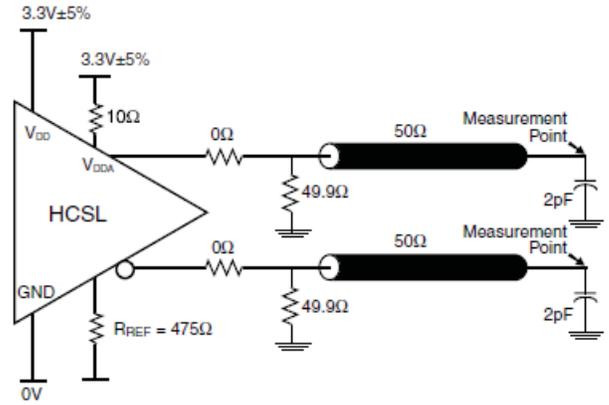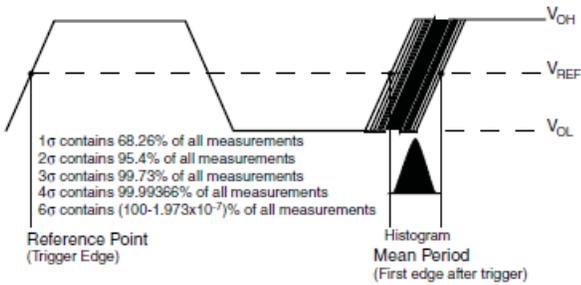
RMS PERIOD JITTER
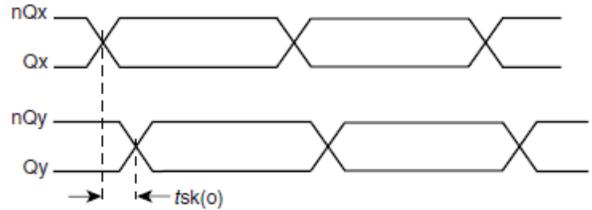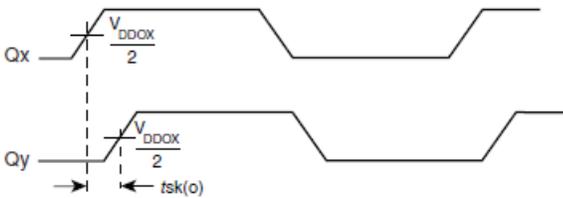
HCSL OUTPUT SKEW

LVCMOS OUTPUT SKEW
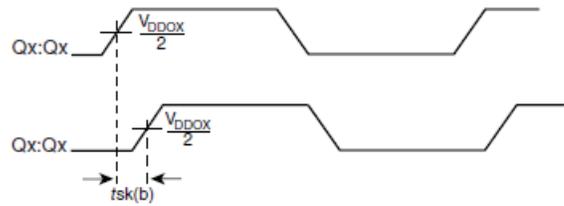
(where X = Bank B or Bank C)

LVCMOS BANK SKEW

Parameter Measurement Information, continued
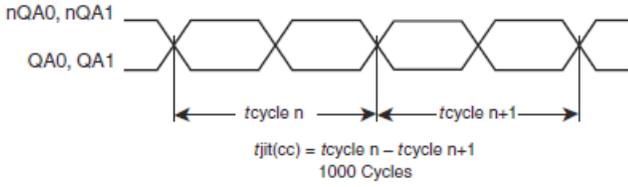
Differential Cycle-to-Cycle Jitter

nQA0, nQA1
QA0, QA1

tcycle n
tcycle n+1

$$tjit(cc) = tcycle\ n - tcycle\ n+1$$
1000 Cycles
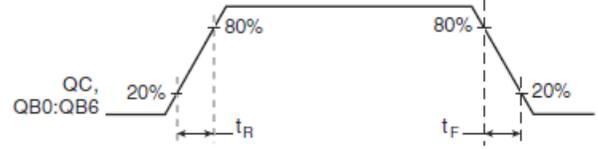
LVCMOS Rise/Fall Time

QC,
QB0:QB6

80%
20%
t_R

80%
20%
t_F
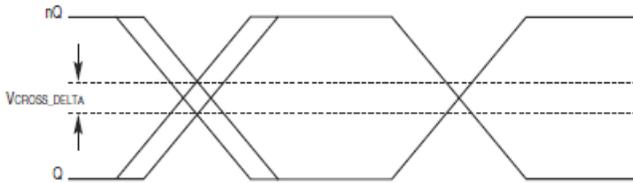
Single-Ended Measurement Points for Delta Cross Point

nQ

V_{CROSS_DELTA}

Q
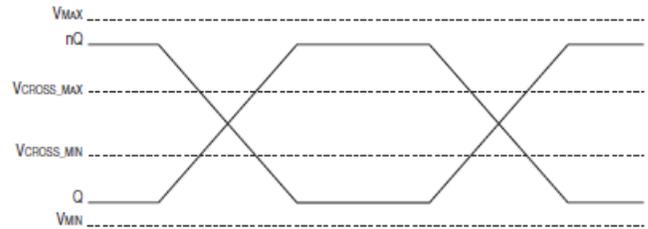
Single-Ended Measurement Points for Absolute Cross Point and Swing

V_{MAX}
nQ
V_{CROSS_MAX}
V_{CROSS_MIN}
Q
V_{MIN}
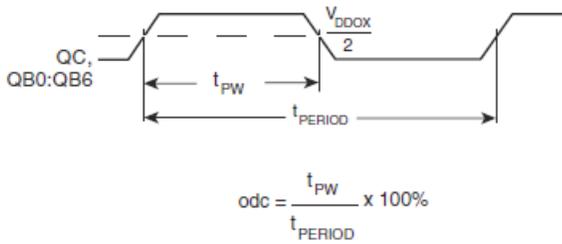
LVCMOS Output Duty Cycle/Pulse Width/Period

QC,
QB0:QB6

$\dfrac{V_{DDOX}}{2}$

t_{PW}
t_{PERIOD}

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$
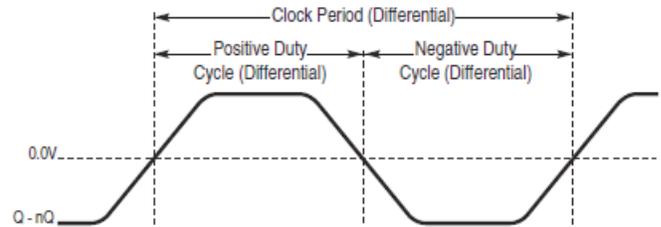
Differential Measurement Points for Duty Cycle/Period

Clock Period (Differential)
Positive Duty Cycle (Differential)
Negative Duty Cycle (Differential)
0.0V
Q - nQ
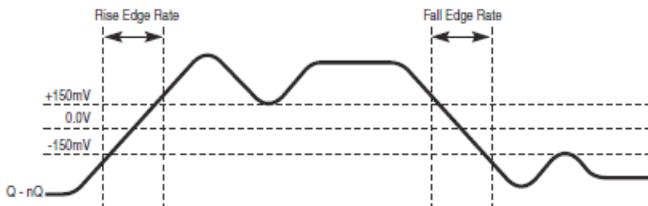
Differential Measurement Points for Rise/Fall Time

Rise Edge Rate
Fall Edge Rate
+150mV
0.0V
-150mV
Q - nQ

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APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 841S012DI provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, V_{DDOB}, and V_{DDOC} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.
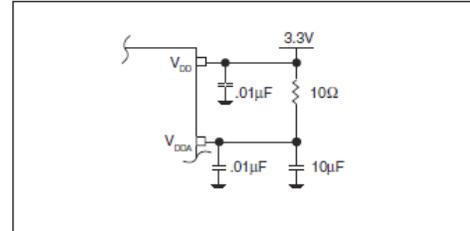
FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_IN INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_IN to ground.

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVCMOS OUTPUTS

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

DIFFERENTIAL OUTPUTS

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

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CRYSTAL INPUT INTERFACE

The 841S012DI has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. NOTE: External tuning capacitors must be used for proper operations.
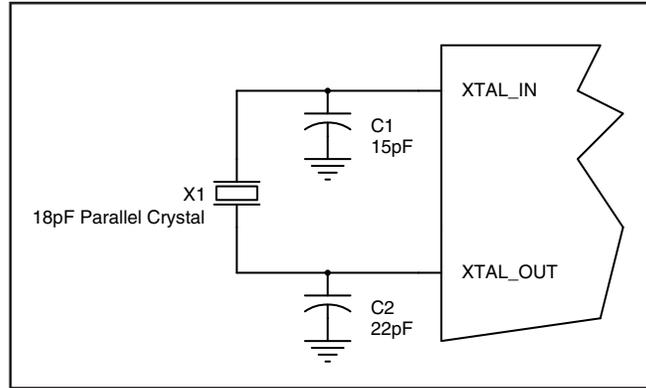

FIGURE 2. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note the device performance is guaranteed by using a quartz crystal.
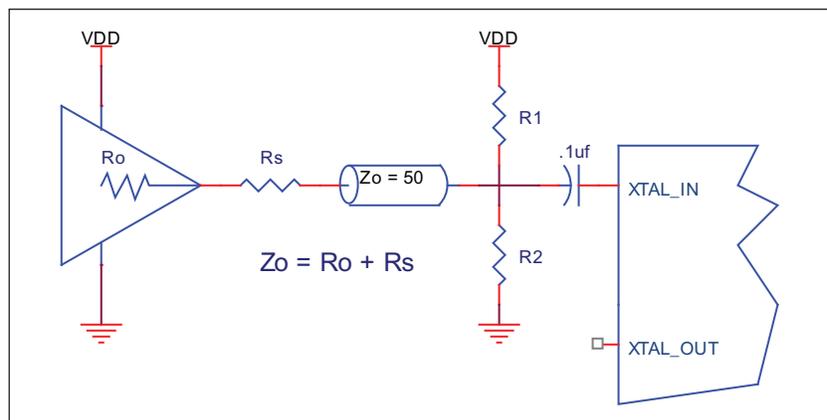
FIGURE 3. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

SPREAD SPECTRUM

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 32kHz triangle waveform is used with 0.6% down-spread (+0.0% / -0.5%) from the nominal output frequency. An example of a triangle frequency modulation profile is shown in *Figure 4A* below. The ramp profile can be expressed as:

Fnom = Nominal Clock Frequency in Spread OFF mode

Fm = Nominal Modulation Frequency (30kHz)

δ = Modulation Factor (0.6% down spread)

$(1 - δ)$ fnom $+ 2$ Fm x δ x Fnom x t when $0 < t < \dfrac{1}{2Fm}$

$(1 - δ)$ fnom $- 2$ Fm x δ x Fnom x t when $\dfrac{1}{2Fm} < t < \dfrac{1}{Fm}$

The 841S012DI triangle modulation frequency deviation will not exceed 0.7% down-spread from the nominal clock frequency (+0.0% / -0.5%). An example of the amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in *Figure 4B.* The ratio of this width to the fundamental frequency is typically 0.4%, and will not exceed 0.7%. The resulting spectral reduction will be greater than 5dB, as shown in *Figure 4B*. It is important to note the 841S012DI 5dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

FIGURE 4A. TRIANGLE FREQUENCY MODULATION
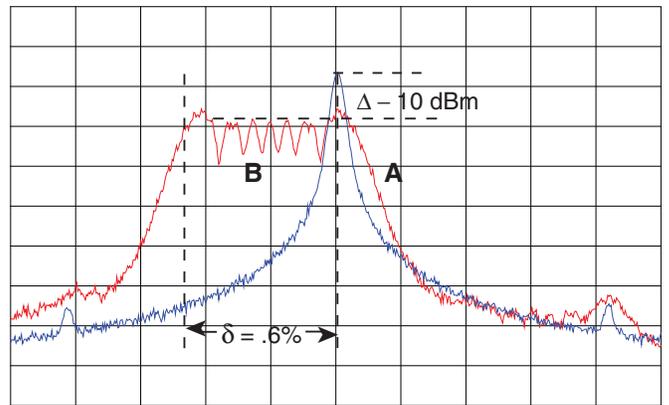
FIGURE 4B. 200MHZ CLOCK OUTPUT IN FREQUENCY DOMAIN
(A) SPREAD-SPECTRUM OFF (B) SPREAD-SPECTRUM ON

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VFQFN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.
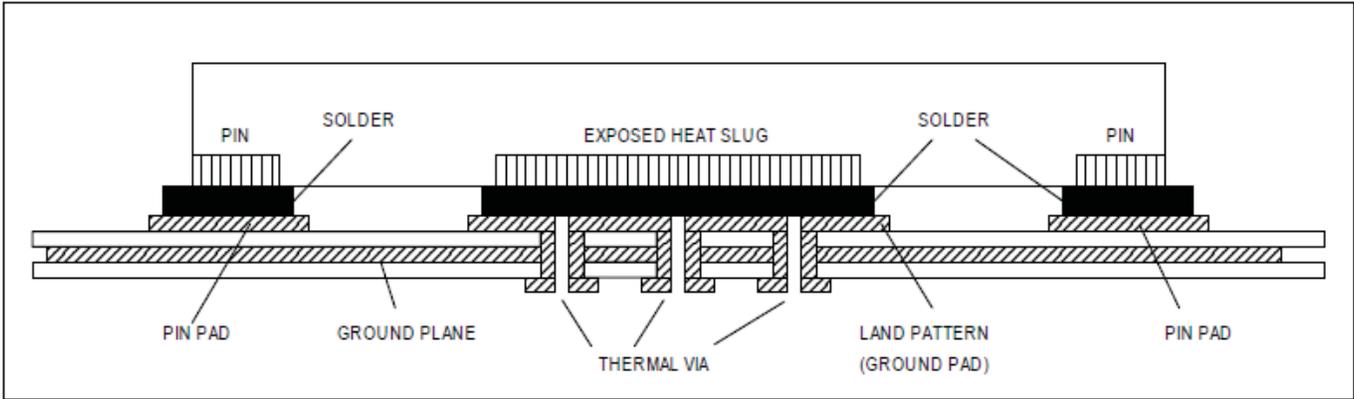

FIGURE 5. P.C. ASSEMBLY FOR EXPOSED PAD THERMAL RELEASE PATH –SIDE VIEW (DRAWING NOT TO SCALE)

RECOMMENDED TERMINATION

Figure 6A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.
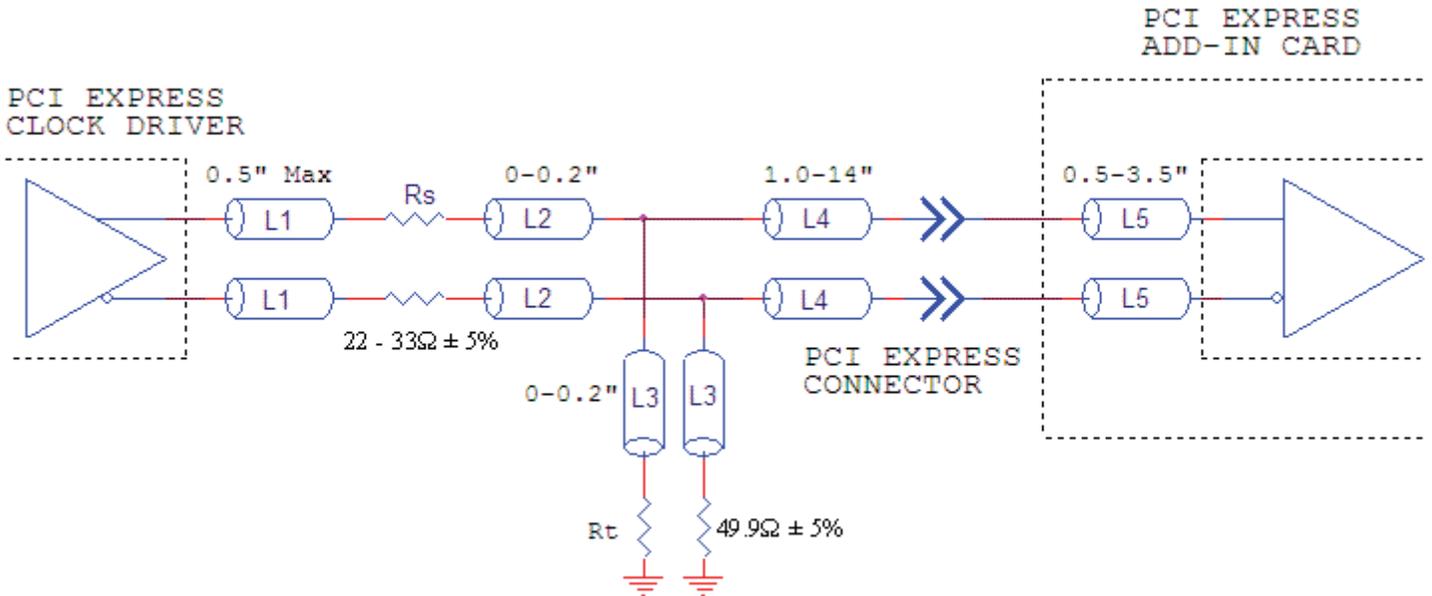

FIGURE 6A. RECOMMENDED TERMINATION

Figure 6B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.
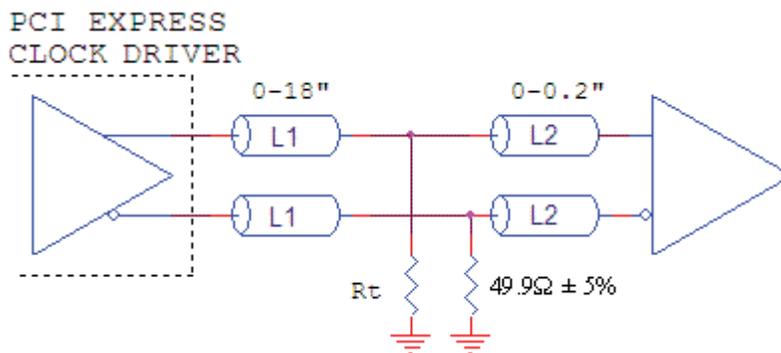

FIGURE 6B. RECOMMENDED TERMINATION

SCHEMATIC EXAMPLE

Figure 7 shows an example of the 841S012DI application schematic. In this example, the device is operated at $V_{DD} = V_{DDOB} = V_{DDOC} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The C1 = 33pF and C2 = 33pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of HCSL and one example of LVCMOS termination are shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.
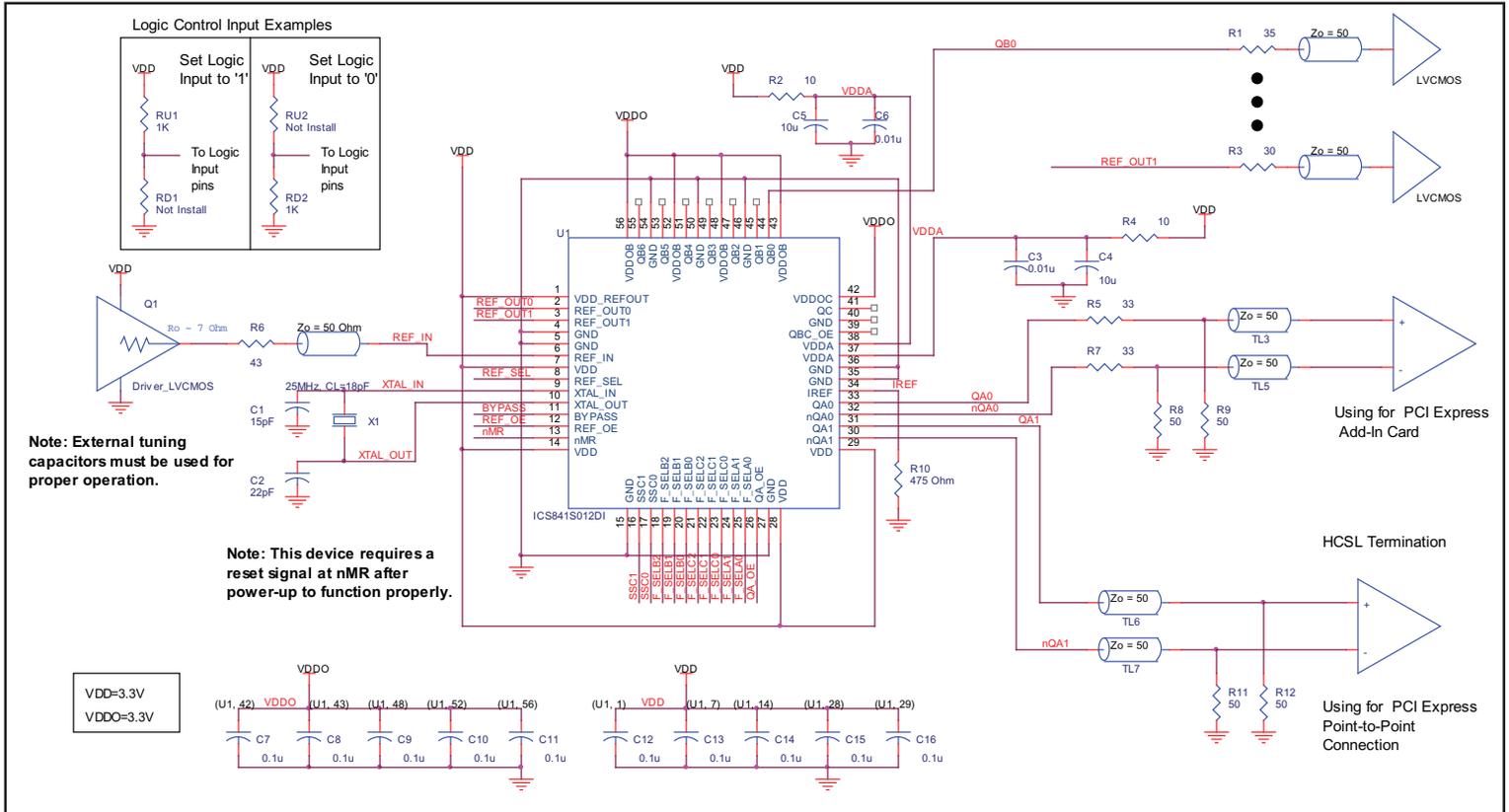
FIGURE 7. 841S012DI SCHEMATIC EXAMPLE

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POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 841S012DI. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 841S012DI is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Core and HCSL Output Power Dissipation
The maximum I_{DD} current at 85° is 284mA. The HCSL output current (17mA per output pair) is included in this value. For power considerations, this output current is treated separately from the core currents, so for power calculations,
I_{DD} = 284mA - 2 * 17mA = 250mA.

- Power (core) = V_{DD_MAX} * (I_{DD} + I_{DDA}) = 3.465V * (250mA + 20mA) = **935.6mW**
  Power (HCSL) = **44.5mW/Load Output Pair**
  If all outputs are loaded, the total power is 2 * 44.5mW = **89mW**

LVCMOS Output Power Dissipation
- Dynamic Power Dissipation at 200MHz, (QB, QC)
  Power (200MHz) = C_{PD} * Frequency * $(V_{DDO})^2$ = 19pF * 200MHz * $(3.465V)^2$ = **45mW per output**
  Total Power (200MHz) = **45mW * 8 = 360mW**

- Dynamic Power Dissipation at 25MHz, (REF_OUT)
  Power (25MHz) = C_{PD} * Frequency * $(V_{DDO})^2$ = 19pF * 25MHz * $(3.465V)^2$ = **5.6mW per output**
  Total Power (25MHz) = **5.6mW * 2 = 11.2mW**

Total Power Dissipation
- **Total Power**
  = Power (core) + Power (HCSL) + Total Power (200MHz) + Total Power (25MHz)
  = 935.6mW + 89mW + 360mW + 11mW
  = **1396mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming 1 meter per second air flow and a multi-layer board, the appropriate value is 27.5°C/W per Table 7.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
    85°C + 1.396W * 27.5°C/W = 123.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 56 LEAD VFQFN, FORCED CONVECTION

θ_{JA} by Velocity (Meters per second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	31.4°C/W	27.5°C/W	24.6°C/W

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3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 8.*
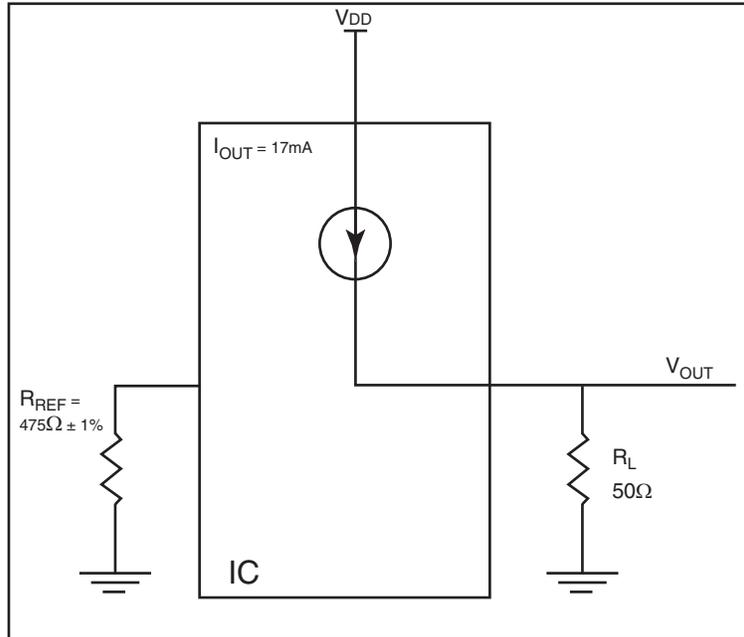
FIGURE 8. HCSL DRIVER CIRCUIT AND TERMINATION

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs at maximum V_{DD}.

Power $= (V_{DD\_MAX} - V_{OUT}) * I_{OUT,}$

since $V_{OUT} = I_{OUT} * R_L$

$= (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * 50Ω) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

RELIABILITY INFORMATION

TABLE 8. θ_{JA} VS. AIR FLOW TABLE FOR 56 LEAD VFQFN

θ_{JA} by Velocity (Meters per second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	31.4°C/W	27.5°C/W	24.6°C/W

TRANSISTOR COUNT

The transistor count for 841S012DI is: 11,537

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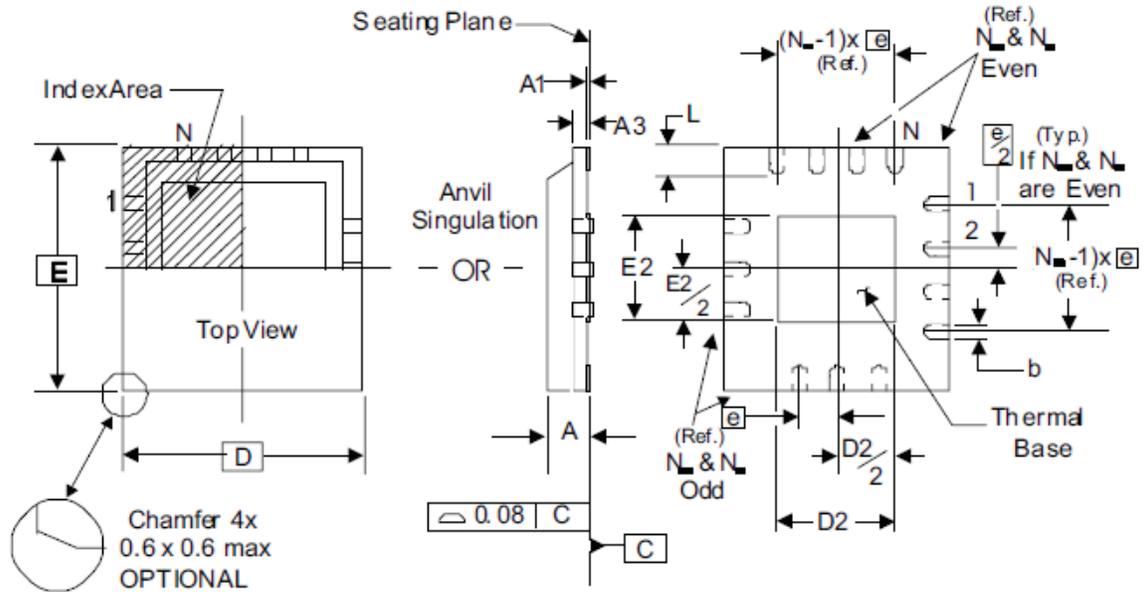
NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9 below.

TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	MINIMUM	MAXIMUM
N	56	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	14	
N_E	14	
D	8.0	
D2	4.35	4.65
E	8.0	
E2	5.05	5.35
L	0.3	0.55

Reference Document: JEDEC Publication 95, MO-220

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
841S012DKILF	ICS841S012DIL	56 lead "Lead-Free" VFQFN	tray	-40°C to 85°C
841S012DKILFT	ICS841S012DIL	56 lead "Lead-Free" VFQFN	tape & reel	-40°C to 85°C

REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
A		1	Removed ICS chip and Hiperclocks from the General Description. Removed ICS from the part number. Updated data sheet header and footer.	1/4/16

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