

## General Description

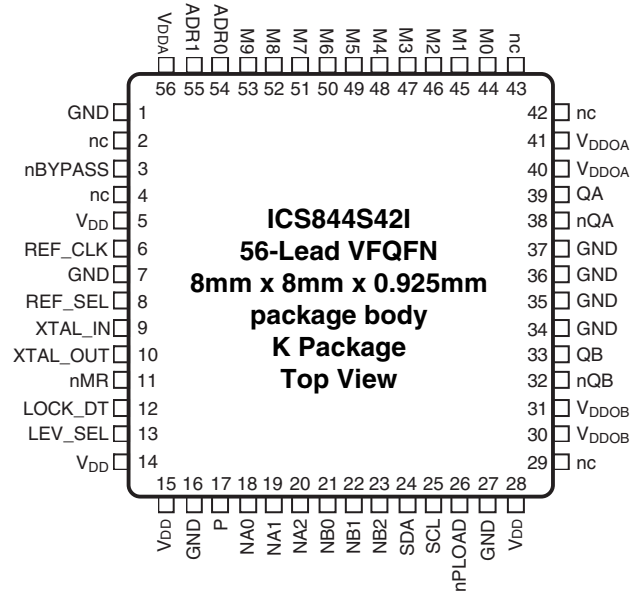
The 844S42I is a 3.3V compatible, PLL based clock synthesizer targeted for clock generation in high-performance instrumentation, networking and computing applications. Using either the serial (I<sup>2</sup>C) or parallel programming interface, the 844S42I enables the generation of clock frequencies in the range of 81MHz to 2592MHz. The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. Alternatively, a LVCMOS compatible clock signal can be used as PLL reference signal. The device uses an integer-N synthesizer architecture and is optimized for low-jitter generation. The VCO within the PLL operates over a range of 1296MHz to 2592MHz. Its output is scaled by a divider that is configured by either the I<sup>2</sup>C or parallel interfaces. The crystal oscillator frequency  $f_{XTAL}$ , the PLL pre-divider P, the feedback-divider M and the PLL post-divider N determine the output frequency. The feedback path of the PLL is internal.

The PLL post-dividers NA and NB are configured through either the I<sup>2</sup>C or the parallel interfaces, each can provide one of seven division ratios (1, 2, 3, 4, 6, 8, 16). This divider extends the performance of the part while providing a typical 50% duty cycle. The high-frequency outputs QA and QB are differential and are capable of driving a pair of transmission lines. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter. The serial interface is I<sup>2</sup>C compatible and provides read and write access to the internal PLL configuration registers. The lock state of the PLL is indicated by the LVCMOS-compatible LOCK\_DT output. The 844S42I is packaged in a 8mm x 8mm 56-lead VFQFN package.

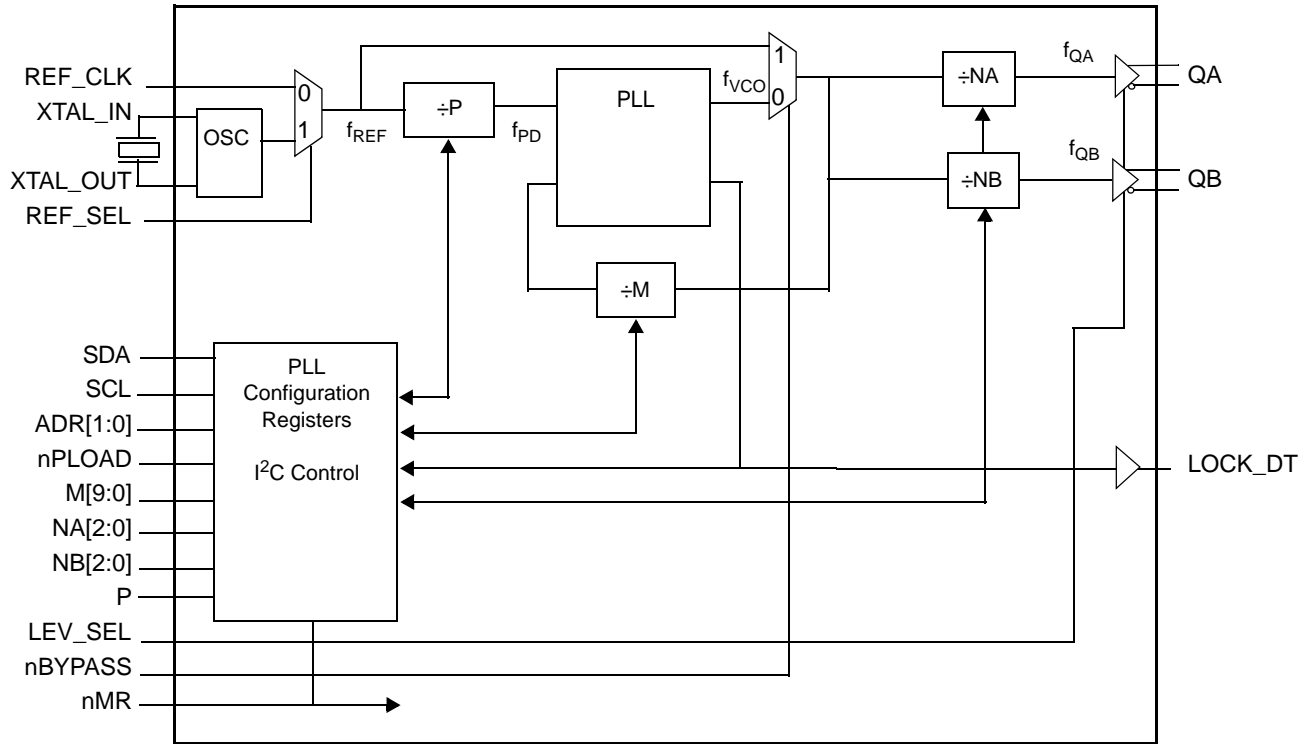
## Features

- Programmable frequency synthesis optimized for instrumentation, networking and computing applications
- 81MHz to 2592MHz synthesized clock output signal
- Two differential, universal LVDS or LVPECL compatible high-frequency outputs
- Output frequency programmable through 2-wire I<sup>2</sup>C bus or parallel interface
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS/LVTTL compatible reference clock input
- Clock stop and output enable functionality
- PLL lock indicator output (LVCMOS/LVTTL)
- LVCMOS/LVTTL compatible control inputs
- Fully integrated PLL
- SiGe Technology
- Full 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in a lead-free (RoHS 6) compliant package

## Pin Assignment



## Block Diagram



**Table 1. Pin Descriptions**

| Number                       | Name                | Type   |          | Description  |
|------------------------------|---------------------|--------|----------|--|
| 1, 7, 16, 27, 34, 35, 36, 37 | GND                 | Power  |          | Power supply ground.   |
| 2, 4, 29, 42, 43             | nc                  | Unused |          | Do not connect.  |
| 3                            | nBYPASS             | Input  | Pulldown | PLL bypass. LVCMOS/LVTTL interface levels.   |
| 5, 14, 15, 28                | V <sub>DD</sub>     | Power  |          | Digital power supply pins.   |
| 6                            | REF_CLK             | Input  | Pulldown | Single-ended reference clock input. LVCMOS/LVTTL interface levels.   |
| 8                            | REF_SEL             | Input  | Pullup   | Reference select pin. LVCMOS/LVTTL interface levels.   |
| 9, 10                        | XTAL_IN<br>XTAL_OUT |        |          | Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.                                    |
| 11                           | nMR                 | Input  | Pullup   | Master reset. nMR resets the I <sup>2</sup> C, output dividers and the LOCK_DT. LVCMOS/LVTTL interface levels. |
| 12                           | LOCK_DT             | Output |          | Lock detect output. LVCMOS/LVTTL interface levels.   |
| 13                           | LEV_SEL             | Input  | Pulldown | Output level select (LVDS and LVPECL). LVCMOS/LVTTL interface levels.  |
| 17                           | P                   | Input  | Pullup   | Parallel configuration of PLL pre-divider. LVCMOS/LVTTL interface levels.                                      |
| 18, 19, 20                   | NA0, NA1, NA2       | Input  | Pulldown | Parallel configuration of QA output dividers. LVCMOS/LVTTL interface levels.                                   |
| 21, 22, 23                   | NB0, NB1, NB2       | Input  | Pulldown | Parallel configuration of QB output dividers. LVCMOS/LVTTL interface levels.                                   |
| 24                           | SDA                 | I/O    | Pullup   | I <sup>2</sup> C data input/output pin. LVCMOS/LVTTL interface levels.   |
| 25                           | SCL                 | I/O    | Pullup   | I <sup>2</sup> C clock. LVCMOS/LVTTL interface levels.   |
| 26                           | nPLOAD              | Input  | Pulldown | Selects the programming interface. LVCMOS/LVTTL interface levels.  |
| 30, 31                       | V <sub>DDOB</sub>   | Power  |          | Bank B output power supply pins.   |
| 32, 33                       | nQB, QB             | Output |          | QB differential clock output pair. LVPECL or LVDS interface levels.  |
| 38, 39                       | nQA, QA             | Output |          | QA differential clock output pair. LVPECL or LVDS interface levels.  |
| 40, 41                       | V <sub>DDOA</sub>   | Power  |          | Bank A output power supply pins.   |
| 44, 48, 49, 50, 53           | M0, M4, M5, M6, M9  | Input  | Pullup   | Parallel configuration of PLL feedback dividers. LVCMOS/LVTTL interface levels.                                |
| 45, 46, 47, 51, 52           | M1, M2, M3, M7, M8  | Input  | Pulldown |  |
| 54, 55                       | ADR0, ADR1          | Input  | Pulldown | Bits 2 and 1 of the device I <sup>2</sup> C address. LVCMOS/LVTTL interface levels.                            |
| 56                           | V <sub>DDA</sub>    | Power  |          | Internal PLL power supply pin.   |

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

| Symbol                | Parameter               | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------|-----------------|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance       |                 |         | 2       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   |                 |         | 51      |         | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor |                 |         | 51      |         | kΩ    |
| R <sub>OUT</sub>      | Output Impedance        | LOCK_DT         |         | 20      |         | Ω     |

## Functional Description

The 844S42I is a programmable high-frequency clock source (clock synthesizer). The internal PLL generates a high frequency output signal based on a low-frequency reference signal. The frequency of the output signal is programmable and can be changed on the fly for frequency margining purpose. The internal crystal oscillator uses the parallel-resonance external quartz crystal as the basis of its frequency reference. Alternatively, an LVCMOS compatible clock signal can be used as a PLL reference signal. The frequency of the internal crystal oscillator is divided by a selectable divider and then multiplied by the PLL. The internal oscillator within the PLL operates over a range of 1296 MHz to 2592 MHz. Its output is scaled by two independent dividers that are configured by either the I<sup>2</sup>C or parallel interfaces. The crystal oscillator frequency  $f_{XTAL}$ , the PLL pre-divider P, the feedback-divider M, and the PLL post-dividers NA, NB determine the output frequency. The feedback path of the PLL is internal.

The PLL post-dividers NA and NB are configured through either the I<sup>2</sup>C or the parallel interfaces, and each can provide one of seven division ratios (1, 2, 3, 4, 6, 8, 16) and can stop the output clock in a logic low state. The divider extends the performance of the part while providing a typical 50% duty cycle. The high-frequency outputs, QA and QB, are differential and are capable of driving a pair of transmission lines. The differential outputs are configured as LVDS or LVPECL by the control input LEV\_SEL. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: I<sup>2</sup>C and parallel. The parallel interface uses the values at the M[9:0], NA[2:0], NB[2:0] and P parallel inputs to configure the internal PLL dividers. The parallel programming interface has priority over the serial I<sup>2</sup>C interface. The serial interface is I<sup>2</sup>C compatible and provides read and write access to the internal PLL configuration registers. The lock state of the PLL is indicated by the LVCMOS-compatible LOCK\_DT output.

## Device Configuration

The ICS844S42I supports an output frequency range of 81MHz to 2592MHz. The output frequency  $f_{OUT}$  is a function of the reference frequency  $f_{REF}$  and the three internal PLL dividers P, M, and N.  $f_{OUT}$  can be represented by this formula:

$$f_{OUT} = (f_{REF} \div P) \cdot M \div (NA, NB)$$

The M, N and P dividers require a configuration by the user to achieve the desired output frequency. The output dividers NA, NB determine the achievable output frequency range (see Table 3A). The PLL feedback-divider M is the frequency multiplication factor and the main variable for frequency synthesis. For a given reference frequency  $f_{REF}$ , the PLL feedback-divider M must be configured to match the specified VCO frequency range in order to achieve a valid PLL configuration:

$$f_{VCO} = (f_{REF} \div P) \cdot M \text{ and } 1296\text{MHz} \leq f_{VCO} \leq 2592\text{MHz}$$

The output frequency may be changed at any time by changing the value of the PLL feedback divider M. The smallest possible output frequency change is the synthesizer granularity G (difference in  $f_{OUT}$  when incrementing or decrementing M). At a given reference frequency, G is a function of the PLL pre-divider P and post-divider N:

$$G = f_{REF} \div (P \cdot NA, NB)$$

The purpose of the PLL pre-divider P is to situate the PLL into the specified VCO frequency range  $f_{VCO}$  (in combination with M). For a given output frequency,  $P = \div 4$  results in a smaller output frequency granularity G,  $P = \div 2$  results in a larger output frequency granularity G and also decreases the PLL bandwidth compared to the  $P = \div 4$  setting. The following example illustrates the output frequency range of the 844S42I using a 16MHz reference frequency.

**Table 3A. Device Configuration Table for  $f_{REF} = 16\text{MHz}$**

| Output Frequency (MHz) | NA, NB | M         | P | G (MHz) |
|------------------------|--------|-----------|---|---------|
| 1296 – 2592            | 1      | 324 – 648 | 4 | 4       |
|                        |        | 162 – 324 | 2 | 8       |
| 648 – 1296             | 2      | 324 – 648 | 4 | 2       |
|                        |        | 162 – 324 | 2 | 4       |
| 432 – 864              | 3      | 324 – 648 | 4 | 1.33    |
|                        |        | 162 – 324 | 2 | 2.66    |
| 324 – 648              | 4      | 324 – 648 | 4 | 1       |
|                        |        | 162 – 324 | 2 | 2       |
| 216 – 432              | 6      | 324 – 648 | 4 | 0.66    |
|                        |        | 162 – 324 | 2 | 1.33    |
| 162 – 324              | 8      | 324 – 648 | 4 | 0.5     |
|                        |        | 162 – 324 | 2 | 1       |
| 81 – 162               | 16     | 324 – 648 | 4 | 0.25    |
|                        |        | 162 – 324 | 2 | 0.5     |

## Example Output Frequency Configuration

If a single reference frequency of 16MHz is available, an output frequency at QA of 2500MHz and a small frequency granularity is desired, the following steps would be taken to identify the appropriate P, M, and N configuration:

1. Use Table 3A to select the output divider, NA, that matches the desired output frequency or frequency range. According to Table 3A a target output frequency of 2500MHz falls in the  $f_{OUT}$  range of 1296MHz to 2592MHz and requires to set NA = 1.
2. Calculate the VCO frequency  $f_{VCO} = f_{OUT} \cdot NA$ , which is 2500MHz in this example.
3. Determine the PLL feedback divider:  $M = f_{VCO} \div P$ . The smallest possible output granularity in this example calculation is 4MHz (set P = 4). M calculates to a value of  $2500MHz \div 4 = 625MHz$ .

4. Configure the 844S421 with the obtained settings:

- M[9:0] = 1001110001b (binary number for M = 625)
- NA[2:0] = 000 ( $\div 1$  divider, see Table 3C)
- P = 1 ( $\div 4$  divider, see Table 3B)
- NB[2:0] = 111 will stop (disable) the QB output

5. Use either parallel or serial interface to apply the setting.

The I<sup>2</sup>C configuration byte for this examples are:

0x00 = 01110001b, 0x01 = 10111000b and 0x02 = 10000000b. See Table 3H for a register map.

## PLL Divider Configuration

Table 3B. Pre-Divider (P) Table

| P           | Pre-Divider P | Operation                 |
|-------------|---------------|---------------------------|
| 0           | 2             | $f_{PD} = f_{REF} \div 2$ |
| 1 (default) | 4             | $f_{PD} = f_{REF} \div 4$ |

Table 3C. Post-Divider (Nx) Table

| NA, NB      |             |             | Post-Divider<br>NA, NB | Operation                          |
|-------------|-------------|-------------|------------------------|------------------------------------|
| 2           | 1           | 0           |                        |                                    |
| 0 (default) | 0 (default) | 0 (default) | 1                      | $f_{QA}, f_{QB} = f_{VCO} \div 1$  |
| 0           | 0           | 1           | 2                      | $f_{QA}, f_{QB} = f_{VCO} \div 2$  |
| 0           | 1           | 0           | 3                      | $f_{QA}, f_{QB} = f_{VCO} \div 3$  |
| 0           | 1           | 1           | 6                      | $f_{QA}, f_{QB} = f_{VCO} \div 6$  |
| 1           | 0           | 0           | 4                      | $f_{QA}, f_{QB} = f_{VCO} \div 4$  |
| 1           | 0           | 1           | 8                      | $f_{QA}, f_{QB} = f_{VCO} \div 8$  |
| 1           | 1           | 0           | 16                     | $f_{QA}, f_{QB} = f_{VCO} \div 16$ |
| 1           | 1           | 1           | N/A                    | Output stopped in logic low state  |

## Programming the 844S42I

The 844S42I has a parallel and a serial configuration interface. The purpose of the parallel interface is to directly configure the PLL dividers through hardware pins without the overhead of a serial protocol. At device startup, the device always obtains an initial PLL frequency configuration through the parallel interface. The parallel interface does not support reading the PLL configuration. The serial interface is I<sup>2</sup>C compatible. It allows reading and writing device settings by accessing internal device registers. The serial interface is designed for host-controller access to the synthesizer frequency settings, for instance, in frequency-margining applications.

### Using the Parallel Interface

The parallel interface supports write-access to the PLL frequency setting directly through 17 configuration pins (P, M[9:0], NA[2:0], and NB[2:0]). The parallel interface must be enabled by setting nPLOAD

to logic low level. During nPLOAD = 0, any change of the logical state of the P, M[9:0], NA[2:0] and NB[2:0] pins will immediately affect the internal PLL divider settings, resulting in a change of the internal VCO frequency and the output frequency. The parallel interface mode disables the I<sup>2</sup>C write-access to the internal registers; however, I<sup>2</sup>C read-access to the internal configuration registers is enabled. Upon startup, when the device reset signal is released (rising edge of the nMR signal), the device reads its startup configuration through the parallel interface and independent of the state of nPLOAD. It is recommended to provide a valid PLL configuration for startup. If the parallel interface pins are left open, a default PLL configuration will be loaded. After the low-to-high transition of nPLOAD, the configuration pins have no more effect and the configuration registers are made accessible through the serial interface.

**Table 3D. PLL Feedback Divider (M) Configuration Table**

| M Bits  | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|---------|----|----|----|----|----|----|----|----|----|----|
| Pin     | M9 | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |
| Default | 1  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 0  | 1  |

**Table 3E. PLL Post-Divider (NA) Configuration Table**

| NA Bits | 2   | 1   | 0   |
|---------|-----|-----|-----|
| Pin     | NA2 | NA1 | NA0 |
| Default | 0   | 0   | 0   |

**Table 3F. PLL Post-Divider (NB) Configuration Table**

| NB Bits | 2   | 1   | 0   |
|---------|-----|-----|-----|
| Pin     | NB2 | NB1 | NB0 |
| Default | 0   | 0   | 0   |

**Table 3G. PLL Pre-Divider (P) Configuration Table**

| P       |   |
|---------|---|
| Pin     | P |
| Default | 1 |

## Using the I<sup>2</sup>C Interface

nPLOAD = 1 enables the programming and monitoring of the internal registers through the I<sup>2</sup>C interface. Device register access (write and read) is possible through the 2-wire interface using SDA (configuration data) and SCL (configuration clock) signals. The 844S42I acts as a slave device at the I<sup>2</sup>C bus. For further information on I<sup>2</sup>C it is recommended to refer to the I<sup>2</sup>C bus specification (version 2.1).

nPLOAD = 0 disables the I<sup>2</sup>C-write-access to the configuration registers and any data written into the register is ignored. However,

the 844S42I is still visible at the I<sup>2</sup>C interface and I<sup>2</sup>C transfers are acknowledged by the device. Read-access to the internal registers during nPLOAD = 0 (parallel programming mode) is supported. Note that the device automatically obtains a configuration using the parallel interface upon the release of the device reset (rising edge of nMR) and independent on the state of nPLOAD. Changing the state of the nPLOAD input is not supported when the device performs any transactions on the I<sup>2</sup>C interface.

## Programming Model and Register Set

The synthesizer contains three fully accessible configuration registers (0x00 through 0x02). Programming the synthesizer frequency through the I<sup>2</sup>C interface is a one step process at which all registers are written at once by a single I<sup>2</sup>C transaction. The PLL frequency is affected as a result of the completion of the entire three register file write access at the end of writing byte 0x02. The configuration registers are read as a single I<sup>2</sup>C transaction. All registers are read back-to-back. Note that the synthesizer does not check any boundary conditions such as the VCO frequency range. Writing the PLL registers could result in invalid VCO frequencies (VCO frequency beyond lock range).

### Register Map

It is always required to configure the entire 844S42I register file (0x00, 0x01, 0x02), addressing single register bytes is not supported. Writing any information to the bits 2, 1 and 0 in register 0x02 is ignored. These bits indicate information updated by the synthesizer (bit 2 is the PLL lock status, bits 1 and 0 are copies of the ADR[1:0] pin status).

**Table 3H. Register File Table**

| Register Address | 7  | 6   | 5   | 4   | 3   | 2    | 1    | 0    | Access |
|------------------|----|-----|-----|-----|-----|------|------|------|--------|
| 0x00H            | M7 | M6  | M5  | M4  | M3  | M2   | M1   | M0   | R/W    |
| Default          | 0  | 1   | 1   | 1   | 0   | 0    | 0    | 1    |        |
| 0x01H            | M9 | M8  | NA2 | NA1 | NA0 | NB2  | NB1  | NB0  | R/W    |
| Default          | 1  | 0   | 0   | 0   | 0   | 0    | 0    | 0    |        |
| 0x02H            | P  | RES | RES | RES | RES | LOCK | ADR1 | ADR0 | R/W    |
| Default          | 1  | 0   | 0   | 0   | 0   | 0    | 0    | 0    |        |

## I<sup>2</sup>C Register Access in Parallel Mode

The 844S42I supports the configuration of the synthesizer through the parallel interface (nPLOAD = 0) and serial interface (nPLOAD = 1). Register contents and the divider configurations are not changed when the user switches from parallel mode to serial mode. However, when switching from serial mode to parallel mode, the PLL dividers immediately reflect the logical state of the hardware pins M[9:0], NA[2:0], NB[2:0], and P. Applications using the parallel interface to obtain a PLL configuration can use the serial interface to verify the

divider settings. In parallel mode (nPLOAD = 0), the 844S42I allows read-access to the registers through I<sup>2</sup>C (if nPLOAD = 0), the current PLL configuration is stored in the registers. After changing from parallel to serial mode (nPLOAD = 1), the last PLL configuration is still stored in the registers. The user now has full write and read access to both configuration registers through the I<sup>2</sup>C bus and can change the configuration at any time.



## Programming the I<sup>2</sup>C Interface

**Table 3I. I<sup>2</sup>C Slave Address Table**

| Bit   | 7 | 6 | 5 | 4 | 3 | 2    | 1    | 0   |
|-------|---|---|---|---|---|------|------|-----|
| Value | 1 | 0 | 1 | 1 | 0 | ADR1 | ADR0 | R/W |

The 844S42I acts as a slave device at the I<sup>2</sup>C bus. The register file is reset to its default values at power-up by an integrated power-on reset circuit or by applying an external device reset signal (nMR). The 7-bit I<sup>2</sup>C slave address of the 844S42I synthesizer is a combination of a 5-bit fixed addresses and two variable bits which are set by the hardware pins ADR[1:0]. Bit 0 of the 844S42I slave address is used by the bus controller to select either the read or write mode. '0' indicates a transmission (I<sup>2</sup>C-WRITE) to the 844S42I. "1" indicates a request for data (I<sup>2</sup>C-READ) from the synthesizer. The hardware pins ADR1 and ADR0 and should be individually set by the user to avoid address conflicts of multiple 844S42I devices on the same I<sup>2</sup>C bus.

Each access to the I<sup>2</sup>C register file must read or write the entire four register bytes at one time. Each transfer starts with register 0x00H, followed by register 0x01H, until register 0x02H. Addressing individual bytes is not supported. The bytes will program internal part circuitry upon receipt of all three bytes and a given I<sup>2</sup>C bus <STOP> signal.

### Device Startup

General Device Configuration: It is recommended to reset the 844S42I after the system powers up. The device acquires an initial PLL divider configuration through the parallel interface pins M[9:0], NA[2:0], NB[2:0] and P<sup>NOTE1</sup> with the low-to-high transition of nMR<sup>NOTE2</sup>. PLL frequency lock is achieved within the specified lock time (t<sub>LOCK</sub>) and is indicated by an assertion of the LOCK\_DT signal which completes the startup procedure. The output frequency can be reconfigured at any time through either the parallel or the serial interface.

### Starting-Up Using the Parallel Interface

The simplest way to use the 844S42I is through the parallel interface. The serial interface pins (SDA, SDL, and ADR[1:0]) can be left open and nPLOAD is set to logic low. After the release of nMR and at any other time the PLL and output frequency configuration is directly set to through the M[9:0], NA[2:0], NB[2:0] and P pins.

**Table 3J. REF\_SEL Configuration Table**

| REF_SEL     | Operation  |
|-------------|--|
| 0           | Selects REF_CLK input as reference frequency input |
| 1 (default) | Selects the XTAL interface as reference frequency  |

NOTE 1: The parallel interface pins M[9:0], NA[2:0], NB[2:0] and P may be left open (floating). In this case the initial PLL configuration will have the default setting of M = 625MHz, P = 1 (÷4), NA[2:0] = 000 (÷1), NB[2:0] = 000 (÷1), resulting in an internal VCO frequency of 2500MHz (f<sub>REF</sub> = 16MHz) and an output frequency of 2500MHz at both outputs.

NOTE 2: The initial PLL configuration is independent on the selected programming mode (nPLOAD low or high).

**Table 3K. nBYPASS Configuration Table**

| nBYPASS     | Operation  |
|-------------|--|
| 0 (default) | f <sub>QA</sub> , f <sub>QB</sub> = ((f <sub>REF</sub> ÷ P) * M) ÷ NA, NB<br>PLL operation                       |
| 1           | f <sub>QA</sub> , f <sub>QB</sub> = f <sub>REF</sub> ÷ NA, NB<br>PLL is bypassed, AC specifications do not apply |

The nBYPASS control should be set to logic LOW for normal operation. nBYPASS = 1 enables the PLL bypass mode for factory test. In PLL bypass mode, the output frequency is equal to the input frequency divided by NA, NB and frequency multiplication is disabled.

**Table 3L. nMR Configuration Table**

| nMR         | Operation  |
|-------------|--|
| 0           | The device is reset and the default settings are loaded into the I <sup>2</sup> C file (low to high transition of nMR) |
| 1 (default) | Normal operation   |

The output type and output voltage levels of both outputs are configured through the configuration input LEV\_SEL. LEV\_SEL connected to logic high results in LVPECL output levels and LEV\_SEL connected to logic low results in LVDS output levels of both QA and QB differential outputs.

**Table 3M. LEV\_SEL Configuration Table**

| LEV_SEL     | Operation                            |
|-------------|--------------------------------------|
| 0 (default) | QA, QB outputs are LVDS compatible   |
| 1           | QA, QB outputs are LVPECL compatible |

**Table 3N. LOCK\_DT Configuration Table**

| LOCK_DT | Operation   |
|---------|---|
| 0       | Device is not locked to the input reference clock |
| 1       | Device is locked to the input reference clock     |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item   | Rating                    |
|--|---------------------------|
| Supply Voltage, $V_{DD}$                                       | 4.6V                      |
| Inputs, $V_I$  | -0.5V to $V_{DD} + 0.5V$  |
| Outputs, $I_O$ (LVPECL)<br>Continuous Current<br>Surge Current | 50mA<br>100mA             |
| Outputs, $I_O$ (LVDS)<br>Continuous Current<br>Surge Current   | 10mA<br>15mA              |
| Outputs, $V_O$ (LVCMOS)  | -0.5V to $V_{DDO} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$                       | 31.4°C/W (0 mps)          |
| Storage Temperature, $T_{STG}$                                 | -65°C to 150°C            |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

| Symbol                     | Parameter             | Test Conditions | Minimum         | Typical | Maximum  | Units |
|----------------------------|-----------------------|-----------------|-----------------|---------|----------|-------|
| $V_{DD}$                   | Core Supply Voltage   |                 | 3.135           | 3.3     | 3.465    | V     |
| $V_{DDA}$                  | Analog Supply Voltage |                 | $V_{DD} - 0.23$ | 3.3     | $V_{DD}$ | V     |
| $V_{DDOA}$ ,<br>$V_{DDOB}$ | Output Supply Voltage |                 | 3.135           | 3.3     | 3.465    | V     |
| $I_{DD}$                   | Power Supply Current  | LEV_SEL = 0     |                 |         | 195      | mA    |
| $I_{DDA}$                  | Analog Supply Current | LEV_SEL = 0     |                 |         | 23       | mA    |
| $I_{DDOA} +$<br>$I_{DDOB}$ | Output Supply Current | LEV_SEL = 0     |                 |         | 52       | mA    |
| $I_{GND}$                  | Power Supply Current  | LEV_SEL = 1     |                 |         | 275      | mA    |

NOTE: Refer to the Power Considerations section. In LVDS output mode, the  $I_{DD}$ ,  $I_{DDA}$  and  $I_{DDO}$  specifications apply.  $I_{DDO}$  is the current through all  $V_{DDOA}$  and  $V_{DDOB}$  pins. In LVPECL mode, the  $I_{GND}$  specification applies.  $I_{GND}$  is the current through all GND pins.

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol   | Parameter           | Test Conditions   | Minimum                        | Typical | Maximum        | Units   |
|----------|---------------------|---|--------------------------------|---------|----------------|---------|
| $V_{IH}$ | Input High Voltage  |   | 2.2                            |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$ | Input Low Voltage   |   | -0.3                           |         | 0.8            | V       |
| $I_{IH}$ | Input High Current  | REF_CLK, nPLOAD, LEV_SEL, ADR[1:0], NA[0:2], NB[0:2], M1, M2, M3, M7, M8, nBYPASS | $V_{DD} = V_{IN} = 3.465V$     |         | 150            | $\mu A$ |
|          |                     | M0, M4, M5, M6, M9, P, nMR, SDA, SCL, REF_SEL                                     | $V_{DD} = V_{IN} = 3.465V$     |         | 10             | $\mu A$ |
| $I_{IL}$ | Input Low Current   | REF_CLK, nPLOAD, LEV_SEL, ADR[1:0], NA[0:2], NB[0:2], M1, M2, M3, M7, M8, nBYPASS | $V_{DD} = 3.465V, V_{IN} = 0V$ | -10     |                | $\mu A$ |
|          |                     | M0, M4, M5, M6, M9, P, nMR, SDA, SCL, REF_SEL                                     | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150    |                | $\mu A$ |
| $V_{OH}$ | Output High Voltage | LOCK_DT   | $I_{OH} = -12mA$               | 2.6     |                | V       |
| $V_{OL}$ | Output Low Voltage  | LOCK_DT   | $I_{OL} = 12mA$                |         | 0.5            | V       |

**Table 4C. LVDS DC Characteristics,  $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol          | Parameter                   | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------|-----------------|---------|---------|---------|-------|
| $V_{OD}$        | Differential Output Voltage | LEV_SEL = 0     | 300     | 400     | 500     | V     |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change   | LEV_SEL = 0     |         |         | 50      | mV    |
| $V_{OS}$        | Offset Voltage              | LEV_SEL = 0     | 1.1     | 1.2     | 1.3     | V     |
| $\Delta V_{OS}$ | $V_{OS}$ Magnitude Change   | LEV_SEL = 0     |         |         | 50      | mV    |

**Table 4D. LVPECL DC Characteristics,  $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

| Symbol      | Parameter                         | Test Conditions | Minimum          | Typical | Maximum          | Units |
|-------------|-----------------------------------|-----------------|------------------|---------|------------------|-------|
| $V_{OH}$    | Output High Voltage; NOTE 1       | LEV_SEL = 1     | $V_{DDOx} - 1.2$ |         | $V_{DDOx} - 0.8$ | V     |
| $V_{OL}$    | Output Low Voltage; NOTE 1        | LEV_SEL = 1     | $V_{DDOx} - 2.0$ |         | $V_{DDOx} - 1.4$ | V     |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | LEV_SEL = 1     | 0.6              |         | 1                | V     |

NOTE 1: Outputs termination with  $50\Omega$  to  $V_{DDOx} - 2V$ .

**Table 5. Crystal Characteristics**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 |             | 16      |         | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 50      | $\Omega$ |
| Shunt Capacitance                  |                 |             |         | 7       | pF       |

## AC Electrical Characteristics

**Table 6. AC Characteristics,  $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$** 

| Symbol         | Parameter                   | Test Conditions      | Minimum   | Typical | Maximum | Units  |
|----------------|-----------------------------|----------------------|---|---------|---------|--------|
| $f_{REF}$      | Input Reference Frequency   |                      |   | 16      |         | MHz    |
| $f_{VCO}$      | VCO frequency range         |                      | 1296  |         | 2592    | MHz    |
| $f_{OUT}$      | QA, QB Output frequency     | NA, NB = $\div 1$    | 1296  |         | 2592    | MHz    |
|                |                             | NA, NB = $\div 2$    | 648   |         | 1296    | MHz    |
|                |                             | NA, NB = $\div 3$    | 432   |         | 864     | MHz    |
|                |                             | NA, NB = $\div 4$    | 324   |         | 648     | MHz    |
|                |                             | NA, NB = $\div 6$    | 216   |         | 432     | MHz    |
|                |                             | NA, NB = $\div 8$    | 162   |         | 324     | MHz    |
|                |                             | NA, NB = $\div 16$   | 81  |         | 162     | MHz    |
| $tsk(o)$       | Output Skew<br>NOTE 1, 2, 3 | $f_{QA} = f_{QB}$    | NA, NB = $\div 1$   |         | 15      | ps     |
|                |                             |                      | NA, NB $\neq \div 1$  |         | 25      | ps     |
|                |                             | $f_{QA} \neq f_{QB}$ | across QA and QB at coincident edges, NA, NB = $\div 2$ or $\div 4$ |         | 80      | ps     |
|                |                             |                      | across QA and QB at coincident edges, NA, NB = $\div 4$ or $\div 8$ |         | 35      | ps     |
| $t_{jit(cc)}$  | Cycle-to-Cycle Jitter       | $f_{QA} = f_{QB}$    |   |         | 25      | ps     |
| $t_{jit(per)}$ | RMS Period Jitter           | $f_{QA} = f_{QB}$    | $f > 2\text{GHz}$   |         | 3.4     | ps rms |
|                |                             | $f_{QA} = f_{QB}$    | $f \leq 1\text{GHz}$  |         | 3.0     | ps rms |
|                |                             | $f_{QA} = f_{QB}$    | $1\text{GHz} < f \leq 2\text{GHz}$                                  |         | 2.5     | ps rms |
| $t_R / t_F$    | Output Rise/Fall Time       | LVDS, LVPECL         | 20% to 80%  | 60      | 220     | ps     |
| odc            | Output Duty Cycle           | QA, QB               | NA, NB = $\div 1$ , LEV_SEL = 0                                     | 45      | 55      | %      |
|                |                             |                      | NA, NB = $\div 1$ , LEV_SEL = 1                                     | 44      | 56      | %      |
|                |                             |                      | NA, NB = $\div 2$   | 46      | 54      | %      |
|                |                             |                      | NA, NB = $\div 3$   | 47      | 53      | %      |
|                |                             |                      | NA, NB = $\div 4, \div 6, \div 8, \div 16$                          | 48      | 52      | %      |

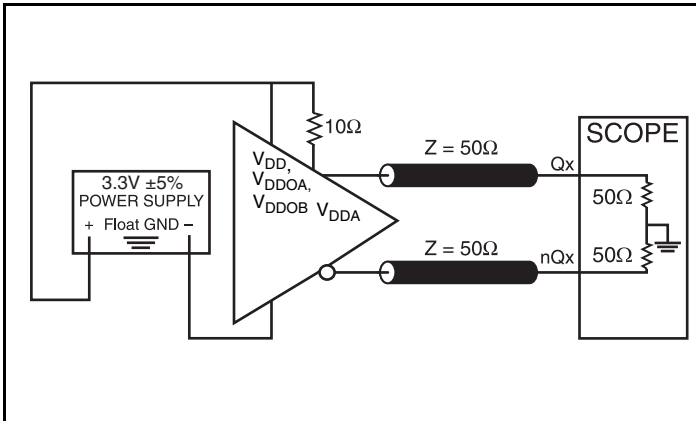
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Defined as skew between output at the same supply voltage and with equal load conditions. Measured from  $V_{DD}/2$  of the input to the differential crossing point.

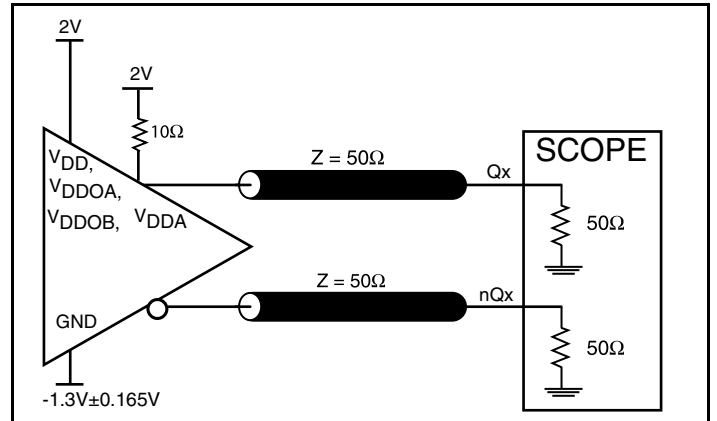
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Other output divider combinations may yield much greater output skews.

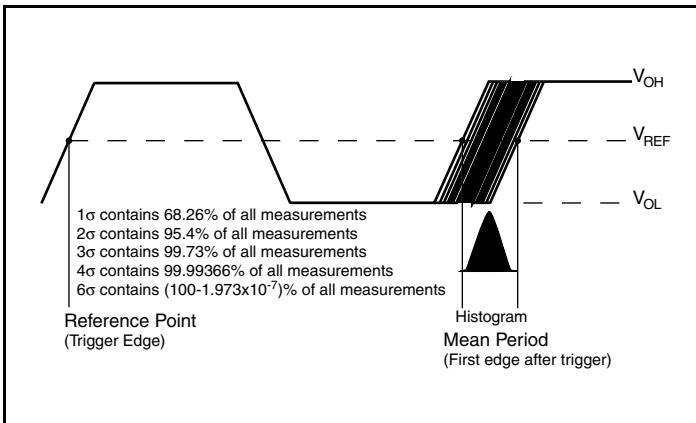
## Parameter Measurement Information



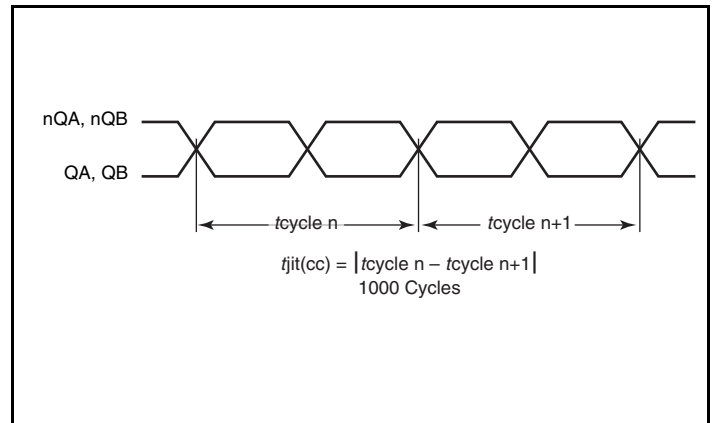
3.3V LVDS Output Load AC Test Circuit



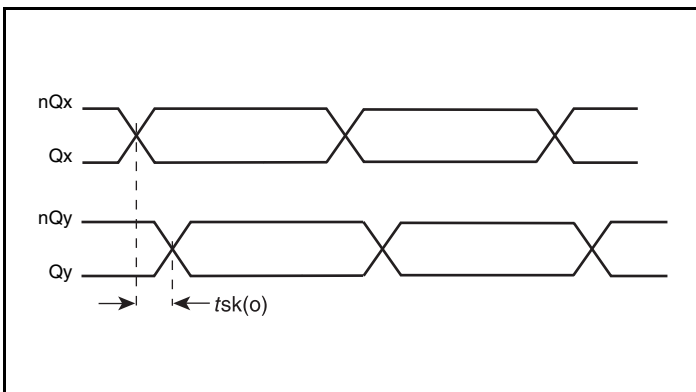
3.3V LVPECL Output Load AC Test Circuit



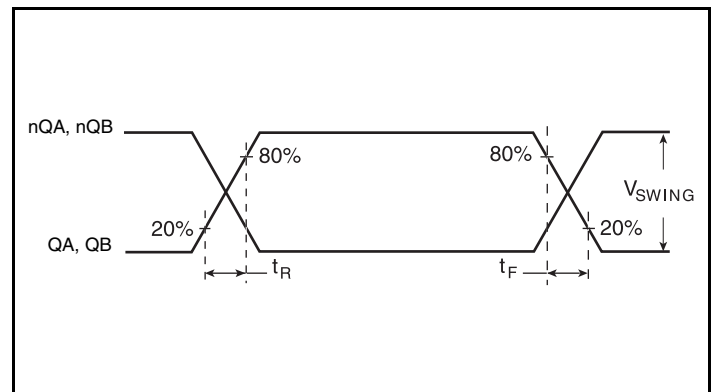
RMS Period Jitter



Cycle-to-Cycle Jitter

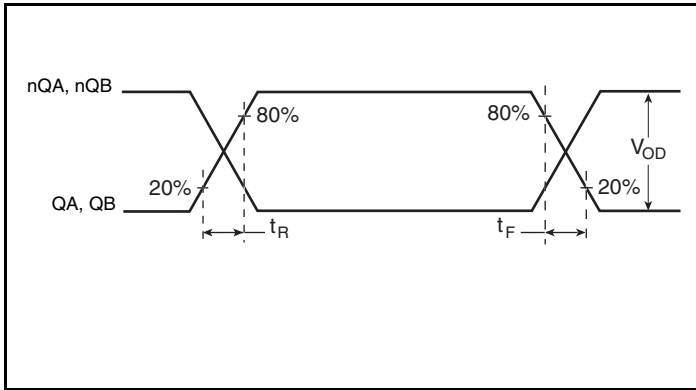


Output Skew

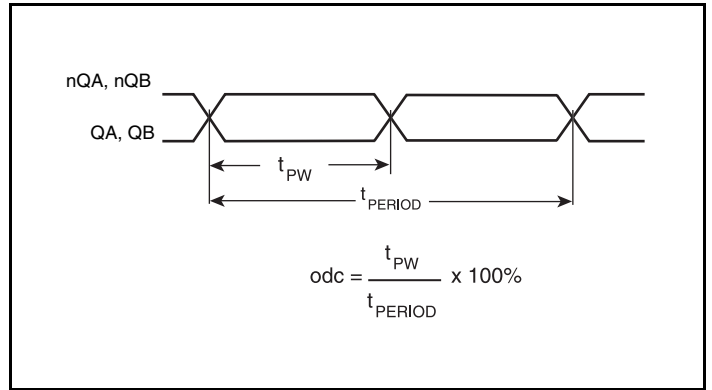


LVPECL Output Rise/Fall Time

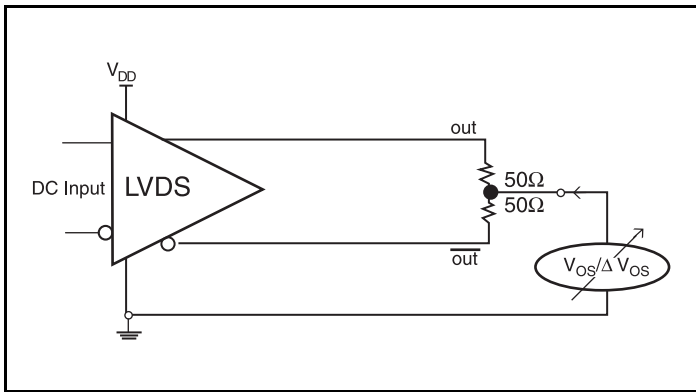
Parameter Measurement Information, continued



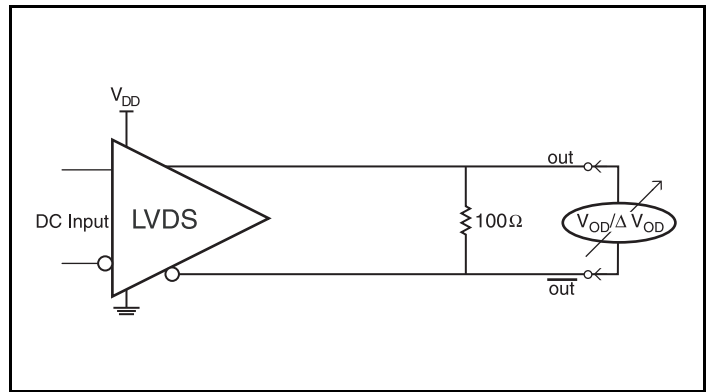
LVDS Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Offset Voltage Setup



Differential Output Voltage Setup

## Application Information

### Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 844S42I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$ ,  $V_{DDOA}$  and  $V_{DDOB}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{DDA}$  pin.

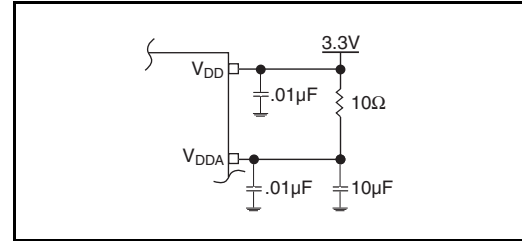


Figure 1. Power Supply Filtering

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

##### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from XTAL\_IN to ground.

##### REF\_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from the REF\_CLK to ground.

#### Outputs:

##### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

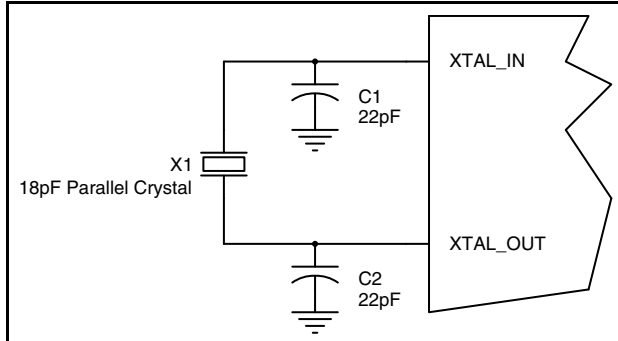
##### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with  $100\Omega$  across. If they are left floating, we recommend that there is no trace attached.

## Crystal Input Interface

The 844S421 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. These same capacitor values will

tune any 18pF parallel resonant crystal over the frequency range and other parameters specified in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

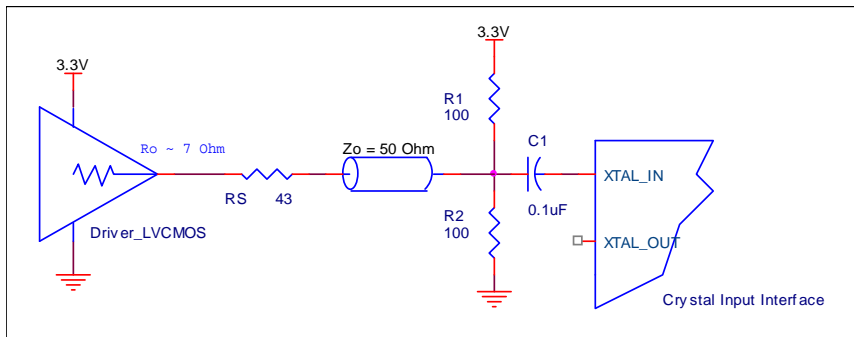


**Figure 2. Crystal Input Interface**

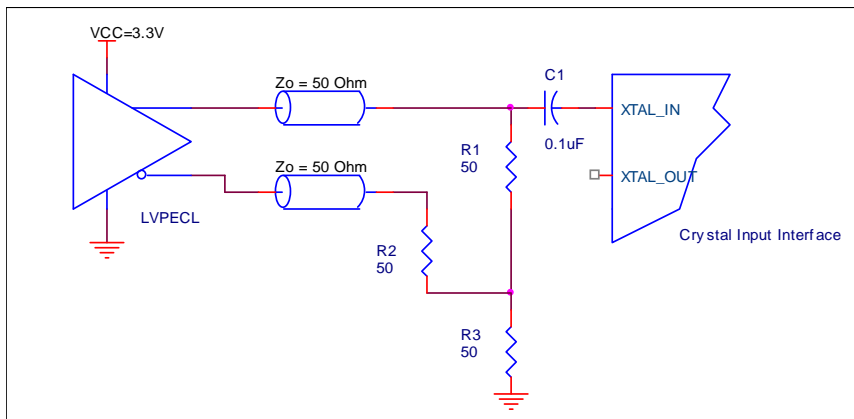
## Overdriving the XTAL Interface

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3A*. The XTAL\_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.



**Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface**



**Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface**

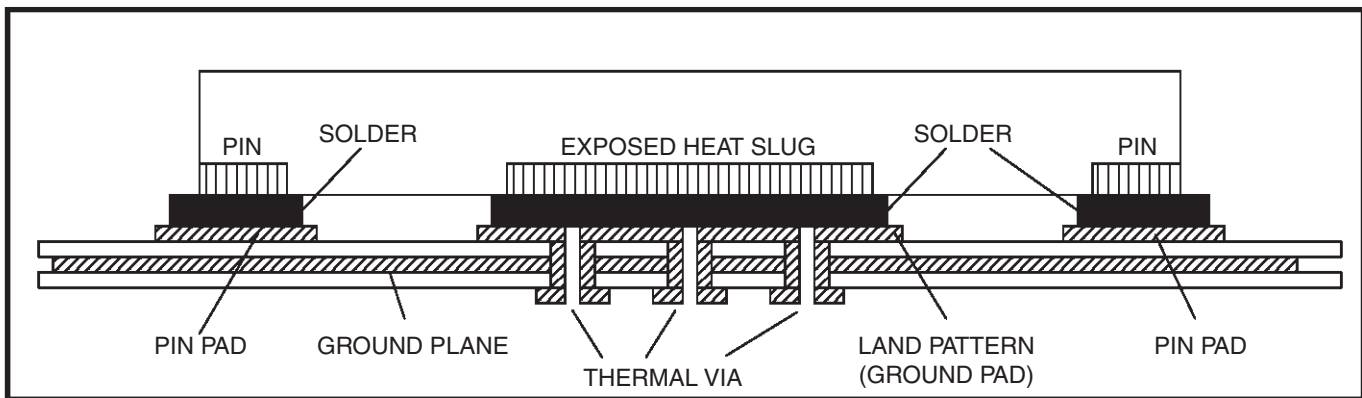


## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

### 3.3V LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between  $90\Omega$  and  $132\Omega$ . The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a  $100\Omega$  parallel resistor at the receiver and a  $100\Omega$  differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source type. The

standard termination schematic as shown in *Figure 5A* can be used with either type of output structure. *Figure 5B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately  $50\text{pF}$ . If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

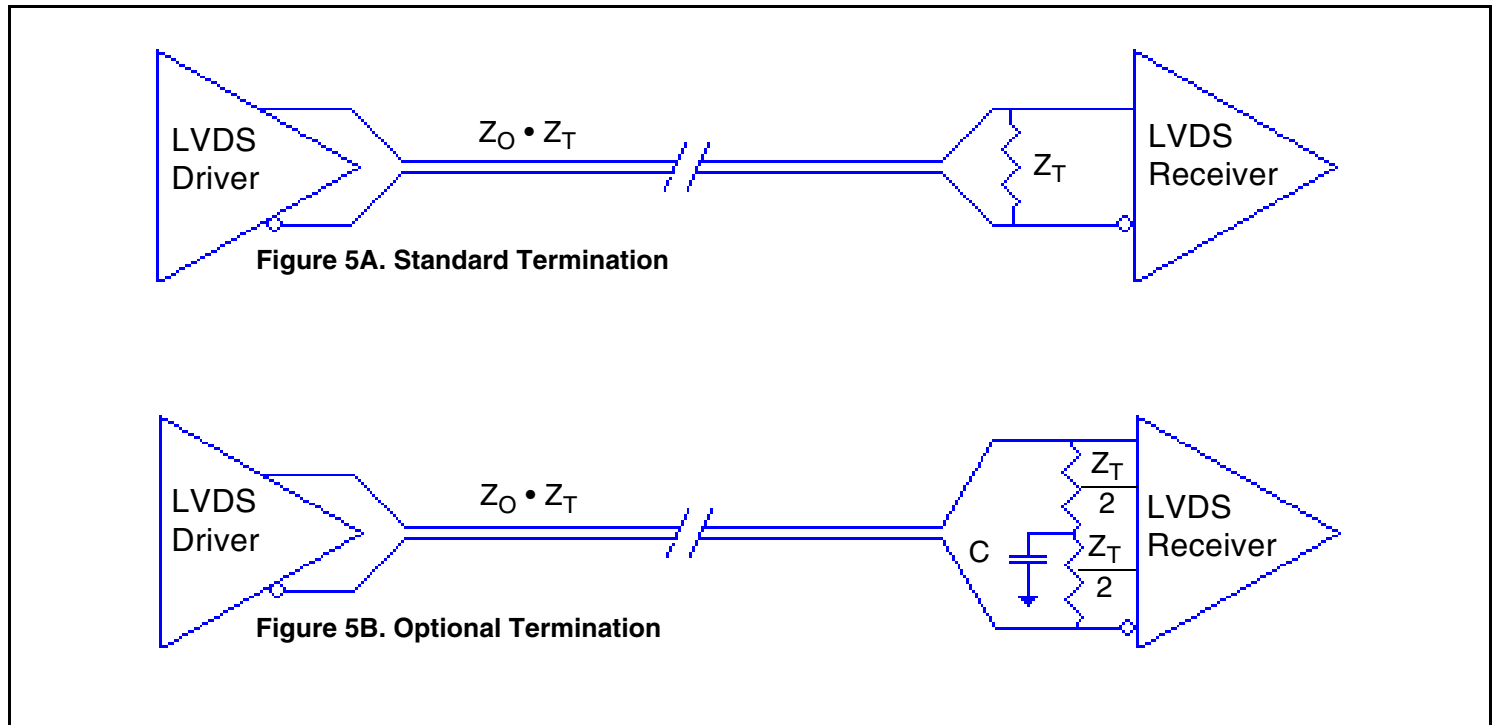


Figure 5. Typical LVDS Driver Termination

### Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines. The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

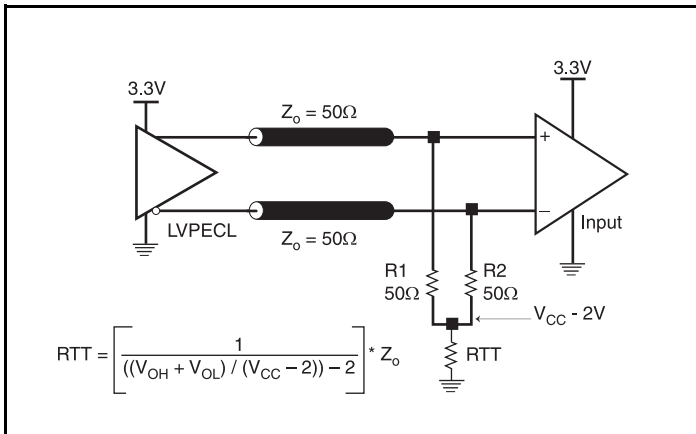


Figure 6A. 3.3V LVPECL Output Termination

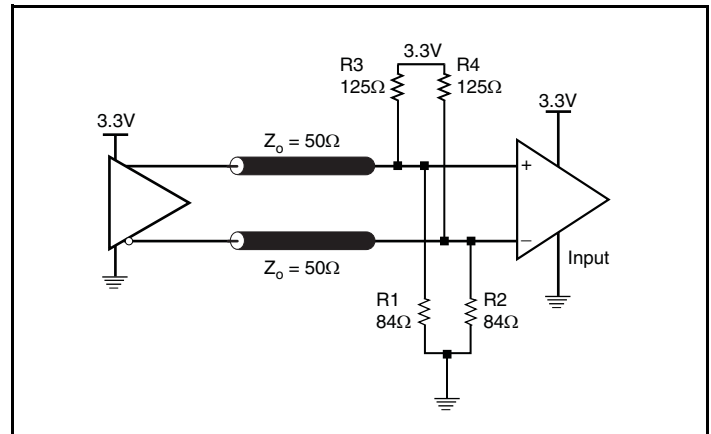


Figure 6B. 3.3V LVPECL Output Termination

## Schematic Example

Figure 7 shows an example of 844S42I application schematic. In this example, the device is operated at  $V_{DD} = V_{DDOA} = V_{DDOB} = 3.3V$ . The 18pF parallel resonant 16MHz crystal is used. The C1 and C2 = 22pF and are recommended for frequency accuracy. For differential board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL terminations and one example LVDS termination are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

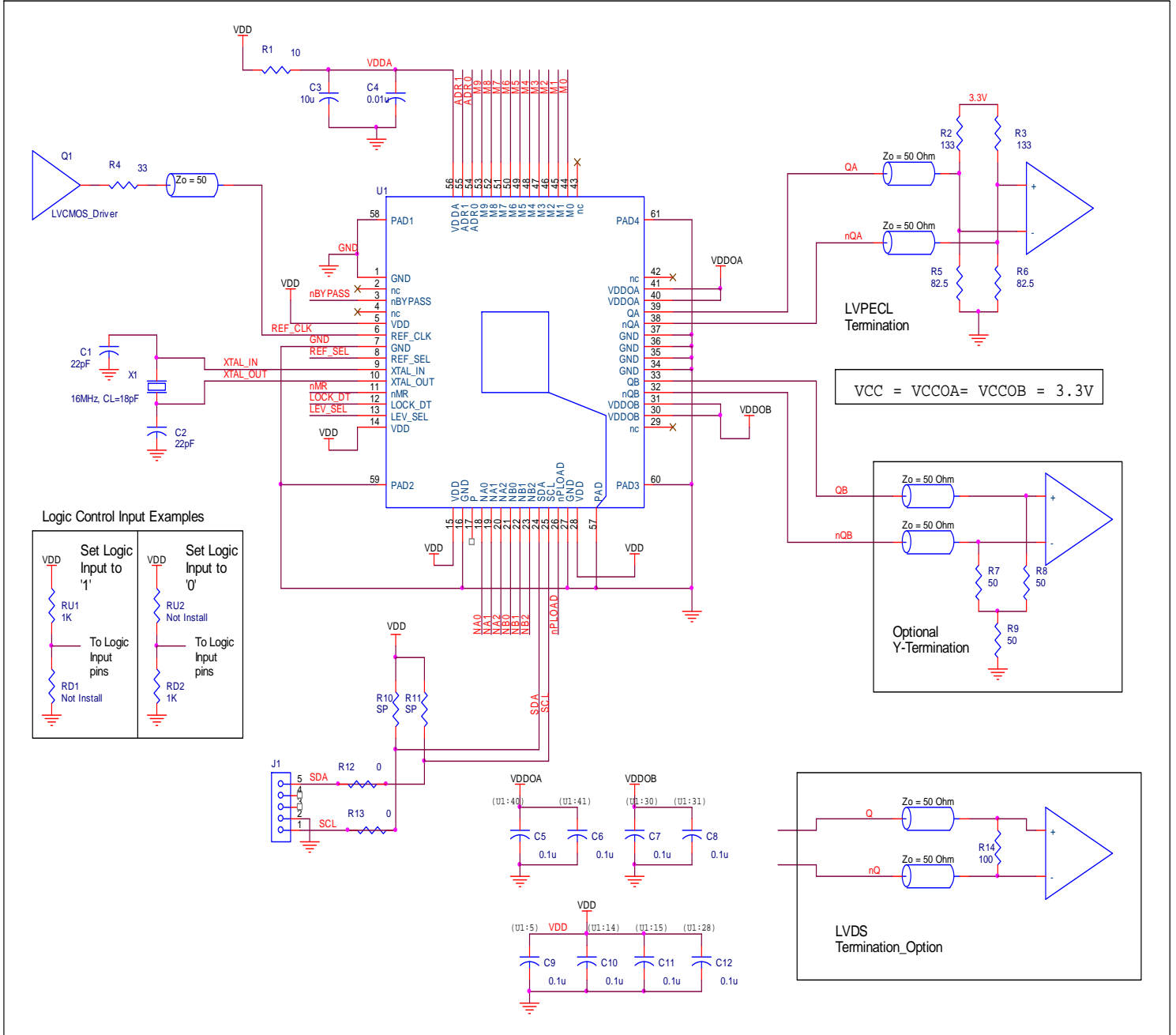


Figure 7. 844S42I Schematic Example

## Power Considerations – LVPECL Outputs

This section provides information on power dissipation and junction temperature for the 844S42I, for all outputs that are configured to LVPECL (LEV\_SEL = 1). Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 844S42I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * I_{GND\_MAX} = 3.465V * 260mA = \mathbf{900.9mW}$
- Power (outputs)<sub>MAX</sub> = **36mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 36mW = \mathbf{72mW}$

**Total Power<sub>MAX</sub>** (3.465V, with all outputs switching) =  $800.9mW + 72mW = \mathbf{972.9mW}$

### 2. Junction Temperature.

Junction temperature, T<sub>j</sub>, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T<sub>j</sub>, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T<sub>j</sub> is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

T<sub>j</sub> = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Pd<sub>total</sub> = Total Device Power Dissipation (example calculation is in section 1 above)

T<sub>A</sub> = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 31.4°C/W per Table 7A below.

Therefore, T<sub>j</sub> for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.973\text{W} * 31.4^\circ\text{C/W} = 115.6^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T<sub>j</sub> will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

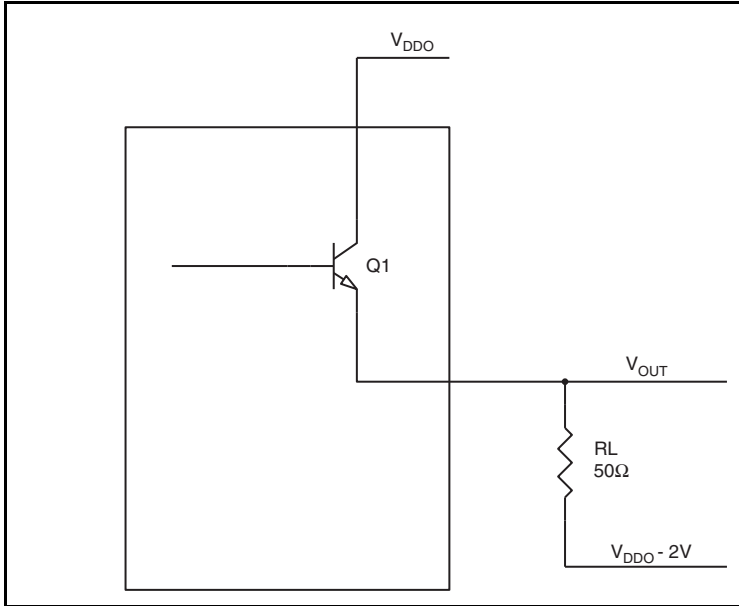
**Table 7A. Thermal Resistance  $\theta_{JA}$  for 56 Lead VFQFN Forced Convection**

| Meters per Second                           | $\theta_{JA}$ by Velocity |          |          |
|---|---------------------------|----------|----------|
|   | 0                         | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 31.4°C/W                  | 27.5°C/W | 24.6°C/W |

### 3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 8*.



**Figure 8. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{DDO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{DDO\_MAX} - 0.8V$   
 $(V_{DDO\_MAX} - V_{OH\_MAX}) = 0.8V$
- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{DDO\_MAX} - 1.4V$   
 $(V_{DDO\_MAX} - V_{OL\_MAX}) = 1.4V$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{DDO\_MAX} - 2V)) / R_L] * (V_{DDO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{DDO\_MAX} - V_{OH\_MAX})) / R_L] * (V_{DDO\_MAX} - V_{OH\_MAX}) = [(2V - 0.8V) / 50\Omega] * 0.8V = 19.2mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{DDO\_MAX} - 2V)) / R_L] * (V_{DDO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{DDO\_MAX} - V_{OL\_MAX})) / R_L] * (V_{DDO\_MAX} - V_{OL\_MAX}) = [(2V - 1.4V) / 50\Omega] * 1.4V = 16.8mW$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 36mW$$

## Power Considerations – LVDS Outputs

This section provides information on power dissipation and junction temperature for the 844S42I for all outputs that are configured to LVDS (LEV\_SEL = 0). Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 844S42I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

The maximum current at 85°C is as follows:

$$I_{DD\_MAX} = 185mA$$

$$I_{DDA\_MAX} = 22mA$$

$$I_{DDO\_MAX} = 50mA$$

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (185mA + 22mA) = 717.255mW$
- Power (output)<sub>MAX</sub> =  $V_{DDO\_MAX} * (I_{DDOA} + I_{DDOB}) = 3.465V * 50mA = 173.25mW$

$$\text{Total Power}_{MAX} = 717.255mW + 173.25mW = 890.505mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 31.4°C/W per Table 7B below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.891W * 31.4^\circ C/W = 113^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7B. Thermal Resistance  $\theta_{JA}$  for 56 Lead VFQFN, Forced Convection**

| $\theta_{JA}$ by Velocity                   |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 31.4°C/W | 27.5°C/W | 24.6°C/W |

## Reliability Information

**Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 56 Lead VFQFN**

| $\theta_{JA}$ vs. Air Flow                  |          |          |          |
|---|----------|----------|----------|
| Meters per Second                           | 0        | 1        | 2.5      |
| Multi-Layer PCB, JEDEC Standard Test Boards | 31.4°C/W | 27.5°C/W | 24.6°C/W |

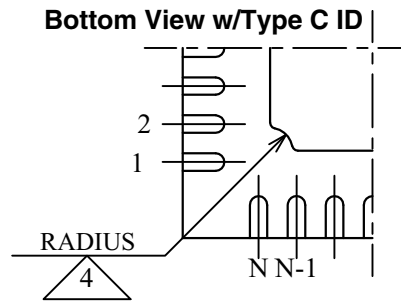
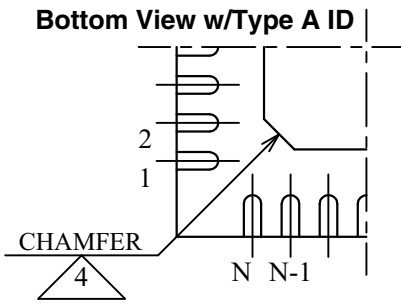
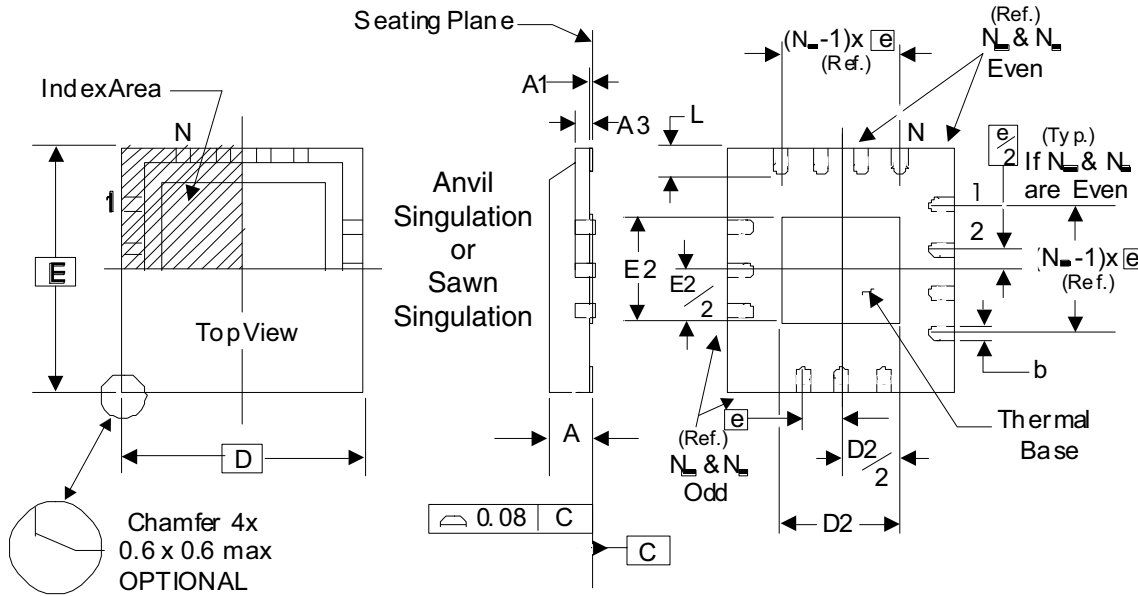
## Transistor Count

The transistor count for 844S42I is: 10,263



# Package Outline and Package Dimensions

## Package Outline - K Suffix for 56 Lead VFQFN



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions

| SPEC NON_JEDEC: VLLD-2/-5<br>All Dimensions in Millimeters |            |         |
|--|------------|---------|
| Symbol   | Minimum    | Maximum |
| N  | 56         |         |
| A  | 0.80       | 1.00    |
| A1   | 0          | 0.05    |
| A3   | 0.25 Ref.  |         |
| b  | 0.18       | 0.30    |
| N <sub>D</sub> & N <sub>E</sub>                            | 14         |         |
| D & E  | 8.00 Basic |         |
| D2   | 4.35       | 4.65    |

| SPEC NON_JEDEC: VLLD-2/-5<br>All Dimensions in Millimeters |            |         |
|--|------------|---------|
| Symbol   | Minimum    | Maximum |
| E2   | 5.05       | 5.35    |
| e  | 0.50 Basic |         |
| L  | 0.30       | 0.50    |

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

## Ordering Information

Table 10. Ordering Information

| Part/Order Number | Marking       | Package                   | Shipping Packaging | Temperature    |
|-------------------|---------------|---------------------------|--------------------|----------------|
| 844S42BKILF       | ICS844S42BKIL | "Lead-Free" 56 Lead VFQFN | Tray               | -40°C to +85°C |
| 844S42BKILFT      | ICS844S42BKIL | "Lead-Free" 56 Lead VFQFN | Tape & Reel        | -40°C to +85°C |

## Revision History

| Revision Date  | Description of Change  |
|----------------|--|
| April 28, 2016 | <ul style="list-style-type: none"><li>▪ Removed ICS from part numbers where needed.</li><li>▪ Ordering Information - Remove quantity from Tape and Reel. Deleted LF note below table.</li><li>▪ Update data sheet headers and footers.</li></ul> |



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).