IPS2200

Inductive Position Sensor IC

Description

The IPS2200 is a magnet-free, inductive position sensor ICs that can be used for high-speed absolute position sensing in industrial, medical, and consumer applications. The IPS2200 uses the physical principle of eddy currents to detect the position of a simple metallic target that is moving above a set of coils, consisting of one transmitter coil and two receiver coils.

The three coils are typically printed as copper traces on a printed circuit board (PCB). They are arranged such that the transmitter coil induces a secondary voltage in the two receiver coils, which depends on the position of the metallic target above the coils.

A signal representative of the target's position over the coils is obtained by demodulating and processing the secondary voltages from the receiver coils. The target can be any kind of metal, such as aluminum, steel, or a PCB with a printed copper layer.

The IPS2200 provides two independent interfaces:

- A high-speed analog or digital interface providing position information in the form of demodulated analog sine/cosine raw data or digital incremental outputs
- An I2C or SPI digital interface for diagnostics and programming

The IPS2200 operates at rotation speeds up to 250000 RPM (with coil designs using 1 period per turn). An ultra-low propagation delay down to 10µs or less provides high dynamic control for fast-moving objects.

The IPS2200 is available in a TSSOP package and is qualified for industrial use at -40°C to +125°C ambient temperature.

Typical Applications

- Rotor position detection for brushless DC motors; adaptable to any pole pair count
- Replacement of brushless resolvers
- Magnet-free rotor speed sensors

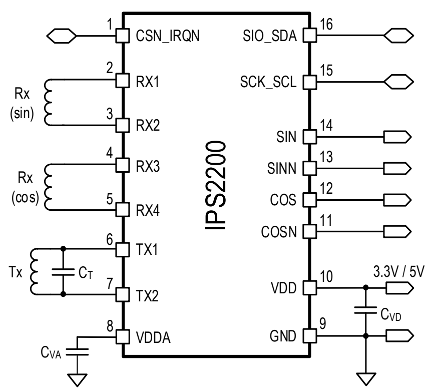
Features

- Position sensing based on an inductive principle
- Cost effective; no magnet required
- Immune to magnetic stray fields; no shielding required
- Suitable for harsh environments and extreme temperatures
- Differential and single-ended sine and cosine outputs
- Digital incremental outputs: 4 counts per period
- Nonvolatile user-configurable memory, programmable via I2C or SPI interface
- Single IC supports on-axis and off-axis rotation, linear motion, and arc motion sensing
- Adaptable to any full-scale angle range
- High accuracy: ≤ 0.2% full scale
- Rotation sensing up to 360º angle range
- ±18V over-voltage and reverse-polarity protection on output pins
- Fast diagnostic alarm through interrupt pin
- Wide operation temperature: -40°C up to +125°C
- Supply voltage programmable for 3.0V to 3.6V or 4.5V to 5.5V
- Small 16-TSSOP package (4.4 ×5.0 mm body)

Available Support

Renesas provides application modules that demonstrate IPS2200 position sensing, including rotary, arc, and linear applications.

Application Circuit Example



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1. Pin Assignments

The IPS2200 is available in a 16-TSSOP 4.4 × 5.0 mm RoHS package. It is qualified for an ambient temperature of -40°C to +125°C.

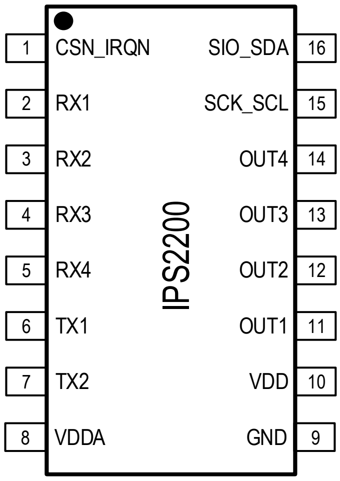


Figure 1. Pin Assignments for 4.4mm × 5.0mm 16-TSSOP Package – Top View

2. Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Name	Type	Description
1	CSN_IRQN	Digital Input/Output	Chip select input for the SPI interface; external pull-up resistor required. Push/pull interrupt output for I2C or SPI interface. Programmable options, see Table 3.
2	RX1	Analog Input	Connect the receiver coil 1 (sine) between the RX2 and RX1 pins.
3	RX2		
4	RX3	Analog Input	Connect the receiver coil 2 (cosine) between the RX4 and RX3 pins.
5	RX4		
6	TX1	Analog Input/Output	Connect the transmitter coil between the TX1 and TX2 pins. The resonant frequency is adjusted with a parallel capacitor C_T between TX1 and TX2 or with capacitors C_{T1} from TX2 to GND and C_{T2} from TX1 to GND.
7	TX2		
8	VDDA	Supply	Internal analog voltage supply. Connect a capacitor C_{VA} to the GND pin.
9	GND	Supply	Common ground connection.
10	VDD	Supply	External supply voltage. Connect two parallel capacitors C_{VD} to the GND pin.
11	OUT1	Analog Output, Digital Output	Buffered analog or digital output; see Table 2.
12	OUT2	Analog Output, Digital Output	Buffered analog or digital output; see Table 2.
13	OUT3	Analog Output, Digital Output	Buffered analog or digital output; see Table 2.
14	OUT4	Analog Output, Digital Output	Buffered analog or digital output; see Table 2.
15	SCK_SCL	Digital Input	Clock input for digital programming and diagnostic interfaces: • I2C interface: SCL clock input; external pull-up resistor mandatory, see Figure 20, Figure 21, and Figure 22. • SPI interface: SCK clock input; external pull-up resistor is optional, see Figure 17 and Figure 18.

Pin Number	Name	Type	Description
16	SIO_SDA	Digital Input/Output	Bi-directional data I/O line for digital programming and diagnostic interfaces: • I2C interface: SDA open drain data line; external pull-up resistor is mandatory, see Figure 20, Figure 21, and Figure 22. • SPI interface: SIO bi-directional push-pull data line; external pull-up resistor is optional, see Figure 17 and Figure 18.

Table 2. Buffered Output Configuration

Pin (See Figure 1)		Output Depending on Mode [a]			Diagnostic State
Pin Number	Pin Name	Analog Differential	Analog Single-Ended	Digital AB Incremental	All Modes, if enabled
14	OUT4	SIN	SIN	A	LOW
13	OUT3	SINN	REF_SIN	A_N	LOW
12	OUT2	COS	COS	B	HIGH
11	OUT1	COSN	REF_COS	B_N	HIGH

[a] Abbreviations used in Table 2:

SIN: Demodulated and buffered output of RX1 (sine, non-inverted)

SINN: Demodulated and buffered output of RX2 (sine, inverted)

COS: Demodulated and buffered output of RX3 (cosine, non-inverted)

COSN: Demodulated and buffered output of RX4 (cosine, inverted)

REF_SIN: Bias voltage of sine signal, typical VDD/2

REF_COS: Bias voltage of cosine signal, typical VDD/2

A: Sign output of RX1 (A, non-inverted): HIGH if positive, LOW if negative

A_N: Sign output of RX2 (A, inverted): HIGH if positive, LOW if negative

B: Sign output of RX3 (B, non-inverted): HIGH if positive, LOW if negative

B_N: Sign output of RX4 (B, inverted): HIGH if positive, LOW if negative

Diagnostic state: Alarm status indication if an enabled alarm occurs

Table 3. Digital Interface and Interrupt Output Configuration

Pin (See Figure 1)		Input/Output Depending on Interface Mode [a]			
TSSOP Pin Number	Pin Name	Half Duplex SPI	Half Duplex SPI with Interrupt	I2C with Address Select	I2C with Interrupt
16	SIO_SDA	SIO	SIO	SDA (PU)	SDA (PU)
15	SCK_SCL	SCK	SCK	SCL (PU)	SCL (PU)
1	CSN_IRQN	CSN (PU)	CSN/IRQN (PU)	SEL	IRQN

[a] Abbreviations used in Table 3:

CSN: Chip-Select Input

CSN/IRQN: Combined Chip-Select Input and Interrupt Output

SIO: Serial Bi-directional Data I/O Port for SPI Modes

SCK: Serial Clock Input for SPI Modes

SEL: Hardware Address-Select Input for I2C Mode (two address options)

SDA: Serial Bi-directional Data I/O Port for I2C Modes`

SCL: Serial Clock Input for I2C Modes

IRQN: Interrupt Output

PU: External Pull-up resistor required

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the IPS2200 at the absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions could affect device reliability.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{VDDmax}	External supply voltage	Continuous	-18	7.5	V
V_{OUT}	OUT1, OUT2, OUT3, and OUT4 output voltage	IC not supplied, permanent	-18	7.5	V
		IC supplied, permanent	-15	18	V
V_{RX1}	Receiver coil pin: RX1		-12	12	V
V_{RX2}	Receiver coil pin: RX2				
V_{RX3}	Receiver coil pin: RX3				
V_{RX4}	Receiver coil pin: RX4				
$V_{DIGITAL}$	Digital IO pins: SCK_SCL, SIO_SDA, CSN_IRQN		-0.3	18	V
V_{CSN_IRQN}	Digital IO pin CSN_IRQN	When used as input for I2C address selection and tied to VDD directly or with pull-up resistor.	Refer to V_{VDDmax}		V
$V_{VDDAmax}$	VDDA internal LDO output	VDDA is internally regulated, no connection to external voltage	Refer to V_{VDDA} in Table 6		V

Table 5. Electrostatic Discharges (ESD)

Symbol	Parameter	Conditions	Min	Max	Units
V_{ESD}	ESD tolerance for all pins:	Human Body Model (HBM) 100pF / 1.5kΩ According to AEC-Q100-002 classification H2	±2		kV
$V_{ESD,OUT}$	ESD tolerance for pins with potential external cable connection: OUT1, OUT2, OUT3, OUT4, CSN_IRQN, VDD	Human Body Model (HBM) 100pF / 1.5kΩ According to AEC-Q100-002 classification H3A	±4		kV

[a] When handling semiconductor devices such as IPS2200, always observe ESD guidelines to avoid electrostatic discharges on these parts.

4. Operating Conditions

Values shown in Table 6 are valid under the following conditions: VDD = 3.3V±0.3V or 5.0V±0.5V , T_{AMB} = -40°C to +125°C, unless otherwise noted.

Table 6. Operating Conditions

Note: See important notes at the end of the table.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
T_{AMB_TSSOP}	Ambient temperature: 16-TSSOP		-40		125	ºC
T_J	Junction temperature		-40		145	ºC
T_{STOR}	Storage temperature	Unmounted units must be limited to 10 hours at temperatures above 125°C	-55		150	ºC
R_{THJA_TSSOP}	Thermal resistance junction to ambient: 16-TSSOP package	JEDEC MO-153		89		ºC/W
t_{pup}	Start-up time	Power-on reset (POR) to valid output signal			3	ms

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{EL}	Input rotational velocity	Electrical speed Sine or cosine periods per minute			250 000	rpm
$V_{VDDA\_TH\_H}$	Power on reset, high threshold	The device is activated when VDDA increases above this threshold			2.6	V
$V_{VDDA\_TH\_L:}$	Power on reset, low threshold	The device is deactivated when VDDA decreases below this threshold	2.1			V
$VDDA_{POR\_HYST}$	Power-on reset hysteresis	At VDDA pin	50			mV
I_{VDDA}	VDDA load current limitation			75		mA
I_{DD}	Current consumption	Without coils. no load		8.4	12	mA
		Programmable transmitter coil drive current (depending on inductance of transmitter coil)	For values, refer to Table 9			mA
C_{VA}	Capacitor from VDDA pin to GND			100		nF
C_{VD}	Capacitor from VDD pin to GND		70			nF
INL_{UV3V}	Accuracy, 3.3V mode, VDD= under-voltage alarm level to 3.0V	With ideal coil input signals, relative to an output signal of 1.8Vpp		±0.3		% FS [a]
INL_{3V}	Accuracy, 3.3V mode, VDD= 3.0 to 3.6V			±0.2		% FS
INL_{OV3V}	Accuracy, 3.3V mode, VDD= 3.6V to over-voltage alarm level			±0.3		% FS
INL_{UV5V}	Accuracy, 5V mode, VDD= under-voltage alarm level to 4.5V	With ideal coil input signals, relative to an output signal of 3.0Vpp		±0.3		% FS
INL_{5V}	Accuracy, 5.0V mode, VDD= 4.5 to 5.5V			±0.2		% FS
INL_{OV5V}	Accuracy, 5.0V mode, VDD= 5.5V to over-voltage alarm level			±0.3		% FS

[a] % FS = percent of full scale = accuracy in % per period, where 100% is the angle range of one electrical period.
For rotary multi-period designs, one electrical period = 360° (one full turn) divided by the number of periods per turn.

Examples:

- A 3-periodic coil design (3 × 120°) has a typical mechanical accuracy of ±0.2% per 120° = ±0.24°
- A 4-periodic coil design (4 × 90°) has a typical mechanical accuracy of ±0.2% per 90° = ±0.18°

5. Ambient Temperature Range

The minimum ambient temperature for the IPS2200 is -40°C.

The maximum ambient temperature depends on the following factors:

- The maximum junction temperature. See Table 6 for details.
- The selected transmitter coil current. The total power consumption of the chip depends on the internal power consumption and the user programmable current for the transmitter coil.
- The minimum usable coil current in a given application. Note that smaller coil inductances require more transmitter coil current, and larger coil inductances can operate with less coil current. The maximum allowed transmitter coil current is shown in Table 6.
- The Renesas internal part qualification. The IPS2200 is qualified for -40°C to +125°C ambient temperature.

6. Electrical Characteristics

The following electrical specifications are valid for the operating conditions as specified in Table 6: (T_{AMB} = -40°C to 125°C).

Table 7. IPS2200 Electrical Characteristics, 3.3V Mode

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD_3	Supply voltage		3.0[a]	3.3	3.6[b]	V
$VDDA_3$	Analog supply voltage	Internally regulated. Connect a C_{VA} = 100nF capacitor from VDDA to GND.	2.85	3.0	3.1	V
$V3_{OVR}$	Over-voltage detection, VDD rising	An over-voltage alarm is created if VDD rises above these limits.	3.8		4.3	V
$V3_{OVF}$	Over-voltage detection, VDD falling	An over-voltage alarm is cleared if VDD falls below these limits.	3.5[c]		4.1	V
$V3_{OVH}$	Over-voltage detection hysteresis		150			mV
$V3_{UVR}$	Under-voltage detection, VDD falling	An under-voltage alarm is created if VDD falls below these limits.	2.2		2.95	V
$V3_{UVF}$	Under-voltage detection, VDD rising	An under-voltage alarm is cleared if VDD rises above these limits.	2.6		3.1[d]	V
$V3_{UVH}$	Under-voltage detection hysteresis		100			mV
$V3VDDA_{UVF}$	VDDA under-voltage detection	An under-voltage alarm is created if VDDA falls below these limits.	2.6		2.85	V
$V3VDDA_{UVRr}$	VDDA under-voltage detection	An under-voltage alarm is created if VDDA rises above these limits.	2.7		2.9	V

[a] If the VDD under-voltage alarm is enabled, the VDD3 must be at least 3.1V.

[b] If the VDD over-voltage alarm is enabled, the VDD3 must be maximum 3.5V.

[c] If the VDD over-voltage alarm is enabled, the VDD3 must be maximum 3.5V.

[d] If the VDD under-voltage alarm is enabled, the VDD3 must be at least 3.1V.

Table 8. IPS2200 Electrical Characteristics, 5.0V Mode

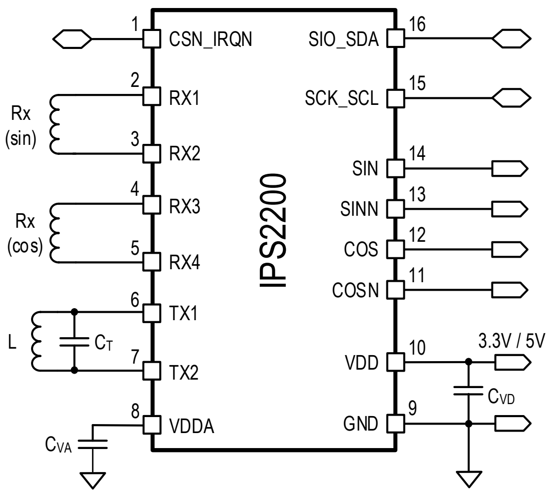
Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD_5	Supply voltage		4.5[a]	5.0	5.5	V
$VDDA_5$	Analog supply voltage	Internally regulated. Connect a C_{VA} = 100nF capacitor from VDDA to GND.	3.9	4.0	4.1	V
$V5_{OVR}$	Over-voltage detection, VDD rising	An over-voltage alarm is created if VDD rises above these limits.	6.2		6.9	V
$V5_{OVF}$	Over-voltage detection, VDD falling	An over-voltage alarm is cleared if VDD falls below these limits.	5.9		6.6	V
$V5_{OVH}$	Over-voltage detection hysteresis		150			mV
$V5_{UVR}$	Under-voltage detection, VDD falling	An under-voltage alarm is created if VDD falls below these limits.	3.8		4.4	V
$V5_{UVF}$	Under-voltage detection, VDD rising	An under-voltage alarm is cleared if VDD rises above these limits.	4.0		4.6[b]	V
$V5_{UVH}$	Under-voltage detection hysteresis		100			mV
$V5VDDA_{UVF}$	VDDA under-voltage detection	A VDDA under-voltage alarm is triggered when VDDA falls below these limits.	3.45		3.9	V
$V5VDDA_{UVRr}$	VDDA under-voltage detection	A VDDA under-voltage alarm is cleared if VDDA rises above these limits.	3.5		3.9	V

[a] If the VDD under-voltage alarm is enabled, the VDD5 must be at least 4.6V.

[b] If the VDD under-voltage alarm is enabled, the VDD5 must be at least 4.6V.

Table 9. LC Oscillator Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$R_{P,eq}$	Equivalent parallel resistance of the LC resonant circuit	See Equation 1 and Equation 2.	100			Ω
f_{LC}	Excitation frequency	LC oscillator; determined by external components L and C.	1.7		5.8	MHz
F_{OSC_ACC}	Accuracy of transmitter oscillator frequency measurement	Gated by the internal oscillator.	-10		10	%
$f_{LC\_DIAG\_L}$	LC oscillator lower frequency diagnostics range	Programmable frequency where an out-of-range frequency diagnostics alarm can be enabled.	0.007			MHz
$f_{LC\_DIAG\_H}$	LC oscillator upper frequency diagnostics range				10	
V_{TX_P}	LC oscillator amplitude	Peak-to-peak voltage; pins TX1 vs. TX2; all modes. The coil current is user programmable.			11	Vpp
I_{LC}	Programmable transmitter coil drive current	Equivalent DC current. Programmable, depending on transmitter coil inductance.	0	3	20	mA
I_{LCmax}	Maximum transmitter coil drive current tolerance	At room temperature	18	20	22	mA
RTx1,RTx2	TX Series resistor	For reduced EMC emission, see Figure 13 to Figure 16		22		Ω



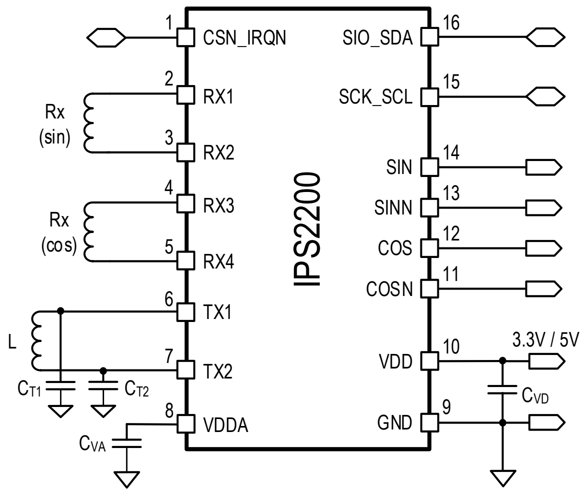
Configuration with a single capacitor CT in the LC oscillator.

The oscillator frequency is determined by the values of coil L and capacitor C_T:

$$f_{TX} = \frac{1}{2\pi\sqrt{LC_T}}$$

Where:
f_{TX} = Oscillator frequency in MHz
L = Coil impedance in µHenry
C_T = Capacitance in µFarad

Figure 2. LC Oscillator Connection with a Single Capacitor



Configuration with split capacitors CT1 and CT2 for improved EMC performance. Both capacitors must have the same capacitance.

The oscillator frequency is determined by the values of coil L and capacitors C_{T1} and C_{T2}:

$$f_{TX} = \frac{1}{2\pi\sqrt{\frac{L*C_{T1}*C_{T2}}{C_{T1}+C_{T2}}}}$$

$\rightarrow$ for $C_{T1} = C_{T2}$: $f_{TX} = \frac{1}{2\pi\sqrt{L\frac{C_{T1}}{2}}}$

Where:

f_{TX} = Oscillator frequency in MHz

L = Coil impedance in μHenry

C_{T1}, C_{T2} = Capacitance in μFarad

Figure 3. LC Oscillator Connection with Split TX Capacitors

The equivalent parallel resistance R_{Peq} of the LC oscillator can be calculated using Equation 2:

$$R_{Peq} = \frac{1}{R_S} \times \frac{L}{C}$$ **Equation 1**

$$R_S = \frac{1}{R_{Peq}} \times \frac{L}{C}$$ **Equation 2**

Where

R_{Peq} Equivalent parallel resistance of the LC oscillator.

R_S Serial resistance of the transmitter coil at the transmitter frequency.

L Coil reactance at the resonant frequency.

C Capacitance of the parallel capacitor C_T.
Note that the capacitor losses are not included in the equation.

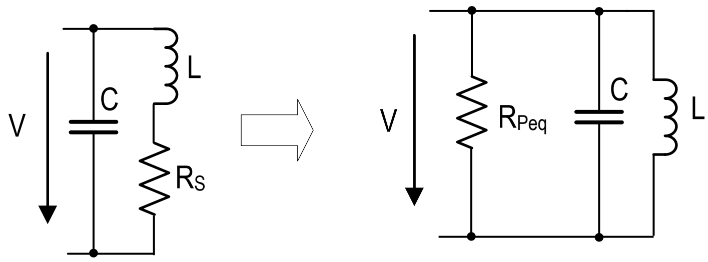


Figure 4. Parallel Resonator Circuit

Table 10. Coil Receiver Front-End Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{RX}	Receiver coil amplitude	Input signal full range. Vout = 3.0Vpp (single ended)	5[a]		5200[a]	mV_{pp}
A_{IN_MM}	Amplitude mismatch correction range	Programmable individual gain mismatch correction of Receiver coil signals (SIN and COS)	0		11	%
A_{MM_RES}	Amplitude mismatch correction granularity			7		Bit
$A_{IN\_OFFSET\_MIN}$	Input offset minimum correction range	Offset of sine and cosine signal, percentage of transmitter coil amplitude. Minimum and maximum values depend on the Rx gain setting.	-0.09		+0.09	%
$A_{IN\_OFFSET\_MAX}$	Input offset maximum correction range		-0.27		+0.27	%
OFF_{CORR_RES}	Input offset correction granularity	Programmable step size.		7		Bit
R_{RX}	Coil receiver DC input resistance	Single-ended to GND.		200		kΩ
		Differential.		800		kΩ
C_{RX1} C_{RX2} C_{RX3} C_{RX4}	Receiver input filter capacitors	For improved EMC immunity, see Figure 13 to Figure 16		100		pF

[a] Minimum and maximum Receiver voltage input levels depend on front-end gain setting, integration cycles, and LC oscillator frequency

Table 11. Diagnostic Checks

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
t_{FAIL}	Failure reaction time (time to flag an error condition at the IRQN pin)	Chip internal diagnostic checks.			500	µs
$R_{\_OPEN\_TH}$	Resistance of Rx coil, open coil detection	Rx coil short/open error flag activated.	2200			kΩ
		Rx coil short/open error flag cleared.			354	kΩ
$R_{\_SHORT\_GND}$	External resistance from any coil input to GND, short to ground detection	Rx coil short/open error flag activated.			19	kΩ
		Rx coil short/open error flag cleared.	630			kΩ
$R_{\_SHORT\_VDD}$	External resistance from any coil input to VDD, short to VDD detection	Rx coil short short/open error flag activated; VDD = 2.7 to 6.4V.			160	kΩ
		Rx coil short/open error flag cleared. VDD = 2.7 to 6.4V	840			kΩ
$R_{\_SHORT\_TH}$	External resistance between coils for detection of a short between coils	R1R2 short error flag threshold; VDD = 3.0 to 3.6V.	35	140	410	kΩ
		R1R2 short error flag threshold; VDD = 4.5 to 5.5V.	20	70	180	kΩ
DC_{OFF_AL}	DC common mode output offset alarm limits	Absolute value relative to VDD/2. Output offset alarm flag activated.	100		200	mV
$Diag_{LO}$	Diagnostic Low indication	SIN, SINN, A, AN Outputs, I_{LOAD} = 1mA sink current	0	1	3	%VDD
$Diag_{HI}$	Diagnostic High indication	COS, COSN, B, BN Outputs I_{LOAD} = 1mA source current	97	98.6	100	%VDD

Table 12. Back-End Specification, Analog Outputs SIN, SINN, COS, COSN

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V3_{OUT}$	Analog output range, 3.3V option	$-1mA \le I_{OUT} \le 1mA$	GND + 0.7		VDD – 0.4	V
$V5_{OUT}$	Analog output range, 5V option		GND + 1.0		VDD – 1.0	V
$V3_{OUT\_PP}$	Analog output voltage amplitude, 3.3V option	Single ended peak-to-peak voltage range	0.9	1.275	1.65	V_{PP}
$V5_{OUT\_PP}$	Analog output voltage amplitude, 5V option		1.4	1.95	2.5	V_{PP}

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD_{OUT_CM}	Output DC offset voltage, common mode voltage	All modes	47.5		52.5	%VDD
$DC_{OFFDRIFT}$	DC offset voltage drift	Over temperature range	-50		50	µV/°C
DC_{OFF}	DC offset voltage after trimming	At trim temperature, over gain range and transmitter frequency range, VDD= 3.0 to 5.5V	-6		6	mV
I_{OUT3}	Output current; 3.3V option	Output load current	-1		+1	mA
I_{OUT5}	Output current; 5V option		-2		+2	mA
I_{OL}	Output overload current,		20		30	mA
C_{RAW_I}	Capacitive load, EMC filters	Refer to section 18 for C_{O1} to C_{O4}			47	nF
Noise	Device output noise	Maximum gain, maximum setting for integration cycles, no output filtering, shorted coil inputs		2		mV_{rms}
C_{OUT1}	Output filter capacitors	For improved EMC immunity, placed close to IC output			47	nF
C_{OUT2}						
C_{OUT3}						
C_{OUT4}						

Table 13. Back-End Specification, Quadrature Pulse Output Option, Pins A, A_N, B, and B_N

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{QUAD_OH}	High level output voltage	Sign of demodulated input voltage: high = positive; low = negative	70		100	%VDD
V_{QUAD_OL}	Low level output voltage		0		30	
I_{O_QUAD3}	Output current; 3.3V option	Output load current	-0.5		+0.5	mA
I_{O_QUAD5}	Output current; 5V option		-1		+1	mA
C_{RAW_I}	Capacitive load				22	nF
$V_{QUAD\_TH\_POS}$	Output switching positive threshold	Comparator levels for changing state of A, A_N, B, B_N digital outputs, relative to amplified input voltage	V_{OUT_CM}+ 0.05			V
$V_{QUAD\_TH\_NEG}$	Output switching negative threshold				V_{OUT_CM}- 0.05	V
$V_{QUAD\_TH\_HYST}$	Quadrature pulse hysteresis	Relative to opposite channel R1(Sin) vs. R2(Cos)		5		%

[a] See Table 2 regarding which of the pins OUT1, OUT2, OUT3, and OUT4 are assigned as A, A_N, B, and B_N.

Table 14. Digital Control Interface, Pins CSN_IRQN, SIO_SDA, SCK_SCL

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High level input voltage, all modes	CSN_IRQN address select input, SCK_SCL clock input, SIO_SDA data input	70		100	%VDD
V_{IL3}	Low level input voltage, 3.3V mode		0		30	%VDD
V_{IL3}	Low level input voltage, 5V mode		0		20	%VDD
I_{LEAK}	Input leakage current		-5		5	µA
V_{I_HYST}	Input hysteresis	SCK_SCL clock input	100			mV
V_{OH}	High level output voltage	All modes	80		100	%VDD
V_{OL_PP}	Low level output voltage – push/pull	Push/pull output CSN_IRQN	0		20	%VDD
V_{OL_OD}	Low level output voltage – open drain	Open-drain output SIO_SDA, 3mA sink current	0		0.4	V
V_{IRQN_H}	Over-voltage detection at CSN_IRQN, SCK_SCL, or SIO_SDA	Over-voltage on these pins can be monitored as a diagnostic feature	6.9	7.4	7.9	V
R_{SDA}, R_{SCL}, R_{SIO}, R_{SCK}	External pull-up resistor at pins SIO_SDA and SCK_SCL	Resistor value and capacitive load on these pins are limiting the	1.8	4.7		kΩ

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
		maximum clock frequency				
R_{ADR}, R_{CSN}	External resistor at pin CSN_IRQN for I2C address selection	Pull-up or pull-down, depending on I2C address setting.	1.8	4.7		kΩ
$I_{OUT\_SIO\_SDA}$	Digital interface output current	Pin SIO_SDA	-2		2	mA
C_L	Capacitive load	All modes			400	pF

Table 15. Nonvolatile Memory

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
	Data retention	According to AEC Q100			> 100 at 25°C >13 at 85°C	Years
	Write temperature	Allowed ambient temperature range for read and write access	-40		125	°C
	Read temperature		-40		125	°C
	Endurance[a]	Over product lifetime			100	NVM Write Cycles
	Read Cycles		5x 10^{11}	1x 10^{12}		NVM Read events

[a] Verified number of program/erase cycles. Qualified with 200 cycles

7. Circuit Description

7.1 Overview

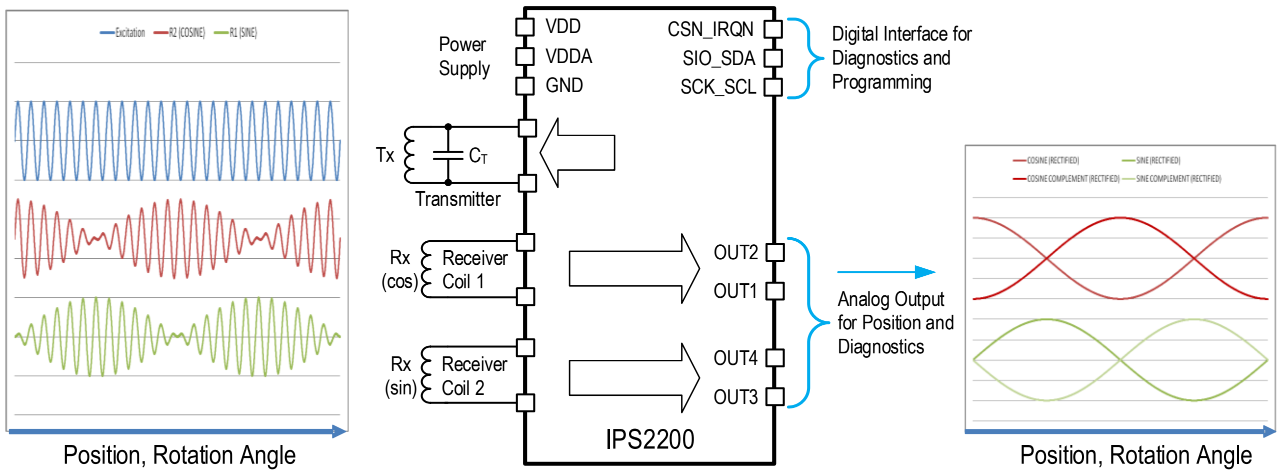
The IPS2200 sensor circuit consists of one transmitter coil and two receiver coils, which are typically designed as traces on a printed circuit board. The two receiver coils have a sinusoidal shape and are shifted by 90° with respect to each other; refer to Figure 6 and Figure 7 for typical coil shapes. A metal target is placed above the coil arrangement.

Circuit signal flow:

1. The IPS2200 drives AC current into the transmitter coil and generates an alternating magnetic field.
2. The magnetic field induces voltages in the receiver coils. Without a metallic target, due to the balanced, anti-serial connection of their segments, the voltages are compensated to achieve zero output at each pair of terminals.
3. If a metal target is placed above the coils:
    a. The magnetic field induces eddy currents on the surface of the metal target.
    b. The eddy currents generate a counter magnetic field, thus reducing the total flux density underneath.
    c. The voltage induced in the receiver coil areas underneath the target is reduced, creating an imbalance in the anti-serial coil segment voltages
    d. An output voltage occurs on the terminals, changing amplitude and polarity with the target position.
4. The IPS2200 IC amplifies, rectifies, and filters the receiver voltages and outputs them for external signal processing.

Due to the 90° phase shift of the two receiver coils, the output signals also have a 90° phase shift in relation to the target position, generating ratiometric sine and cosine signals. The signals can be converted into an absolute position, for example by applying an arctangent operation of Vsin and Vcos.

$$Position = arctan\left(\frac{Vsin}{Vcos}\right)$$ **Equation 3**



Note: See Table 2 for definitions of the OUT1, OUT2, OUT3, and OUT4 pins.

Figure 5. Response of the IPS2200

Figure 6 shows an example of a linear motion sensor with one transmitter coil (transmitter loop) and two receiver coils (Sin loop and Cos loop). Due to the alternating clockwise and counterclockwise winding direction of each segment in a loop (for example RxCos = clockwise Cos Loop1 + counterclockwise Cos Loop 2), the induced voltages in each segment have alternating opposite polarity.

$V_{Cos\ Loop1} = -V_{Cos\ Loop2}$ **Equation 4**

If no target is present, the secondary voltages cancel each other:

$V_{Cos} = V_{Cos\ Loop1} - V_{Cos\ Loop2} = 0V$ **Equation 5**

With a target placed above the coils, the secondary voltage induced in the covered area is lower than the secondary voltage without a target above it.

$V_{Cos\ Loop1} \neq -V_{Cos\ Loop2}$ **Equation 6**

This creates an imbalance of the secondary voltage segments, and thus, a secondary voltage ≠ 0V is generated, depending on the location of the target.

$V_{Cos} = V_{Cos\ Loop1} - V_{Cos\ Loop2} \neq 0V$ **Equation 7**

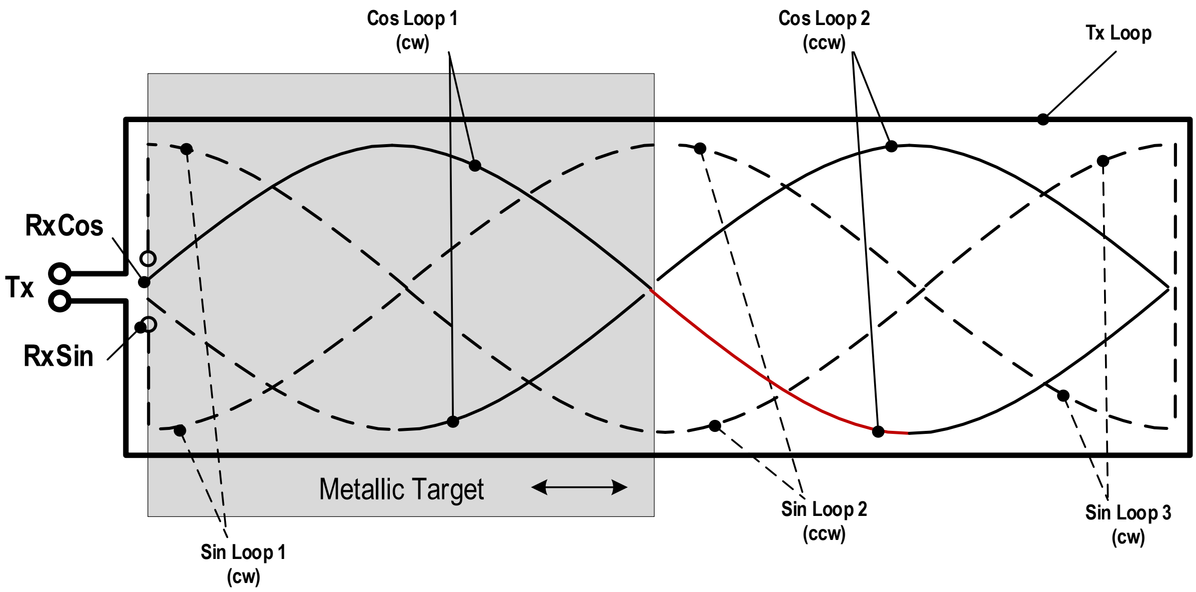


Figure 6. Coil Design for a Linear Motion Sensor

The same principles shown for the linear motion sensor in Figure 6 can be applied to an arc or rotary sensor as shown in Figure 7.

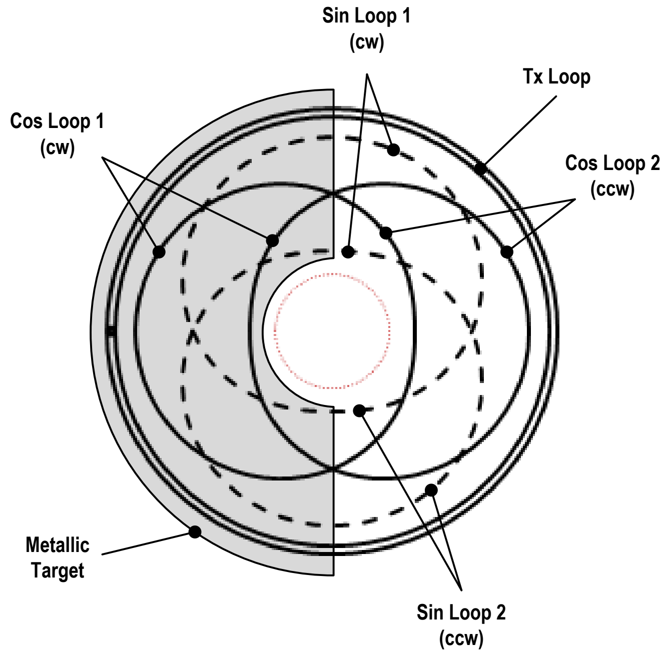


Figure 7. Coil Design for a 360° Rotary Sensor

8. Sampling Rate, Resolution, Output Data Rate, and Propagation Delay

Since the IPS2200 uses analog signal processing (no ADC), there is no sampling rate and the resolution is virtually infinite.

Due to the internal chopping and demodulation processes, there is a programmable output data rate and corresponding propagation delay.

The overall signal processing is very fast, allowing operation at very high speeds up to 250000 rpm (electrical) and more with very fast update rates and propagation delays in the range of 4.3µs to 7.7µs for the shortest integration factor (5×) and 13.6µs to 31.3µs for the longest integration factor (31×).

The coil receiver circuit automatically locks to the transmitter coil oscillator frequency. It automatically corrects for LC oscillator frequency drifts due to temperature changes or air gap changes for the target. Consequently, the demodulator at the receiver is also dependent on the LC oscillator frequency.

In addition to the LC oscillator frequency, a second contributing factor is the integration factor of the demodulator (essentially a digital filtering process). The data rate and propagation delay are defined as a step response on the input when the output reaches > 90% of the maximum signal level.

It can be calculated via Equation 8:

$$\text{Output Data Rate [µs]} = \frac{(IF+1)}{f_{LC}} \qquad \textbf{Equation 8}$$

$$\text{Data Propagation Delay [µs]} = \frac{2 \cdot (IF+1)}{f_{LC}} + 1 \cdot \tau \qquad \textbf{Equation 9}$$

Where

IF Integration factor: a programmable factor of 5 to 31

f_{LC} LC oscillator frequency

τ Internal time constant (tau) = 2.2µs

Table 16. Output Data Rate, Propagation Delay

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
t_{PD}	Raw data update rate, propagation delay of R1 and R2 input signals at output.	f_{LC} = 5.6MHz, integration factor = 5× to 31× (programmable)	4.3		13.6	µs
		f_{LC} = 2.2MHz, integration factor = 5× to 31× (programmable)	7.65		31.3	µs

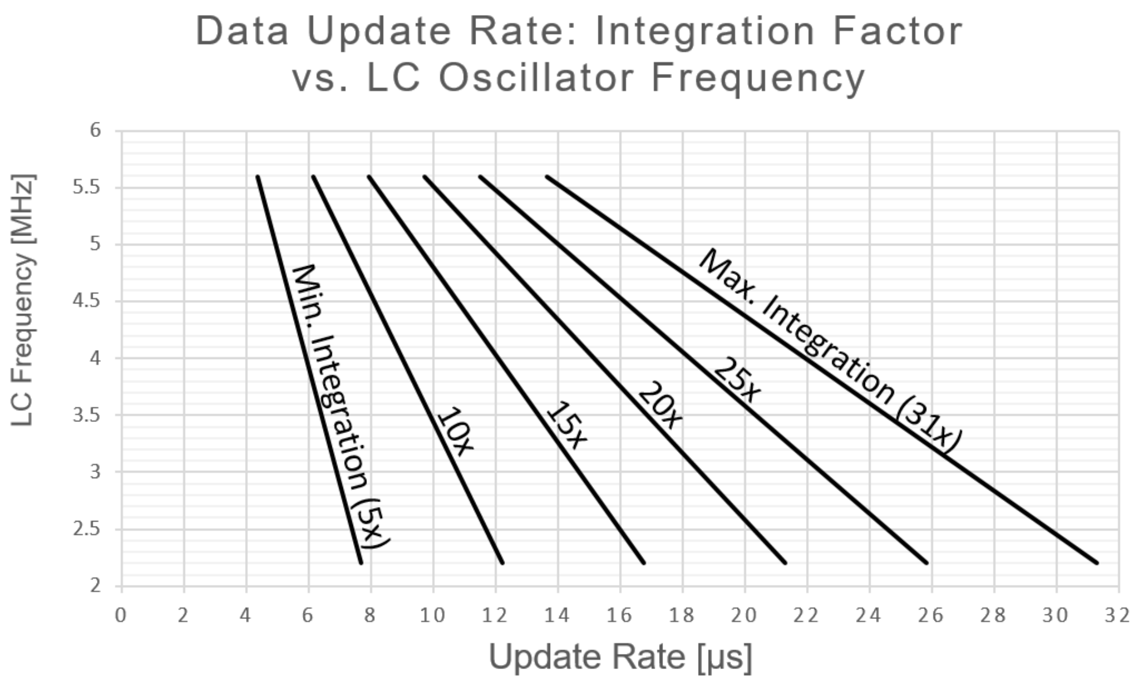


Figure 8. Data Update Rate vs. LC Oscillator Frequency vs. Integration Factor

9. Output Modes

9.1 Analog Differential Sine-Cosine Analog Output Mode

In this mode, both sine and cosine signals are available as full differential outputs. This configuration is recommended for best signal integrity and EMC performance.

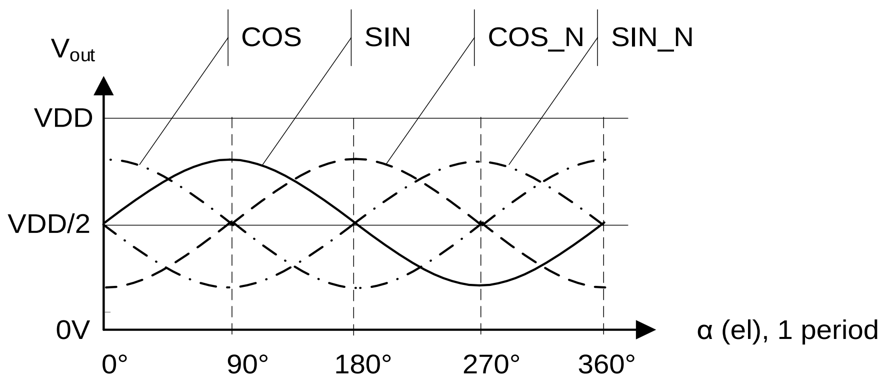


Figure 9. Sine-Cosine Analog Mode Output Signals

9.2 Analog Single Ended Sine-Cosine Analog Output Mode

In single ended mode, the SIN and COS signals are available with respect to GND. SIN_N and COS _N signals provide a buffered reference signal (VDD/2).

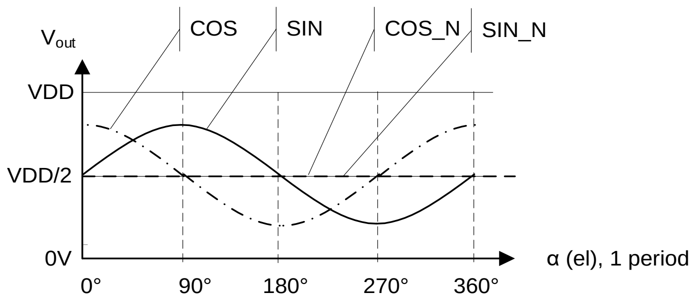


Figure 10. Sine-Cosine Analog Mode Output Signals

9.3 Digital Incremental Differential AB Mode

In AB incremental mode, four digital output signals have one symmetric period in every 360° electrical period.

Signal B is shifted by 90° (electrical) relative to signal A, allowing four states per 360° (electrical period), see Table 17.

Table 17**. Output Status in AB Incremental Mode**

State #	Position (Electrical)	Signal A	Signal A_N	Signal B	Signal B_N
1	0° >pos >=90°	1	0	1	0
2	90° >pos >=180°	1	0	0	1
3	180° >pos >=270°	0	1	0	1
4	270° >pos >=360°	0	1	1	0

Signals A_N and B_N are the inverted signals of A and B, allowing differential signal transmission for best signal integrity and EMC performance.

By having A and B phase shifted, the direction of rotation can be determined:

- Clockwise rotation: signal B is high at rising edge of A as shown in Figure 11 at 360° where moving from left to right (0° to 360°)
- Counter clockwise rotation: signal B is low at rising edge of A as shown in Figure 11 at 180° where moving from right to left (360° to 0°)

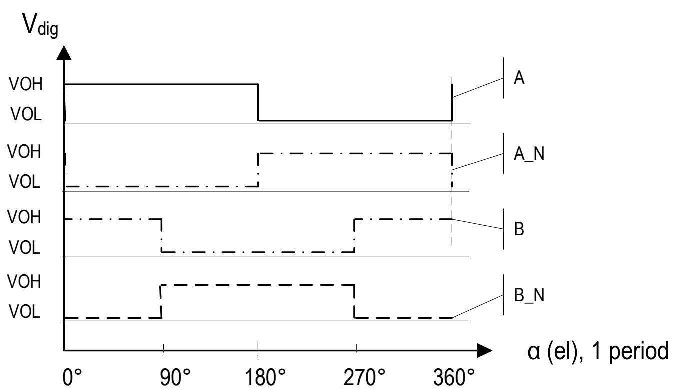


Figure 11. Digital Incremental Differential AB Mode Output Signals

Note that the AB output provides only one pulse per phase on each output. The number of pulses per revolution can be increased by coil designs having multiple periods per turn.

10. Operating at High Speed

The IPS2200 uses analog signal processing, so it can handle inputs signals at very high speed. The input signal can have a frequency of up to 4.16kHz, which is equivalent to 250000 RPM (electrical phases per minute). Even higher frequencies and therefore higher speeds are possible, but with reduced performance and signal amplitude.

The mechanical rotor speed can be calculated with Equation 10:

$$\text{rpm(mech)} = \frac{\text{rpm (el)}}{\text{coil periods}}$$ **Equation 10**

Where

rpm (mech) Rotation speed of the rotor (and target) in revolutions per minute.

rpm (el) Maximum electrical input frequency of the sensor in rpm (electrical)
= 250000 electrical periods per minute (rpm)
= 4166 electrical periods per second = 4.166kHz

coil periods Number of electrical periods per turn
= number of coil periods per 360° circle
= number of metal target segments

Figure 25 shows a design for a 6 pole motor (having 3 pole pairs) using a 3-periodic coil design.

The maximum mechanical rotation speed of this motor is calculated according to Equation 11.

$$\frac{250000\text{ rpm}}{3} = 83333\text{ rpm}$$ **Equation 11**

Table 18. Output Modes and Maximum Speed

	SIN/COS Output Mode	AB Output Mode		Maximum Rotor Speed
Target Design (metal/no metal)	**Sine, Cosine Cycles per Revolution**	**Quadrature Pulses per Revolution**	**Quadrature Counts per Revolution**	**Mechanical Speed**
1 × (180° / 180°)	1 × 360°	1	4	250000 rpm
2 × (90° / 90°)	2 × 180°	2	8	125000 rpm
3 × (60° / 60°)	3 × 120°	3	12	83333 rpm
4 × (45° / 45°)	4 × 90°	4	16	62500 rpm
6 × (30° / 30°)	6× 60°	6	24	41666 rpm
8 × (22.5° / 22.5°)	8 × 45°	8	32	31250 rpm
10 × (18° / 18°)	10 × 36°	10	40	25000 rpm
…	1 cycle per target	1 pulse per target	4 × counts per target	250000 RPM / targets per wheel

11. Block Diagram

Figure 12 shows the block diagram of the IPS2200.

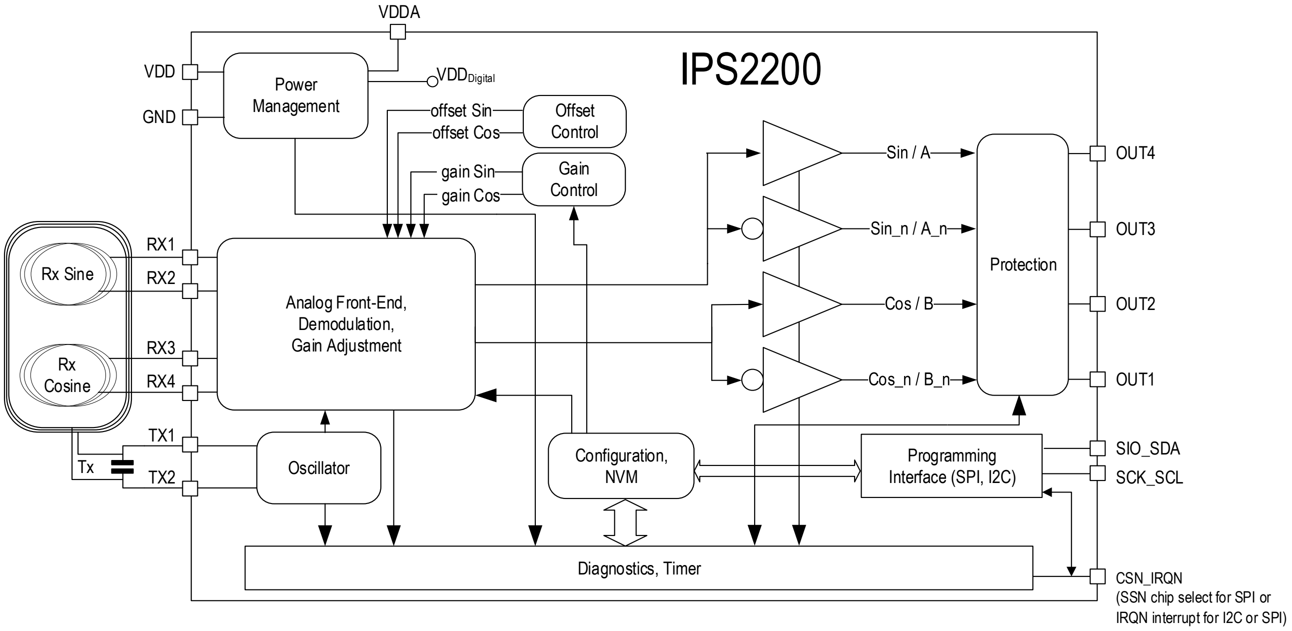


Figure 12. Block Diagram

The main building blocks include the following:

- Power Management: power-on-reset (POR) circuit; low drop-out (LDO) regulators for analog and digital supplies.
- Oscillator: generation of the transmitter coil signal.
- Analog Front-End:
  - Input filter, offset, and gain setting: analog AM signal preconditioning.
  - Synchronous integrator: demodulation of the AM signal.
- Offset Control: correction of offsets at the receiver coil inputs RX1/RX2 and RX3/RX4.
- Gain Control: correction of amplitude mismatching from RX1/RX2 and RX3/RX4 input signals.
- Configuration, NVM: nonvolatile storage of factory and user-programmable settings.
- Programming Interface: configuration, communication, and diagnostics via selectable I2C or SPI bidirectional interface.
- Diagnostics, Timer: Diagnostics for critical blocks to ensure functional safety and watchdog timer.
- Protection: over-voltage, reverse polarity and short circuit protection.

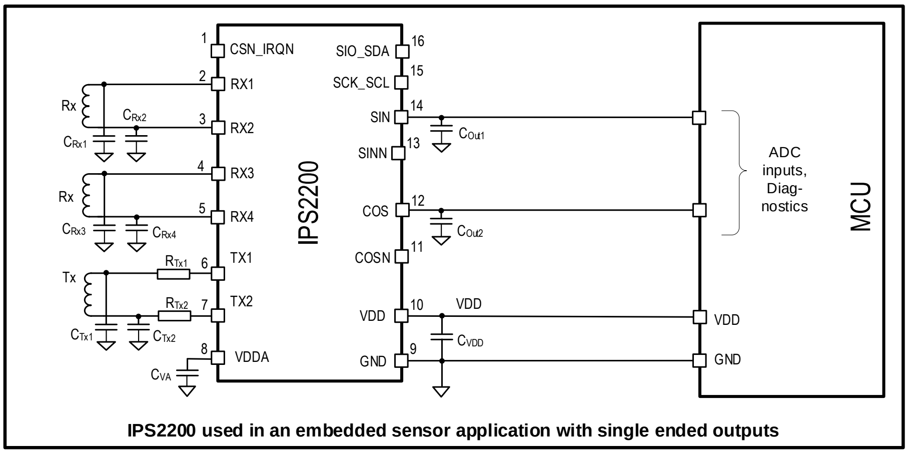
There are four interface options for the OUT1, OUT2, OUT3, and OUT4 pins (see Table 2):

- Differential analog output
- Single-ended analog output with reference
- Incremental digital AB pulse output (one pulse per phase)

12. Connection Options

Note: The IPS2200 must be programmed to match to the correct VDD voltage supply level (3.3V or 5.0V).
C_{RX1} to C_{RX4}, C_{Out1} to C_{OUT4}, and R_{Tx1}, R_{Tx2} are optional passive components for improved EMC performance. See Table 9, Table 10 and Table 12 for recommended component values.
Embedded applications include both position sensor and MCU on the same PCB, while in a remote application, the position sensor module and MCU are located on separate PCBs, connected by a cable.

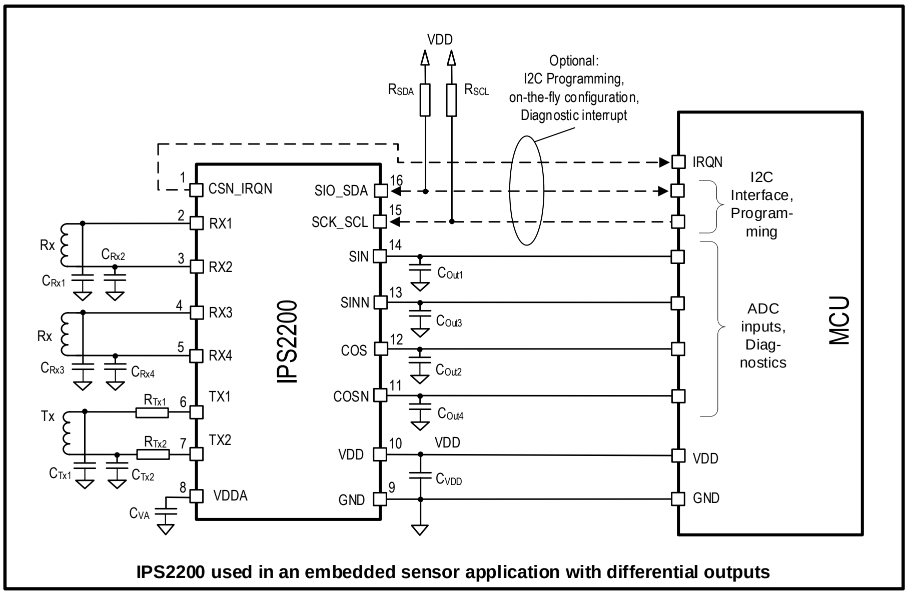
In the simplest form, the IPS2200 can be used as a position sensor with single ended sine and cosine outputs, as shown in Figure 13. The digital interface (SPI or I2C) used for programming and on the fly configuration is optional; it is not mandatory for normal operation.



IPS2200 used in an embedded sensor application with single ended outputs

Figure 13. Embedded Single Ended Sine, Cosine Outputs

A differential output configuration, as shown in Figure 14, provides improved signal robustness towards common mode disturbances. Either I2C or SPI may be used for on the fly configuration and programming without interrupting the analog signal flow on the sine and cosine outputs (see Figure 14, Figure 15 and Figure 16 for details).



IPS2200 used in an embedded sensor application with differential outputs

Figure 14. Embedded Differential Sine, Cosine Outputs

In remote applications, where sensor and microcontroller unit (MCU) are separated by a cable, additional safety measures may be implemented, for example the detection of broken or shorted wires between sensor and MCU. For this purpose, pull-up resistors (R_{P1} to R_{P4}, as shown in Figure 15 and Figure 16) or pull-down resistors may be introduced on the MCU inputs to detect these types of errors.

In normal operation, the output signal levels lie within the normal operating range, typically within 5% to 95% VDD. In case of broken signal wires or supply lines, the pull-up or pull-down resistors pull the output voltage into the signal diagnostic range: <5% VDD for pull-down and >95% for pull-up.

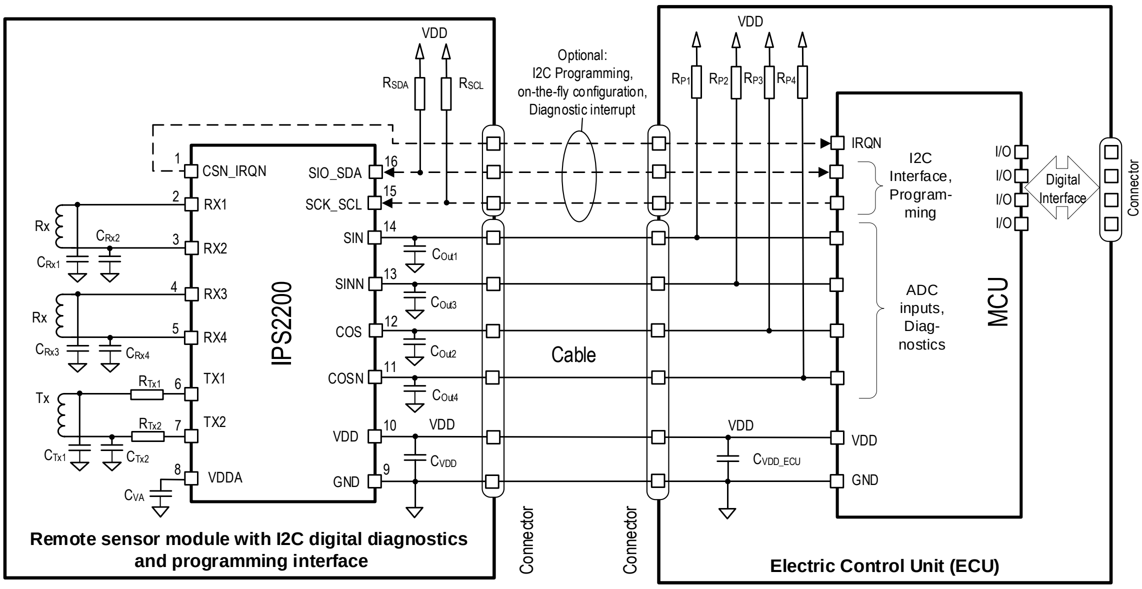


Figure 15. Remote Differential Sine, Cosine Outputs with I2C Interface

If I2C is selected as digital diagnostic and programming interface (Figure 15), pull-up resistors R_{SDA} and R_{SCL} are required, for the SPI interface (Figure 16) a pull-up resistor R_{CSN} is required for the CSN input. In the SPI interface, pin #1 (CSN_IRQN) may be used for both chip select input (CSN) and interrupt output (IRQN). In this case, the CSN output of the MCU must be an open drain output.

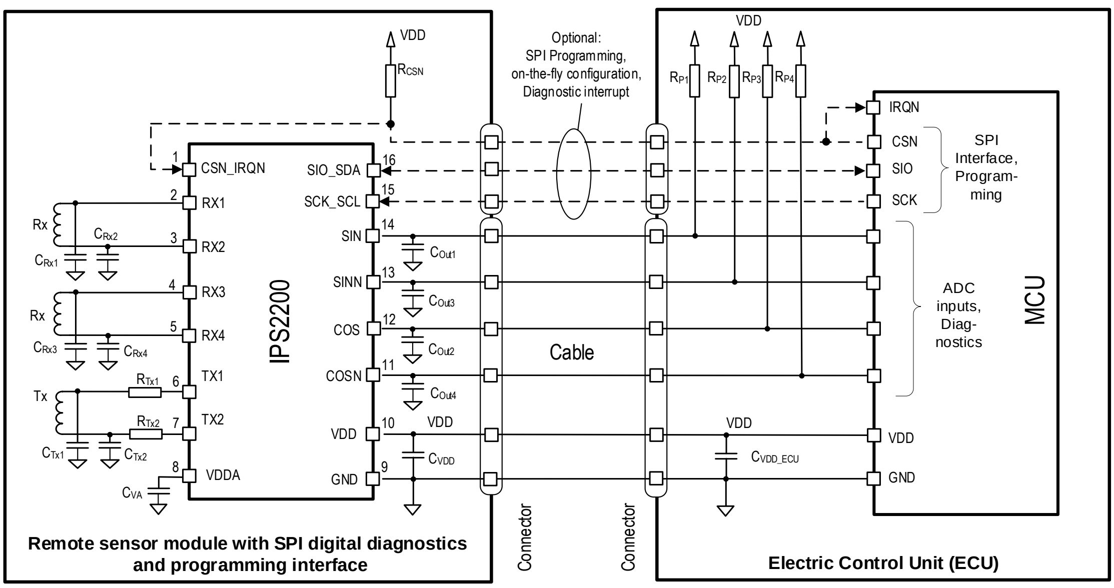


Figure 16. Remote Differential Sine, Cosine Outputs with SPI Interface

13. Digital Diagnostics and Programming Interfaces

In order to program the IPS2200 and to enable fast diagnostics without interrupting the analog high speed signal path, an additional digital serial interface is available.

The IPS2200 offers four modes of digital communication for the diagnostics and programming interface:

- I2C interface with interrupt (programming option).
- I2C interface with address select (default setting).
- Half duplex SPI interface (programming option).
- Half duplex SPI interface with interrupt (programming option).

13.1 Supply Voltage Operation: 3.3V or 5V

The IPS2200 can be programmed to operate with either a 3.3V ±10% or a 5.0V ±10% supply voltage.

If the IPS2200 is programmed for the 5V operation, but connected to a 3.3V supply, it will be in a 5V under-voltage state. However, it can still be programmed for 3.3V operation. After the next power-on-reset, the IPS2200 boots as a 3.3V device.

If the IPS2200 is programmed for 3.3V operation, but connected to a 5V supply, it will be in a 3.3V over-voltage state. However, it can still be programmed for 5.0V operation. After the next power-on-reset, the IPS2200 boots as a 5.0V device.

13.2 Half-Duplex SPI Interface

This is a standard bi-directional, half-duplex SPI interface.

Note: By default, I2C is enabled as the standard communication interface. To enable communication over SPI, it must be enabled through programming over the I2C interface.

To operate the I2C interface, pull-up resistors are required for pins SIO_SDA and SCK_SCL. Optionally, these two resistors can either remain active or be removed for SPI operation. A pull-up resistor is always required for pin CSN, see Figure 17.

After re-programming, the SPI interface becomes active with the next POR and the chip remains with SPI enabled as communication interface.

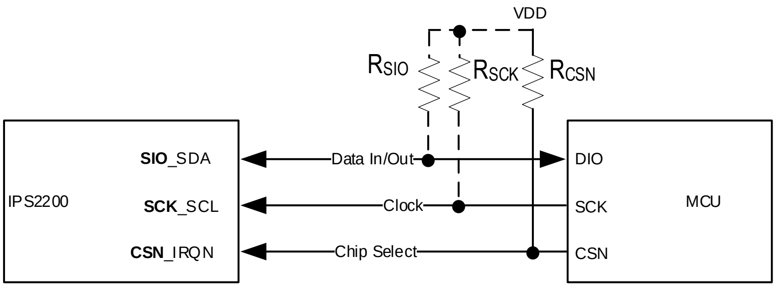


Figure 17. Half Duplex 3-3 Wire SPI Interface

A master can communicate with multiple slaves. Each slave device has an independent CSN line but shares the SCK and SIO lines with all slaves. A slave is only addressed when the corresponding CSN pin is pulled low.

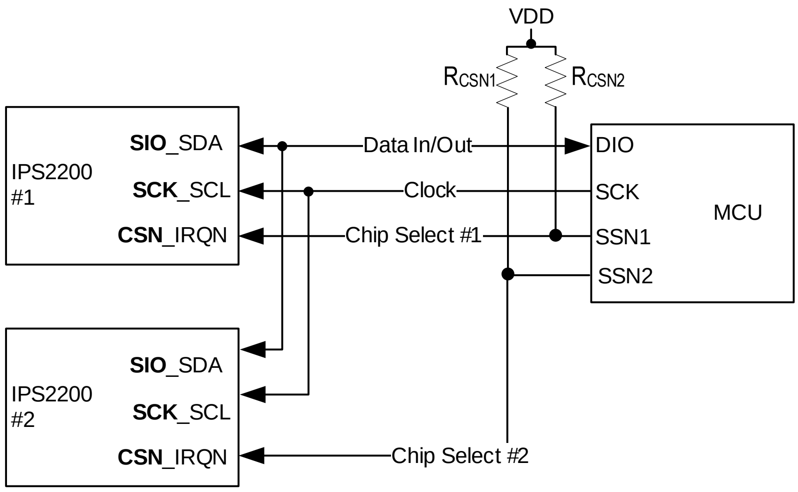


Figure 18. Half Duplex 3-3 Wire SPI Multi-slave Interface

The SPI slave module is activated by the SPI 3-wire master, which initiates the transaction by pulling the chip-select pin low (CSN_IRQN, pin 1). A serial clock (SCK_SCL, pin 15), is driven by the master. The Serial Data In/Out line (SIO_SDA, pin 16) is a bidirectional data line between master and slave. In a typical scenario, the master transmits a command with a specified length of 8-bit over the SIO line. If it is a write command, the master keeps transmitting data over the same line. If the first bits were a READ command, the slave transmits a fixed length of data over the SIO line to the master.

Table 19. SPI Interface Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
CL_{SPI}	SPI clock rate				100	Kbit/s
t_{R_SIO}	Rise time of SIO	Signal level change from 10 to 90%; ≤15pF capacitive load			35	ns
t_{F_SIOL}	Fall time of SDA or SCL	Signal level change from 90 to 10%; ≤15pF capacitive load			35	ns

Note: In Figure 17, Figure 18, Figure 20, Figure 21, and Figure 22, for IPS2200 pins that have dual functions, the function that is active is shown in **bold** font**.**

For a detailed description of the SPI interface, refer to the *IPS2200 Programming Guide.*

13.3 I2C Interface

The IPS2200 includes a standard I2C interface as the default interface. The I2C address is programmable. In addition, the CSN_IRQN pin can be programmed as either an I2C address selection (SEL) pin or as an interrupt output (IRQN) pin when using the I2C interface (see Table 3). The IPS2200 is configured as a I2C slave, several slaves can be connected in parallel on the I2C bus.

Table 20. I2C Interface Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
CL_{I2C}	I2C clock rate				100	Kbit/s
t_{SCL_LOW}	Low level state of SCL clock		4.7			µs
t_{SCL_HIGH}	High level state of SCL clock		4.0			µs
$t_{R\_SDA\_SCL}$	Rise time of SDA or SCL	Signal level change from 10 to 90%			1000	ns
$t_{F\_SDA\_SCL}$	Fall time of SDA or SCL	Signal level change from 90 to 10%			300	ns

Two wires, serial data (SIO_**SDA**, pin 16) and serial clock (SCK_**SCL**, pin 15), carry information between the devices connected to the bus. Both SDA and SCL are-connected to the positive supply voltage VDD via an external pull-up resistor. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function.

An external master (host controller) initiates a transfer, generates clock signals, and terminates a transfer. The implementation supports the I2C slave function, which is addressed by the master and supports the I2C bus specification version 2.1.

13.3.1. I2C with Address Selection (Default Setting)

When the IPS2200 is programed to use the I2C interface with address selection, the **CSN**_IRQN pin is used to select the I2C slave address by hardware.

By default, the CSN_IRQN pin (#1) is used to define the IPS2200 I2C slave address by hardware pin strapping.

The status of this pin is mirrored in I2C Address Bit A3 and the inverted status of this pin is mirrored in I2C Address Bit A0 of the 7-bit I2C address (see Figure 19).

The default setting of I2C Address bit A4 =1.

If CSN_IRQN is tied to ground, the IPS2200 default slave address is 001**0**00**1** (binary) = 0x11 (Hex), while if this pin is connected to VDD, the IPS2200 I2C address is 001**1**00**0** (binary) = 0x18 (Hex).

In addition, hardware address pin strapping may be disabled and the user may define a specific I2C address, storing it into the NVM address bits A6 to A3 (see the *IPS2200 Programming Guide* document for details).

Table 21 shows the different options for selecting the I2C Address by combinations of pin addressing and NVM Address register setting.

I2C address bits A3 to A6 can be configured in the NVM for an individual I2C address, allowing up to 14 devices to be addressed in parallel, see the *IPS2200 Programming Guide* document for details.

Table 21. I2C Address Selection Options in NVM

I2C Address Selection Mode	A6	A5	A4	A3	A2	A1	A0
Default setting	0	0	1	Pin#1	0	0	Pin#1 inverted
User programmable range, with I2C address selection by pin #1	001 to 110 (binary)			Pin#1	0	0	Pin#1 inverted
User programmable range, with fixed I2C address	0001 to 1110 (binary)				0	0	0

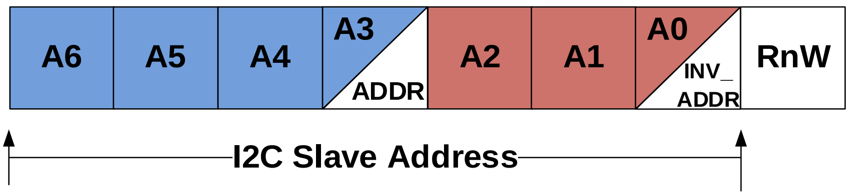


Figure 19. I2C Address Select Bits

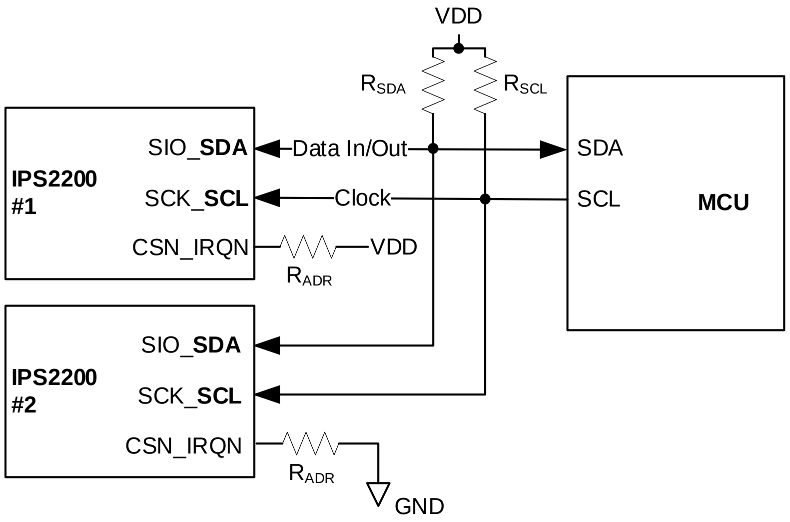


Figure 20. I2C Interface with Address Select

13.3.2. I2C Interface with Interrupt (Programming Option)

When the IPS2200 is programed to use the I2C interface with the interrupt function, it operates as a standard I2C interface. The I2C address is programmable in the NVM. In this mode, the CSN_**IRQN** pin, which is by default used as an address input pin (see 13.3.1) can be programmed as a push/pull interrupt output for fast signaling of diagnostic events.

Note: to program this option from the default setting (where CSN_IRQN = Address select, see 13.3.1), the CSN_IRQN pin is initially configured as an address input pin, therefore it must be forced to GND or to VDD so it has a defined hardware I2C address for this initial programming. Once the mode “I2C Interface with Interrupt” is programmed, the new I2C address is taken from the programmed address in the nonvolatile memory and CSN_IRQN becomes a push/pull output.

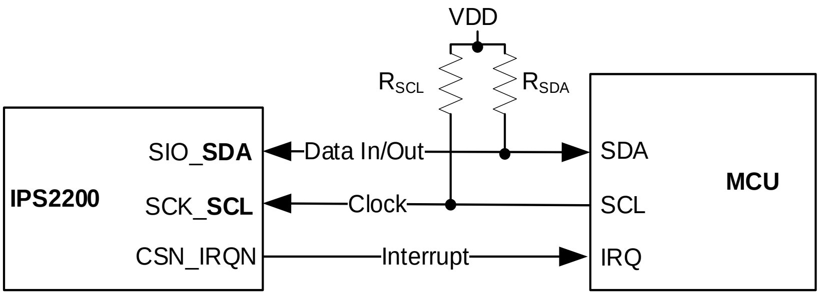


Figure 21. I2C Interface Configuration with Interrupt on a Single Slave

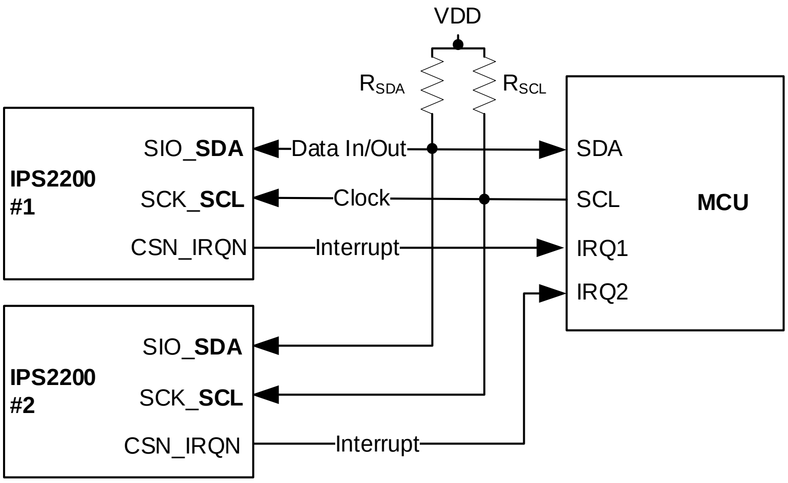


Figure 22. I2C Interface Configuration with Multi-slave Interrupt

For a detailed description of the I2C interface, refer to the *IPS2200 Programming Guide.*

14. Protection and Diagnostics

14.1 I/O Protection

In order to meet the requirements for over-voltage and reverse-polarity protection on both the output and power supply pins, the IPS2200 includes several protection and diagnosis features:

1. Protection against short circuit of the output pins SIN, SINN, COS, and COSN to GND or to VDD
2. Over-voltage and reverse-polarity protection:
   a. On supply pin VDD to GND
   b. On analog output pins SIN, SINN, COS, and COSN to GND
   c. On digital output pins SIO_SDA, CSN_IRQN, and SCK_SCL to GND

15. Programming Options

The IPS2200 family offers a variety of programming options. The IC is programmed through the digital bi-directional SPI or I2C interface. The main programming functions are described in Table 22.

15.1 Lock Feature (Cyber Security)

The IPS2200 contains a write lock bit option, which can be set by the user. Once the write lock bit is set, no further writing to the chip is possible.

Note: For programming details, see the *IPS2200 Programming Guide*, which is available from Renesas on request.

Table 22. Programming Options Overview

Function	Programming Options
Supply voltage range	3.3V ±10% or 5.0V ±10%, alarm levels
High speed interface	Sine/cosine differential, single-ended, A/B
Digital diagnostic and programming interface	Half-duplex SPI, half-duplex SPI with interrupt, I2C with address select, I2C with interrupt
SPI interface	SPI modes with/without interrupt, clock polarity, clock phase Data order: MSB first / LSB first
I2C interface	Slave address, I2C mode with address select or with interrupt
Diagnostic signaling on high speed interface	Enable/disable: Output pins are pulled low or high in diagnostic state
Security lock function	Register access R/W / read-only

Function	Programming Options
RF front end integration cycles	Number of integration cycles; adjust noise vs. speed
Receiver overall gain	Overall gain coarse adjustment
Sine, cosine channel gain	Amplitude mismatch correction, fine adjustment
Sine, cosine offset	Pre-adjustment of input offsets
Tx oscillator	Bias current, optimization of coil performance
Time base counter	Measurement of Tx oscillator frequency, upper/lower frequency alarm
Interrupt	Enable/disable interrupt events

16. Diagnostics

The diagnostics described in Table 23 are performed on the chip level and are flagged in corresponding registers if a fault detection occurs. Each of these diagnostic functions can be enabled or disabled to generate an interrupt event at the CSN_IRQN output. In addition, an interrupt event can also be signaled through the high speed interface pins (SIN, SINN, COS, COSN; see Table 2) by putting them into the diagnostic state.

Alarm types marked as "Static" will remain set while the error persists and are cleared only by power-on-reset (POR); alarm types marked as "Temporary" will be cleared when the source of the error is removed.

Diagnostic flags marked as "Continuous" are continuously tested; diagnostic flags marked as "Start-up" are checked at start-up only.

Table 23. Diagnostic Features

Diagnostic Flag	Type	Active	Description
VDD over-voltage	Temporary	Continuous	If the external supply voltage exceeds the maximum limit of typical +10%, this flag is asserted. To avoid a flag toggling, a comparator hysteresis is implemented. See Table 7 for alarm levels in 3.3V Mode and Table 8 for alarm levels in 5V Mode.
VDD under-voltage	Temporary	Continuous	If the external supply voltage falls short of the minimum limit of typical -10%, this flag is asserted. To avoid a flag toggling, a comparator hysteresis is implemented. See Table 7 for alarm levels in 3.3V Mode and Table 8 for alarm levels in 5V Mode.
Data access fail	Temporary	Continuous	Chip internal failure.
Protocol integrity fail	Temporary	Continuous	Failure in the I2C/SPI data transfer.
Shadow register DED	Static	Continuous	Shadow register bank double-bit error detection.
Shadow register SED	Temporary	Continuous	Shadow register bank single-bit error detection. Each single-bit error detection triggers a single-bit error correction (SEC) of the register output.
Nonvolatile memory DED	Static	Start-up	NVM double-bit error detection. Each individual addressed word is checked and flagged for bit error.
Nonvolatile memory SED	Temporary	Start-up	NVM single-bit error detection. Each individual addressed word is checked and flagged for bit errors. Each single-bit error detection triggers a single-bit error correction (SEC) of the NVM output.
LC oscillator failure	Temporary	Continuous	This flag is set when the LC oscillator frequency is out of range. The frequency range is programmable; see section 16.2 for details.
LC oscillator stuck	Temporary	Continuous	This flag is set when the LC oscillator stops running.
VDDA under-voltage or CSN_IRQN over-voltage or SIO_SDA over-voltage	Temporary	Continuous	This flag is set when the internally regulated analog supply voltage VDDA falls below specified limits or when an over-voltage on pins CSN_IRQN or SIO_SDA is detected. See Table 7 or Table 8 for VDDA alarm levels and Table 4 for IRQN_CSN and SIO_SDA over-voltage alarm levels.
Low amplitude	Temporary	Continuous	In the Incremental Digital Mode, a minimum signal level must be defined (gain factor) for a valid output function. If this flag is asserted, the gain factor must be increased.
Internal bus failure	Temporary	Continuous	Chip internal failure.
IRQN watchdog failure	Static	Continuous	A cyclic interrupt request can be initiated by starting a watchdog counter. When the timer is expired, the interrupt flag is asserted and the timer restarts. The timer can be stopped by resetting the watchdog value to zero.
Mechanical damage	Static	Continuous	The chip is checked for mechanical damage (cracks in the silicon)

Diagnostic Flag	Type	Active	Description
Output buffer failure	Temporary	Continuous	This flag is set when the mean value of analog outputs SIN+SINN or COS+COSN differs from VDD / 2 by more than the specified limits described in Table 12.
Output buffer overload	Temporary	Continuous	This flag is set when the output amplifier load current is above the specified limits.
R1 to R2 coil short	Static	Start-up	A short between the receiver coils R1 and R2 is checked after POR. The check result is stored and flagged until the next POR.
R2 coil failure	Temporary	Continuous	This flag is set if there is a short between receiver coil R2 and GND, a short between receiver coil R2 and VDD, or an open receiver coil R2.
R1 coil failure	Temporary	Continuous	This flag is set if there is a short between receiver coil R1 and GND, a short between receiver coil R1 and VDD, or an open receiver coil R1.

16.1 Internal Register and Memory Errors

For all registers, volatile and nonvolatile memories, a cyclic redundancy check (CRC) is implemented, allowing 2-bit error detection and 1-bit error correction. An alarm flag is set when a CRC error occurs.

16.2 LC Oscillator Frequency Out of Range

The typical frequency range for the transmitter LC oscillator is from ~2MHz to 5MHz, which is the open frequency band between the medium-wave radio band (0.52MHz to 1.73MHz) and the short-wave radio band (5.8MHz to 6.3MHz). Due to the use of external components (printed inductor and discrete capacitor), the Tx oscillation frequency will change over temperature, mainly depending on the temperature coefficient of the discrete capacitor (see C_T in the application circuit on page 1).

Recommendation: Use a capacitor with a low temperature coefficient (see the recommendation given below Table 9).

In order to ensure that the oscillation frequency is within the boundaries of a given application, the oscillation frequency of the Tx oscillator is internally measured and displayed as a proportional value in a register. The user can select upper and lower limits for these register values that will create an alarm flag when the oscillation frequency is outside of these programmable boundaries.

17. Application Examples

Typical coil and target arrangements are shown in Figure 23 to Figure 26: As examples, rotary designs for 1 × 360°, 2 × 180°, 3 × 120° and 4 × 90° are shown. Many other combinations (essentially any *n* x 360/*n*) are possible, where *n* is an integer number.

For example, in sensor designs for brushless DC rotor position feedback, *n* could be the number of pole pairs on the rotor. In such cases, the output signal of the IPS2200 would be one electric period per each pole pair.

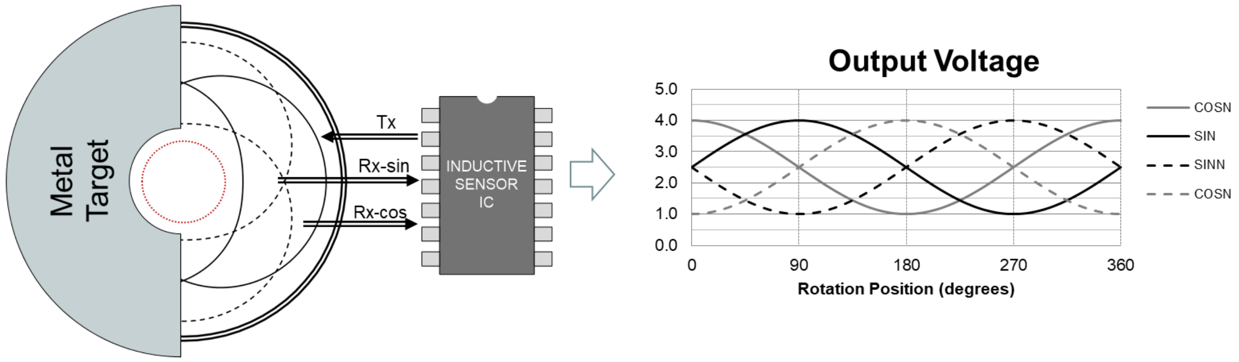


Figure 23. Coil Design and Signal Output for a 360° Rotary Sensor

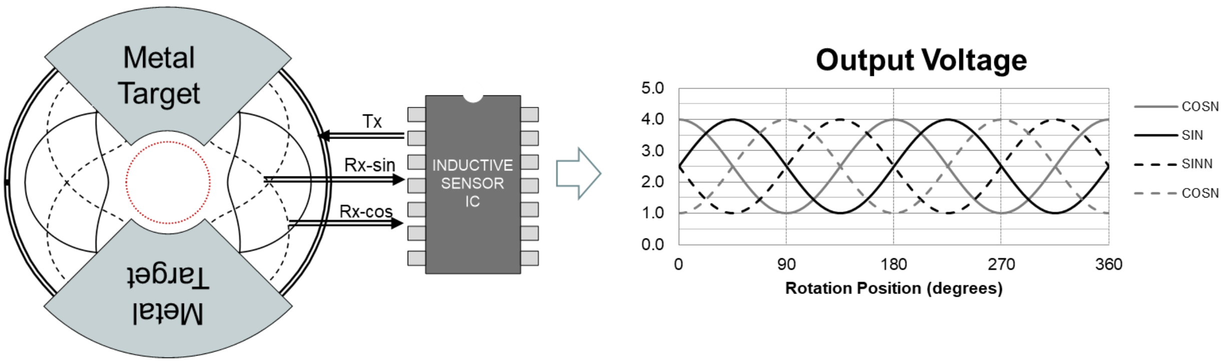


Figure 24. Coil Design and Signal Output for a 2 × 180° Rotary Sensor

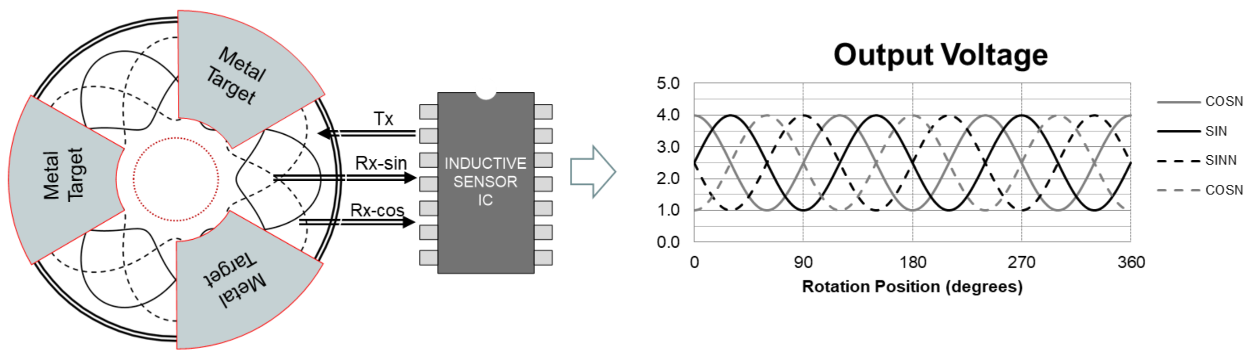


Figure 25. Coil Design and Signal Output for a 3 × 120° Rotary Sensor

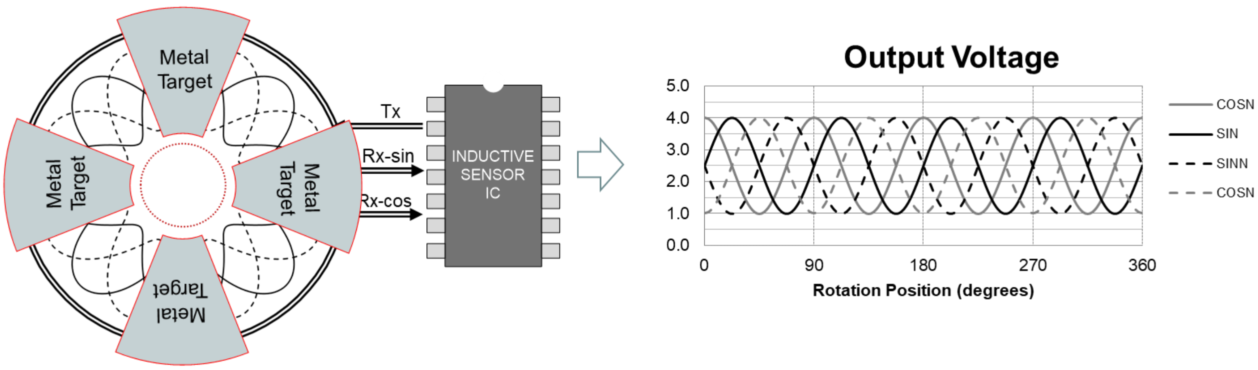


Figure 26. Coil Design and Signal Output for a 4 × 90° Rotary Sensor

18. Electromagnetic Compatibility (EMC)

Guidelines for EMC compliant circuit designs are available in a separate document "IPS2200 EMC recommendations" on request.

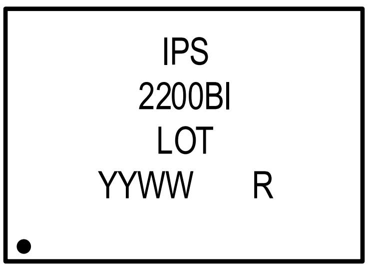
19. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/16-tssop-package-outline-drawing-44mm-body-065mm-pitch-pgg16t1

20. Marking Diagram

20.1 Marking of Production Parts



Line 1: First characters of part code (IPS); "ES" is added for engineering samples

Line 2: Next four characters of the part code (2200) followed by
B = Design revision
I = Operation temperature range, Industrial

Line 3: "LOT" = Lot number

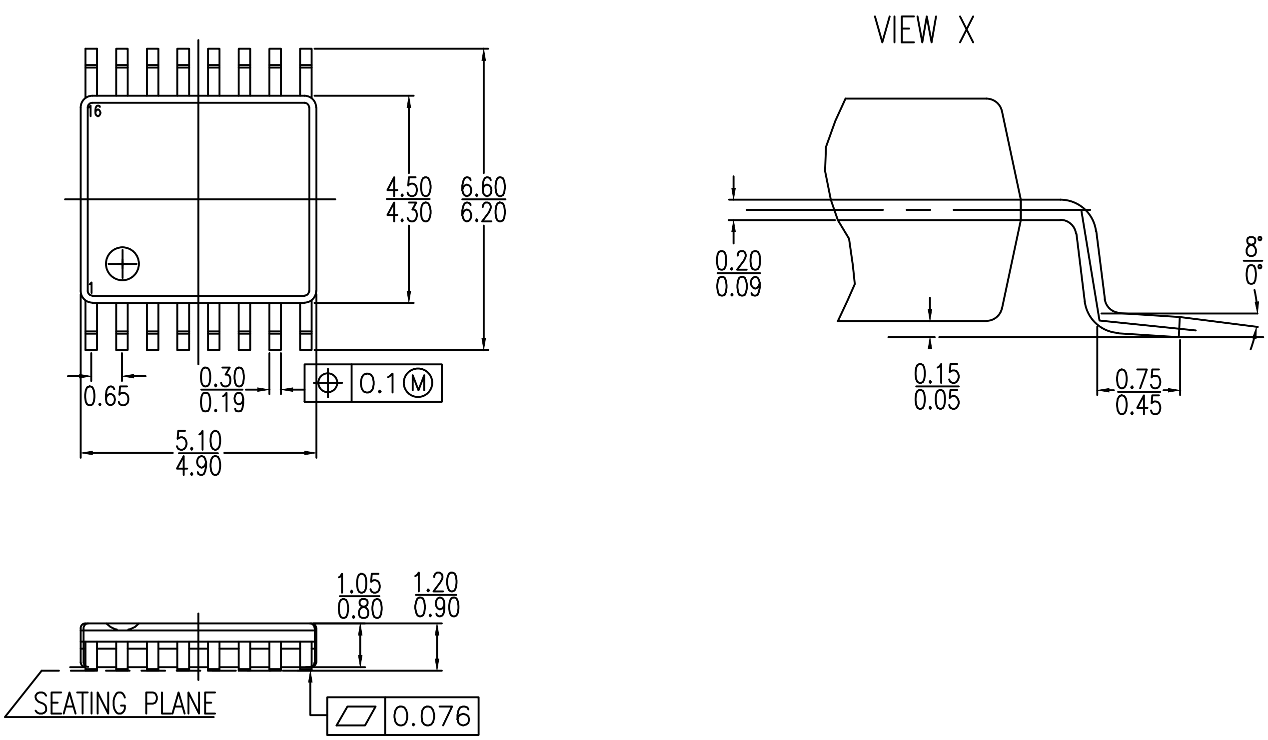
Line 4: "YYWW" = Manufacturing date:
YY = last two digits of manufacturing year
WW = manufacturing week
R = RoHS compliant statement

21. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
IPS2200BI1W	16-TSSOP, 4.4 ×5.0 mm	1	7” Reel, 500 parts / reel	-40° to +125°C
IPS2200BI1R	16-TSSOP, 4.4 ×5.0 mm	1	13” Reel, 4000 parts / reel	-40° to +125°C
IPS2200STKIT	IPS2200 Starter Kit including USB communication board, application module and connection cables			

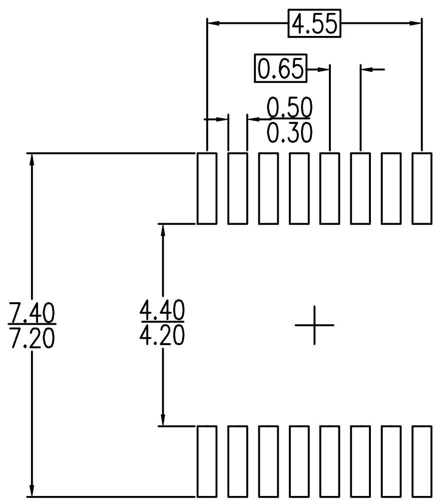
22. Revision History

Revision	Date	Description
1.5	Aug.5.22	• I2C with Address Selection (Default Setting) updated • Updated connection options, chapter 12 • Corrected ESD limits, Table 5 • Updated operating conditions, Table 6
1.4	Apr.22.21	Order information updated
1.3	Jan.18.21	SPI interface description updated
1.2	Jul.15.20	Pin naming aligned with other position sensor products
1.1	Jul.1.20	Formulas added for calculating the LC oscillator frequency.
1.0	Apr.15.20	Official release for product launch • 3.3V and 5V supply voltage operation changed. • Circuit and block descriptions updated. • Values updated for absolute maximum ratings, operating conditions, and electrical characteristics. • Updated formatting. • Section 9 (Output Modes) is added.
0.1	Feb.16.19	Preliminary release.



NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS



LAND PATTERN DIMENSIONS

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
Jan 26, 2018	Rev 00	Revised from PSC-4056-02 PGG16

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