# ISL1801

sPMIC for Micro Converter Bias and Drivers

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The ISL1801 is a power management IC (PMIC) optimized for solar array micro converters and other systems operating from a high voltage DC supply. The ISL1801 can be used in buck, boost or buck-boost microconverter topologies in order to maximize the energy harvest from a solar array. In addition to the power stage and main controller, the ISL1801 includes the bias regulators, gate drivers, current sense amplifier and comparators needed for micro converters.

The ISL1801 integrates two switching regulators that can be used to generate the driver and the micro-controller (MCU) power supplies. In addition, it has a low offset, low drift amplifier for current sensing, two comparators for overvoltage and overcurrent protection plus a watchdog timer to reset the MCU if necessary. This single IC solution offers high integration and dramatically reduces the total number of components in the microconverter system improving the system reliability and reducing cost.

The first regulator takes input voltages ranging from 9V to 90V from the solar panel and outputs a regulated supply for drivers and the secondary regulator. The secondary regulator converts the output of the first regulator to a programmable micro-controller supply, typically 3.3V. A high voltage start-up LDO provides the necessary bias voltage until the switching regulator is operating.

The ISL1801 integrates two high-speed MOSFET drivers for buck, flyback or boost converters configured as shown in the application schematics. The Drive3 also has the integrated peak current limiting capabilities.

The ISL1801 includes comprehensive start-up, shutdown and fault logic to ensure reliable operation of micro converters in solar applications.

## Features

- 90V input buck switching regulator
  - 120mA (minimum) output with OCP, OVP, OTP
  - Integrated upper and lower MOSFETs
- 90V on-chip start-up 6.7V LDO
- Low voltage buck switching regulator
  - 200mA (minimum) output with OCP, OVP
  - Integrated upper and lower MOSFETs
  - PGOOD output
- Low voltage bias LDO
  - Input voltage range from 6V to 14V
  - Regulated 5V output up to 10mA
- Dual high-speed gate driver
  - 14V voltage rating
  - 2A peak sourcing and 5A peak sinking current
  - Peak current limit for DRIVE3
- Dedicated amplifier for accurate current sense
- Two comparators for general purpose protection
- Integrated watchdog timer

## Applications

- Solar power optimizer
- Solar power micro-inverter
- Solar charge controller
- Telecom power supply

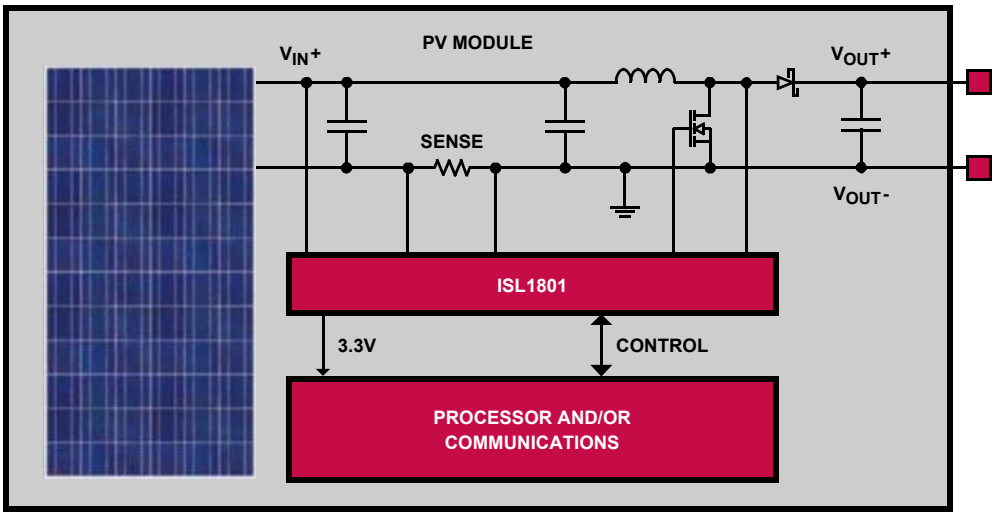



FIGURE 1. TYPICAL APPLICATION

# Table of Contents

# Block Diagram

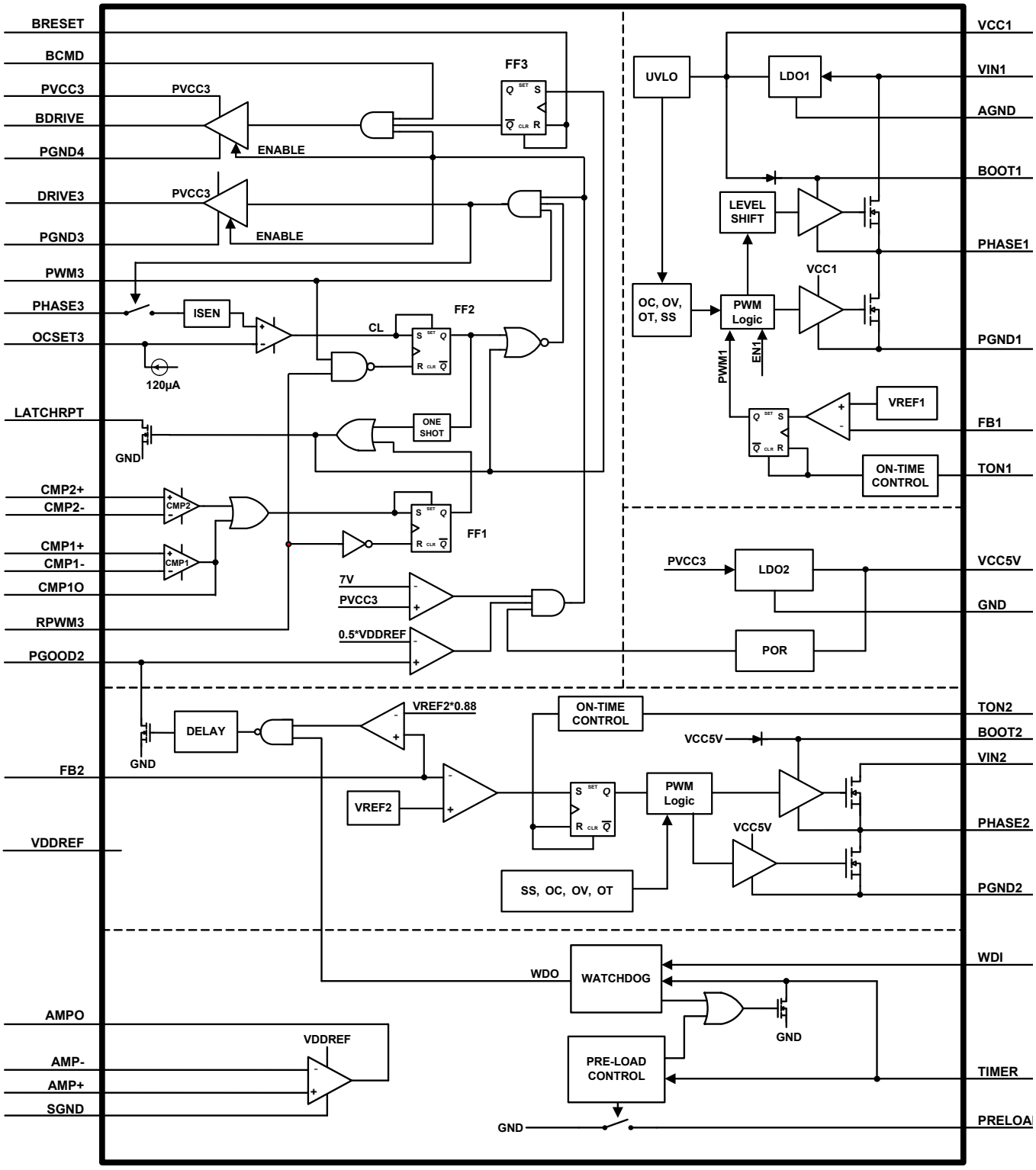
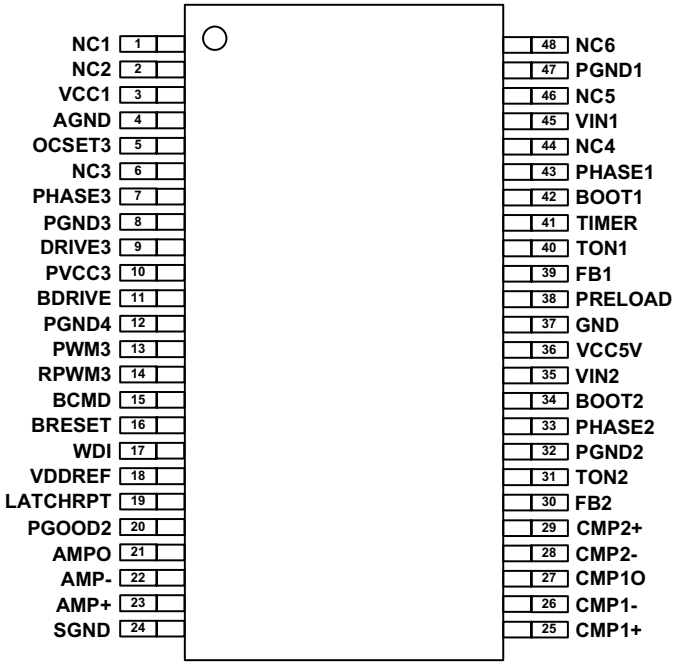



FIGURE 2. ISL1801 BLOCK DIAGRAM

# Pin Configuration

ISL1801
(48 LD TSSOP)
TOP VIEW




# Pin Descriptions

| PIN# | PIN NAME | DESCRIPTION |
|---|---|---|
| 1, 2, 6, 44, 46, 48 | NC1, NC2, NC3, NC4, NC5, NC6 | NC pin. |
| 3 | VCC1 | High voltage start-up LDO1 output and also the pin providing bias to the HV circuitry on the ISL1801. Place a 1µF ceramic capacitor from this pin to ground as decoupling cap. Connect this pin to the output of the high voltage regulator. When the output of the switching regulator is stable, the start-up LDO is disabled and the chip bias is supplied by the more efficient switching regulator.<br>Note: As VCC1 is the power supply of the high voltage die, DO NOT connect it to any low impedance potential by any means. This may damage the device. |
| 4 | AGND | Analog ground pin for VCC1. |
| 5 | OCSET3 | A resistor between this pin and ground set the peak current limit threshold for the power stage MOSFET at Phase3. The 0.01µF capacitor can be used at this pin to filter any switching noise. |
| 7 | PHASE3 | The phase node pin of the power stage controlled by DRIVE3. This pin should be connected to the drain of the power MOSFET through one resistor and diode which prevent the voltage at Phase3 pin from dropping below -0.6V. Refer to the typical application schematics starting on page 24. for correct connections. |
| 8 | PGND3 | The ground pin for the high-speed driver DRIVE3. |
| 9 | DRIVE3 | The output of the high-speed driver. |
| 10 | PVCC3 | The bias input pin for both the high-speed driver and the low speed driver. It is normally connected to $V_{OUT1}$. The PVCC3 also powers LDO2 which provides the bias supply for all internal control circuits. |
| 11 | BDRIVE | The output of the high-speed driver controlled by the BCMD signal. |
| 12 | PGND4 | The ground pin for BDRIVE. |
| 13 | PWM3 | The PWM input signal for DRIVE3. |

## Pin Descriptions (Continued)

| PIN# | PIN NAME | DESCRIPTION |
|---|---|---|
| 14 | RPWM3 | The reset signal for both flip-flops in the LATCHRPT circuit and overcurrent-protection circuit of DRIVE3/PHASE3. The RPWM3=0 will reset both flip-flops. Avoid running PWM3=1 with RPWM3=0 for a long time or at very high frequency, since it may result in very high switching frequency at DRIVE3 in the overcurrent protection condition. |
| 15 | BCMD | Logic input to control BDRIVE. |
| 16 | BRESET | Logic input to reset the LATCHRPT flip-flop in the BDRIVE control circuit. |
| 17 | WDI | Watchdog circuit clock input signal. |
| 18 | VDDREF | Reference signal for output signals to the MCU. Connect this pin to $V_{OUT2}$, which provides a clamp voltage for all the output pins (CMP1O, AMPO) interfacing with the MCU. |
| 19 | LATCHRPT | Open drain output signal. When either comparator or Phase3 overcurrent protection is triggered, this pin is pulled LOW to inform the MCU. The two internal flip-flops used to latch these faults can be reset by setting RWPM3=0. |
| 20 | PGOOD2 | Open drain output pin indicating power-good for the low voltage regulator. A logic low signal at the watchdog output will also pull this pin LOW allowing it to reset the MCU in either fault condition. |
| 21 | AMPO | Integrated amplifier output. |
| 22 | AMP- | Integrated amplifier inverting input. |
| 23 | AMP+ | Integrated amplifier non-inverting input. |
| 24 | SGND | The ground pin of the sensitive control circuits biased by VCC5V. Connect this pin to a ground plane with minimum noise. |
| 25 | CMP1+ | Comparator 1 non-inverting input. |
| 26 | CMP1- | Comparator 1 inverting input. |
| 27 | CMP1O | Comparator 1 output. This signal also triggers the flip-flop for the LATCHRPT signal. |
| 28 | CMP2- | Comparator 2 inverting input. |
| 29 | CMP2+ | Comparator 2 non-inverting input. |
| 30 | FB2 | The feedback sense pin for the low voltage switching regulator. The output voltage is programmable by a resistor divider feeding back the output voltage. |
| 31 | TON2 | On time adjustment for the secondary (low voltage) switching regulator. Connect a resistor from this pin to the input voltage of the low voltage regulator to adjust the on time and switching frequency. |
| 32 | PGND2 | The ground pin of the low voltage switching regulator's power stage. There are switching power current pulses coming out of this pin. Place the ground pad of the input power stage decoupling cap as close to this pin as possible. |
| 33 | PHASE2 | The phase node of the low voltage switching regulator. This pin should be connected to the output inductor. |
| 34 | BOOT2 | The boot pin of the low voltage switching regulator. An external bootstrap capacitor is required. This pin provides bias voltage to the high-side MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive the internal N-channel MOSFET. The boot diode is included within the IC. |
| 35 | VIN2 | Input of the low voltage switching regulator. This pin is connected to the drain of the internal high-side MOSFET. |
| 36 | VCC5V | The output of the internal 5V LDO providing the bias supply for the IC. A 1µF ceramic decoupling capacitor should be placed from this pin to ground. |
| 37 | GND | The analog ground pin. |
| 38 | PRELOAD | Place a resistor from this pin to $V_{OUT1}$ to provide the loading for the high voltage switching regulator. When this load can be successfully driven, the low voltage switching regulator will be enabled. If the PV module output power is insufficient, the low voltage switching regulator will not start. |
| 39 | FB1 | The feedback sense pin for the high voltage switching regulator. The output voltage is programmable by a resistor divider feeding back the output voltage. |
| 40 | TON1 | On time adjustment for the high voltage switching regulator. Connect a resistor from this pin to the input voltage of the high voltage regulator to adjust the on time and switching frequency. |
| 41 | TIMER | Tie a resistor from VCC5V to this pin and a cap from this pin to ground. The RC time constant sets the time needed for both start-up and watchdog timing. A minimum of 0.01µF should be connected to this pin to filter the switching noise from BOOT1. The pull-up resistor should not be more than 200kΩ to assure correct operation. |

## Pin Descriptions (Continued)

| PIN# | PIN NAME | DESCRIPTION |
|---|---|---|
| 42 | BOOT1 | The boot pin of the high voltage switching regulator. An external bootstrap capacitor is required. This pin provides bias voltage to the high-side MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive the internal N-channel MOSFET. The boot diode is included within the IC. |
| 43 | PHASE1 | The phase node of the high voltage switching regulator, VR1. This pin should be connected to the output inductor. |
| 45 | VIN1 | Input to both the high voltage switching regulator and the high voltage start-up LDO1. This pin connects the high voltage supply to the drain of the internal high-side MOSFET. |
| 47 | PGND1 | The ground pin of the high voltage switching regulator's power stage. There are switching power current pulses coming out of this pin. Place the VIN1 decoupling capacitor as close as possible to this pin. |

## Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | $V_{IN1}$ RANGE (V) | TEMP RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|---|
| ISL1801IVZ | ISL1801 IVZ | 9 to 90 | -40 to +85 | 48 Ld TSSOP | M48.240 |
| ISL1801EVAL1ZA | Evaluation Board | | | | |

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL1801. For more information on MSL please see tech brief TB363.

## Absolute Maximum Ratings

Supply Voltage, VCC1, VBOOT1-VPHASE1 . . . . . -0.3V to 16V
Voltage on VIN1 . . . . . -0.3V to 100V
Voltage on BOOT1 . . . . . -0.3V to 116V
Voltage on PHASE1, PHASE3 . . . . . -0.3V to 100V
Voltage on VIN2, PRELOAD . . . . . -0.3V to 16V
Voltage on PHASE2 . . . . . -0.3V to 16V
Voltage on BOOT2 . . . . . -0.3V to 22.5V
BDRIVE, DRIVE3 Voltages . . . . . -0.3V to PVCC3 +0.3V
Supply Voltage, VCC5V . . . . . -0.3V to 6.5V
Voltage on All Other Pins . . . . . -0.3V to VCC5V +0.3V
LDO(VCC5V) Current (Continuous) . . . . . 10mA
LDO(VCC1) Current (Continuous) . . . . . 10mA
ESD Rating
Human Body Model (Tested per JESD22-A114E) . . . . . 2kV
Machine Model (Tested per JESD22-A115-A) . . . . . 200V
Latch Up (Tested per JESD-78B; Class 2, Level A) . . . . . 100mA

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 48 Ld TSSOP Package (Notes 4, 5) . . . . . | 58 | 16 |

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

## Recommended Operating Conditions

Temperature Range . . . . . -40°C to +85°C
Supply Voltage, VCC1 . . . . . 6V to 14V
Voltage on VIN1 Pin . . . . . 9V to 90V
Voltage on BOOT1 Pin . . . . . 15V to 104V
Voltage on VIN2 Pin . . . . . 6V to 14V
Voltage on BOOT2 Pin . . . . . 10.5V to 19.5V
Supply Voltage, VCC5V . . . . . 4.5V to 5.5V

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For $\theta_{JC}$, the "case temp" location is taken at the package top center.

## High Voltage 10V Bias Regulator VR1 Electrical Specifications

$T_A$ = +25°C, VR1 = 10V, VR2 = 3.3V. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Notes 6, 7)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 7) | TYP (Note 6) | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| **$V_{IN1}$ SUPPLY** | | | | | | |
| $V_{IN1}$ | Input Voltage Range | | 9 | | 90 | V |
| | Shut-Down Current | $V_{IN1}$ = 9V to 90V | | 700 | **1000** | µA |
| | Operating Current | $V_{IN1}$ = 9V to 90V, PVCC3 = 0V, all inner circuits of the low voltage section are disabled, and only LDO1 and some inner circuits of the high voltage section are running. | | 1.3 | **2** | mA |
| **VCC1 SUPPLY** | | | | | | |
| | VCC1 LDO Regulator Output | | | 6.8 | | V |
| | Rising UV Threshold | | **5.2** | 5.9 | **6.6** | V |
| | UV Threshold Hysteresis | | | 1 | | V |
| **REFERENCE AND SOFT-START** | | | | | | |
| $V_{FB1}$ | Internal Reference Voltage | | **1.960** | 2.000 | **2.040** | V |
| **POWER MOSFETS** | | | | | | |
| $r_{DS(ON)}$ | Upper Switch ON-Resistance | $I_{OUT}$ = 50mA, BOOT1-PHASE1 = 6V, test at wafer sort | | 2.3 | 3.2 | Ω |
| $r_{DS(ON)}$ | Lower Switch ON-Resistance | $I_{OUT}$ = 50mA, VCC1 = 10V, test at wafer sort | | 1.2 | 2 | Ω |
| **ON TIME GENERATOR** | | | | | | |
| | $t_{ON}$ | $V_{IN1}$ = 10V, $r_{ON}$ = 1M | 2.75 | 3 | 3.25 | µs |
| | $t_{ON}$ | $V_{IN1}$ = 90V, $r_{ON}$ = 1M | | 0.3 | | µs |
| **MINIMUM OFF TIME** | | | | | | |
| | $t_{MINOFF}$ | | | 0.3 | | µs |

## High Voltage 10V Bias Regulator VR1 Electrical Specifications

$T_A$ = +25°C, VR1 = 10V, VR2 = 3.3V. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Notes 6, 7) (Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 7) | TYP (Note 6) | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| **MINIMUM ON TIME** | | | | | | |
| | $t_{MINON}$ | | | 0.3 | | µs |
| **REGULATION AND RIPPLE** | | | | | | |
| | Output Voltage Ripple | $V_{IN1}$ = 40V, $V_{OUT}$ = 10V, $F_{SW}$ = 100kHz, $L_{OUT}$ = 470µH, $C_{OUT}$ = 22µF | | 100 | | mV |
| **OVERCURRENT PROTECTION** | | | | | | |
| | Overcurrent Protection Threshold | Test on Wafer Sort and characterized on bench | **120** | 185 | **250** | mA |
| **OVERVOLTAGE PROTECTION** | | | | | | |
| | FB1 OVP Threshold | | | 2.4 | | V |
| **THERMAL SHUTDOWN** | | | | | | |
| | Thermal Shut-down Temperature | Rising Threshold | | 150 | | °C |
| | Thermal Shut-down Hysteresis | | | 30 | | °C |

## Low Voltage 3.3V Bias Regulator VR2 Electrical Specifications

$T_A$ = +25°C, VR1 = 10V, VR2 = 3.3V. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Notes 6, 7)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 7) | TYP (Note 6) | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| **$V_{IN2}$ SUPPLY** | | | | | | |
| | Input Voltage Range | | | | **14** | V |
| **VCC5 SUPPLY** | | | | | | |
| | VCC5 LDO Output | | | 5 | | V |
| | Rising UV Threshold | | **4.760** | 5.000 | **5.190** | V |
| | Hysteresis | | | 165 | | mV |
| **REFERENCE AND SOFT-START** | | | | | | |
| $V_{FB2}$ | Internal Reference Voltage | | **0.686** | 0.700 | **0.714** | V |
| | Soft-Start Interval | Current Limiting Threshold of VR2 Ramps from 25% to 100% | | 1.5 | | ms |
| **POWER MOSFETs** | | | | | | |
| $r_{DS(ON)}$ | Upper Switch ON-Resistance | $I_{OUT}$ = 200mA | | 1 | 2 | Ω |
| $r_{DS(ON)}$ | Lower Switch ON-Resistance | $I_{OUT}$ = 200mA | | 1 | 2 | Ω |
| **ON TIME GENERATOR (4 trim options)** | | | | | | |
| | $t_{ON}$ | $V_{IN2}$ = 10V, $r_{ON}$ = 1M | 950 | 1100 | 1250 | ns |
| | $t_{ON}$ | $V_{IN2}$ = 12V, $r_{ON}$ = 1M | | 800 | | ns |
| **MINIMUM ON TIME** | | | | | | |
| | $t_{MINON}$ | | | 150 | | ns |
| **MINIMUM OFF TIME** | | | | | | |
| | $t_{MINOFF}$ | | | 150 | | ns |
| **REGULATION AND RIPPLE** | | | | | | |
| | Output Voltage Ripple | $V_{IN2}$ = 10V, $V_{OUT2}$ = 3.3V, $F_{SW}$ = 300kHz, $L_{OUT}$ = 47µH, $C_{OUT}$ = 22µF | | 30 | | mV |

## Low Voltage 3.3V Bias Regulator VR2 Electrical Specifications

$T_A$ = +25°C, VR1 = 10V, VR2 = 3.3V. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Notes 6, 7)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 7) | TYP (Note 6) | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| **OVERCURRENT PROTECTION** | | | | | | |
| | Overcurrent Protection Threshold | | **200** | 245 | **300** | mA |
| **OVERVOLTAGE PROTECTION** | | | | | | |
| | FB2 OVP Threshold | | | 0.775 | | V |
| **PGOOD2 (OPEN DRAIN OUTPUT)** | | | | | | |
| | Power-Good Lower Threshold | Fraction of $V_{OUT2}$ set point; 3µs noise filter | **83** | 90 | **95** | % |
| | PGOOD2 Leakage Current | $V_{PULLUP}$ = 3.3V | | | 1 | µA |
| | PGOOD2 Voltage Low | $I_{PGOOD2}$ = 4mA | | | 0.5 | V |

## Driver Electrical Specifications

$T_A$ = +25°C, VR1 = 10V, VR2 = 3.3V. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Notes 6, 7)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 7) | TYP (Note 6) | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| **PVCC3 SUPPLY** | | | | | | |
| | Shutdown Current | PVCC3 = 3V | | 0.85 | **1.1** | mA |
| | Operating Current | PVCC3 = 10V, Drive3 = Bdrive = 1, or 0 | | 1.75 | 3.2 | mA |
| | Operating Current | PVCC3 = 10V, $F_S$ = 50kHz, 10nF load on Drive3 | | 8 | **11** | mA |
| **LOGIC INPUT PINS** | | | | | | |
| | Low Level Voltage Threshold | PWM3, RPWM3, BCMD, BRESET, VDDRFE = 3.3V | | | 0.7 | V |
| | High Level Voltage Threshold | PWM3, RPWM3, BCMD, BRESET, VDDRFE = 3.3V | 2.4 | | | V |
| | Hysteresis | | | 187 | | mV |
| | Input Pull-Down Current | | | 500 | | nA |
| **DRIVE3 AND BDRIVE GATE DRIVER** | | | | | | |
| | Low Level Output Voltage | $I_{DRIVE}$ = 100mA | | 50 | 250 | mV |
| | High Level Output Voltage | $I_{DRIVE}$ = -100mA | 9.25 | 9.8 | | V |
| | Peak Pull-Down Current | $V_{DRIVE}$ = 0V | | 5 | | A |
| | Peak Pull-Up Current | $V_{DRIVE}$ = 10V | | 2 | | A |
| | Active Pull-Down Resistance Before POR | VCC1 = 10V | | 270 | 600 | Ω |
| **OVERCURRENT PROTECTION OCSET3** | | | | | | |
| | OC Threshold Current | Current from OCSET3 Pin | 110 | 120 | 130 | µA |
| | OC Comparator Input Offset | | | 3 | | mV |
| **DRIVE3 AND BDRIVE SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{PHL}$ | Turn-Off Propagation Delay | PWM Falling to DRIVE Falling | | 200 | **320** | ns |
| $t_{PLH}$ | Turn-On Propagation Delay | PWM Rising to DRIVE Rising | | 150 | **300** | ns |
| $t_{RC}$ | Output Rise Time (10% to 90%) | $C_L$ = 10nF | | 90 | | ns |
| $t_{FC}$ | Output Fall Time (90% to 10%) | $C_L$ = 10nF | | 50 | | ns |
| $t_{PW}$ | Input Pulse Width that Changes the Output | | **300** | | | ns |

## WatchDog Timer Electrical Specifications

$T_A$ = +25°C, VR1 = 10V, VR2 = 3.3V. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Notes 6, 7)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 7) | TYP (Note 6) | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| **INPUT PIN** | | | | | | |
| | WDI Rising Threshold | WDI, VDDRFE = 3.3V, VCC5 = 5V | **1.50** | 1.64 | **1.80** | V |
| | WDI Falling Threshold | WDI, VDDRFE = 3.3V, VCC5 = 5V | **1.40** | 1.56 | **1.70** | V |
| | WDI Hysteresis | | | 80 | | |
| | Disable Mode Input Voltage Threshold | WDI, VDDRFE = 3.3V, VCC5 = 5V | | 4.5 | | V |
| | Inner Pull-up Resistor | Pull up to VCC5 | **37** | 50 | **61** | kΩ |
| | Minimum Pulse Width | WDI, VDDRFE = 3.3V, VCC5 = 5V | | 300 | | ns |
| **TIME-OUT CHARACTERISTICS** | | | | | | |
| | Timer Rising Threshold | VCC5 = 5V | | 4.5 | | V |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| | Timer Reset Pulse Width | | | 1.5 | | ms |
| | Timer Leakage Current | Timer = 5V | | | 1.2 | µA |
| | Timer Voltage Low | $I_{Timer}$ = 4mA | | | 0.5 | V |
| | PGOOD2 Reset Pulse Width | | | 1 | | ms |

## Current Sense Op amp Electrical Specifications

$T_A$ = +25°C, VR1 = 10V, VR2 = 3.3V. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Notes 6, 7)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 7 | TYP (Note 6) | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| | Input Offset Voltage | | | -1000 | | µV |
| | Input Bias Current | | | 3 | | nA |
| | Input Offset Current | | | ±1 | | nA |
| $V_{CM\_min}$ | Minimum Common-Mode Voltage | | | -0.1 | | V |
| $V_{CM\_max}$ | Maximum Common-Mode Voltage | | | 2 | | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM}$ = -0.1V to 2V | | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_{CC}$ = 3.3V to 5.5V, $V_{OUT2}$ = 3.3V | | 100 | | dB |
| | Large Signal Voltage Gain | | | 220 | | V/mV |
| | Maximum Output Voltage Swing | Output low, $R_L$ = 100kΩ to $V_{CM}$ | | 5.3 | | mV |
| | | Output high, $R_L$ = 100kΩ to $V_{CM}$; VDDREF tied to 3.3V $V_{OUT2}$ | | 3.0 | | V |
| | Short-Circuit Output Source Current | $R_L$ = 10Ω to $V_{CM}$ | | 30 | | mA |
| **AC SPECIFICATIONS** | | | | | | |
| | Gain Bandwidth Product | $R_L$ = 10kΩ to $V_{CM}$ | | 130 | | kHz |
| | Input Noise Voltage Peak-to-Peak | F = 0.1Hz to 10Hz | | 1.4 | | $\mu V_{P-P}$ |
| | Input Noise Voltage Density | $f_O$ = 1kHz | | 64 | | $nV/\sqrt{Hz}$ |
| | Input Noise Current Density | $f_O$ = 10kHz | | 0.19 | | $pA/\sqrt{Hz}$ |
| | Slew Rate | | | 100 | | V/ms |

## Dual High-Speed Comparator Electrical Specifications

$T_A$ = +25°C, VR1 = 10V, VR2 = 3.3V. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Notes 6, 7)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 7) | TYP (Note 6) | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| | Input Offset Voltage | | **-5.5** | 0 | **5.5** | mV |
| | Input Bias Current | | | ±1 | | pA |
| | Input Offset Current | | | ±1 | | pA |
| $V_{CM\_min}$ | Minimum Common-Mode Voltage | | | -0.2 | | V |
| $V_{CM\_max}$ | Maximum Common-Mode Voltage | | | 3.3 | | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM}$ = -0.2V to $V_{OUT2}$ | | 62 | | dB |
| | Input Common-Mode Capacitance | | | 2 | | pF |
| | Input Differential Capacitance | | | 4 | | pF |
| | Output High Voltage | $I_{OUT}$ = -0.3mA; VDDREF Tied to 3.3V $V_{OUT2}$ | 2.7 | 3 | | V |
| | Output Low Voltage | $I_{OUT}$ = 0.3mA | | 175 | 300 | mV |
| | Short Circuit Current | | | 1 | | mA |
| **SWITCHING SPECIFICATIONS** | | | | | | |
| | Low-to-High Propagation Delay Time | Input overdrive = 100mV | | | **0.55** | µs |
| | High-to-low Propagation Delay Time | Input overdrive = 100mV | | | **0.2** | µs |
| | CMP1 Rise Time | CL = 10pF, CMP1+ toggled from 0V to 1V | **5** | 100 | **550** | ns |
| | CMP1 Fall Time | CL = 10pF, CMP1+ toggled from 1V to 0V | **5** | 100 | **550** | ns |
| **LATCHRPT (OPEN DRAIN OUTPUT)** | | | | | | |
| | LATCHRPT One-Shot Pulse Width | Under pulse by pulse OC condition, LATCHRPT pulled low for one-shot period of each OC cycle | | 1.1 | **2.5** | µs |
| | LATCHRPT Leakage Current | $V_{PULLUP}$ = 3.3V | | | **1** | µA |
| | LATCHRPT Voltage Low | $I_{LATCHRPT}$ = 4mA | | | **0.5** | V |

## Preload Electrical Specifications

$T_A$ = +25°C, VR1 = 10V, VR2 = 3.3V. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Notes 6, 7)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN (Note 7 | TYP (Note 6) | MAX (Note 7) | UNITS |
|---|---|---|---|---|---|---|
| **POWER MOSFET** | | | | | | |
| $r_{DS(ON)}$ | Switch 1 ON ON-Resistance | Pull-up to VCC1 = 10V through 100Ω resistor (Note 8) | **242** | 350 | **472** | Ω |
| $r_{DS(ON)}$ | Switch 2 ON ON-Resistance | Pull-up to VCC1 = 10V through 100Ω resistor (Note 8) | **90** | 120 | **165** | Ω |
| $r_{DS(ON)}$ | Switch 3 ON ON-Resistance | Pull-up to VCC1 = 10V through 100Ω resistor (Note 8) | **40** | 56 | **76** | Ω |
| $r_{DS(ON)}$ | Switch 4 ON ON-Resistance | Pull-up to VCC1 = 10V through 100Ω resistor (Note 8) | **8.7** | 11.4 | **14.8** | Ω |

NOTES:

6. Compliance to datasheet values is assured by one or more methods: production test, characterization and/or design.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. Not production tested.

# Typical Performance Curves

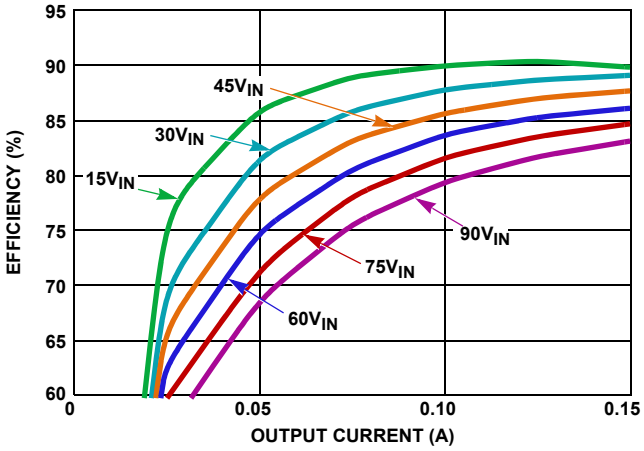



FIGURE 3. VR1 EFFICIENCY vs LOAD CURRENT WITH $V_{OUT1}$ = 10V at $F_{SW1}$ = 170kHz

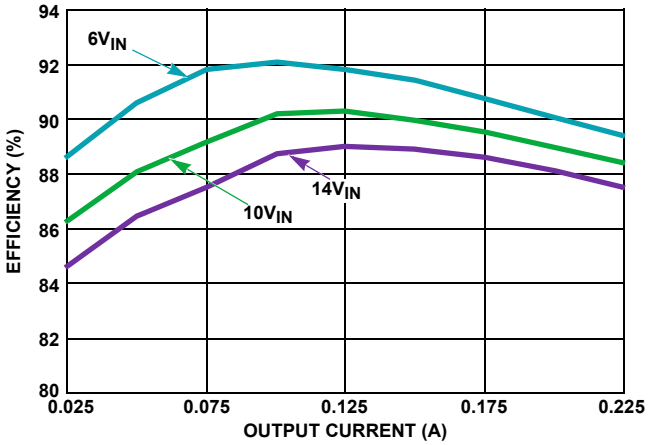



FIGURE 4. VR2 EFFICIENCY vs LOAD CURRENT WITH $V_{OUT2}$ = 2.5V at $F_{SW2}$ = 210kHz

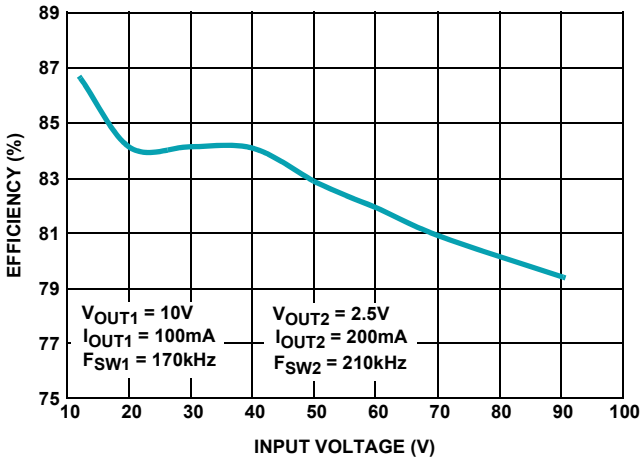



FIGURE 5. VR1 + VR2 EFFICIENCY vs INPUT VOLTAGE

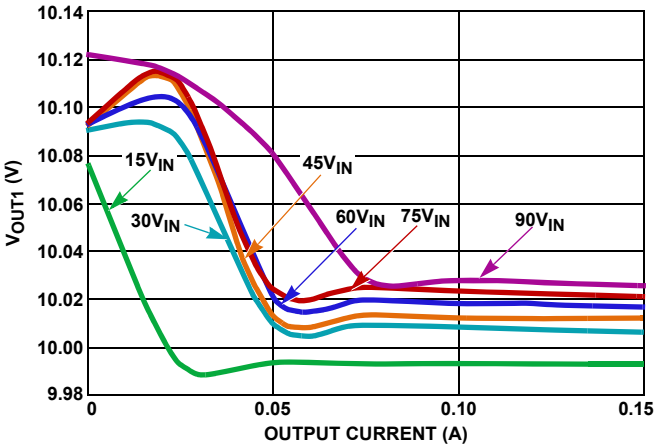



FIGURE 6. VR1 REGULATION vs LOAD CURRENT WITH $V_{OUT1}$ = 10V at $F_{SW1}$ = 170kHz

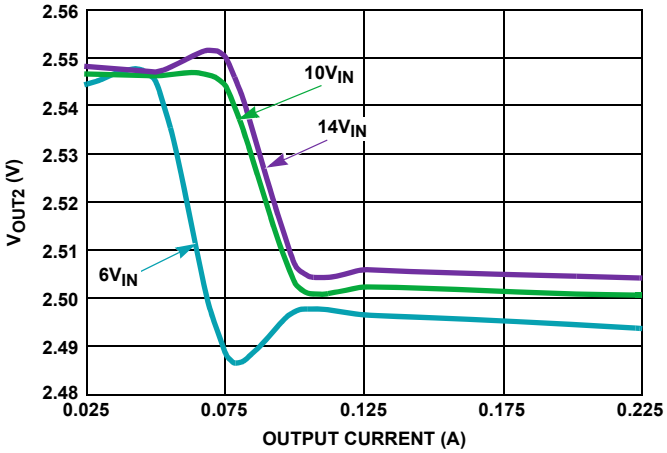



FIGURE 7. VR2 REGULATION vs LOAD CURRENT WITH $V_{OUT2}$ = 2.5V at $F_{SW2}$ = 210kHz

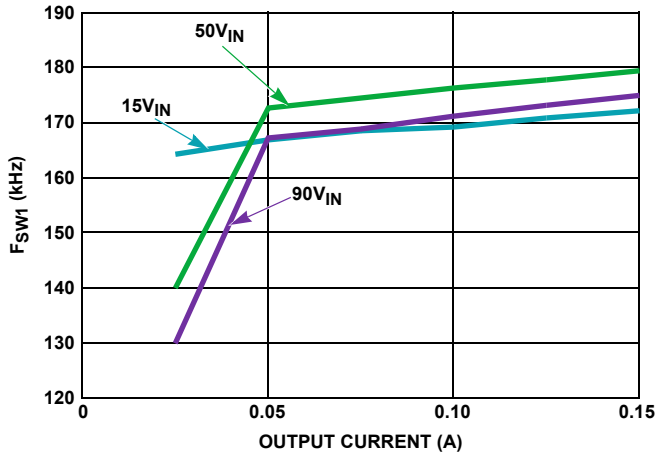



FIGURE 8. VR1 SWITCHING FREQUENCY vs LOAD CURRENT WITH $V_{OUT1}$ = 10V

## Typical Performance Curves (Continued)

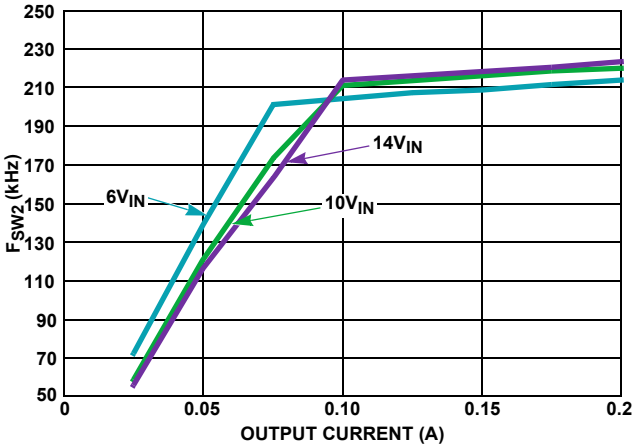



FIGURE 9. VR2 SWITCHING FREQUENCY vs LOAD CURRENT WITH $V_{OUT2}$ = 2.5V

# Test Waveforms

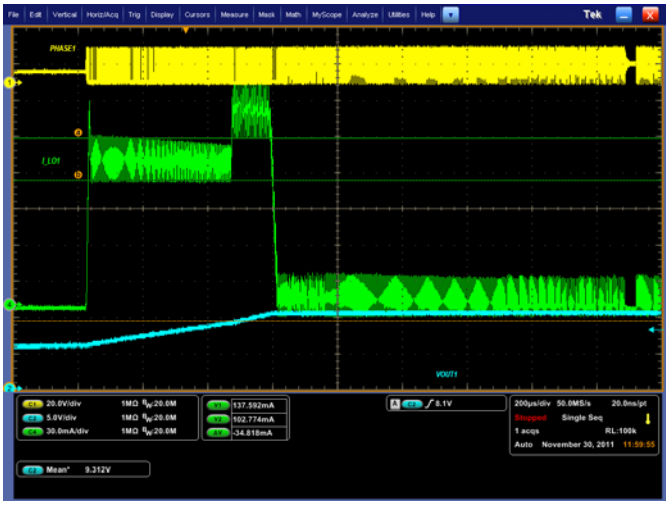


FIGURE 10. VR1 SOFT-START (FROM TOP TO BOTTOM: PHASE1, I_L1, $V_{OUT1}$)

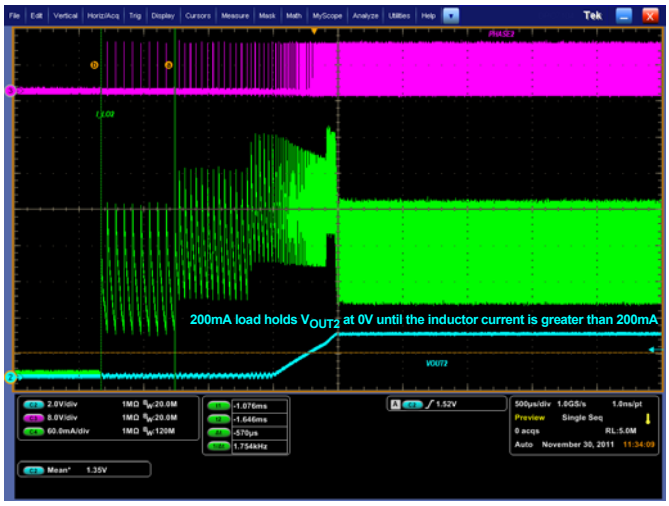



FIGURE 11. VR2 SOFT-START WITH 200mA LOAD (FROM TOP TO BOTTOM: PHASE2, I_L2, $V_{OUT2}$)

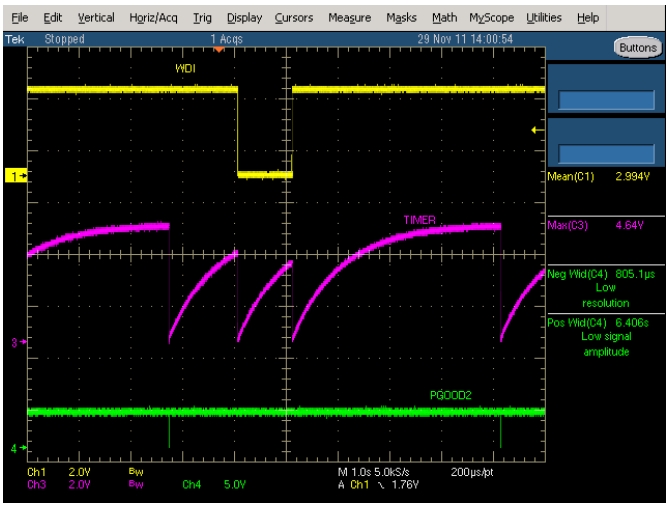



FIGURE 12. WATCHDOG OPERATION

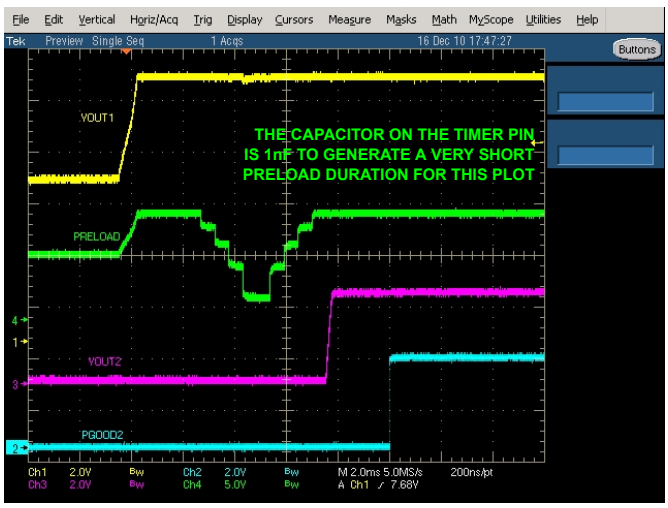



FIGURE 13. NORMAL POWER-UP SEQUENCE

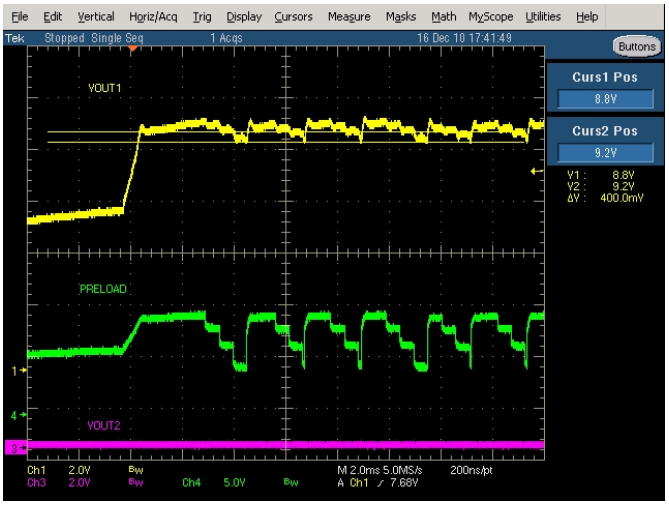



FIGURE 14. SOFT-START WHEN PRELOAD TEST FAILS

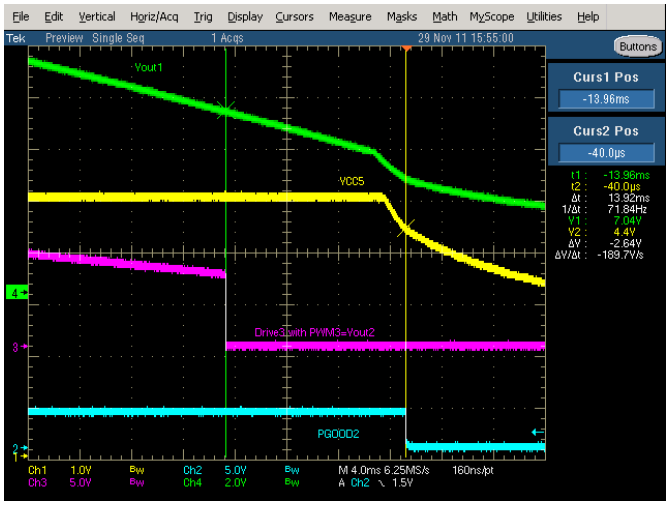



FIGURE 15. NORMAL POWER-DOWN SEQUENCE

## Test Waveforms (Continued)

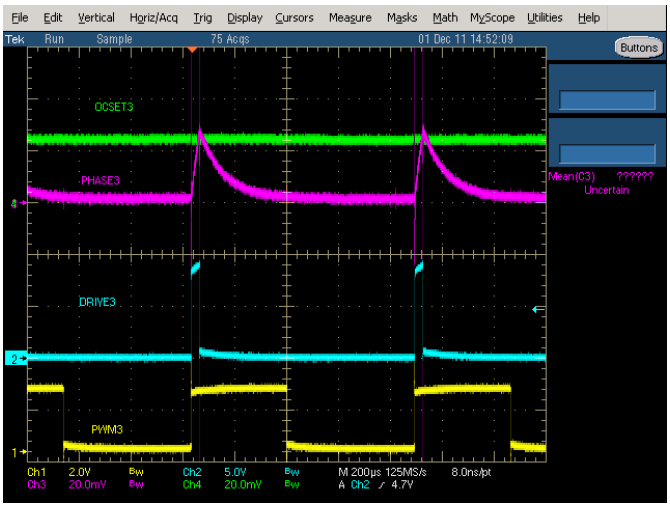



FIGURE 16. OCSET3 THRESHOLD CROSSING TRIGGERS OCP

# Summary of Operation

The ISL1801 is a versatile Solar Power Management IC (sPMIC). It has two switching regulators, two LDOs, two general purpose comparators, two power MOSFET drivers, a current sense OPAMP and other logic functions. Figure 17 shows the main blocks in the ISL1801.

The high voltage LDO1 can be directly connected to a high voltage input power source up to 90V. The output can be used to start-up the high voltage switching regulator VR1. Once the VR1's output is greater than 6.7V, LDO1 is disabled to save power. The second low voltage regulator, LDO2, can be connected to the output of VR1 to generate the 5V supply required for the internal control circuits including those that operate VR1 and VR2.

The first switching regulator, VR1, can be directly connected to an input voltage up to 90V. The VR1 provides a regulated voltage for the second switching regulator, VR2, and the two integrated MOSFET drivers. The low voltage switching regulator, the VR2, can be used to generate the regulated voltage for an MCU or other external circuitry. The PGOOD2 signal is used to indicate that VR2 output voltage is within the regulation window. The output voltage of both VR1 and VR2 can be set through resistor dividers at the FB1 and FB2 pins respectively. The switching frequencies of VR1 and VR2 are determined by the resistors at the TON1 and TON2 pins respectively.

There are two low-side drivers for the external power MOSFETs. Both drivers are powered by the PVCC3 pin, which is normally connected to the output of VR1.

The integrated amplifier has low offset and drift so, the MCU can accurately sense the amplified module current.

Overcurrent and overvoltage conditions can be monitored by the two general purpose high-speed comparators. Any detected fault condition can be used to trigger an MCU interrupt.

The preload function is specially designed for solar applications. It applies a resistive load to the input power source to verify that it is sufficient for device operation. VR2, the MCU supply, will not be enabled until the input power source has enough power. This function can significantly reduce the power cycling of the MCU at system start-up and shutdown.

The ISL1801 also includes a watchdog circuit to prevent the software in the MCU from hanging in an unknown state. The MCU can use the watchdog input (WDI) pin to periodically restart the timer. The watchdog timeout is set by a resistor to VCC5V and a capacitor to ground, both connected to the TIMER pin. If the RC timer expires before an MCU reset on the WDI pin the PGOOD2 pin will be pulled low to reset the MCU.

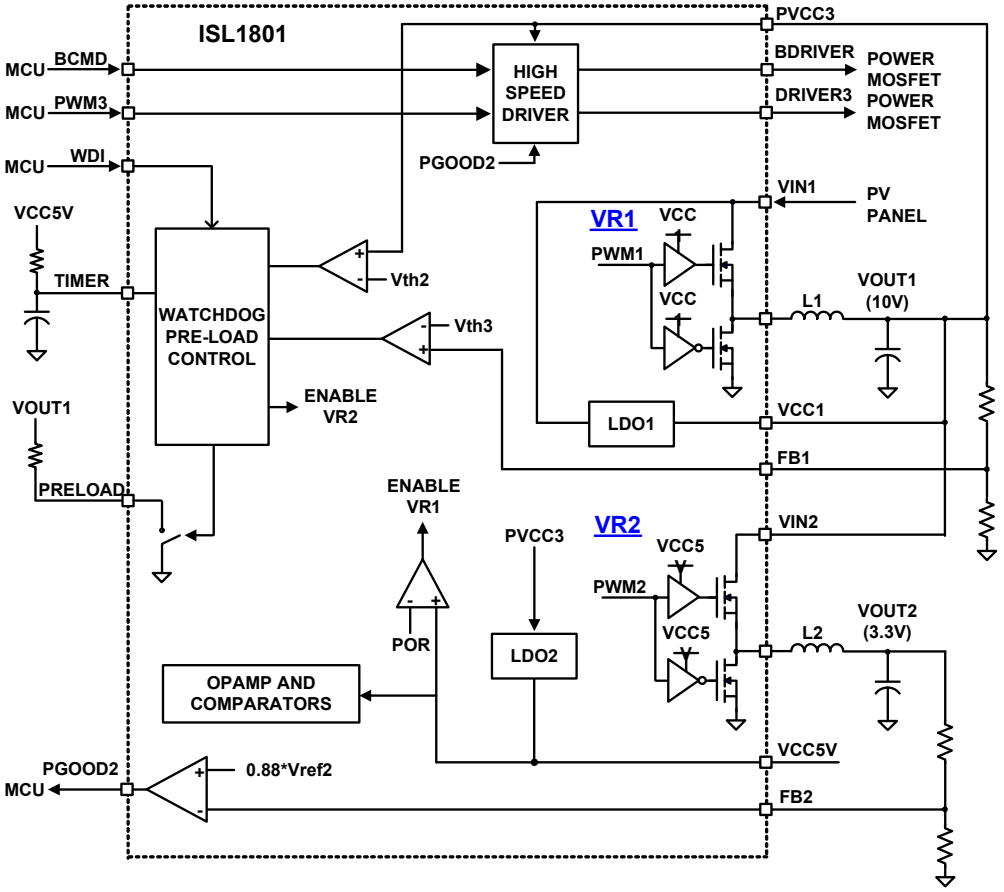



FIGURE 17. ISL1801 SIMPLIFIED BLOCK DIAGRAM

# Detailed Operation

## Dual Synchronous Buck Switching Regulators With Constant On Time Control

There are two synchronous Buck switching regulators in the ISL1801. The high voltage switching regulator, VR1, can be connected to a power source up to 90V. The low voltage switching regulator, VR2, supports input voltages up to 14V. Typically, VR2 is connected to the output of VR1. Both switching regulators include integrated MOSFETs.

Both VR1 and VR2 employ a constant on time PWM control architecture with input voltage feed-forward. The constant on time PWM control architecture relies on the output ripple voltage to provide the PWM ramp signal; thus the output filter capacitor's ESR acts as a current feedback resistor. For some applications with ceramic capacitors, the output voltage ripple is small due to very low ESR. In order to achieve the stable operation for very low voltage ripple applications, one internal ramp is generated and added to the FB signal to emulate the output voltage ripple. The high-side switch ON time is determined by a one-shot, which period is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum OFF time (300ns typical for VR1 and 150ns typical for VR2). The ON time one-shot triggers when the following conditions are met; the error comparator's output is high, the synchronous rectifier current is below the current limit threshold, and the minimum OFF time one-shot has timed out. The controller utilizes the valley point of the output ripple to regulate and determine the OFF time.

### SWITCHING FREQUENCY OF VR1 AND VR2

Each PWM core includes a one-shot that sets the ON time for the high-side switch of each voltage regulator. Each fast, low jitter, adjustable one-shot includes circuitry that varies the ON time in response to the input voltage and output voltage. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator.

The high-side switch ON time is inversely proportional to the input voltage as measured by the TON1 and TON2 pins for VR1 and VR2 respectively. Both TON1 and TON2 pins are tied to an internal voltage reference and the current flowing into these pins is monitored to generate the ON time one-shot.

For high voltage VR1, the TON1 pin is tied to an internal 1V reference and the width of the ON time one-shot is:

$$T_{ON1} = \frac{2.7e^{-11} \cdot R_{ON1}}{V_{IN1} - 1} \quad \text{(EQ. 1)}$$

$V_{IN1}$ is the input voltage for high voltage VR1, while $R_{ON1}$ is the resistor from $V_{IN1}$ to the TON1 pin.

The switching frequency of VR1 is:

$$F_{SW1} = \frac{V_{OUT1} \cdot (V_{IN1} - 1)}{2.7e^{-11} \cdot R_{ON1} \cdot V_{IN1}} \quad \text{(EQ. 2)}$$

When $V_{IN1}$ is much larger than 1V, the switching frequency of VR1 is almost independent of its input voltage:

$$F_{SW1} \approx \frac{V_{OUT1}}{2.7e^{-11} \cdot R_{ON1}} \quad \text{(EQ. 3)}$$

For a 10V output, the switching frequency of VR1 is about 370kHz with $R_{ON1}$ = 1MΩ.

For low voltage VR2, the TON2 pin is tied to an internal 0.5V reference and the width of the ON time one-shot is:

$$T_{ON1} = \frac{1.05e^{-11} \cdot R_{ON2}}{V_{IN2} - 0.5} \quad \text{(EQ. 4)}$$

$V_{IN2}$ is the input voltage for VR2, while $R_{ON2}$ is the resistor from $V_{IN2}$ to the TON2 pin.

The switching frequency of VR2 is:

$$F_{SW2} = \frac{V_{OUT2} \cdot (V_{IN2} - 0.5)}{1.05e^{-11} \cdot R_{ON2} \cdot V_{IN2}} \quad \text{(EQ. 5)}$$

When $V_{IN2}$ is much larger than 0.5V, the switching frequency of VR2 is almost independent of its input voltage:

$$F_{SW2} \approx \frac{V_{OUT2}}{1.05e^{-11} \cdot R_{ON2}} \quad \text{(EQ. 6)}$$

For a 3.3V output, the switching frequency of VR2 is about 314kHz with $R_{ON2}$ = 1MΩ.

### CURRENT LIMITING OF VR1 AND VR2

To prevent the output current from becoming too high, a new ON time pulse can start only when the current through the synchronous MOSFET is below the current limiting threshold. This limits the valley of the output inductor current to a fixed value, typically 140mA for VR1 and 200mA for VR2.

The maximum peak current through the output inductor is the sum of the current limiting threshold and the current ripple determined by the ON time, inductor value and the input/output voltage.

### DIODE EMULATION OPERATION

To improve the efficiency for light loads, the synchronous MOSFET is turned off when its current drops to 0. This prevents negative current through the output inductor emulating diode operation.

With diode emulation operation under light load conditions, the output voltage may drop slowly after the synchronous MOSFET turns OFF. It may take a long time for the output voltage to drop below the reference voltage to start a new switching cycle. This will have the effect of reducing the switching frequency under light load conditions.

### OVERVOLTAGE PROTECTION

The feedback voltage for VR1 and VR2 is continuously monitored to prevent the output voltage from going too high.

When the VR1 output voltage feedback FB1 is higher than 120% of VREF1, the Overvoltage Protection (OVP) is triggered. When this condition occurs, the lower-side MOSFET of VR1 is turned on immediately. At the same time, the preload current will be applied to $V_{OUT1}$ to discharge the output. When the current through the lower side MOSFET drops to 0, turn off this MOSFET to prevent the negative inductor current. the OVP is reset when FB1 voltage drops to VREF1.

For low voltage VR2, OVP is triggered when the FB2 voltage is above 0.775V. When this condition occurs, the lower synchronous MOSFET of VR2 is turned on immediately. It is held on until the FB2 voltage drops below 0.73V.

### POWER-GOOD SIGNAL (PGOOD2)

Both VR1 and VR2 have their own power-good signals to indicate that their output voltage is within the regulation window. Only the VR2 power-good signal is externally available at the PGOOD2 pin. VR1's power-good signal is used internally and is not available on an external pin.

The PGOOD2 pin is a true open drain output. The power-good comparator continuously monitors the feedback voltage FB2 for an undervoltage condition. PGOOD2 is active low during shutdown or when FB2 is below the threshold voltage. When the FB2 voltage goes above 88% of its reference voltage (0.88 * 0.73V = 0.64V), PGOOD2 is released and the pin will be a high impedance.

The PGOOD2 signal can be used to reset the MCU powered by the output of VR2.

The watchdog timer will also pull PGOOD2 low when a timeout occurs. Please refer to "WatchDog Timer" on page 20 for more information.

## Dual LDO Bias Supplies

There are two LDOs in the ISL1801 to manage start-up and power internal control circuitry.

The high voltage LDO1 can be directly connected to an input power source up to 90V. Its output is connected to the VCC1 pin and is typically about 6.7V. VCC1 provides the bias voltage for the power stage of high voltage regulator. Typically, the VCC1 pin should be connected to $V_{OUT1}$, the output of high voltage regulator VR1. Before VR1 starts to operate, LDO1 can charge up the capacitor at VCC1 when it is tied to $V_{OUT1}$. When the $V_{OUT1}$/VCC1 voltage reaches 6.5V, VR1 starts to operate and will ramp $V_{OUT1}$/VCC1 to a higher voltage. Once the VCC1 voltage is above 6.7V, LDO1 is disabled. LDO1 limits its output current to 10mA.

There is a second low voltage LDO2 which can be connected to inputs up to 14V. LDO2's 5V output is connected to the VCC5V pin. Typically, LDO2 is connected to the input voltage of low voltage VR2 (typically $V_{OUT1}$). LDO2 supplies power for internal circuitry such as the current sense Op amp, logic circuits, comparators and the VR2 control circuits. One 2.2µF capacitor is recommended at the VCC5V pin. LDO2 limits its output current to 10mA.

## Dual Low-Side MOSFET Drivers

The ISL1801 has two low-side drivers for power MOSFETs connected to the DRIVE3 and BDRIVE pins. Their high output current enables them to rapidly charge and discharge the gate capacitance of power MOSFETs. Both drivers are powered by the PVCC3 pin, and each driver has its own ground pin. PGND3 is the ground connection for DRIVE3 and PGND4 is the ground connection for BDRIVE. The gate drivers (DRIVE3 and BDRIVE) are always pull-down to ground by internal 14kΩ resistor. Additional 250Ω pull-down resistor is available only after the 5V LDO VCC5V has come up higher than 3.2V.

### DRIVE3 CONTROL LOGIC

DRIVE3 is controlled by the PWM3 signal. When PWM3 = 1, the DRIVE3 output is connected to PVCC3 by its upper switch. When PWM3 = 0, DRIVE3 is connected to PGND3 through its lower switch. However there are other logic signals which influence the state of DRIVE3.

Before Power On Reset (POR) DRIVE3 is forced low. When the output of comparator 1 (CMP1O) or comparator 2 (CMP2O) is high it triggers a flip-flop (FF1) setting the open drain latch report (LATCHRPT) signal low. It also connects DRIVE3 to PGND3 immediately. The RPWM3 pin has to be forced low to reset this condition. Since the set input of flip-flop FF1 overrides the reset input, DRIVE3 is always held low when CMP1O or CMP2O is high even when RPWM3 = 0.

### DRIVE3 OVERCURRENT LIMITING

A comparator monitors the PHASE3 voltage when DRIVE3 is high to detect a possible overcurrent condition. When this comparator output is high, DRIVE3 is immediately connected to PGND3. This action provides overcurrent protection (OCP) for the power stage driven by DRIVE3. Figure 18 shows the block diagram of the PHASE3 OCP function.

The PHASE3 overcurrent limiting level is defined by the OCSET3 pin. A 120µA current is supplied by the OCSET3 pin. Placing a resistor from the OCSET3 pin to PGND3 sets the overcurrent threshold voltage. A capacitor may be placed in parallel with the OCSET3 resistor to filter noise and provide a more consistent OCP threshold.

When DRIVE3 = 1, the internal switch S3 is turned on feeding the PHASE3 signal to the OCP comparator. The PHASE3 voltage is equal to the product of the current I1 and the conduction resistance $r_{DS(ON)}$ of the power MOSFET Q1. When the PHASE3 pin voltage is higher than the OCSET3 pin voltage, the DRIVE3 OCP is triggered. The overcurrent limiting level is:

$$I_{OC3} = \frac{120\mu A \cdot R1}{r_{DS(ON)}} \quad \text{(EQ. 7)}$$

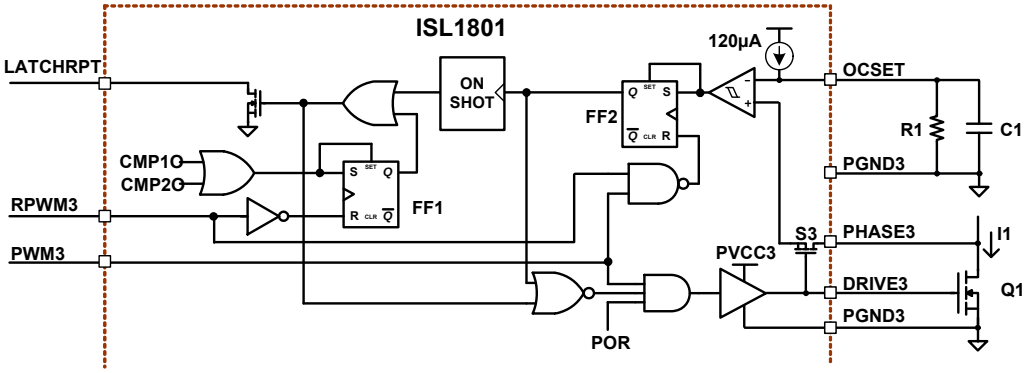



FIGURE 18. LOW-SIDE DRIVER LOGIC

Once the overcurrent protection is triggered flip-flop FF2 is set forcing DRIVE3 low. RPWM3 or PWM3 must be pulled low to reset an OCP event. Since the set input of flip-flop FF2 overrides the reset input, DRIVE3 is always held low in an overcurrent condition even if RWPM3 = 0.

The OCP flip-flop output also triggers a one-shot block to generate a narrow pulse setting LATCHRPT low for 1µs.

For normal operation an OCP event terminates the DRIVE3 on state early by forcing DRIVE3 to PGND3. The OCP event is reset by setting PWM3 = 0. This allows DRIVE3 to be turned on by the following PWM3 = 1 pulse. However, special attention is needed for long-term or continuous OCP operation. If the OCP is continuously triggered with RPWM3 = 0 and PWM3 = 1, then a very high switching frequency may occur on the DRIVE3 pin. Referring to Figure 18 the following sequence of events will lead to this oscillation. When I1 is larger than the preset OCP level, it may trigger OCP immediately when DRIVE3 = 1. Once OCP is triggered, DRIVE3 is pulled low, and S3 is turned off setting the OCP comparator output low. Since RPWM3 = 0, the flip-flop FF2 is reset immediately. However, the 1µs one-shot will keep LATCHRPT low for at least 1µs forcing the DRIVE3 pin low for at least 1µs. After 1µs DRIVE3 is forced high resulting in another OCP. This operation repeats until PWM3 = 0, RPWM3 = 1 or I1 drops below the OCP threshold. This condition may result in a 100kHz switching frequency at DRIVE3.

### BDRIVE CONTROL LOGIC

The BDRIVE pin is controlled by the BCMD signal. When BCMD = 1, the BDRIVE output is connected to PVCC3 by its upper switch. When BCMD = 0 the BDRIVE pin is connected to PGND4 through its lower switch.

When any fault condition occurs, the LATCHRPT signal is set low. It will also set flip-flop FF3 and connect the BDRIVE pin to PGND4 until flip-flop FF3 is reset by setting BRESET = 1. BDRIVE is held at PGND4 prior to POR. The BDRIVE logic is shown in Figure 19.

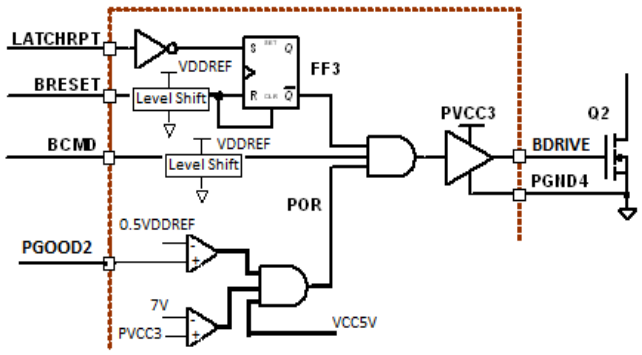



FIGURE 19. BDRIVE CONTROL LOGIC

When VDDREF is not applied during the start, the output of the level shift block is undefined. In order to prevent BDRIVE turning on by mistake, it's recommended adding some offset (~50mV) on VDDREF pin to make the POR AND gate output low.

## Dual High-Speed Comparator

The ISL1801 has two high-speed comparators for fault detection. The output of either comparator can set the flip-flop FF1 to indicate a fault at the open-drain LATCHRPT pin. The fault can be cleared by setting RPWM3 = 0 to reset flip-flop FF1.

The two comparators are identical but only the output of comparator 1 (CMP1) is available at the CMP1O pin. CMP1O is a push-pull output and its output high level is clamped to VDDREF. The fault detection logic is shown in Figure 20.

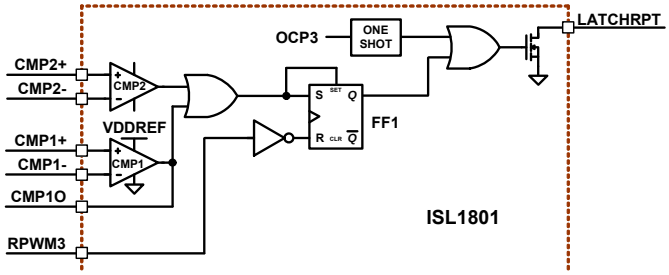



FIGURE 20. FAULT DETECTION LOGIC

## Precision Amplifier

The ISL1801 includes a precision amplifier for current sensing. This low offset and low temperature drift Op amp can be used to accurately amplify the voltage drop across a known shunt resistor to provide a current measurement for the MCU. Due to the very low amplitude input signal, it is necessary to include some capacitance as a noise filter. The typical application circuit is shown in Figure 21. The current sense gain is set by the ratio of R1/R2. Capacitor C1 implements a low-pass filter to reduce high frequency noise effectively averaging the desired signal. C2 is optional and can provide additional noise filtering if required.

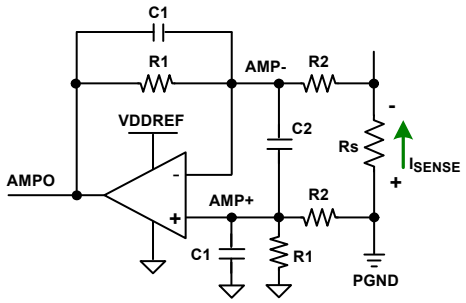



FIGURE 21. PRECISION CURRENT SENSE AMPLIFIER

## Preload Operation

During morning start-up, shading events or evening shutdown, PV modules may not provide enough output power to run the micro converter. When this happens it may result in a repetitive voltage dropout at the VR2 output. When the VR2 output powers the MCU, this may cause a system reset after each dropout. The repetitive restart operation of MCU may impact on the system reliability.

To avoid this issue, the ISL1801 includes the preload feature to test the power source before enabling VR2. This test is performed by gradually applying a preload current to the output of VR1/$V_{OUT1}$. If the preloaded VR1 output voltage drops below the preset threshold, the preload is removed immediately. After the VR1 output voltage recovers, the preload test is repeated. If VR1 can support the preload current and maintain its output voltage above the preset threshold for some time the input power source has enough power for the system operation. The preload is then removed, and VR2 is enabled and will perform a soft-start.

Figure 22 shows the ISL1801s preload circuit. The four MOSFETs each have a different ON resistance that can be connected to the preload pin. This allows the ISL1801 to increase the preload current step-by-step, as shown in Figure 23. When the preload is enabled, Q1 turns on for about 500µs. During this time the current applied to the VR1 output as shown by Equations::

$$I_{VR1} = \frac{V_{VR1}}{R_{PL} + r_{DS(ON)1}} \quad \text{(EQ. 8)}$$

Next, Q2 turns on with Q1 and the preload current becomes:

$$I_{VR1} = \frac{V_{VR1}}{R_{PL} + (r_{DS(ON)1} \parallel r_{DS(ON)2})} \quad \text{(EQ. 9)}$$

Next, Q3 turns on with Q1 and Q2; Finally all the MOSFETs are on resulting in the minimum resistance from the PRELOAD pin to GND:

$$I_{VR1} = \frac{V_{VR1}}{R_{PL} + (r_{DS(ON)1} \parallel r_{DS(ON)2} \parallel r_{DS(ON)3} \parallel r_{DS(ON)4})} \quad \text{(EQ. 10)}$$

After all the MOSFET switches are on the TIMER pin is pulled to GND for 1ms and then released to ramp-up. If the VR1 output voltage stays above the preset threshold until the TIMER pin ramps to 90% of VCC5V, the preload is removed step-by-step, as shown in Figure 23. If the VR1 output drops below the preset threshold all the switches are turned off immediately. The "Power-Up Sequence" on page 22 provides additional details.

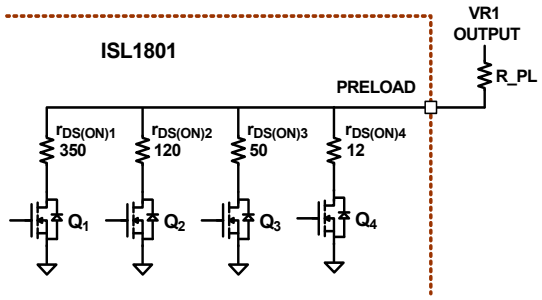



FIGURE 22. PRELOAD SWITCHES

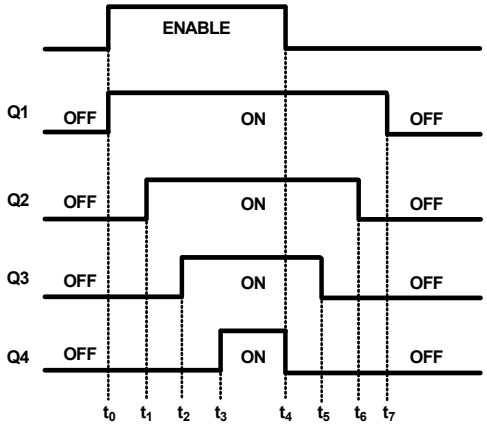



FIGURE 23. PRELOAD TIMING DIAGRAM

## WatchDog Timer

The Watchdog Timer circuit in Figure 24 verifies correct MCU operation by monitoring the WDI input pin. The MCU must periodically toggle the WDI pin to prevent a timeout. If a timeout occurs, the PGOOD2 pin will be pulsed low for 0.5ms providing a signal that can reset the MCU. PGOOD2 will then remain high until the next timeout or invalid voltage event.

The timeout interval is determined by the capacitor and resistor connected to the TIMER pin. Any low-to-high or high-to-low transition on the WDI pin forces the TIMER pin low for 1.5ms to discharge the capacitor from the TIMER pin to ground. After the 1.5ms period the TIMER pin is released so the resistor can start charging the capacitor. When the TIMER pin voltage reaches 90% of the VCC5V supply voltage a time-out event is triggered.

The WDI pin is pulled to VDDREF by an internal 40kΩ resistor. When the WDI pin is floating, the WDI voltage will be VDDREF. The WDI signal is compared to two threshold voltages resulting in the periodic discharge of the capacitor on the TIMER pin or disabling the watchdog function.

The WDI pin voltage is compared to VDDREF/2 to determine if there is any activity on the pin. Any rising or falling transition on the WDI pin that crosses the VDDREF/2 threshold will generate a one-shot pulse to pull the TIMER pin low for 1.5ms.

The WDI pin voltage is also compared to 90% of VCC5V. If the WDI pin is above 90% of VDD5V the watchdog feature will be disabled and the TIMER capacitor will not be discharged.

If the WDI pin voltage stays at any constant voltage below the disable threshold the resistor from TIMER to VCC5V will charge the capacitor. When the TIMER pin voltage reaches 90% of VCC5V a time-out event is triggered and PGOOD2 will be set low for 0.5ms.

Whenever WDI enters or exits its disable mode the TIMER pin is pulled low for 1.5ms.

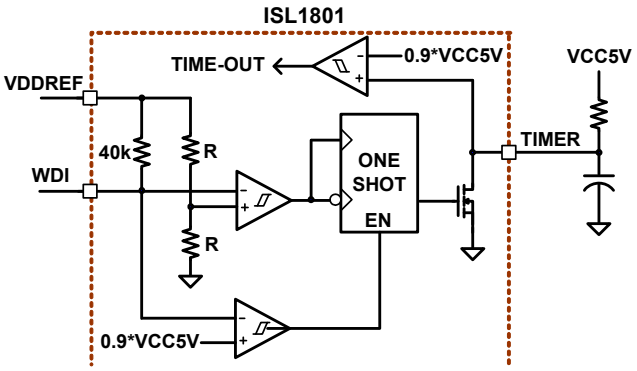



FIGURE 24. WATCHDOG TIMER LOGIC

It is important to note that the maximum leakage current into the TIMER pin is 1µA. This leakage current across the pull-up resistor will set the maximum voltage on the TIMER pin. In order to assure correct operation, the pull-up resistor from the TIMER pin to VCC5V should never be more than 200kΩ. The voltage drop for 1µA across 200kΩ is 200mV, well below the 90% threshold value of 5V - (5V * 90%) or 5V - 4.5V = 500mV. This is important because soft-start is initiated by crossing the 90% of VDD5V threshold and the watchdog timeout also depends on crossing this threshold.

Figure 25 shows the typical operational waveforms of the watch-dog timer circuit.

- $t_0$: The VR1/$V_{OUT1}$ voltage ramps up to its threshold voltage; WDI is pulled to VDDREF, which is 0V; TIMER starts to ramp-up.
- $t_1$: TIMER reaches the 90% threshold (0.9 * 5V = 4.5V) and starts to initialize the ISL1801.
- $t_2$: All preloads are sequentially applied, reset TIMER and hold it low for 1.5ms.
- $t_3$: 1.5ms timeout, TIMER starts to ramp up.
- $t_4$: TIMER voltage reaches 90% threshold, release all preloads and enable VR2 soft-start.
- $t_5$: VR2 finishes soft-start and PGOOD2 goes high; reset TIMER and hold for 1.5ms, then enable the watchdog function; MCU starts to run, WDI is floating at VDDREF, TIMER ramps up.
- $t_6$: MCU sends out the first pulse and the WDI falling edge (from high to low) resets TIMER for 1.5ms; then TIMER ramps up.
- $t_7$: TIMER is reset for 1.5ms by the WDI rising edge; then TIMER ramps up.
- $t_8$: TIMER is reset for 1.5ms by the WDI falling edge; then TIMER ramps up.
- $t_9$: TIMER is not reset in time and reaches 90% threshold level; PGOOD2 is pulled low for 1ms to reset MCU; and TIMER is reset for 1.5ms.
- $t_{10}$: PGOOD2 goes back high to exit MCU reset.
- $t_{11}$: 1.5ms timeout, TIMER ramps up.
- $t_{12}$: TIMER is reset for 1.5ms by the WDI rising edge; then TIMER ramps up.
- $t_{13}$: TIMER is not reset in time and reaches the 90% threshold level; PGOOD2 is pulled low for 1ms to reset MCU; and TIMER is reset for 1.5ms.
- $t_{14}$: PGOOD2 goes back high to exit MCU reset; then TIMER ramps up.

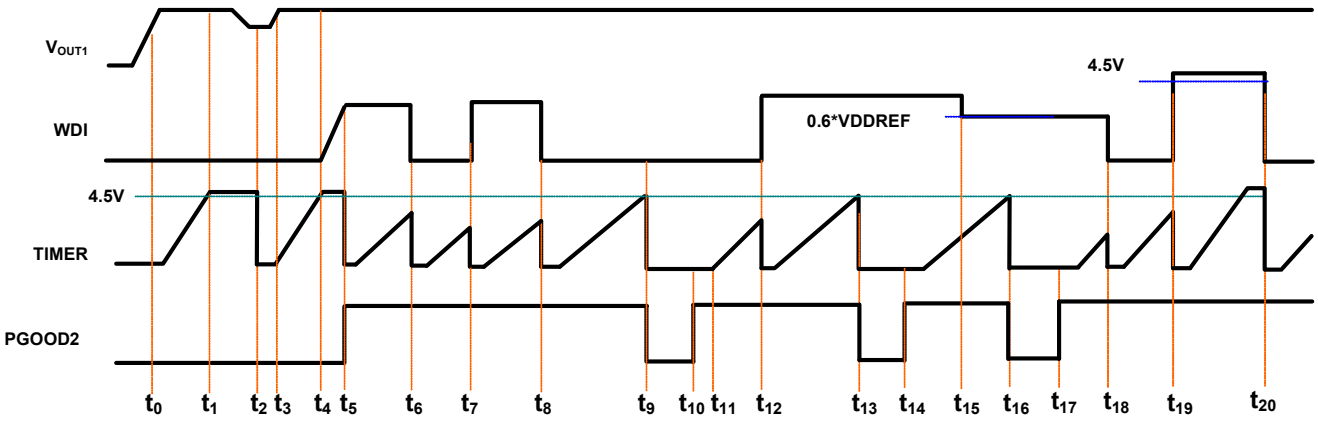



FIGURE 25. WATCHDOG TIMER WAVEFORMS

$t_{15}$: WDI voltage changes from VDDREF to 0.6*VDDREF; Since it does not cross the VDDREF/2 threshold no falling edge signal is generated; TIMER continues ramping up.

$t_{16}$: TIMER is not reset in time, and reaches the 90% threshold level; PGOOD2 is pulled low for 1ms to reset MCU; and TIMER is reset for 1.5ms.

$t_{17}$: PGOOD2 goes back high to exit MCU reset; then TIMER ramps up.

$t_{18}$: TIMER is reset for 1.5ms by the WDI falling edge; then TIMER ramps up.

$t_{19}$: TIMER is reset by the WDI rising edge; WDI is above 90%*VCC5V threshold level, watchdog function is disabled. TIMER ramps up and stays at its high state however it does not trigger a time-out.

$t_{20}$: WDI drops below the 90%*VCC5V threshold level, watch-dog function is enabled; TIMER is reset for 1.5ms by the WDI falling edge; then TIMER ramps up.

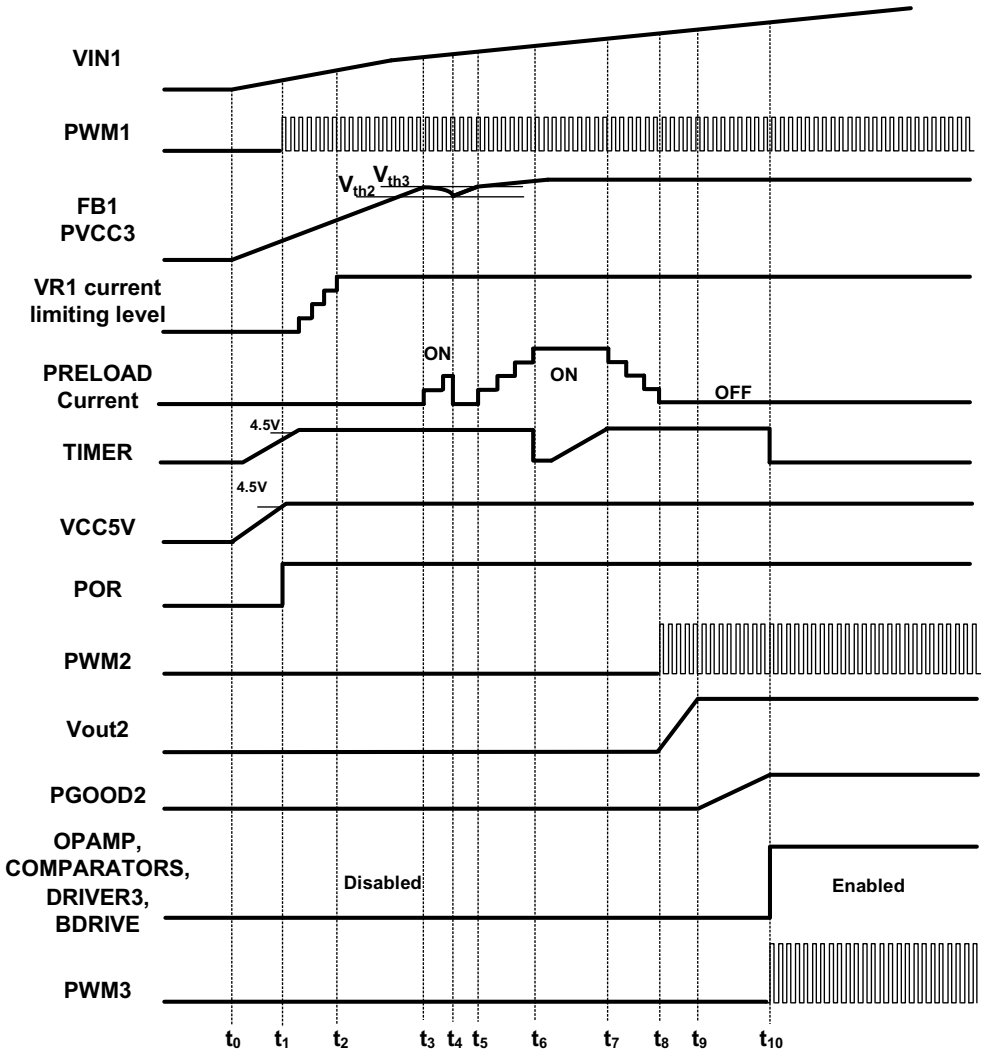



FIGURE 26. POWER-UP SEQUENCE

## Power-Up Sequence

Before $t_0$, the PV module does not output any voltage

$t_0$: Panel output voltage $V_{IN1}$ starts to ramp up; LDO1 is ON to pull $V_{OUT1}$ (=PVCC3) up; LDO2 runs in saturated condition to pull VCC5V up.

$t_1$: When VCC5V reaches its power on reset (POR) level (4.5V), the ISL1801 starts to operate and monitor the voltage at the TIMER pin; after TIMER reaches its threshold (90% * VCC5), the ISL1801 starts to initialize all internal circuits; then VR1 starts to run at the maximum duty cycle, and the VR1 current limiting level starts to ramp up step-by-step; LDO1 continues to output some current until PVCC3 reaches about 6.2V.

$t_2$: VR1 current limiting level ramps up to its final value.

$t_3$: FB1 reaches $V_{th3}$ (90% of its final value), the preload switches are turned on in sequence to apply the preload current to the VR1 output.

$t_4$: If the PV module does not have sufficient output power, PVCC3 will drop to $V_{th2}$ (fixed at 7V) when the preload is applied; this triggers the immediate removal of all preload current followed by a 500µs delay.

$t_5$: When PVCC3 goes above $V_{th2}$ again, slowly apply the preload current to VR1 output.

$t_6$: If PVCC3 stays above $V_{th2}$ after the maximum preload current is applied the TIMER voltage is pulled to 0V for 1.5ms and released; the external R-C causes the TIMER pin voltage to ramp up.

$t_7$: TIMER voltage reaches its 90% threshold; starts to remove preload step-by-step; from now on, PVCC3 and FB1 are not monitored for shut-down. Only VCC5V is monitored for undervoltage lock out (UVLO).

$t_8$: Preload is removed; VR2 starts to ramp up.

$t_9$: FB2 reaches 90% of its final value; PGOOD2 open-drain switch is open to allow PGOOD2 to rise.

$t_{10}$: PGOOD2 is high; all internal circuits, including driver, OPAMP and comparators are enabled.

NOTE: VR1 current limiting level will ramp up step-by-step with a 25% increase for each step. The preload will be applied only after the VR1 current limiting level reaches its final value and FB1 is above $V_{th3}$.

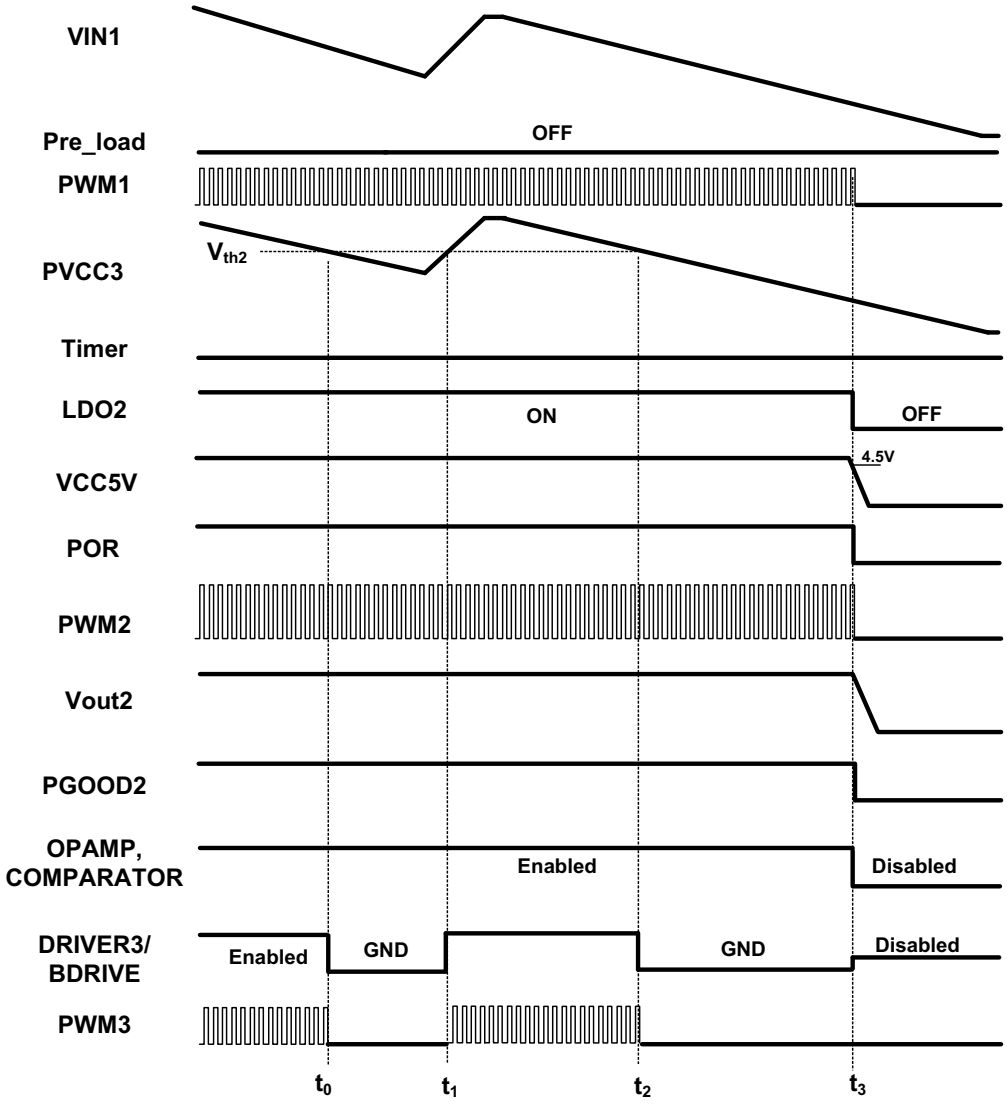



FIGURE 27. POWER-DOWN SEQUENCE

## Power-Down Sequence

Before $t_0$, the system runs in normal mode:

$t_0$: PVCC3 drops below $V_{th2}$, both drivers' outputs are pulled to GND; MCU should stop sending PWM signal; both VR1 and VR2 continue operating.

$t_1$: PVCC3 returns above $V_{th2}$, both drivers are ready to run.

$t_2$: PVCC3 drops below $V_{th2}$, both drivers' outputs are pulled to GND; both VR1 and VR2 continue operating.

$t_3$: PVCC3 drops to a very low level and VCC5V drops below the POR level (4.5V); the IC shuts down and all internal circuits are disabled.

When VCC1 drops below 6V, the VR1 power stage stops operating. The VR1 control circuit will still run until VCC5V drops below the 90% * VCC5 (4.5V) POR threshold.

## Over-Temperature Protection

Over-temperature protection (OTP) is placed on the HV die. Temperature higher than +150°C (typical) will trip the OTP disabling VR1, VR2 and the MOSFET drivers. When the temperature decreases to +135°C (typical), the ISL1801 will restart.

## Overvoltage Protection

VR1 and VR2 include overvoltage protection (OVP):

When the VR1 output voltage feedback is higher than 120% of $V_{REF1}$, the PWM output will be tri-stated and at the same time the PRELOAD current will be applied to $V_{OUT1}$ to discharge the output. When $V_{OUT1}$ is discharged and FB1 reaches $V_{REF1}$ the OCP will turn off and normal PWM operation will resume.

When the VR2 output voltage feedback is higher than 120% of $V_{REF2}$, the PWM output will be tri-stated. After $V_{OUT2}$ falls so that FB2 is equal to $V_{REF2}$ the OCP will turn off and normal PWM operation will resume.

# Applications Information

## Application Circuits

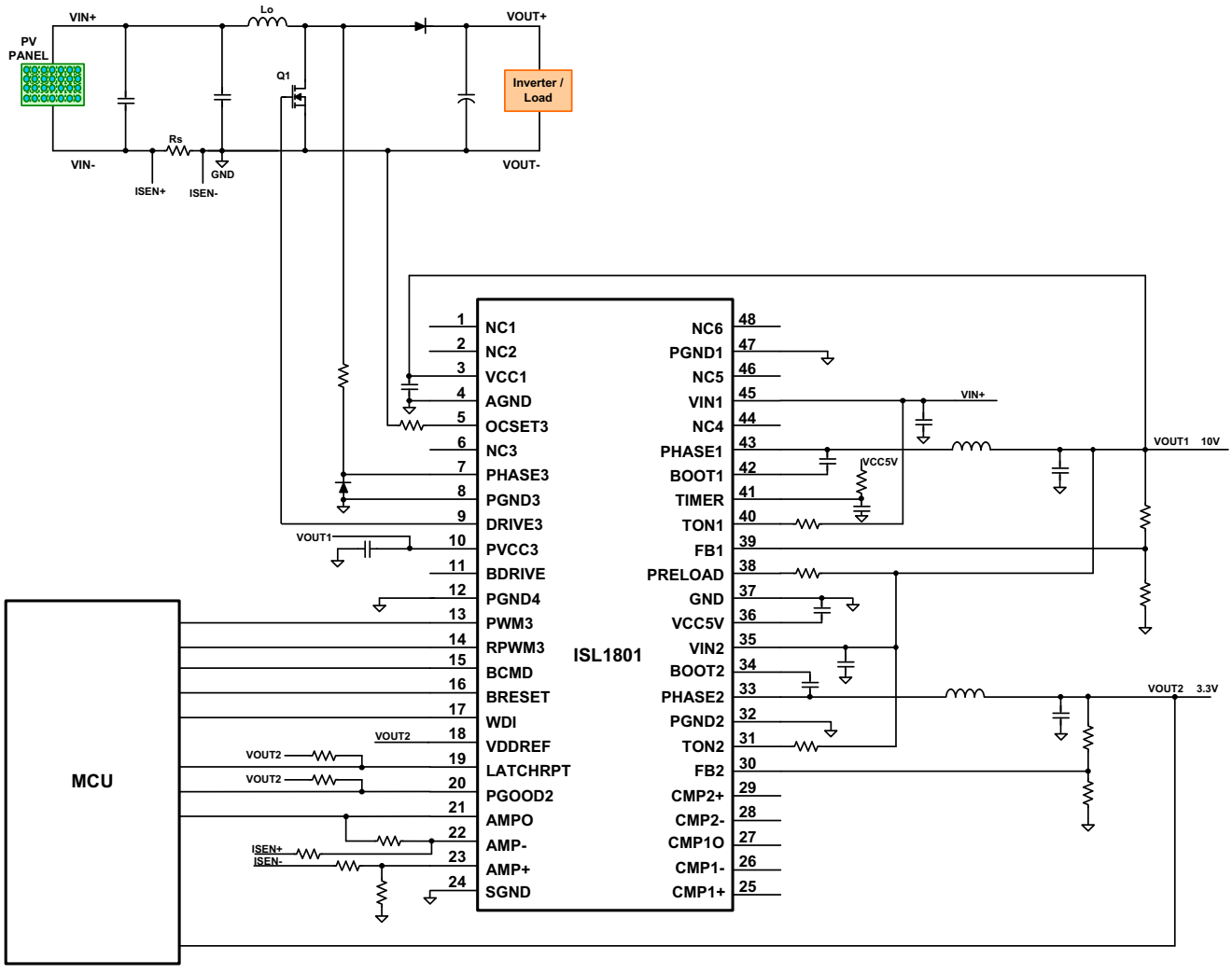



FIGURE 28. BOOST REGULATOR

## Application Circuits (Continued)

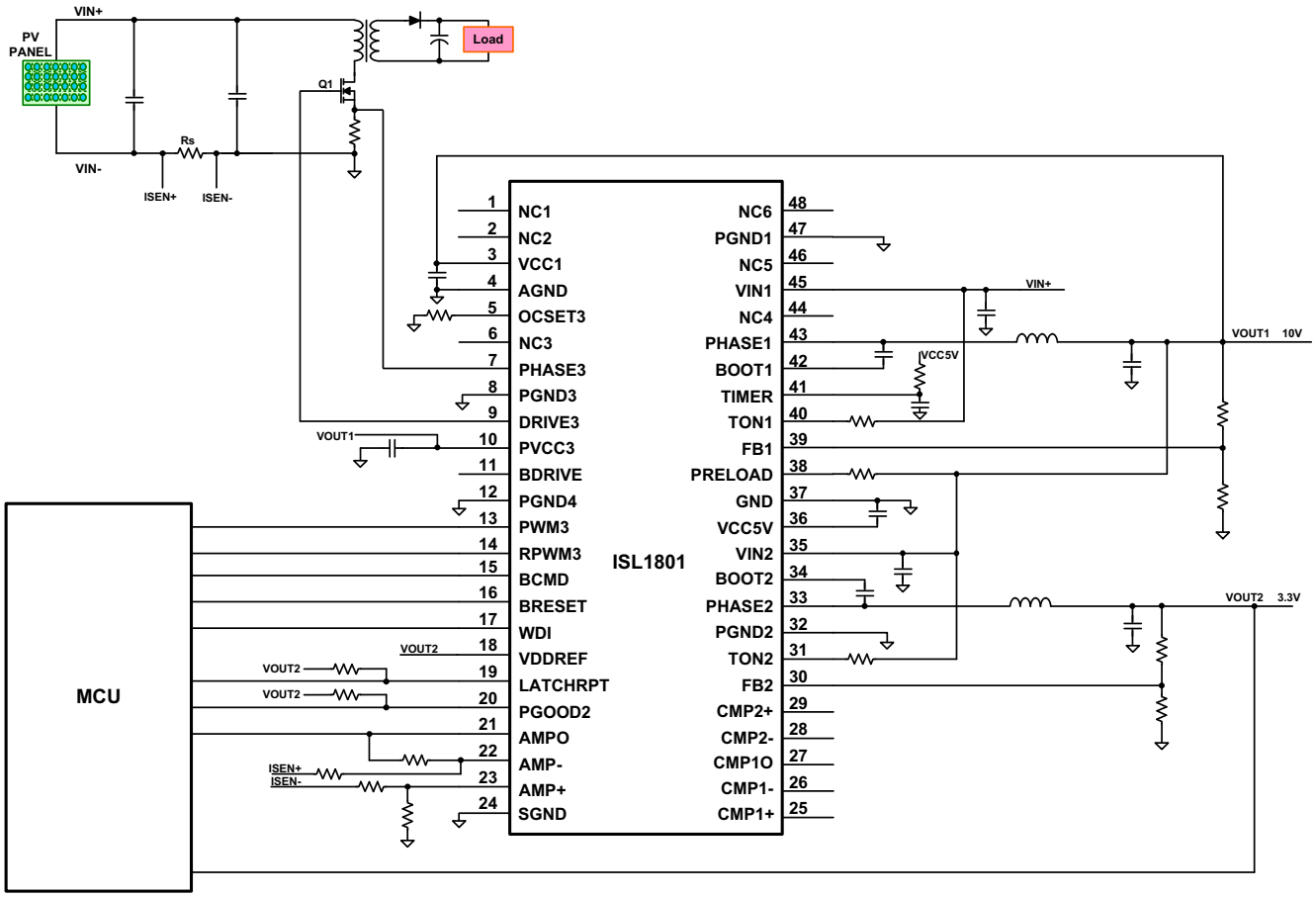



FIGURE 29. FLY BACK REGULATOR

## Application Circuits (Continued)

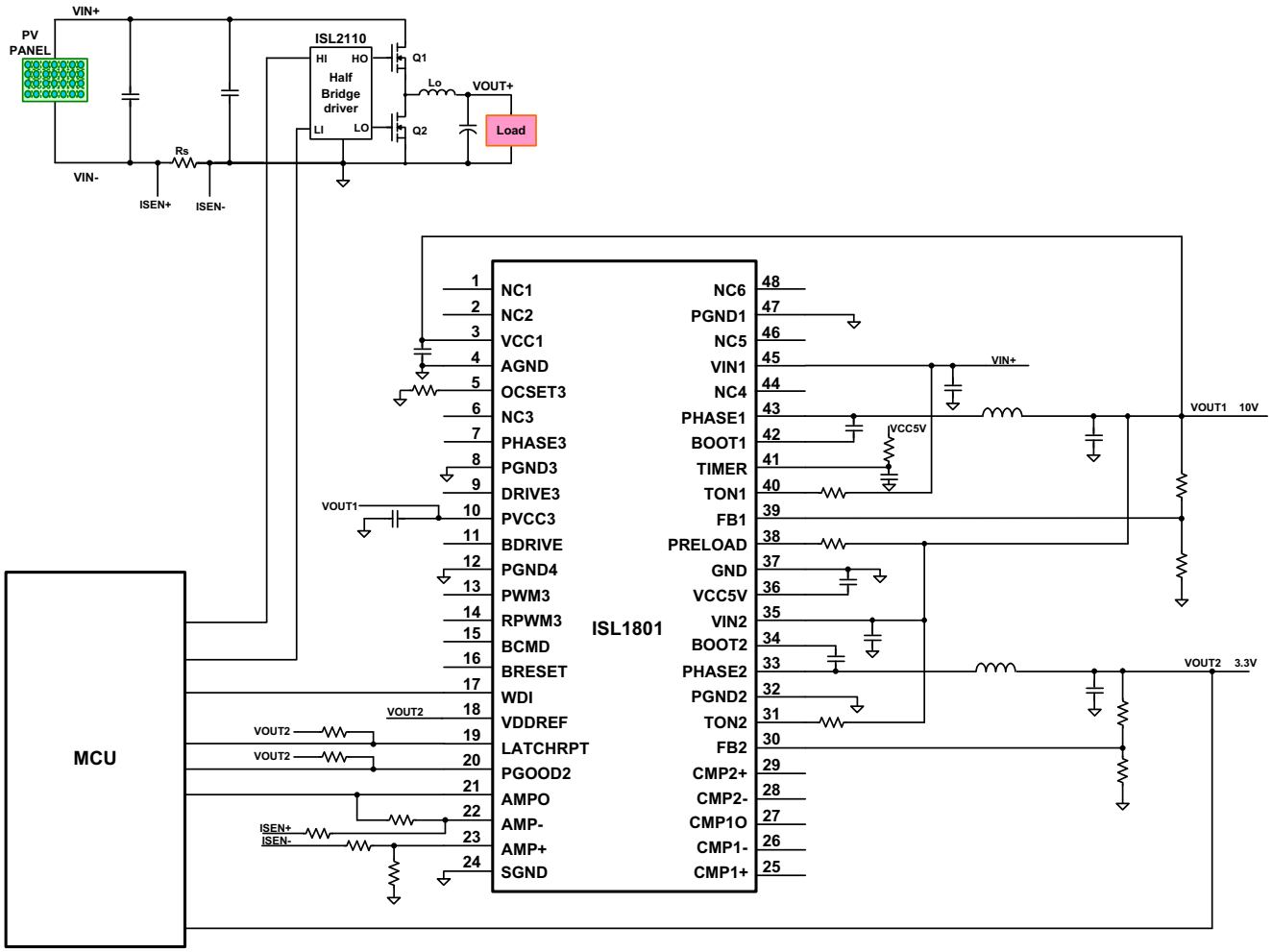



FIGURE 30. SYNCHRONOUS BUCK REGULATOR WITH EXTERNAL HALF BRIDGE DRIVER

## Application Circuits (Continued)

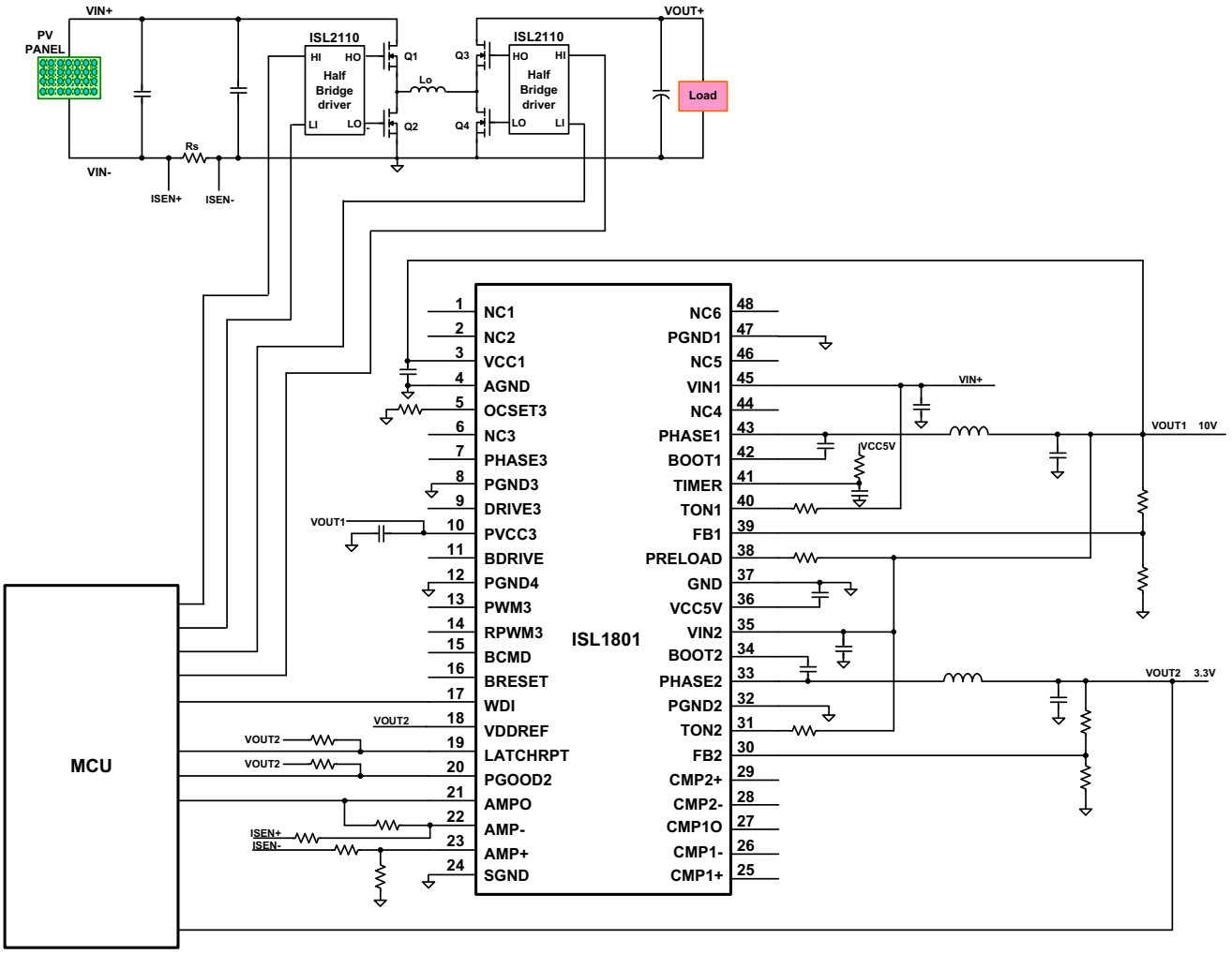



FIGURE 31. BUCK-BOOST REGULATOR WITH EXTERNAL HALF BRIDGE DRIVERS

# PC Board Layout Guidelines

Careful PC board layout is critical to achieve minimal switching losses and clean, stable operation. This is especially true when multiple converters are on the same PC board where one circuit can affect the other. For specific layout example of the ISL1801EVAL1ZA evaluation board please contact Intersil sales support with your needs.

Mount all of the power components on the top side of the board with their ground terminals flush against one another, if possible. Follow these guidelines for good PC board layout:

- Isolate the power components on the top side from the sensitive analog components on the bottom side with a ground shield. Use a separate PGND plane under the $V_{OUT1}$ and $V_{OUT2}$ sections (called PGND1 and PGND2). Avoid the introduction of AC currents into the PGND1 and PGND2 ground planes. Run the power plane ground currents on the top side only, if possible.
- Use a star ground connection on the power plane to minimize the crosstalk between $V_{OUT1}$ and $V_{OUT2}$.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PC boards (2oz vs 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PC board traces must be approached in terms of fractions of centimeters, where a single mW of excess trace resistance causes a measurable efficiency penalty.
- PHASE3 and GND connections to the synchronous rectifiers for current limiting must be made using Kelvin-sense connections to guarantee the current-limit accuracy. This is best done by routing power to the MOSFETs from outside using the top copper layer, while connecting PHASE traces inside (underneath) the MOSFETs.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the

discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the synchronous rectifier or between the inductor and the output filter capacitor.

- Ensure that the OUT connection to COUT is short and direct. However, in some cases it may be desirable to deliberately introduce some trace length between the OUT connector node and the output filter capacitor.
- Route high-speed switching nodes (BOOT, PHASE, DRIVE3 and BDRIVE) away from sensitive analog areas (VDDREF, FB and AMP±). Use PGND1 and PGND2 as an EMI shield to keep radiated switching noise away from the IC's feedback divider and analog bypass capacitors.
- Make all pin-strap control input connections to GND or VCC of the device.

## Layout Procedure

Place the power components first with ground terminals adjacent. If possible, make all these connections on the top layer with wide, copper-filled areas.

Mount the controller IC adjacent to the synchronous rectifier MOSFETs close to the hottest spot, preferably on the back side in order to keep DRIVE3, GND, and the BDRIVE gate drive lines short and wide. The DRIVE3 gate trace must be short and wide, measuring 50 mils to 100 mils wide if the MOSFET is 1” from the controller device.

Group the gate-drive components (BOOT capacitor, VIN bypass capacitor) together near the controller device.

Make the DC/DC controller ground connections as follows:

1. Near the device, create a small analog ground plane.
2. Connect the small analog ground plane to GND and use the plane for the ground connection for the VDDREF and VCC bypass capacitors, FB dividers and ILIM resistors (if any).
3. Create another small ground island for PGND and use the plane for the VIN bypass capacitor, placed very close to the device.
4. Connect the GND and PGND planes together under device.

On the board's top-side (power planes), make a star ground to minimize crosstalk between the two sides. The top-side star ground is a star connection of the input capacitors and synchronous rectifiers. Keep the resistance low between the star ground and the source of the synchronous rectifiers for accurate current limit. Connect the top-side star ground (used for MOSFET, input, and output capacitors) to the small island with a single short, wide connection (preferably just a via). Create PGND islands on the layer just below the top-side layer to act as an EMI shield if multiple layers are available (highly recommended). Connect each of these individually to the star ground via, which connects the top-side to the PGND plane. Add one more solid ground plane under the device to act as an additional shield, and also connect the solid ground plane to the star ground via.

Connect the output power planes directly to the output filter capacitor positive and negative terminals with multiple vias.

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| July 24, 2014 | FN8259.1 | "Absolute Maximum Ratings" on page 7: changed BDRIVE, DRIVE3 Voltages from: -0.3V to VCC1+0.3V BDRIVE, to:-0.3V to PVCC3+0.3V.<br>Updated description of pin VCC1 on page 4.<br>Updated Electrical Spec Tables. |
| June 29, 2012 | FN8259.0 | Initial Release. |

# About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

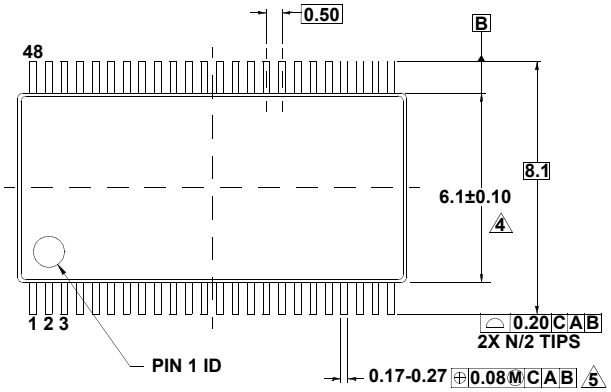
You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support

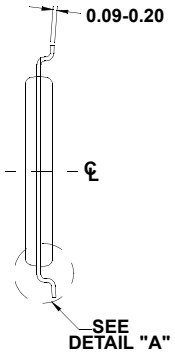
# Package Outline Drawing

## M48.240

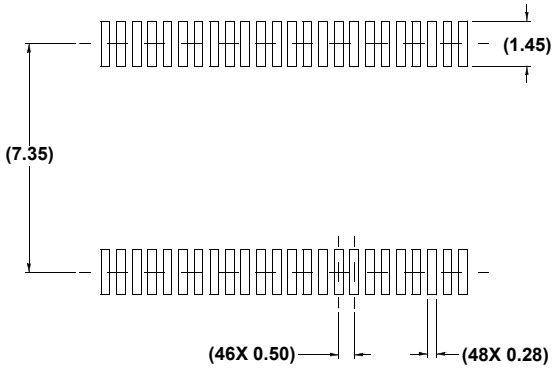
**48 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)**
**Rev 1, 11/10**



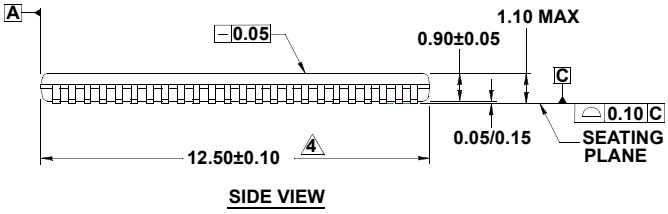

TOP VIEW



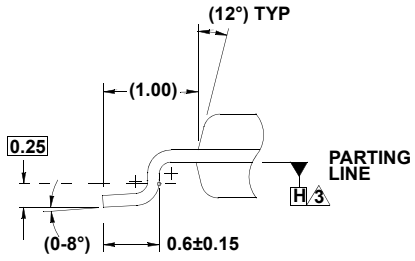

BOTTOM VIEW




TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW




DETAIL "A"
SCALE: (NONE)
(VIEW ROTATED 90° C.W.)

**NOTES:**

1. All dimensions are in millimeters (angles in degrees).
2. Dimensioning & tolerances per ASME. Y14.5m-1994.
3. Datum plane H located at mold parting line and coincident with lead where lead exits plastic body at bottom of parting line.
4. At reference datum and does not include mold flash or protrusions, and is measured at the bottom parting line. Mold flash or protrusions shall not exceed 0.15mm on the package ends and 0.25mm between the leads.
5. The lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusions and an adjacent lead should be 0.07mm.
6. This part is compliant with JEDEC specification MO-153 variation ED except it is 0.1mm thinner.
7. Dimensions in ( ) are for reference only.