ISL267450

12-Bit, 1MSPS SAR ADCs

FN8341
Rev 0.00
August 10, 2012

The ISL267450 is a 12-bit, 1MSPS sampling SAR-type ADC with a differential input span of $2*V_{REF}$ volts. The ISL267450 features excellent linearity over supply and temperature variations and is drop-in compatible with the AD7450. The device can operate from a supply voltage of either 5V or 3V and maintain measurement accuracy with input signals up to the supply rails.

The serial digital interface is SPI compatible and is easily interfaced to popular FPGAs and microcontrollers. Power dissipation is 9.0mW at a sampling rate of 1MSPS, and just 5µW between conversions utilizing Auto Power-Down mode (with a 3V supply).

The ISL267450 is available in 8 Ld SOIC or MSOP packages, and are specified for operation over the Industrial temperature range (–40°C to +85°C).

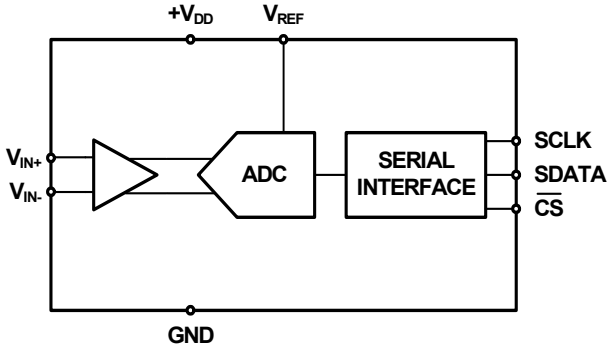
Features

- Drop-in Compatible with AD7450
- Differential Input
- Simple SPI-compatible Serial Digital Interface
- Guaranteed No Missing Codes
- 1MHz Sampling Rate
- 3V or 5V Operation
- Low Operating Current
  - 1.25mA at 833kSPS with 3V Supplies
  - 1.7mA at 1MSPS with 5V Supplies
- Power-down Current between Conversions: 1µA
- Excellent Differential Non-Linearity
- Low THD: -83dB (typ)
- Pb-Free (RoHS Compliant)
- Available in SOIC and MSOP Packages

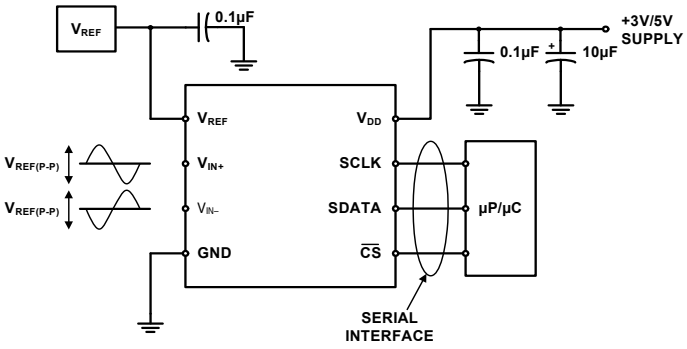
Applications

- Remote Data Acquisition
- Battery Operated Systems
- Industrial Process Control
- Energy Measurement
- Data Acquisition Systems
- Pressure Sensors
- Flow Controllers

Block Diagram

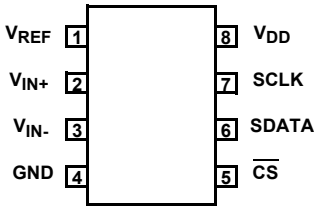


Typical Connection Diagram



Pin Configuration

ISL267450
(8 LD SOIC, MSOP)
TOP VIEW



Pin Description

ISL267450		DESCRIPTION
PIN NAME	PIN NUMBER	
V_{DD}	8	Supply voltage, +2.7V to 5.25V.
SCLK	7	Serial clock input. Controls digital I/O timing and clocks the conversion.
SDATA	6	Digital conversion output.
$\overline{CS}$	5	Chip select input. Controls the start of a conversion when going low.
GND	4	Ground
V_{IN-}	3	Negative analog input.
V_{IN+}	2	Positive analog input.
V_{REF}	1	Reference voltage.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	VDD RANGE (V)	TEMP RANGE (°C)	PACKAGE (PB-free)	PKG. DWG. #
ISL267450IBZ	267450 IBZ	2.7 to 5.25	-40 to +85	8 Ld SOIC	M8.15
ISL267450IUZ	67450	2.7 to 5.25	-40 to +85	8 Ld MSOP	M8.118

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL267450. For more information on MSL please see techbrief TB363.

Table of Contents

Absolute Maximum Ratings 5
Thermal Information 5
Electrical Specifications 5
Typical Performance Characteristics 9
Functional Description 11
ADC Transfer Function 12
Analog Input 12
Voltage Reference Input 13
Converter Operation 14
Power-On Reset 14
Acquisition Time 14
Short Cycling 14
Power vs Throughput Rate 14
Serial Interface 15
Data Format 15
Application Hints 15
Grounding and Layout 15
Terminology 15
Signal-to-(Noise + Distortion) Ratio (SINAD) 15
Total Harmonic Distortion 15
Peak Harmonic or Spurious Noise (SFDR) 15
Intermodulation Distortion 15
Aperture Delay 16
Aperture Jitter 16
Full Power Bandwidth 16
Common-Mode Rejection Ratio (CMRR) 16
Integral Nonlinearity (INL) 16
Differential Nonlinearity (DNL) 16
Zero-Code Error 16
Positive Gain Error 16
Negative Gain Error 16
Track and Hold Acquisition Time 16
Power Supply Rejection Ratio (PSRR) 16
Revision History 17
Products 17
Package Outline Drawing 18
Package Outline Drawing 19

Absolute Maximum Ratings

Any Pin to GND . . . . . -0.3V to +6.0V
Analog Input to GND. . . . . -0.3V to V_{DD}+0.3V
Digital I/O to GND. . . . . -0.3V to V_{DD}+0.3V
Digital Input Voltage to GND . . . . . -0.3V to V_{DD}+0.3V
Maximum Current In to Any Pin 10mA
ESD Rating
Human Body Model (Tested per JESD22-A114F). 8kV
Machine Model (Tested per JESD22-A115B) 400V
Charged Device Model (Tested per JESD22-C101E). 1.5kV
Latch Up (Tested per JESD78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (Notes 4, 5).	120	64
8 Ld MSOP Package (Notes 4, 5).	165	64

Operating Temperature . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_{DD} = +3.0V to +3.3V, F_{SCLK} = 15MHz, F_S = 833kSPS, V_{REF} = 1.25V, F_{IN} = 200kHz; V_{DD} = +4.75V to +5.25V, F_{SCLK} = 18MHz, F_S = 1MSPS, V_{REF} = 2.5V, F_{IN} = 300kHz; V_{CM} = V_{REF}, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
DYNAMIC PERFORMANCE						
SINAD	Signal-to (Noise + Distortion) Ratio	V_{DD} = 5V	**70**			dB
		V_{DD} = 3V	**67**			dB
THD	Total Harmonic Distortion	V_{DD} = 5V		-80	**-75**	dB
		V_{DD} = 3V		-78	**-73**	dB
SFDR	Spurious Free Dynamic Range	V_{DD} = 5V		-82	**-75**	dB
		V_{DD} = 3V		-80	**-73**	dB
IMD	Intermodulation Distortion	2nd Order Terms		–89		dB
		3rd Order Terms		-85		dB
tpd	Aperture Delay			10		ns
Δtpd	Aperture Jitter			50		ps
β3dB	Full Power Bandwidth	@ –3dB		20		MHz
		@ –0.1dB		2.5		MHz
PSRR	Power Supply Rejection Ratio			-87		dB
DC ACCURACY						
N	Resolution		**12**			Bits
INL	Integral Nonlinearity		**-1**		**1**	LSB
DNL	Differential Nonlinearity	Guaranteed no missed codes to 12 bits	**-0.95**		**0.95**	LSB
OFFSET	Zero-Code Error	V_{DD} = 5V	**-3**		**3**	LSB
		V_{DD} = 3V	**-6**		**6**	LSB
GAIN	Positive Gain Error	V_{DD} = 5V	**-3**		**3**	LSB
		V_{DD} = 3V	**-6**		**6**	LSB
	Negative Gain Error	V_{DD} = 5V	**-3**		**3**	LSB
		V_{DD} = 3V	**-6**		**6**	LSB

Electrical Specifications V_{DD} = +3.0V to +3.3V, F_{SCLK} = 15MHz, F_S = 833kSPS, V_{REF} = 1.25V, F_{IN} = 200kHz; V_{DD} = +4.75V to +5.25V, F_{SCLK} = 18MHz, F_S = 1MSPS, V_{REF} = 2.5V, F_{IN} = 300kHz; V_{CM} = V_{REF}, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
ANALOG INPUT (Note 7)						
|AIN|	Full-Scale Input Span	2 x V_{REF}		V_{IN+} - V_{IN-}		V
V_{IN+}, V_{IN-}	Absolute Input Voltage Range	V_{CM} = V_{REF}				V
	V_{IN+}			V_{CM} ± V_{REF}/2		V
	VIN–			V_{CM} ± V_{REF}/2		V
I_{LEAK}	Input Leakage Current		-1		1	µA
C_{VIN}	Input Capacitance	Track Mode		12		pF
		Hold Mode		6		pF
REFERENCE INPUT						
V_{REF}	V_{REF} Input Voltage Range	V_{DD} = 5V (±1% tolerance for specified performance)		2.5		V
		V_{DD} = 3V (±1% tolerance for specified performance)		1.25		V
I_{LEAK}	DC Leakage Current		-1		1	µA
C_{VREF}	V_{REF} Input Capacitance			19		pF
LOGIC INPUTS						
V_{IH}	Input High Voltage		2.4			V
V_{IL}	Input Low Voltage				0.8	V
I_{LEAK}	Input Leakage Current		-1		1	µA
C_{IN}	Input Capacitance				10	pF
LOGIC OUTPUTS						
V_{OH}	Output High Voltage	I_{SOURCE} = 200µA	V_{DD} - 0.3			V
V_{OL}	Output Low Voltage	I_{SINK} = 200µA			0.4	V
I_{LEAK}	Floating-State Leakage Current		-1		1	µA
C_{OUT}	Floating-State Output Capacitance				10	pF
	Output Coding		Two's Complement			
CONVERSION RATE						
t_{CONV}	Conversion Time	888ns with F_{SCLK} = 18MHz		16		SCLK Cycles
		1.07µs with F_{SCLK} = 15MHz		16		SCLK Cycles
t_{ACQ}	Acquisition Time (Note 8)	Sine Wave Input			200	ns
F_{max}	Throughput Rate	V_{DD} = 5V			1	MSPS
		V_{DD} = 3V			833	kSPS
POWER REQUIREMENTS						
V_{DD}	Positive Supply Voltage Range	3.3V ± 10%	3.0		3.6	V
		5V ± 5%	4.75		5.25	V

Electrical Specifications V_{DD} = +3.0V to +3.3V, F_{SCLK} = 15MHz, F_S = 833kSPS, V_{REF} = 1.25V, F_{IN} = 200kHz; V_{DD} = +4.75V to +5.25V, F_{SCLK} = 18MHz, F_S = 1MSPS, V_{REF} = 2.5V, F_{IN} = 300kHz; V_{CM} = V_{REF}, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
I_{DD}	Positive Supply Input Current					
	Static	V_{DD} = 3V/5V; SCLK ON or OFF			1	µA
	Dynamic	V_{DD} = 5V; f_S = 1MSPS			1.7	mA
		V_{DD} = 3V; f_S = 833kSPS			1.25	mA
P_D	Power Dissipation					
	Static Mode	V_{DD} = 3V/5V; SCLK ON or OFF			5	µW
	Dynamic	V_{DD} = 5V; f_S = 1MSPS			8.5	mW
		V_{DD} = 3V; f_S = 833kSPS			3.75	mW

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. The absolute voltage applied to each analog input must not exceed V_{DD}.
8. Read about “Acquisition Time” on page 14 for a discussion of this parameter.

Electrical Specifications Limits established by characterization and are not production tested. V_{DD} = +4.75V to +5.25V, F_{SCLK} = 18MHz, F_S = 1MSPS, V_{REF} = 2.5V, F_{IN} = 300kHz; V_{CM} = V_{REF}, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
fSCLK	Clock Frequency		0.05		18	MHz
t_{SCLK}	Clock Period		55			ns
$t_{CONVERT}$	Conversion Time	16 x t_{SCLK}			888	ns
t_{QUIET}	Quiet Time Before Sample		25			ns
t_{CSS}	$\overline{CS}$ Falling Edge to S_{CLK} Falling Edge Setup Time		10			ns
$t_{DISABLE}$	$\overline{CS}$ Falling Edge to SDATA Disable Time (Note 9)	Extrapolated back to true bus relinquish	10		35	ns
	Data Access Time after SCLK Falling Edge					
t_{SWH}	SCLK High Pulsewidth		0.4 x t_{SCLK}		0.6 x t_{SCLK}	ns
t_{SWL}	SCLK Low Pulsewidth		0.4 x t_{SCLK}		0.6 x t_{SCLK}	ns
t_{CLKDV}	SCLK Falling Edge to SDATA Valid				40	ns
t_{SDH}	SCLK Falling Edge to SDATA Hold		10			ns
t_{ACQ}	Acquisition Time (Note 8)					ns
t_{CSW}	$\overline{CS}$ Pulse Width		10			ns
t_{CDV}	$\overline{CS}$ Falling Edge to SDATA Valid				20	ns

Electrical Specifications Limits established by characterization and are not production tested. V_{DD} = +3.0V to +3.3V, F_{SCLK} = 15MHz, F_S = 833kSPS, V_{REF} = 1.25V, F_{IN} = 200kHz; V_{REF} = 2.5V; V_{CM} = V_{REF}, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
fSCLK	Clock Frequency		0.05		15	MHz
t_{SCLK}	Clock Period		55			ns
$t_{CONVERT}$	Conversion Time	16 x t_{SCLK}			1.07	µs

Electrical Specifications Limits established by characterization and are not production tested. V_{DD} = +3.0V to +3.3V, F_{SCLK} = 15MHz, F_S = 833kSPS, V_{REF} = 1.25V, F_{IN} = 200kHz; V_{REF} = 2.5V; V_{CM} = V_{REF}, T_A = T_{MIN} to T_{MAX} unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
t_{QUIET}	Quiet Time Before Sample		25			ns
t_{CSS}	$\overline{CS}$ Falling Edge to S_{CLK} Falling Edge Setup Time		10			ns
$t_{DISABLE}$	$\overline{CS}$ Falling Edge to SDATA Disable Time (Note 9)	Extrapolated back to true bus relinquish	10		35	µs
t_{SWH}	SCLK High Pulsewidth		0.4 x t_{SCLK}		0.6 x t_{SCLK}	ns
t_{SWL}	SCLK Low Pulsewidth		0.4 x t_{SCLK}		0.6 x t_{SCLK}	ns
t_{CLKDV}	SCLK Falling Edge to SDATA Valid				40	ns
t_{SDH}	SCLK Falling Edge to SDATA Hold		10			ns
t_{ACQ}	Acquisition Time (Note 8)					ns
t_{CSW}	$\overline{CS}$ Pulse Width		10			ns
t_{CDV}	$\overline{CS}$ Falling Edge to SDATA Valid				20	ns

NOTE:

9. During characterization, $t_{DISABLE}$ is measured from the release point with a 10pF load (see Figure 2 on page 8) and the equivalent timing using the AD7450 loading (50pF) is calculated.

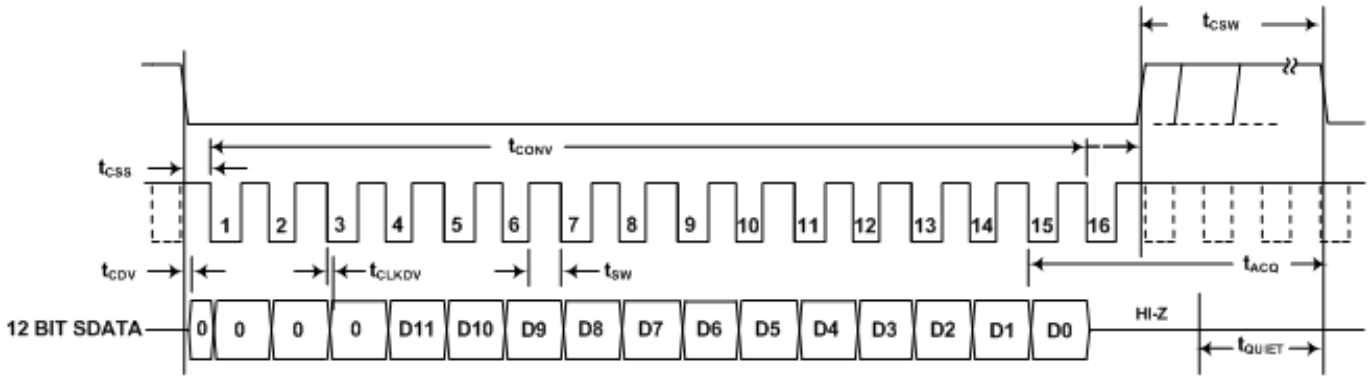


FIGURE 1. SERIAL INTERFACE TIMING DIAGRAM

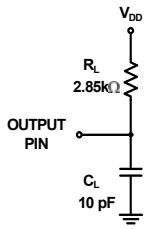


FIGURE 2. EQUIVALENT LOAD CIRCUIT

Typical Performance Characteristics

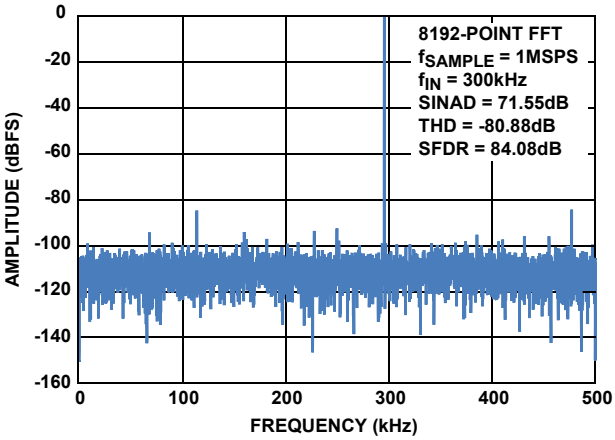


FIGURE 3. DYNAMIC PERFORMANCE AT 1MSPS WITH V_{DD} = 5V

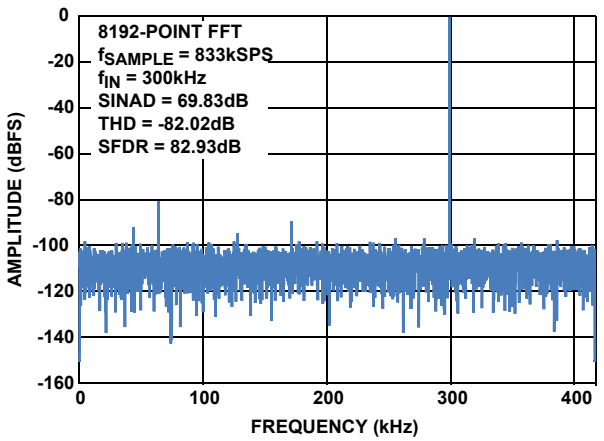


FIGURE 4. DYNAMIC PERFORMANCE AT 833KSPS WITH V_{DD} = 3V

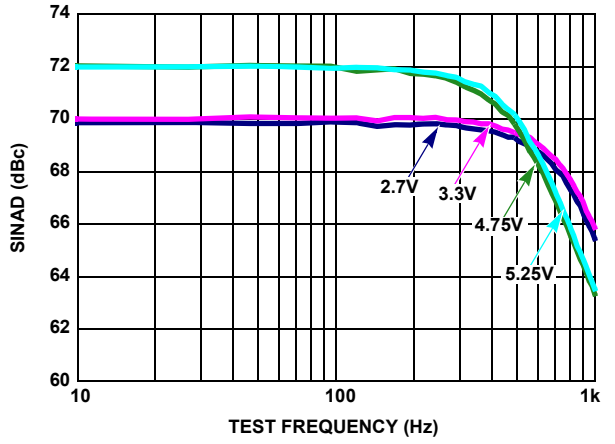


FIGURE 5. SINAD vs ANALOG FREQUENCY FROM VARIOUS SUPPLY VOLTAGES

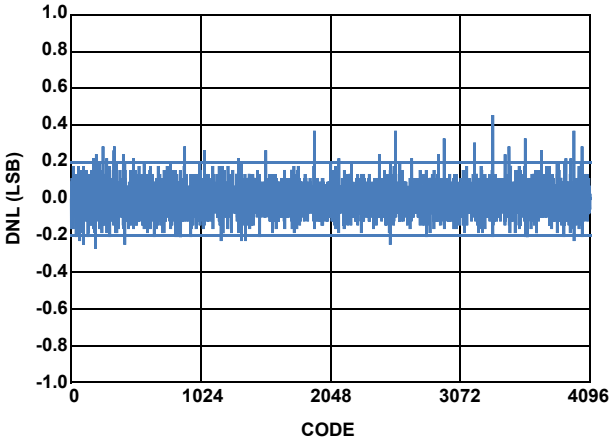


FIGURE 6. TYPICAL DNL FOR V_{DD} = 5V

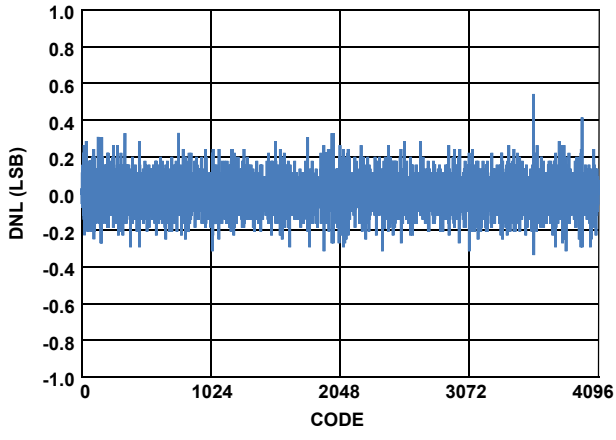


FIGURE 7. TYPICAL DNL FOR V_{DD} = 3V

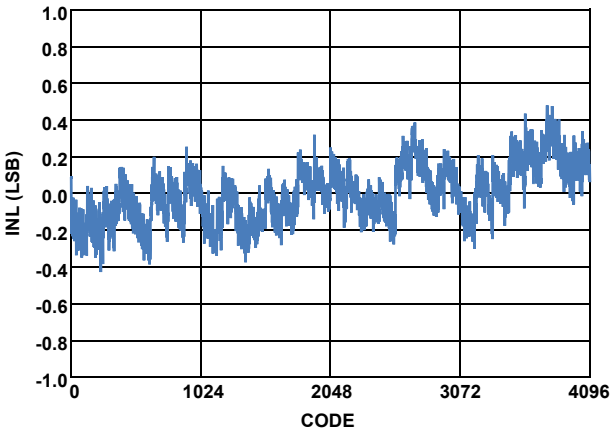


FIGURE 8. TYPICAL INL FOR V_{DD} = 5V

Typical Performance Characteristics (Continued)

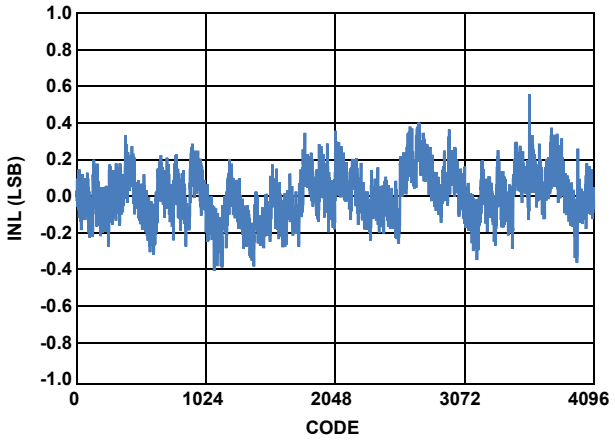


FIGURE 9. TYPICAL INL FOR V_{DD} = 3V

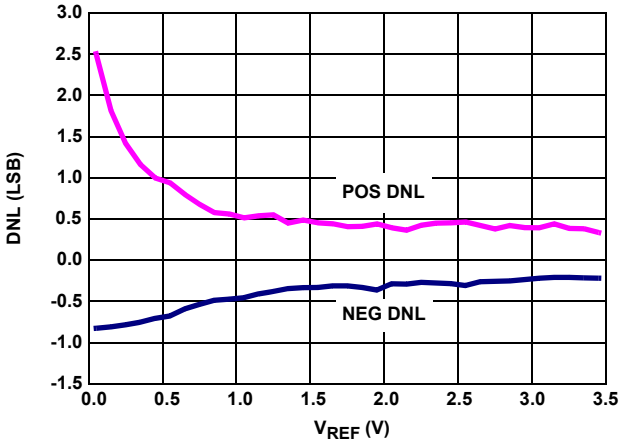


FIGURE 10. CHANGE IN DNL vs V_{REF} FOR V_{DD} = 5V

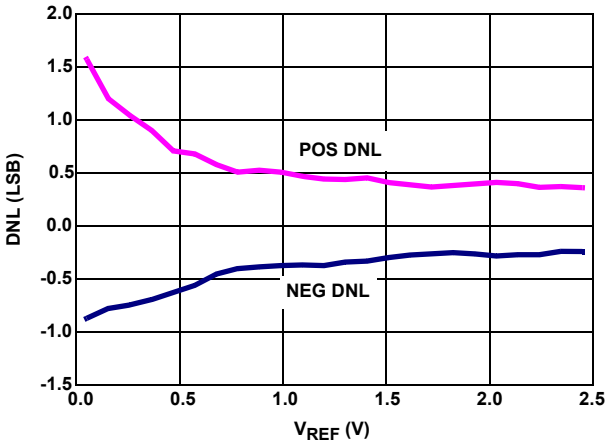


FIGURE 11. CHANGE IN DNL vs V_{REF} FOR V_{DD} = 3.3V

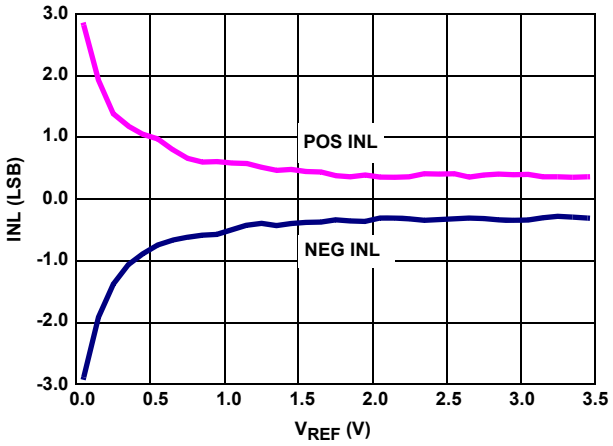


FIGURE 12. CHANGE IN INL vs V_{REF} FOR V_{DD} = 5V

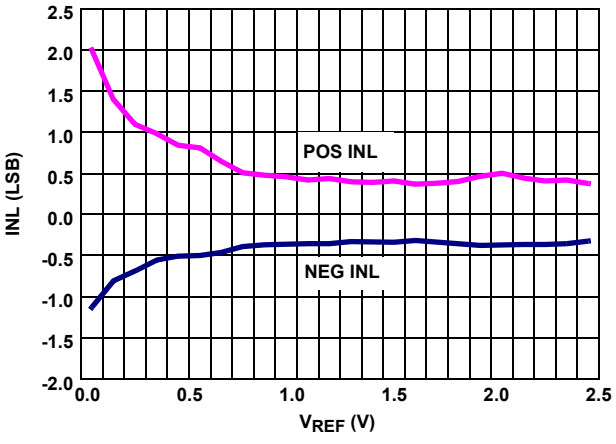


FIGURE 13. CHANGE IN INL vs V_{REF} FOR V_{DD} = 3.3V

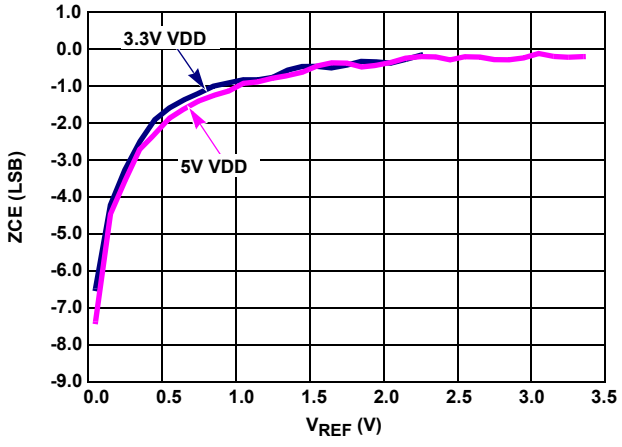


FIGURE 14. CHANGE IN OFFSET ERROR vs V_{REF} FOR V_{DD} = 5V AND 3.3V

Typical Performance Characteristics (Continued)

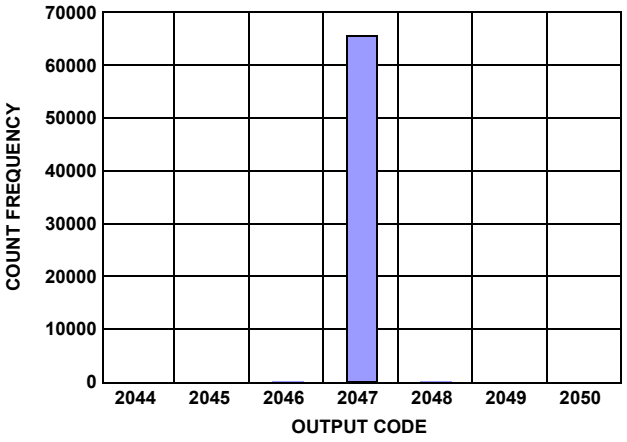


FIGURE 15. HISTOGRAM OF THE OUTPUT CODES WITH A DC INPUT FOR V_{DD} = 5V

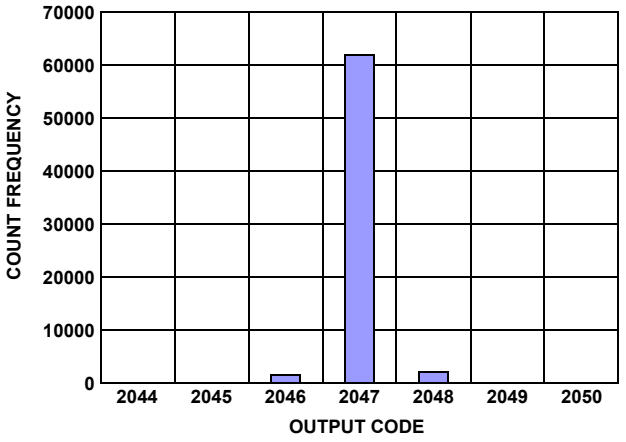


FIGURE 16. HISTOGRAM OF THE OUTPUT CODES WITH A DC INPUT FOR V_{DD} = 3V

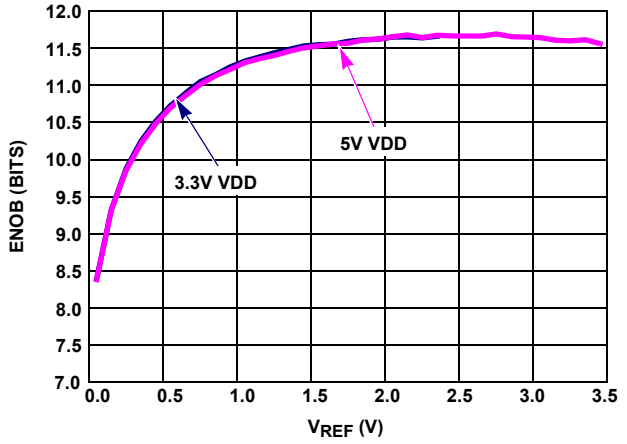


FIGURE 17. CHANGE IN ENOB vs V_{REF} FOR V_{DD} = 5V AND 3.3V

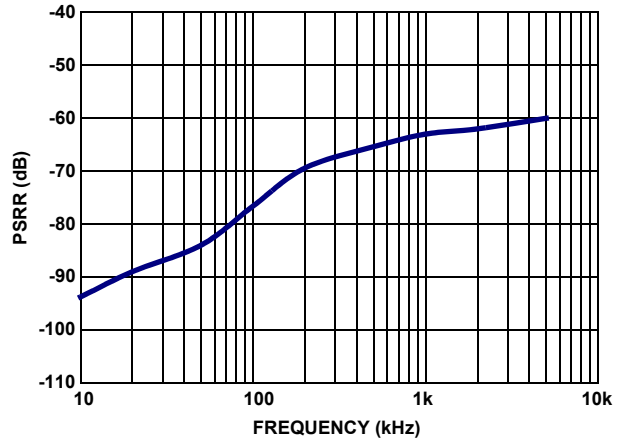


FIGURE 18. CMRR vs INPUT FREQUENCY FOR V_{DD} = 5V AND 3V

Functional Description

The ISL267450 is based on a successive approximation register (SAR) architecture utilizing capacitive charge redistribution digital-to-analog converters (DACs). Figure 19 shows a simplified representation of the converter. During the acquisition phase (ACQ), the differential input is stored on the sampling capacitors ($\overline{CS}$). The comparator is in a balanced state since the switch across its inputs is closed. The signal is fully acquired after t_{ACQ} has elapsed, and the switches then transition to the conversion phase (CONV) so the stored voltage may be converted to digital format. The comparator will become unbalanced when the differential switch opens and the input switches transition (assuming that the stored voltage is not exactly at mid-scale). The comparator output reflects whether the stored voltage is above or below mid-scale, which sets the value of the MSB. The SAR logic then forces the capacitive DACs to adjust up or down by one quarter of full-scale by switching in binarily weighted capacitors. Again the comparator output reflects whether the stored voltage is above or below the new value, setting the value of the next lowest bit. This process repeats until all 12 bits have been resolved.

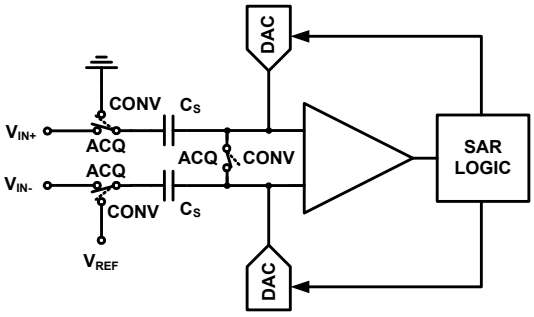


FIGURE 19. SAR ADC ARCHITECTURAL BLOCK DIAGRAM

An external clock must be applied to the SCLK pin to generate a conversion result. The allowable frequency range for SCLK is 50kHz to 18MHz. Serial output data is transmitted on the falling edge of SCLK. The receiving device (FPGA, DSP or Microcontroller) may latch the data on the rising edge of SCLK to maximize set-up and hold times.

A stable, low-noise reference voltage must be applied to the V_{REF} pin to set the full-scale input range and common-mode voltage. See “Voltage Reference Input” on page 13 for more details.

ADC Transfer Function

The output coding for the ISL267450 is two’s complement. The first code transition occurs at successive LSB values (i.e., 1 LSB, 2 LSB, and so on). The LSB size of the ISL267450 is $2*V_{REF}/4096$. The ideal transfer characteristic of the ISL267450 is shown in Figure 20.

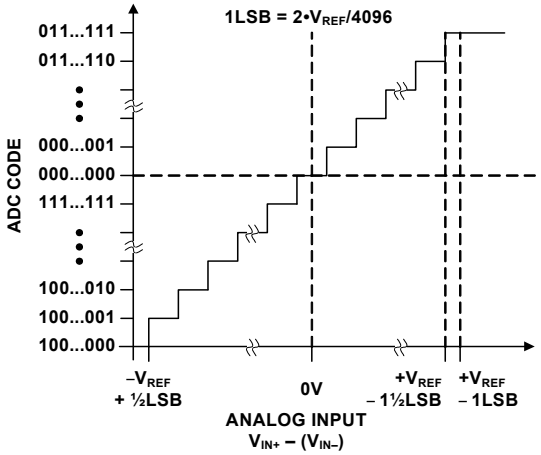


FIGURE 20. IDEAL TRANSFER CHARACTERISTICS

Analog Input

The ISL267450 features a fully differential input with a nominal full-scale range equal to twice the applied V_{REF} voltage. Each input swings V_{REF} V_{P-P}, 180° out-of-phase from one another for a total differential input of $2*V_{REF}$ (see Figure 21).

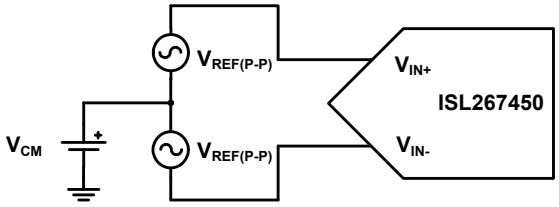
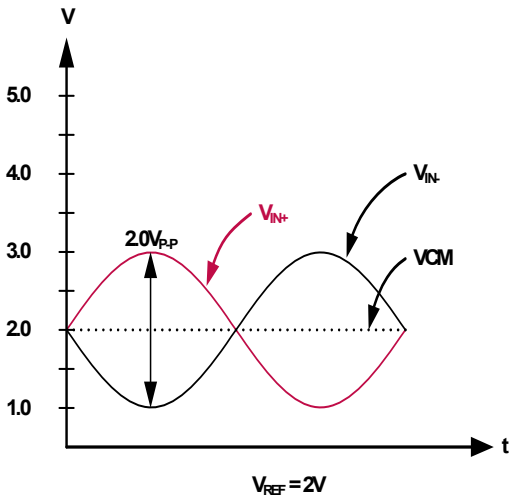


FIGURE 21. DIFFERENTIAL INPUT SIGNALING

Differential signaling offers several benefits over a single-ended input, such as:

- Doubling of the full-scale input range (and therefore the dynamic range)
- Improved even order harmonic distortion
- Better noise immunity due to common mode rejection



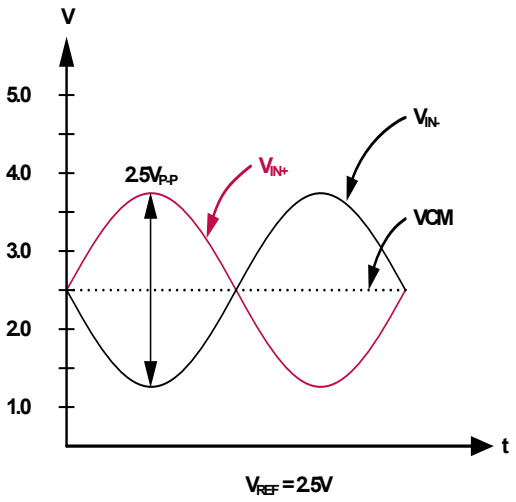


FIGURE 22. RELATIONSHIP BETWEEN V_{REF} AND FULL-SCALE RANGE

Figure 22 shows the relationship between the reference voltage and the full-scale input range for two different values of V_{REF}. Note that there is a trade-off between V_{REF} and the allowable common mode input voltage (VCM). The full-scale input range is proportional to V_{REF}; therefore the VCM range must be limited for larger values of V_{REF} in order to keep the absolute maximum and minimum voltages on the V_{IN+} and V_{IN-} pins within specification. Figures 23 and 24 illustrate this relationship for 5V and 3V operation, respectively. The dashed lines show the theoretical VCM range based solely on keeping the V_{IN+} and V_{IN-} pins within the supply rails. Additional restrictions are imposed due to the required headroom of the input circuitry, resulting in practical limits shown by the shaded area.

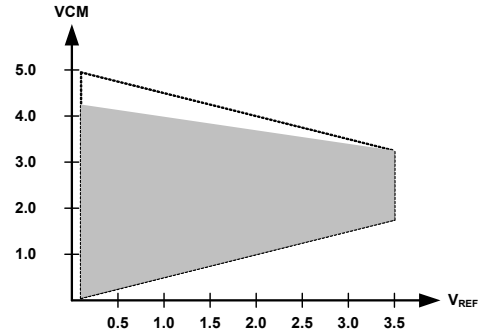


FIGURE 23. RELATIONSHIP BETWEEN V_{REF} AND VCM FOR V_{DD} = 5V

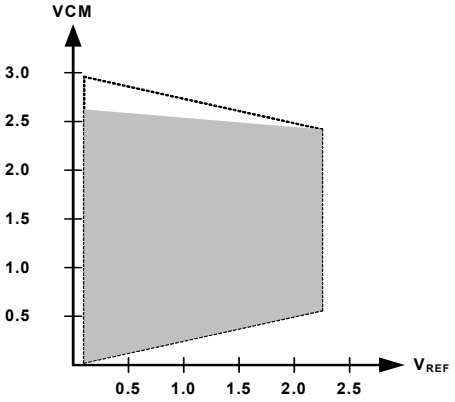


FIGURE 24. RELATIONSHIP BETWEEN VREF AND VCM FOR V_{DD} = 3V

Voltage Reference Input

The voltage magnitude applied to the V_{REF} pin defines the full scale span of the ADC as 2* V_{REF}. The device is specified with a voltage reference of 2.5V for 5V operation and with a voltage reference of 2.0V for 3V operation. But, V_{REF} input accepts voltages ranging from 0.1V to 3.5V for operation from 5 V V_{DD} and voltages ranging from 0.1V to 2.2V for operation from a 3V V_{DD}.

Figures 25 and 26 illustrate possible voltage reference options for the ISL267450. Figure 25 uses the ISL21090 precision voltage reference, which exhibits exceptionally low drift and low noise. The ISL21090 must use a power supply greater than 4.7V. The V_{REF} input pin on the ISL267450 uses very low current, so the decoupling capacitor can be small (0.1µF).

Figure 26 illustrates the ISL21010 voltage reference. The ISL21010 is available in various output voltages. It has higher noise and drift than the ISL26090, but consumes very low operating current, which makes it an excellent choice for battery-powered applications.

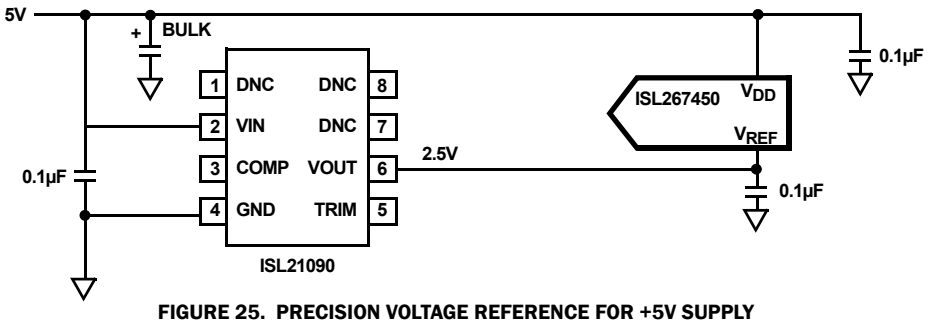


FIGURE 25. PRECISION VOLTAGE REFERENCE FOR +5V SUPPLY

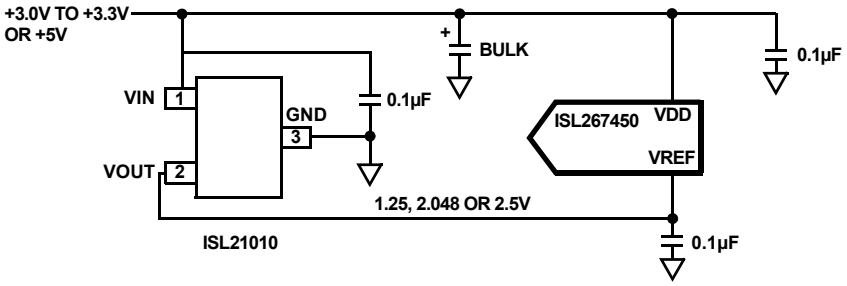


FIGURE 26. VOLTAGE REFERENCE FOR +3.0V TO +3.3V, OR FOR +5V SUPPLY

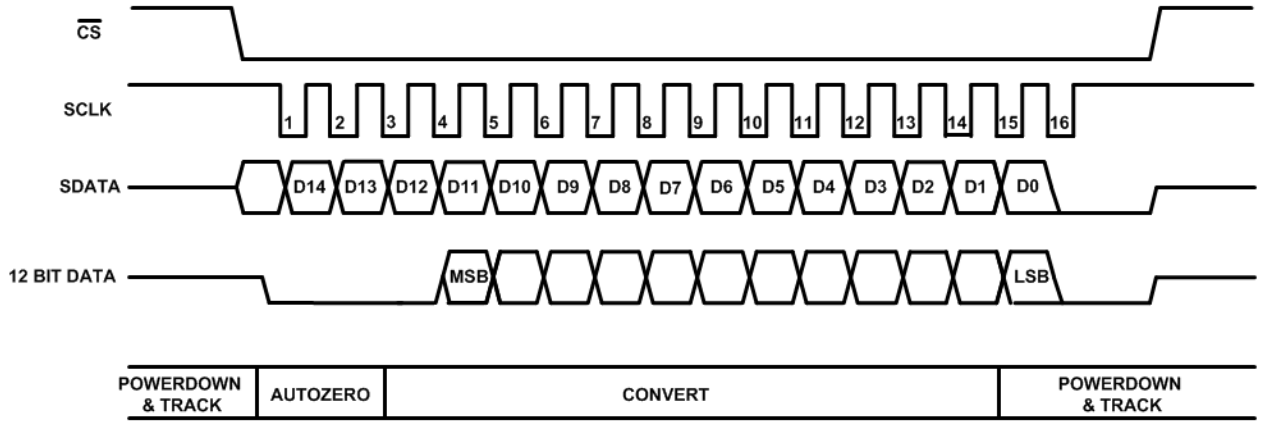


FIGURE 27. NORMAL MODE OPERATION

CONVERTER OPERATION

The ISL267450 is designed to minimize power consumption by only powering up the SAR comparator during conversion time. When the converter is in track mode (its sample capacitors are tracking the input signal), the SAR comparator is powered down. The state of the converter is dictated by the logic state of $\overline{CS}$. When $\overline{CS}$ is high, the SAR comparator is powered down while the sampling capacitor array is tracking the input. When $\overline{CS}$ transitions low, the capacitor array immediately captures the analog signal that is being tracked. After $\overline{CS}$ is taken low, the SCLK pin is toggled 16 times. For the first 3 clocks, the comparator is powered up and auto-zeroed, then the SAR decision process is begun. This process uses 12 SCLK cycles. Each SAR decision is presented to the SDATA output on the next clock cycle after the SAR decision is performed. The SAR process (12 bits) is completed on SCLK cycle 15. At this point in time, the SAR comparator is powered down and the capacitor array is placed back into Track mode. The last SAR comparator decision is output from SDATA on the 16th SCLK cycle. When the last data bit is output from SDATA, the output switches to a logic 0 until $\overline{CS}$ is taken high, at which time, the SDATA output enters a High-Z state.

Figure 27 illustrates the serial port system timing for the ISL267450.

POWER-ON RESET

When power is first applied, the ISL267450 performs a power-on reset that requires approximately 2.5ms to execute. After this is complete, a single dummy conversion must be executed (by taking $\overline{CS}$ low) in order to initialize the switched capacitor track and hold. The dummy conversion cycle will take 889ns with an 18MHz SCLK. Once the dummy cycle is complete, the ADC mode will be determined by the state of $\overline{CS}$. Regular conversions can be started immediately after this dummy cycle is completed and time has been allowed for proper acquisition.

ACQUISITION TIME

To achieve the maximum sample rate (1MSps) in the ISL267450 device, the maximum acquisition time is 200ns. For slower conversion rates, or for conversions performed using a slower SCLK value than 18MHz, the minimum acquisition time is 200ns. This minimum acquisition time also applies to the device when operated at 3V supply or if short cycling is utilized.

SHORT CYCLING

In cases where a lower resolution conversion is acceptable, $\overline{CS}$ can be pulled high before all 12 bits are clocked out. This is referred to as short cycling, and it can be used to further optimize power dissipation. In this mode, a lower resolution result will be output, but the ADC will enter static mode sooner and exhibit a lower average power consumption than if the complete conversion cycle were carried out. The minimum acquisition time (tACQ) requirement of 200ns must be met for the next conversion to be valid.

POWER vs THROUGHPUT RATE

The ISL267450 provides reduced power consumption at lower conversion rates by automatically switching into a low-power mode after completing a conversion. The average power consumption of the ADC decreases at lower throughput rates. Figure 28 shows the typical power consumption over a wide range of throughput rates.

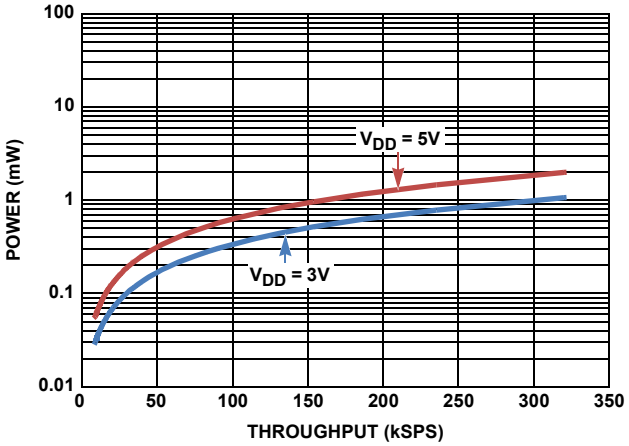


FIGURE 28. POWER CONSUMPTION vs THROUGHPUT RATE

Serial Interface

Conversion data is accessed with an SPI-compatible serial interface. The interface consists of the serial clock (SCLK), serial data output (SDATA), and chip select ($\overline{CS}$).

A falling edge on the $\overline{CS}$ signal initiates a conversion by placing the part into the acquisition (ACQ) phase. After t_{ACQ} has elapsed, the part enters the conversion (CONV) phase and begins outputting the conversion result starting with a null bit followed by the most significant bit (MSB) and ending with the least significant bit (LSB). The $\overline{CS}$ pin can be pulled high at this point to put the device into Standby mode and reduce the power consumption. If $\overline{CS}$ is held low after the LSB bit has been output, the conversion result will be repeated in reverse order until the MSB is transmitted, after which the serial output enters a high impedance state. The ISL267450 will remain in this state, dissipating typical dynamic power levels, until $\overline{CS}$ transitions high then low to initiate the next conversion.

Data Format

Output data is encoded in two's complement format as shown in Table 1. The voltage levels in the table are idealized and don't account for any gain/offset errors or noise.

TABLE 1. TWO'S COMPLEMENT DATA FORMATTING

INPUT	VOLTAGE	DIGITAL OUTPUT
–Full Scale	$-V_{REF}$	1000 0000 0000
–Full Scale + 1LSB	$-V_{REF}$ + 1LSB	1000 0000 0001
Midscale	0	0000 0000 0000
+Full Scale – 1LSB	$+V_{REF}$ – 1LSB	0111 1111 1110
+Full Scale	$+V_{REF}$	0111 1111 1111

Application Hints

Grounding and Layout

The printed circuit board that houses the ISL267450 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes since it gives the best shielding. Digital and analog ground planes should be joined in only one place, and the connection should be a star ground point established as close to the GND pin on the ISL267450 as possible. Avoid running digital lines under the device, as this will couple noise onto the die. The analog ground plane should be allowed to run under the ISL267450 to avoid noise coupling.

The power supply lines to the device should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feed-through through the board. A microstrip technique is by far the best but is not always possible with a double-sided board.

In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with µF tantalum capacitors in parallel with 0.1µF capacitors to GND. To achieve the best from these decoupling components, they must be placed as close as possible to the device.

Terminology

Signal-to-(Noise + Distortion) Ratio (SINAD)

This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding DC. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by Equation 1:

$$\text{Signal-to-(Noise + Distortion)} = (6.02\ N + 1.76)\text{dB} \quad \text{(EQ. 1)}$$

Thus, for a 12-bit converter this is 74dB, and for a 10-bit it is 62dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the ISL267450, it is defined as Equation 2:

$$\text{THD(dB)} = 20\log\sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}{V_1^2}} \quad \text{(EQ. 2)}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Peak Harmonic or Spurious Noise (SFDR)

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to fS/2 and excluding DC) to the rms value of the fundamental. It is also referred to as Spurious Free Dynamic Range (SFDR). Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m and n = 0, 1, 2 or 3. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa –2fb).

The ISL267450 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Aperture Delay

This is the amount of time from the leading edge of the sampling clock until the ADC actually takes the sample.

Aperture Jitter

This is the sample-to-sample variation in the effective point in time at which the actual sample is taken.

Full Power Bandwidth

The full power bandwidth of an ADC is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1dB or 3dB for a full-scale input.

Common-Mode Rejection Ratio (CMRR)

The common-mode rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 200mV$_{P-P}$ sine wave applied to the common-mode voltage of V_{IN+} and V_{IN-} of frequency fs as shown by Equation 3.:

$$CMRR(dB) = 10\log(Pfl/Pfs) \quad \text{(EQ. 3)}$$

Pf is the power at the frequency f in the ADC output; *Pfs* is the power at frequency fs in the ADC output.

Integral Nonlinearity (INL)

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero-Code Error

This is the deviation of the midscale code transition (111...111 to 000...000) from the ideal $V_{IN+} - V_{IN-}$ (i.e., 0 LSB).

Positive Gain Error

This is the deviation of the last code transition (011...110 to 011...111) from the ideal $V_{IN+} - V_{IN-}$ (i.e., $+V_{REF} - 1$ LSB), after the zero code error has been adjusted out.

Negative Gain Error

This is the deviation of the first code transition (100...000 to 100...001) from the ideal V_{IN+} – VIN– (i.e., $-V_{REF} + 1$ LSB), after the zero code error has been adjusted out.

Track and Hold Acquisition Time

The track and hold acquisition time is the minimum time required for the track and hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal.

Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f, to ADC V_{DD} supply of frequency f_S. The frequency of this input varies from 1kHz to 1MHz.

$$PSRR(dB) = 10\log(Pf/Pfs) \quad \text{(EQ. 4)}$$

Pf is the power at frequency f in the ADC output; *Pfs* is the power at frequency f_S in the ADC output.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
August 10, 2012	FN8341.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL267450

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

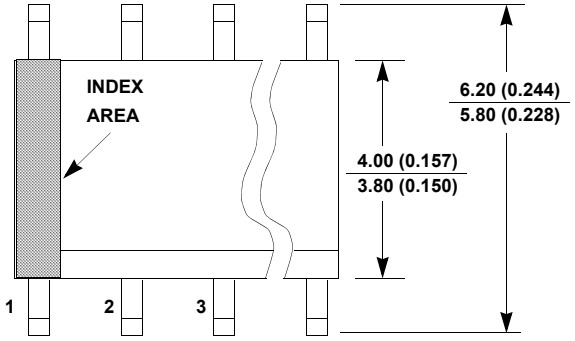
FITs are available from our website at: http://rel.intersil.com/reports/search.php

Package Outline Drawing

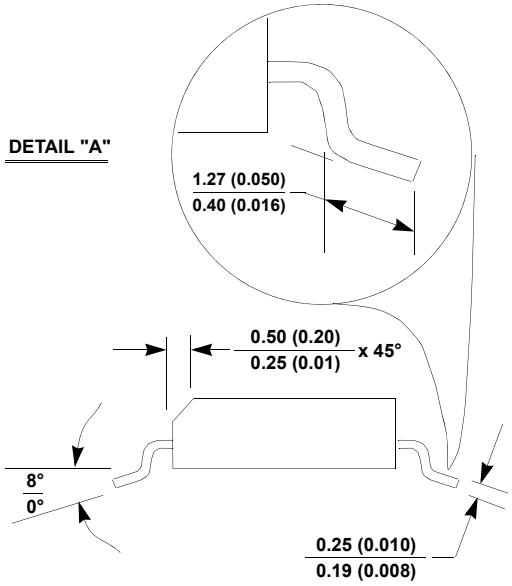
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

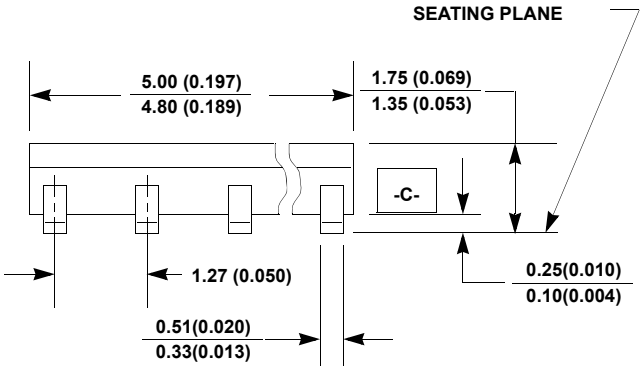
Rev 4, 1/12



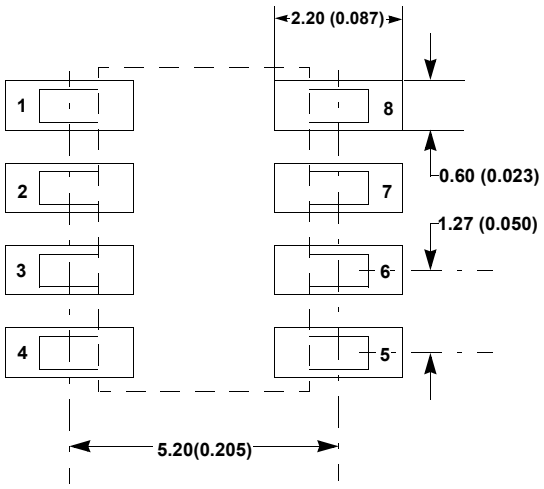
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

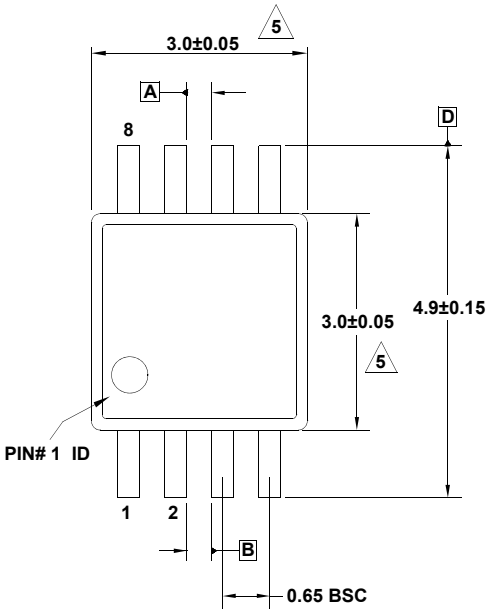
1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Package Outline Drawing

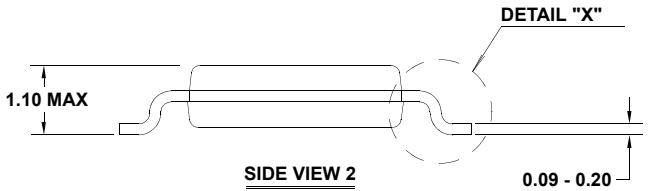
M8.118

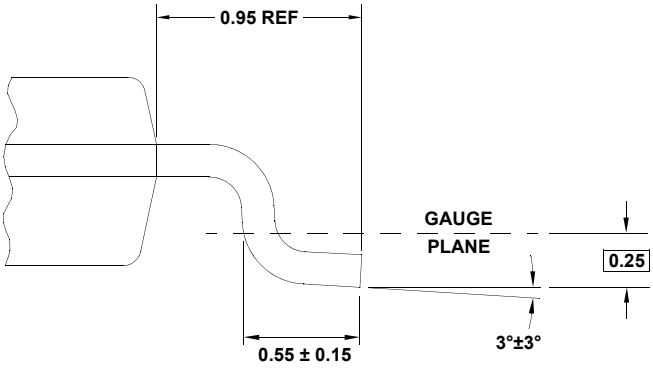
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 7/11

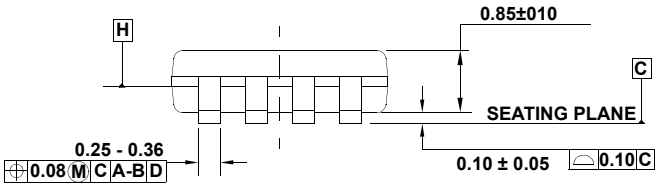


TOP VIEW

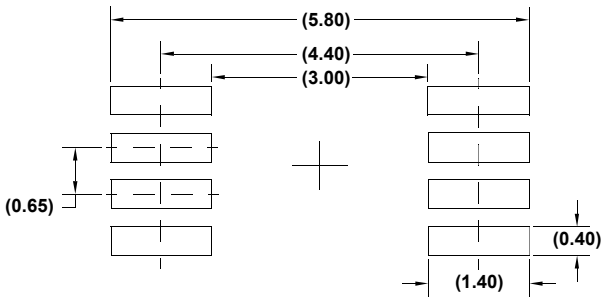




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.