ISL54058

Ultra Low ON-Resistance, Low-Voltage, Single Supply, Dual 4 to 1 Analog Multiplexer

FN6380
Rev 0.00
Sep 29, 2006

The Intersil ISL54058 device contains precision, bidirectional, analog switches configured as a dual 4-channel multiplexer/demultiplexer, designed to operate from a single +1.6V to +3.6V supply.

ON resistance is 0.41Ω with a +3V supply and 0.61Ω with a single +1.8V supply. Each switch can handle rail to rail analog signals. The off-leakage current is only 4nA max at +25°C or 40nA max at +85°C with a +3.3V supply.

All digital inputs are 1.8V logic-compatible when using a single +3V supply.

The ISL54058 is a dual 4 to 1 multiplexer device that is offered in a 16 Ld 2.6x1.8x0.5mm μTQFN package.

Table 1 summarizes the performance of this family.

TABLE 1. FEATURES AT A GLANCE

	ISL54058
Configuration	Dual 4:1 Mux
3V R_{ON}	0.41Ω
3V t_{RANS}	29ns
1.8V R_{ON}	0.61Ω
1.8V t_{RANS}	34ns
Packages	16 Ld 2.6x1.8x0.5mm μTQFN

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

Features

- Pb-Free Plus Anneal Available (RoHS Compliant)
- ON Resistance (R_{ON})
  - V+ = +3.0V 0.41Ω
  - V+ = +1.8V 0.61Ω
- R_{ON} Matching Between Channels. 0.09Ω
- R_{ON} Flatness Across Signal Range 0.07Ω
- Single Supply Operation. . . . . +1.6V to +3.6V
- Low Power Consumption (PD). . . . . <0.18μW
- Fast Switching Action (V_S = +3V)
  - t_{RANS} 29ns
- Break-Before-Make
- High Current Handling Capacity (300mA Continuous)
- Available in 16 Ld 2.6x1.8x0.5mm μTQFN
- 1.8V CMOS-Logic Compatible (+3V Supply)

Applications

- Battery Powered, Handheld, and Portable Equipment
  - Cellular/Mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Portable Test and Measurement
- Medical Equipment
- Audio and Video Switching

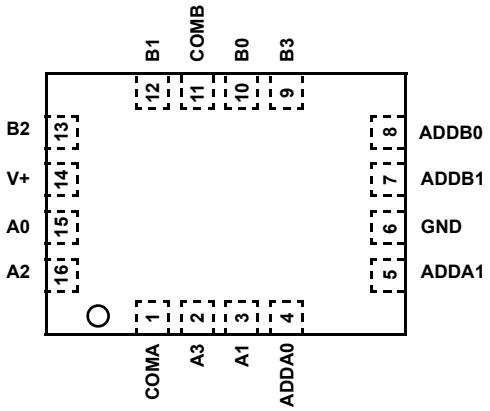
Ordering Information

PART NUMBER (NOTE)	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL54058IRUZ-T	GAC	-40 to +85	16 Ld Thin μQFN Tape and Reel (Pb-free)	L16.2.6x1.8A

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Pinouts (Note 1)

ISL54058
(16 LD μTQFN)
TOP VIEW)



NOTE:

1. 2.6mmx1.8mmx0.5mm

Truth Table

ISL54058				
ADDA1	**ADDA0**	**ADDB1**	**ADDB0**	**SWITCH ON**
0	0	X	X	A0
0	1	X	X	A1
1	0	X	X	A2
1	1	X	X	A3
X	X	0	0	B0
X	X	0	1	B1
X	X	1	0	B2
X	X	1	1	B3

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V, with a 3V supply.
X = Don’t Care.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (1.6V to 3.6V)
GND	Ground Connection
COMA	Analog Switch Channel A Output
COMB	Analog Switch Channel B Output
A0-A3	Analog Switch Channel A Input
B0-B3	Analog Switch Channel B Input
ADDAx	Address Input Pin
ADDBx	Address Input Pin

Absolute Maximum Ratings

V+ to GND . . . . . -0.3 to 4.7V
Input Voltages
Ax, Bx, ADDx (Note 2) . . . . . -0.3 to (V+) + 0.3V
Output Voltages
COMx (Note 2) . . . . . -0.3 to (V+) + 0.3V
Continuous Current NO or COM . . . . . ±300mA
Peak Current NO or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±500mA
ESD Rating
HBM . . . . . >4kV
MM . . . . . >300V
CDM . . . . . >1kV

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
µTQFN Package 93
Maximum Junction Temperature (Plastic Package). . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(Lead Tips Only)

Operating Conditions

Temperature Range
ISL54058IRUZ. . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. Signals on Ax, Bx, COMx, ADDx exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications: 3V Supply

Test Conditions: V_{SUPPLY} = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 4, 8), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{Ax} or V_{Bx} = 0V to V+ (See Figure 4)	25	-	0.43	0.75	Ω
		Full	-	-	0.8	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 2.7V, I_{COM} = 100mA, V_{Ax} or V_{Bx} = Voltage at max R_{ON} (Note 6)	25	-	0.09	0.2	Ω
		Full	-	-	0.2	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 2.7V, I_{COM} = 100mA, V_{Ax} or V_{Bx} = 0V t0 V+ (Note 7)	25	-	0.07	0.15	Ω
		Full	-	-	0.15	Ω
Ax or Bx OFF Leakage Current, $I_{Ax(OFF)}$ or $I_{Bx(OFF)}$	V+ = 3.3V, V_{COM} = 0.3V, 3V, V_{Ax} or V_{Bx} = 3V, 0.3V	25	-4	-	4	nA
		Full	-40	-	40	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 3.3V, V_{COM} = V_{Ax} or V_{Bx} = 0.3V, 3V	25	-8	-	8	nA
		Full	-60	-	60	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	1.4	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	0.5	V
Input Current, I_{INH}, I_{INL}, I_{ADDH}, I_{ADDL}	V+ = 3.3V, V_{INH} = V_{ADD} = 0V or V+	Full	-0.5	-	0.5	µA
DYNAMIC CHARACTERISTICS						
Address Transition Time, t_{TRANS}	V+ = 2.7V, V_{Ax} or V_{Bx} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure)	25	-	29	-	ns
		Full	-	40	-	ns
Break-Before-Make Time, t_{BBM}	V+ = 3.3V, V_{Ax} or V_{Bx} = 1.5V, R_L = 50Ω, C_L = 35pF (See Figure 2)	25	-	4	-	ns
		Full	-	1	-	ns
Ax or Bx OFF Capacitance, C_{OFF}	f = 1MHz, V_{Ax} or V_{Bx} = V_{COM} = 0V (See Figure 6)	25	-	44	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{Ax} or V_{Bx} = V_{COM} = 0V (See Figure 6)	25	-	201	-	pF
OFF Isolation	R_L = 50Ω, C_L = 35pF, f = 100kHz (See Figures 3 and 5)	25	-	65	-	dB
Crosstalk (Note 9)		25	-	-100	-	dB

Electrical Specifications: 3V Supply

Test Conditions: V_{SUPPLY} = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V (Note 4, 8), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.6		3.6	V
Positive Supply Current, I+	V+ = 3.3V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	25	-	-	0.05	µA
		Full	-	-	1.1	µA

NOTES:

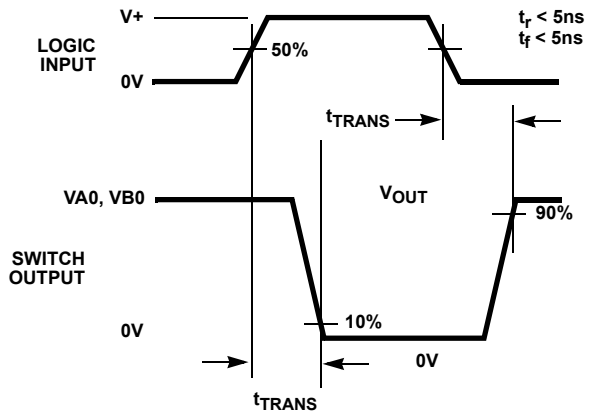
4. V_{IN} = Input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. R_{ON} matching between channels is calculated by subtracting the channel with the highest max R_{ON} value from the channel with lowest max R_{ON} value.
7. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
8. Parts are 100% tested at +25°C. Limits across the full temperature range are guaranteed by design and correlation.
9. Between any two switches.

Electrical Specifications: 1.8V Supply

Test Conditions: V+ = +1.8V, GND = 0V, V_{INH} = 1V, V_{INL} = 0.4V (Note 4, 8), Unless Otherwise Specified

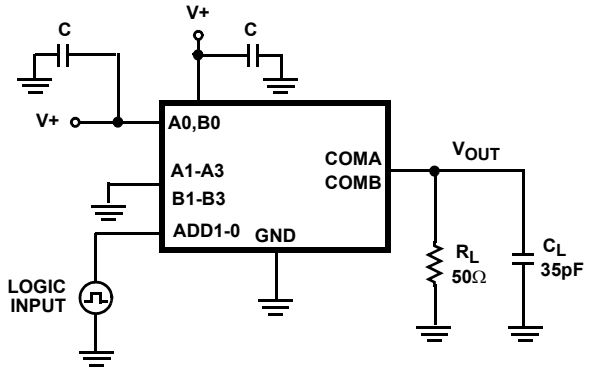
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 5)	TYP	MAX (NOTE **5**)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 1.8V, I_{COM} = 10.0mA, V_{Ax} or V_{Bx} = 1.0V (See Figure 4)	25	-	0.61	0.85	Ω
		Full	-	-	0.9	Ω
R_{ON} Matching Between Channels, ΔR_{ON})	V+ = 1.8V, I_{COM} = 10.0mA, V_{Ax} or V_{Bx} = 1.0V (Note 6)	25	-	0.11	-	Ω
		Full	-	0.12	-	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 1.8V, I_{COM} = 10.0mA, V_{Ax} or V_{Bx} = 0V, 0.9V, 1.6V (Note 7)	25	-	0.19	-	Ω
		Full	-	0.19	-	Ω
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	1	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	0.4	V
Input Current, I_{INH}, I_{INL}, I_{ADDH}, I_{ADDL}	V+ = 1.8V, V_{INH}, V_{ADD} = 0V or V+	Full	-0.5	-	0.5	µA
DYNAMIC CHARACTERISTICS						
Address Transition Time, t_{TRANS}	V+ = 1.8V, V_{Ax} or V_{Bx} = 1.0V, R_L = 50Ω, C_L = 35pF(See Figure 1)	25	-	34	-	ns
		Full	-	44	-	ns
Break-Before-Make Time, t_{BBM}	V+ = 1.8V, V_{Ax} or V_{Bx} = 1.0V, R_L = 50Ω, C_L = 35pF (See Figure 2)	25	-	9	-	ns

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. ADDRESS t_{TRANS} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. ADDRESS t_{TRANS} TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

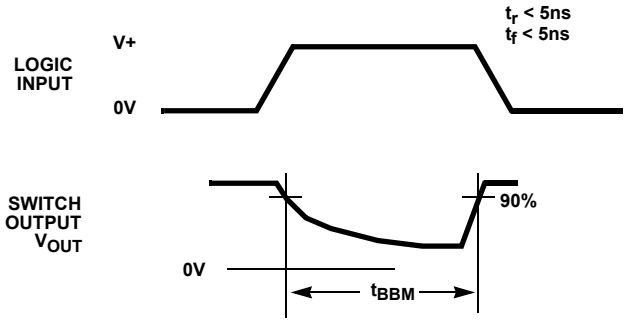
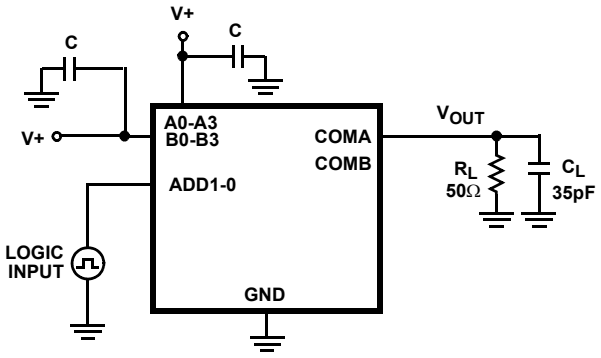


FIGURE 2A. t_{BBM} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

FIGURE 2B. t_{BBM} TEST CIRCUIT

FIGURE 2. BREAK-BEFORE-MAKE TIME

Test Circuits and Waveforms (Continued)

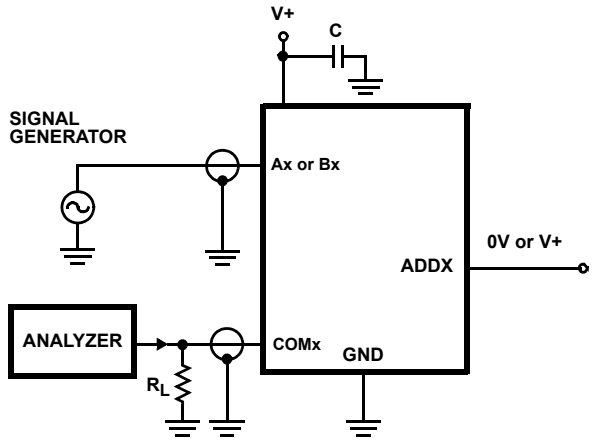


FIGURE 3. OFF ISOLATION TEST CIRCUIT

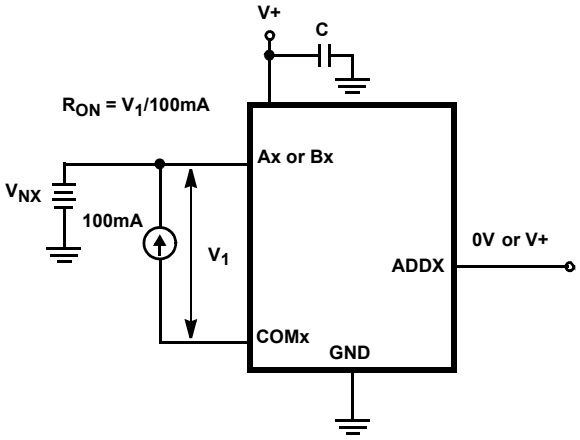


FIGURE 4. R_{ON} TEST CIRCUIT

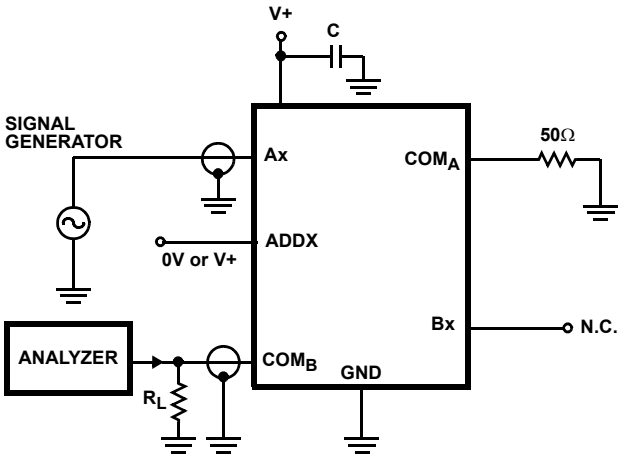


FIGURE 5. CROSSTALK TEST CIRCUIT

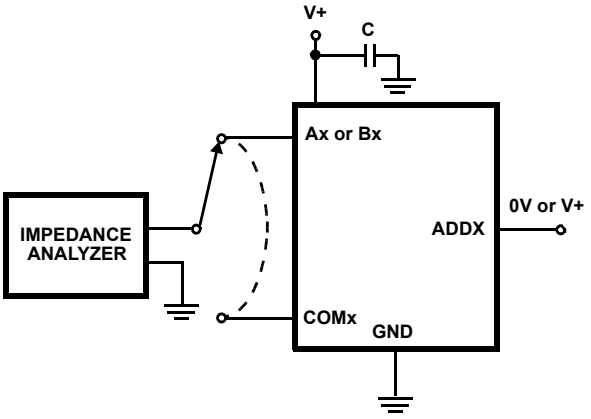


FIGURE 6. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL54058 analog switches offer precise switching capability from a single 1.6V to 3.6V supply with low on-resistance (0.41Ω) and high speed operation (t_{RANS} = 29ns). The device is especially well suited to portable battery powered equipment thanks to the low operating supply voltage (1.6V), low power consumption (0.17µW), low leakage currents (60nA max) , and the tiny µTQFN package. The ultra low on-resistance and R_{ON} flatness provide very low insertion loss and distortion to applications that require signal reproduction.

Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 7). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND.

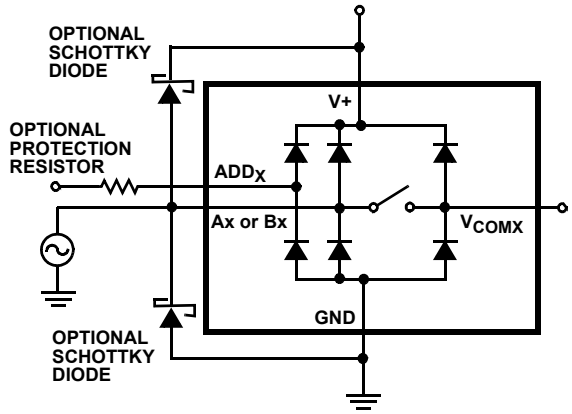


FIGURE 7. OVERVOLTAGE PROTECTION

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pin and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provided additional protection to limit the current in the event that the voltage at a signal pin or logic pin goes below ground or above the V+ rail.

Logic inputs can be protected by adding a 1kΩ resistor in series with the logic input (see Figure 7). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch. Connecting schottky diodes to the signal pins as shown in Figure 7 will shunt the fault current to the supply or to ground thereby protecting the switch. These schottky diodes must be sized to handle the expected fault current.

Power-Supply Considerations

The ISL54058 construction is typical of most CMOS analog switches, in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4V maximum supply voltage, the ISL54058 4.7V maximum supply voltage provides plenty of room for the 10% tolerance of 3.6V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.6V but the part will operate with a supply below 1.5V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance* curves for details.

V+ and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switched V+ and V- signals to drive the analog switch gate terminals.

Logic-Level Thresholds

This device is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2.7V to 3.6V. At 2.7V the V_{IL} level is about 0.54V. This is still above the 1.8V CMOS guaranteed low output maximum level of 0.5V but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 10MHz with a -3dB bandwidth of 70MHz (see Figure 12). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch's input to its output. Off Isolation is the resistance to this feed through, while Crosstalk indicates the amount of feed through from one switch to another.
Figure 11 details the high Off Isolation and Crosstalk rejection provided by this family. At 100kHz, Off Isolation is about 65dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

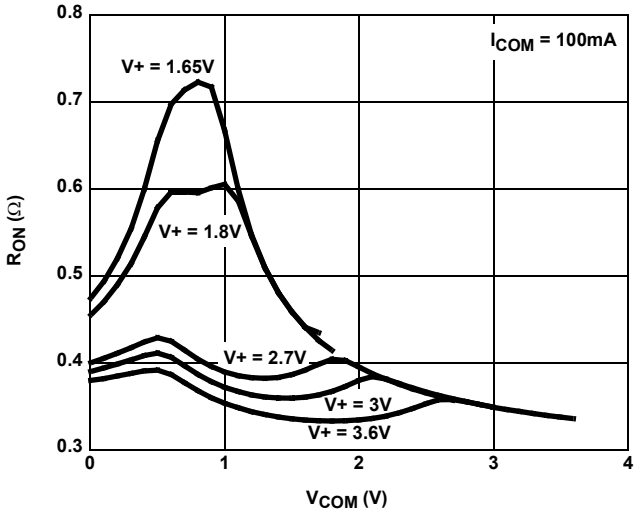


FIGURE 8. ON RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

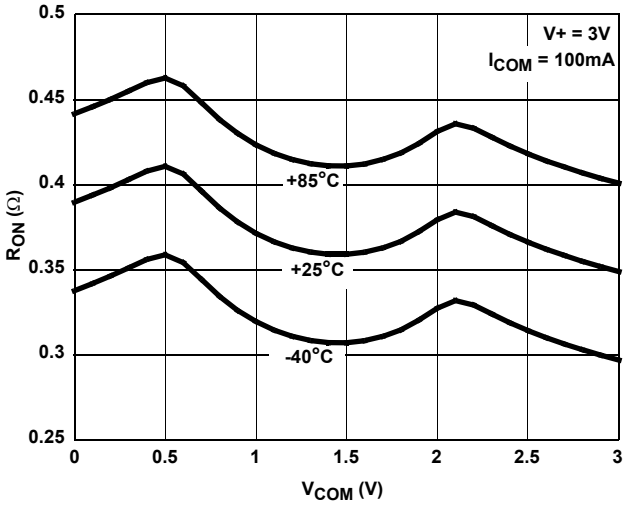


FIGURE 9. ON RESISTANCE vs SWITCH VOLTAGE

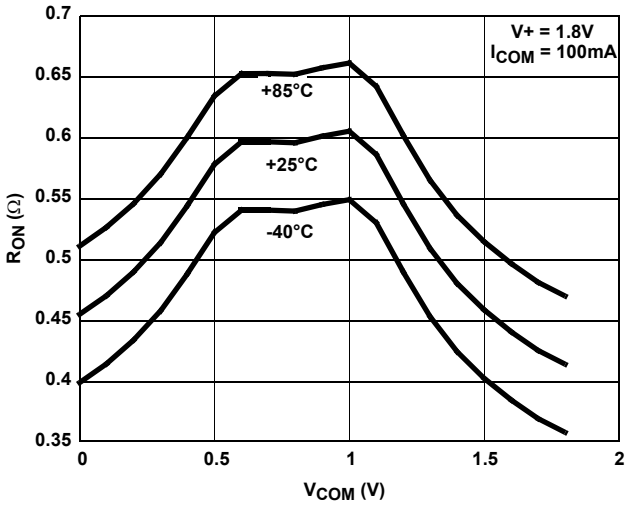


FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

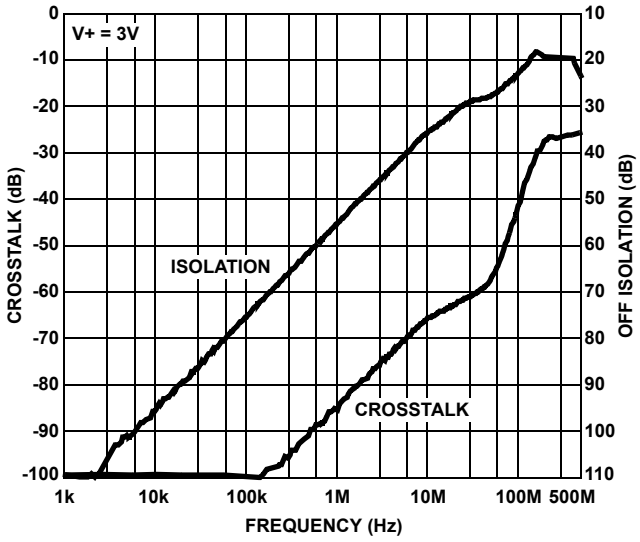


FIGURE 11. CROSSTALK AND OFF ISOLATION

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

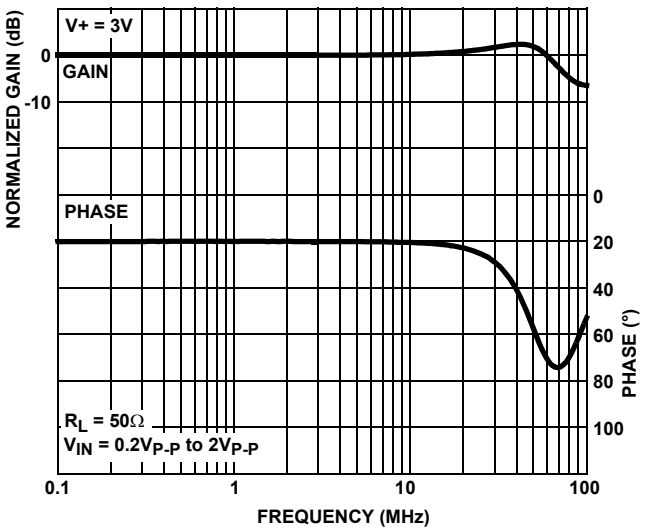


FIGURE 12. FREQUENCY RESPONSE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

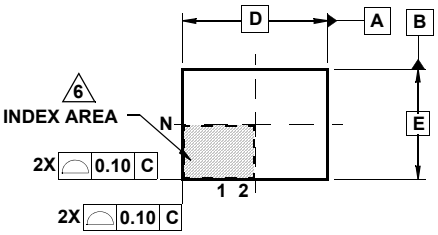
TRANSISTOR COUNT:

228

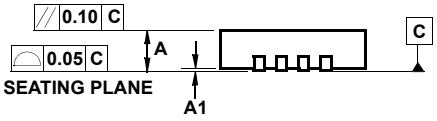
PROCESS:

Submicron CMOS

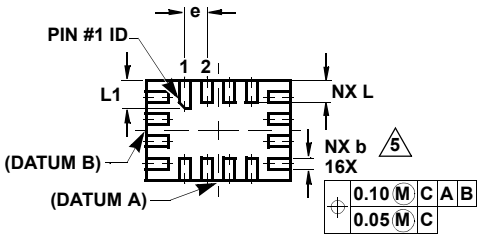
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



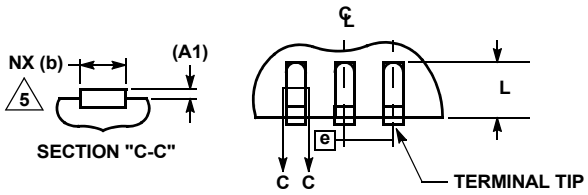
TOP VIEW

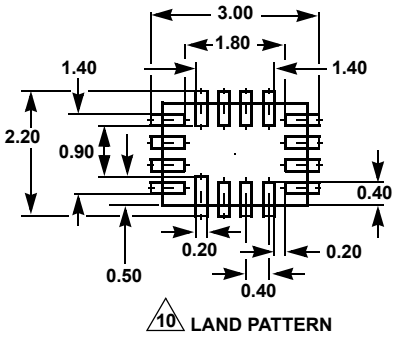


SIDE VIEW



BOTTOM VIEW





L16.2.6x1.8A

16 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.55	2.60	2.65	-
E	1.75	1.80	1.85	-
e		0.40 BSC		-
L	0.35	0.40	0.45	-
L1	0.45	0.50	0.55	-
N		16		2
Nd		4		3
Ne		4		3
θ	0	-	12	4

Rev. 4 8/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. JEDEC Reference MO-255.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.