ISL6131, ISL6132

Multiple Voltage Supervisory ICs

FN9119
Rev 6.00
February 11, 2014

The ISL6131 and ISL6132 are a family of high-accuracy, multi-voltage supervisory ICs designed to monitor voltages greater than 0.7V in applications ranging from microprocessors to industrial power systems. The ISL6131 is an undervoltage four-supply supervisor, and the ISL6132 is a two-voltage supervisor monitoring for undervoltage (UV) and overvoltage (OV) conditions.

Both ICs feature four external resistor programmable voltage monitoring (VMON) inputs, each with a related STATUS output that individually reports the related monitor input condition. In addition, there is a Power-Good (PGOOD) signal that asserts high when the STATUS outputs are in their correct state. A stability delay of approximately 160ms ensures that the monitored supply is stable before STATUS and PGOOD are released to go high. The PGOOD and STATUS outputs are open-drain to allow OR'ing of the signals and interfacing to a wide range of logic levels.

STATUS and PGOOD outputs are guaranteed to be valid with IC bias lower than 1V, eliminating concern about STATUS and PGOOD outputs during IC bias up and down. VMON inputs are designed to ignore momentary transients on the monitored supplies.

Features

- Operates from 1.5V to 5.5V Supply Voltage
- Four Adjustable Voltage Monitoring Thresholds
- 150ms STATUS/PGOOD Stability Time Delay
- Four Individual Open Drain STATUS Outputs
- Guaranteed STATUS/PGOOD Valid to V_{DD} <1V
- V_{DD} and VMON Glitch Immunity
- V_{DD} Lock-Out
- 4mm X 4mm QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free (RoHS Compliant)

Applications

- Multivoltage DSPs and Processors
- µP Voltage Monitoring
- Embedded Control Systems
- Graphics Cards
- Intelligent Instruments
- Medical Equipment
- Network Routers
- Portable Battery-Powered Equipment
- Set-Top Boxes
- Telecommunications Systems

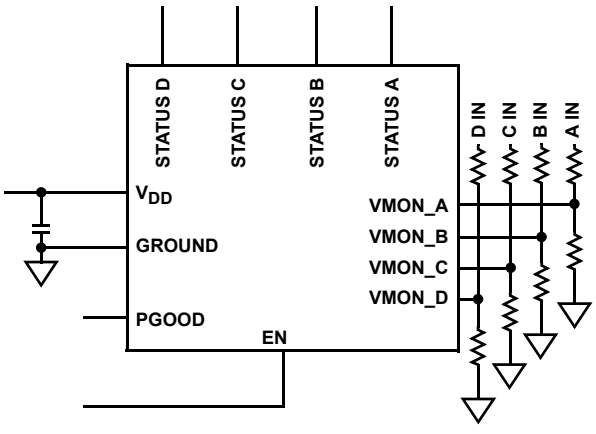


FIGURE 1. ISL6131 TYPICAL APPLICATION USAGE

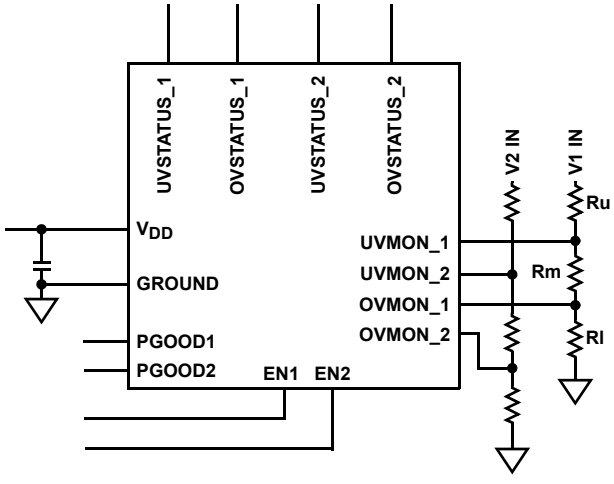


FIGURE 2. ISL6132 TYPICAL APPLICATION USAGE

Ordering Information

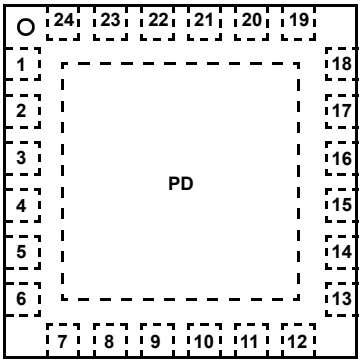
PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6131IRZA (Note 1)	61 31IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6132IRZA (Note 1)	61 32IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4
ISL6131EVAL1Z	Evaluation Board			
ISL6132EVAL1Z	Evaluation Board			

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6131, ISL6132. For more information on MSL, please see Tech Brief TB363.

Pin Configuration

ISL6131, ISL6132
(24 LD QFN)
TOP VIEW



Pin Descriptions

PIN		PIN NAME	FUNCTION DESCRIPTION
6131	6132		
23	23	V_{DD}	Bias IC from nominal 1.5V to 5V
10	10	GND	IC ground
20	NA	VMON_A	On the ISL6131, these inputs provide a programmable UV threshold referenced to an internal 0.633V. The related STATUS output asserts when the related input > internal reference voltage. On the ISL6132, these inputs provide a programmable UV and OV threshold referenced to an internal 0.633V reference. In the 'AB' pair, VMON_A is the UV input, and VMON_B is the OV input. In the 'CD' pair, VMON_C is the UV input, and VMON_D is the OV input. These inputs have a 30µs glitch filter to prevent PGOOD reset caused by a transient.
12	NA	VMON_B	
17	NA	VMON_C	
14	NA	VMON_D	
NA	12	OVMON_1	
NA	20	UVMON_1	
NA	17	UVMON_2	
NA	14	OVMON_2	
24	24	PGOOD	On the ISL6131, PGOOD is the Boolean AND function of all four STATUS outputs. On the ISL6132, PGOOD is for the AB pair and signals high when the monitored voltage is within the specified window and the A and B STATUS output states are correct. This is an open-drain output and is to be pulled high to the appropriate level with an external resistor to a V_{DD} maximum level.
NA	9	PGOOD2	PGOOD2 is for the CD pair and signals high when the monitored voltage is within the specified window and when the C and D STATUS output states are correct. This is an open-drain output and is to be pulled high to the appropriate level with an external resistor to a V_{DD} maximum level.

Pin Descriptions (Continued)

PIN		PIN NAME	FUNCTION DESCRIPTION
6131	6132		
2	NA	STATUS_A	On the ISL6131, each STATUS provides a high signal through pull-up resistors about 160ms after its related VMON has continuously been > Vuv_vth. This delay is for stabilization of monitored voltages. STATUS de-asserts and pulls low upon VMON not being satisfied for about 30µs. On the ISL6132, the STATUS outputs indicate compliance with a high output state for each pair of monitors.
5	NA	STATUS_B	
6	NA	STATUS_C	
7	NA	STATUS_D	
NA	5	OVSTATUS_1	
NA	2	UVSTATUS_1	
NA	6	UVSTATUS_2	
NA	7	OVSTATUS_2	
1	1	EN1	On the ISL6131, this pin provides four voltage UV functions for enabling/disabling input. Internally pulled up to V_{DD}. Controls monitor 1 (AB pair) on ISL6132.
NA	11	EN2	On the ISL6132, this pin controls monitor 2 (CD pair) voltage and voltage monitoring function enabling input; pulled up to V_{DD}.
-	-	PD	Thermal Pad. Should be electrically connected to GND.
NC	3, 4, 8, 13, 15, 16, 18, 19, 21, 22		No Connect

Absolute Maximum Ratings

V_{DD} . . . . . +6.0V
VMON, ENABLE, STATUS, PGOOD . . . . . -0.3V to V_{DD}+0.3V
ESD Classification. . . . . 2kV (HBM)

Operating Conditions

V_{DD} Supply Voltage Range . . . . . +1.5V to +5.5V
Temperature Range (T_A) . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4x4 QFN Package.	48	9

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

Nominal V_{DD} = 1.5V to +5V, T_A = T_J = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
VMON/ENABLE INPUTS						
VMON Falling Threshold	$V_{VMONvth}$	T_J = +25°C	619	633	647	mV
VMON Threshold Temp. Coeff.	$TC_{VMONvth}$	T_J from -40°C to +85°C	-	40	-	µV/°C
VMON Hysteresis	$V_{VMONhys}$		-	10	-	mV
VMON Glitch Filter	Tfil		-	30	-	µs
VMON Minimum Input Impedance	Zin_min	T_J = +40°C, VMON within 63mV of $V_{VMONvth}$		8		MΩ
ENABLE L2H, Delay to STATUS & PGOOD		VMON valid, EN high to STATUS and PG high	-	160	-	ms
EN H2L, Delay to PGOOD		EN low to PGOOD low	-	-	**0.1**	µs
EN H2L, Delay to STATUS		EN low to STATUS low	-	13	-	µs
ENABLE Pull-up Voltage		EN open	-	V_{DD}	-	V
ENABLE Threshold Voltage	V_{ENVTH}		-	V_{DD}/2	-	V
STATUS/PGOOD OUTPUTS						
STATUS Pull-Down Current	$I_{\overline{RST}pd}$	RST = 0.1V	-	88	-	mA
STATUS/PGOOD Delay after VMON Valid	T_{delST}	VMON > V_{UVvth} to STATUS = 0.2V	-	160	-	ms
STATUS/PGOOD Output Low	Vol	Measured at V_{DD} = 1.0V	-	0.04	**0.1**	V
BIAS						
IC Supply Current	$I_{VDD\_5.5V}$	V_{DD} = 5V	-	170	-	µA
IC Supply Current	$I_{VDD\_3.3V}$	V_{DD} = 3.3V	-	145	-	µA
IC Supply Current	$I_{VDD\_1.5V}$	V_{DD} = 1.5V	-	100	-	µA
V_{DD} Power On	V_{DD_POR}	V_{DD} high to low	-	0.89	**1**	V
V_{DD} Power On Lock Out	V_{DD_LO}	V_{DD} low to high	-	0.91	-	V

NOTE:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Description and Operation

The ISL6131 is a four-voltage, high-accuracy, supervisory IC designed to monitor multiple voltages greater than 0.7V relative to Pin 10 of the IC.

Upon V_{DD} bias power-up, the STATUS and PGOOD outputs are held correctly low once V_{DD} is as low as 1V. Once biased to 1.5V, the IC continuously monitors from one to four voltages independently through external resistor dividers, comparing each voltage monitoring (VMON) pin voltage to an internal 0.633V ($V_{VMONvth}$) reference.

With the EN input driven high or open, as each VMON input rises above $V_{VMONvth}$, a timer is set to ensure ~160ms of continuous compliance. Then the related STATUS output is released to be pulled high. The STATUS outputs are open-drain to allow OR'ing of these signals and interfacing to a logic high level up to V_{DD}. The STATUS outputs are designed to reject short transients (~30µs) on the VMON inputs. Once all STATUS outputs are high, a Power-Good (PGOOD) output signal is generated high to indicate that all monitored voltages are greater than minimum compliance level.

Once any VMON input falls below $V_{VMONvth}$ for longer than the glitch filter time, both the PGOOD and the related STATUS output are pulled low. The other STATUS outputs remain high as long as their corresponding VMON voltage remains valid and the PGOOD validation process is reset.

Figure 1 shows the ISL6131 typical application schematic, and Figure 3 is an operational timing diagram. See Figures 10 to 17 for ISL6131 function and performance. Figures 10 and 11 show the V_{DD} rising along with STATUS and PGOOD response. Figures 12 and 13 illustrate VMON falling below $V_{VMONvth}$, and Figure 14 shows VMON rising above $V_{VMONvth}$ with STATUS and PGOOD response. Figure 15 shows V_{DD} failing, with STATUS and PGOOD response. Figures 16 and 17 show ENABLE to STATUS and PGOOD timing.

If less than four voltages are being monitored, connect the unused VMON pins to V_{DD} for proper operation. All unused STATUS outputs can be left open.

The ISL6132 is a dual voltage monitor for undervoltage and overvoltage compliance. Figure 2 shows the typical ISL6132 implementation schematic, and Figure 4 is the operational timing diagram.

There are two pairs of monitors, each with an undervoltage (UVMON) input and an overvoltage (OVMON) input, along with associated STATUS and PGOOD outputs.

Upon V_{DD} bias power-up, the STATUS and PGOOD outputs are held correctly low, once V_{DD} is as low as 1V. Once biased to 1.5V, the IC continuously monitors the voltage through external resistor dividers, comparing each VMON pin voltage to an internal 0.633V reference. At proper bias, OVSTATUS is pulled high, and UVSTATUS and PGOOD are pulled low. Once the UVMON input > VMON Vth continuously for ~160ms, its associated STATUS output releases high, indicating that the minimum voltage condition has been met. As both UVMON and OVMON inputs are satisfied, the PGOOD output is released to go high, indicating that the monitored voltage is within the specified window. Figure 18 shows this performance for a 4V to 5V window.

When VMON does not satisfy its voltage high or low criteria for more than the glitch filter time, the associated STATUS and PGOOD are pulled low. Figures 19 and 20 show this performance for a 4V to 5V compliant window.

Figures 21 through 23 show the VMON glitch filter timing to STATUS and PGOOD notification and transient immunity.

The ENABLE input, when pulled low, allows the monitoring and reporting functions to be disabled. Figure 24 shows ENABLE high to PGOOD timing for compliant voltage.

When choosing resistors for the divider, remember to keep the current through the string bounded by power loss tolerance at the top end and noise immunity at the bottom end. For most applications, total divider resistance in the 10kΩ -100kΩ range is advisable, with 1% tolerance resistors being used to reduce monitoring error.

Figures 1 and 2 show that choosing the two resistor values is straightforward for the ISL6131, because the ratio of resistance should equal the ratio of the desired trip voltage to the internal reference, 0.633V.

For the ISL6132, two dividers of two resistors each can be employed to monitor the OV and UV levels for each voltage. Otherwise, use a single three-resistor string for each voltage. In the three-resistor divider string, the ratio of the desired overvoltage trip point to the internal reference is equal to the ratio of the two upper resistors to the lowest (GND connected) resistor. The desired undervoltage trip point ratio to the internal reference voltage is equal to the ratio of the uppermost (voltage connected) resistor to the two lower resistors, as shown in the following example:

1. Establish lower and upper trip level: 3.3V ±20% or 2.64V (UV) and 3.96V (OV)
2. Establish total resistor string value: 10kΩ, Ir = divider current
3. (Rm + Rl) * Ir = 0.623V @ UV and Rl * Ir = 0.633V @ OV
4. Rm + Rl = 0.623V/Ir @ UV => Rm + Rl = 0.623V/(2.64V/10kΩ) = 2.359kΩ
5. Rl = 0.633V/Ir @ OV => Rl = 0.633V/(3.96V/10kΩ) = 1.598kΩ
6. Rm = 2.359kΩ - 1.598kΩ = 0.761kΩ
7. Ru = 10kΩ - 2.397kΩ = 7.641kΩ

Choose standard value resistors that most closely approximate these ideal values. Choosing a different total divider resistance value may yield a more ideal ratio with available resistors values.

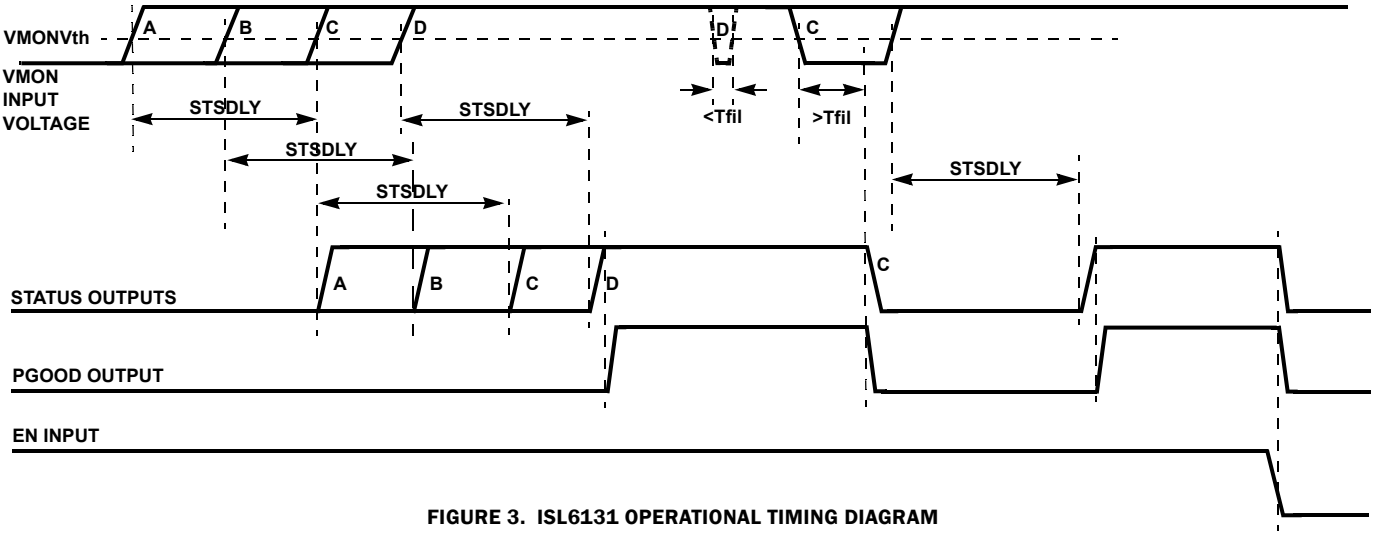


FIGURE 3. ISL6131 OPERATIONAL TIMING DIAGRAM

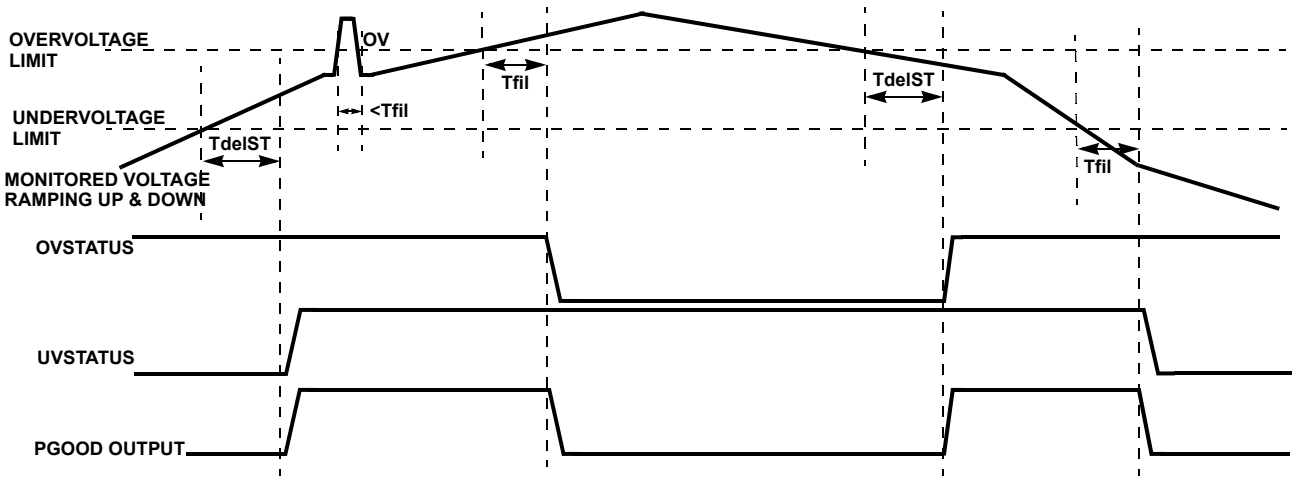


FIGURE 4. ISL6132 OPERATIONAL DIAGRAM

Typical Performance Curves

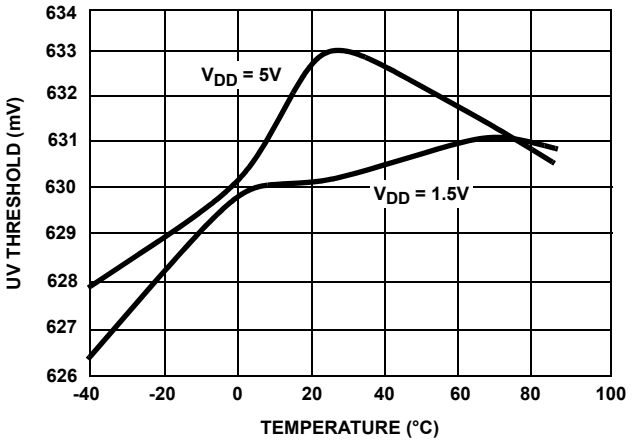


FIGURE 5. UV THRESHOLD

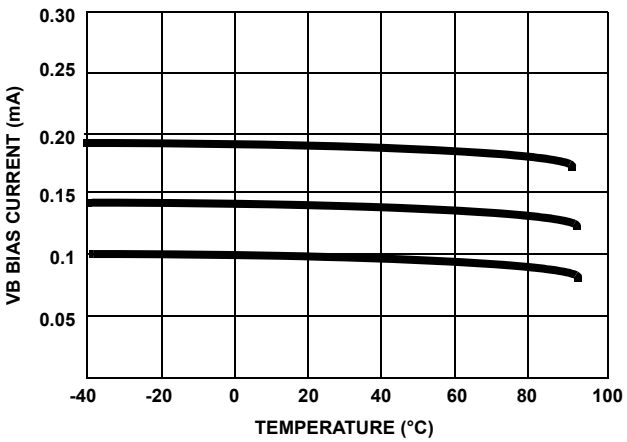


FIGURE 6. V_{DD} CURRENT

Applications Usage

Using the ISL6131EVAL1Z and ISL6132EVAL1Z Platforms

The ISL6131EVAL1Z platform is set up to monitor and report an undervoltage condition on each of 12V, 5V, 3.3V and 1.2V supplies to a -20% tolerance.

Each monitored supply has an individual STATUS output and an AND'ed PGOOD output signal for all four supplies. An OFF LED is the PGOOD indicator for all four supplies. The ENABLE input enables or disables the voltage monitoring function. See Figures 10 to 17 for performance and function examples.

The ISL6132EVAL1Z platform is set up to monitor and report either an undervoltage or an overvoltage condition on 5V and 12V supplies to a ±10% tolerance. There is an OV and a UV STATUS output for each of the two supplies and individual AND'ed PGOOD outputs when each voltage is within the programmed voltage range. An OFF LED indicates compliance to the voltage range upper and lower limits.

The ENABLE inputs enable or disable the voltage monitoring functions for each monitor supply.

See Figures 18 to 24 for performance and function examples. Figures 25 and 26 illustrate the ISL6131EVAL1Z and ISL6132EVAL1Z platforms respectively in image and schematic.

Using the ISL6131, ISL6132 for Negative Voltage Monitoring Applications

The ISL6131, ISL6132 can be used for -V monitoring because it monitors any voltage that is more positive relative to its GND pin. With correct bias differential, these parts can monitor any voltage, regardless of polarity or amplitude.

Using the ISL6131 for "Lossless" Sequencing Applications

The ISL6131 can be used in a "lossless" sequencing application in which a monitored output voltage determines the start of the next sequenced turn-on. As shown in Figure 7, VMON_A input looks at the common V_{IN} of several DC-DC converters and enables DC-DC_A with STATUS _A, once both V_{IN} and ENABLE are satisfied. VMON_B monitors the output of DC-DC_A, and when the acceptable output voltage is reached, DC-DC_B is enabled with STATUS_B output. This sequencing pattern continues until all DC-DC outputs are on, at which time PGOOD signal is released. A delay of 160ms from VMON > $V_{VMONVth}$ to STATUS high ensures stability at each step prior to subsequent turn-on. Additional ISL6131s can be employed in parallel to sequence any number of DC-DC convertors in this fashion.

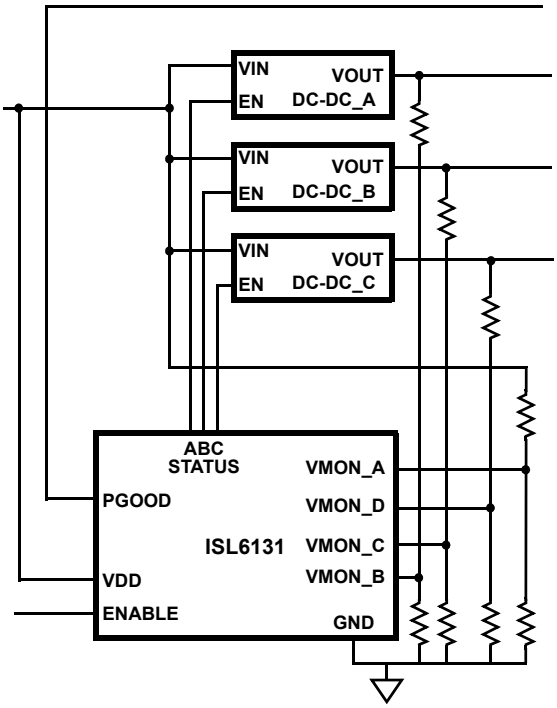


FIGURE 7. ISL6131 "LOSSLESS" SEQUENCING CONFIGURATION

Using the ISL6131 for System Voltage and Over-Temperature Monitoring

As a multi-voltage monitoring IC, the ISL6131 can monitor over-temperature as well as voltage for more complete coverage of system stability. Using a Negative Temperature Coefficient (NTC) passive device in place of one of the resistors in a VMON divider provides over-temperature monitoring either locally or remotely.

Evaluations of this application configuration have involved the QT0805T-202J, QT0805Y-502J and QT0805Y-103J NTCs from Quality Thermistor.

ISL6131 over-temperature monitoring is not as accurate as specific temperature monitor ICs, but this implementation provides a cost-efficient solution with 5% tolerances achievable.

See Figures 8 and 9 for over-temperature sensing configuration and operation results. In this example, the desired maximum temperature is 100°C. The QT0805Y-103J NTC was placed at the end of 3 feet of twisted pair wire to emulate a remote sensing application. According to the Quality Thermistor data sheet, this NTC device has a +25°C value of 10K and a +100°C value of 0.923K. An accompanying standard value resistor of 3.83K was chosen for the divider so that at 100°C, VMON ~0.633V with the bias voltage at 3.3V.

The resulting falling VMON trip point with the configuration shown is ~0.634V, with ~0.642V for rising, which equates to ~95°C for under-temperature and ~97°C for over-temperature, respectively. Choosing the standard resistor value above and below R1 allows for small adjustments in the temperature trip point.

The low ISL6131 VMON temperature coefficient makes it a viable and low-cost addition to complete system monitoring.

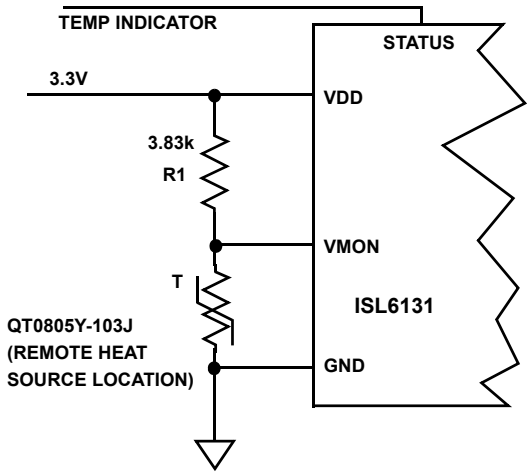


FIGURE 8. ISL6131 OVER-TEMP SENSING CONFIGURATION

TEMP (°C)	VMON (V)	TEMP STATUS
25	2.36	H = Under Temp
50	1.61	H = Under Temp
75	1.01	H = Under Temp
95	0.67	H = Under Temp
100	0.61	L = Over Temp
105	0.54	L = Over Temp

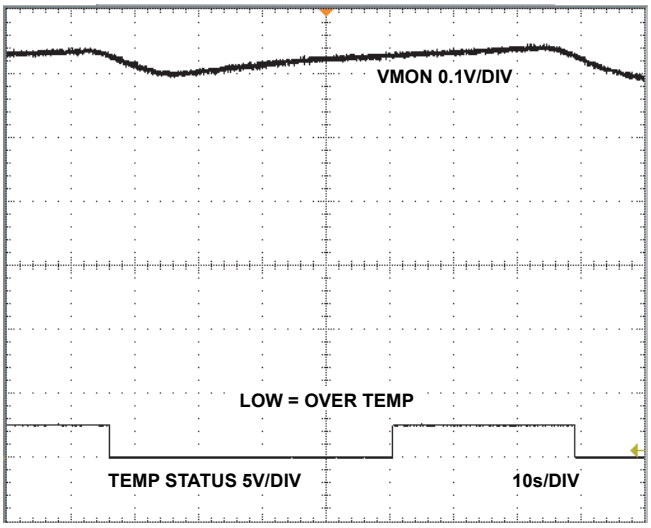


FIGURE 9. ISL6132 OVER-TEMP SENSING RESULT

Functional and Performance Waveforms

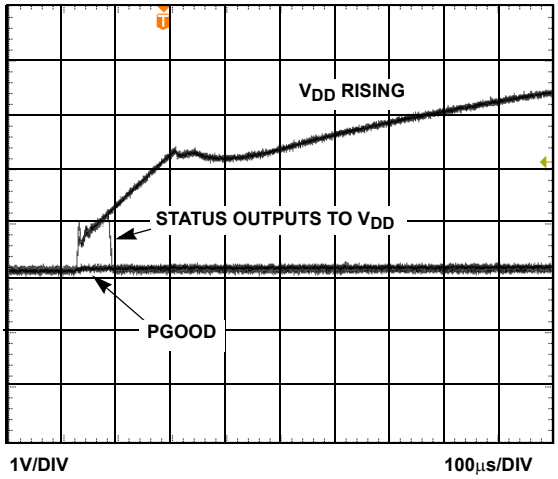


FIGURE 10. ISL6131 V_{DD} RISING

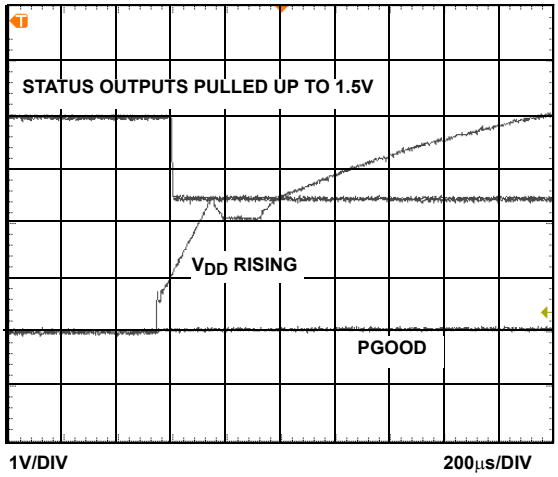


FIGURE 11. ISL6131 V_{DD} RISING WITH PULL-UP

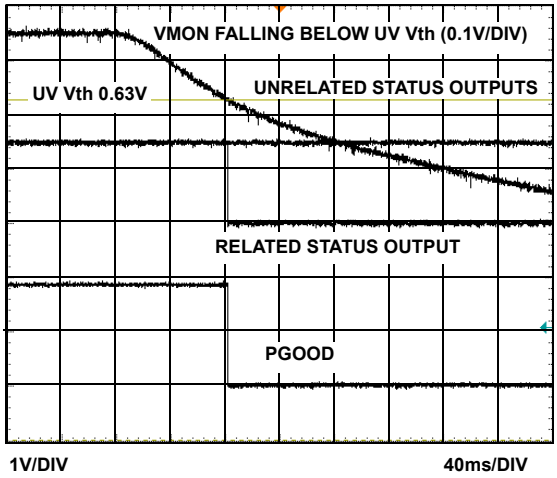


FIGURE 12. ISL6131 VMON FALLING TO PGOOD

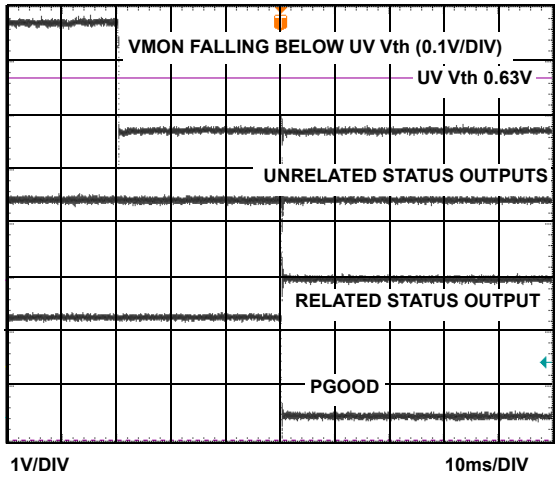


FIGURE 13. ISL6131 VMON FALLING TO PGOOD

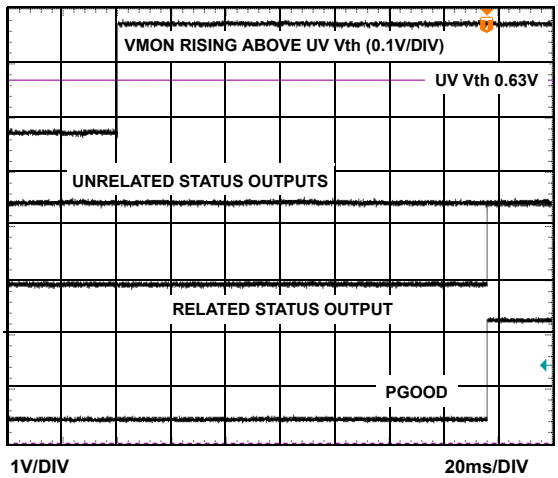


FIGURE 14. ISL6131 UV RISING TO PGOOD

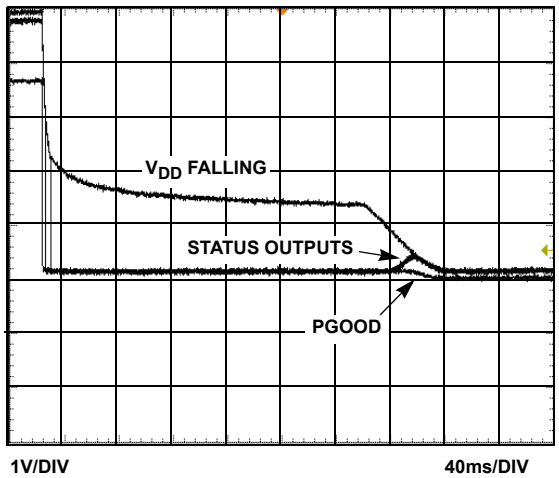


FIGURE 15. ISL6131 V_{DD} FALLING

Functional and Performance Waveforms (Continued)

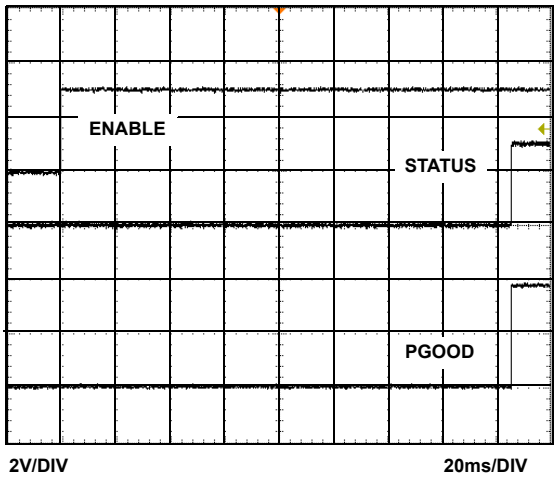


FIGURE 16. ISL6131 ENABLE L2H TO PGOOD

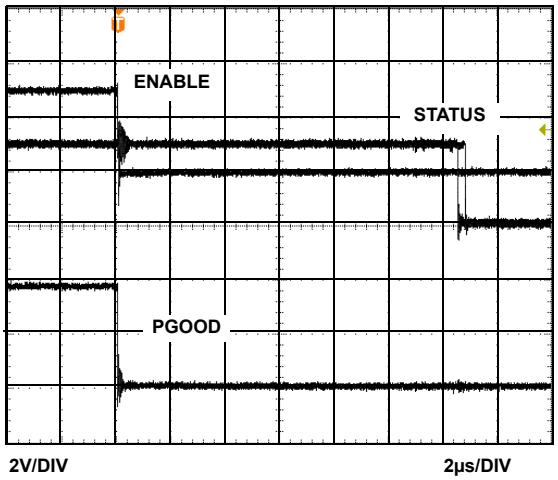


FIGURE 17. ISL6131 $\overline{\text{EN}}$ H2L TO PGOOD

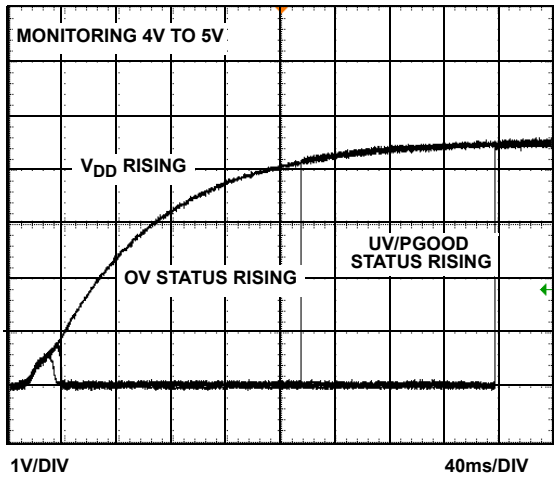


FIGURE 18. ISL6132 TURN-ON

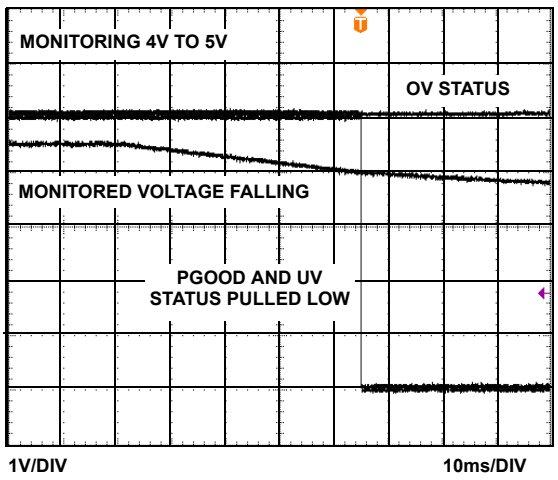


FIGURE 19. ISL6132 IN UV CONDITION

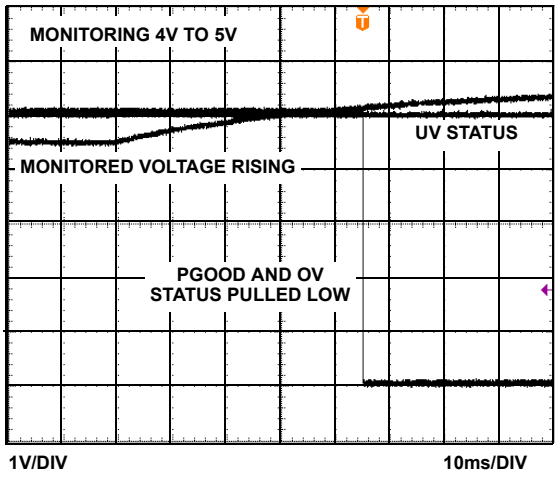


FIGURE 20. ISL6132 IN OV CONDITION

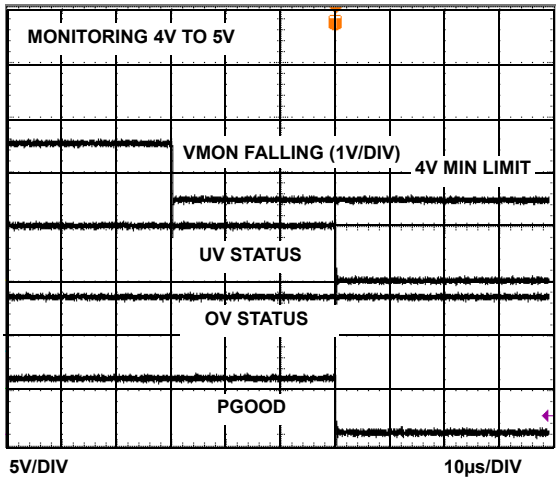


FIGURE 21. ISL6132 UV GLITCH FILTER TIMING

Functional and Performance Waveforms (Continued)

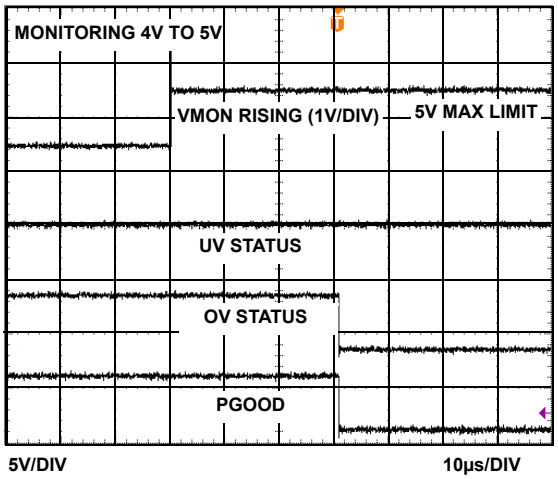


FIGURE 22. ISL6132 OV GLITCH FILTER TIMING

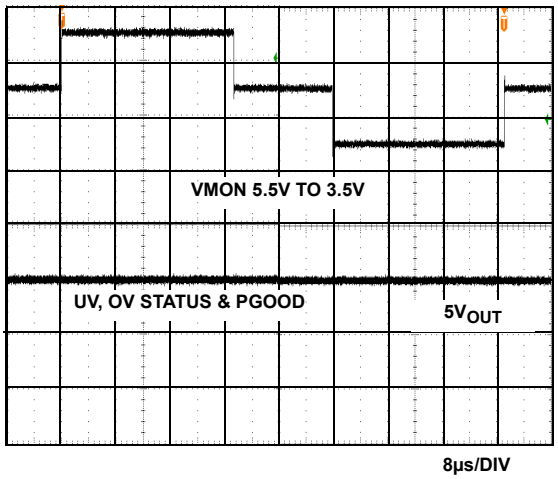


FIGURE 23. ISL6132 GLITCH FILTER TRANSIENT IMMUNITY

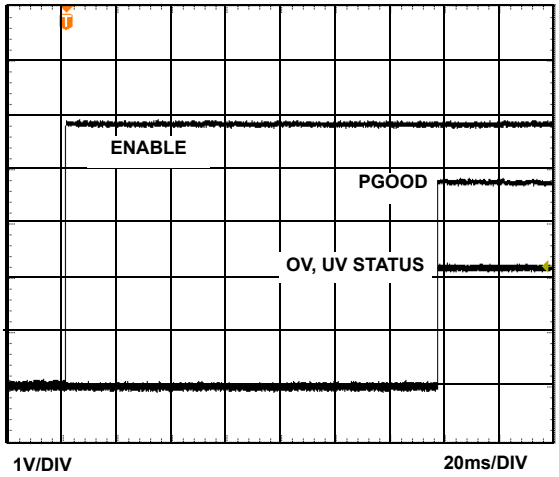


FIGURE 24. ISL6132 ENABLE TO PGOOD

ISL6131EVAL1Z and ISL6132EVAL1Z Descriptions

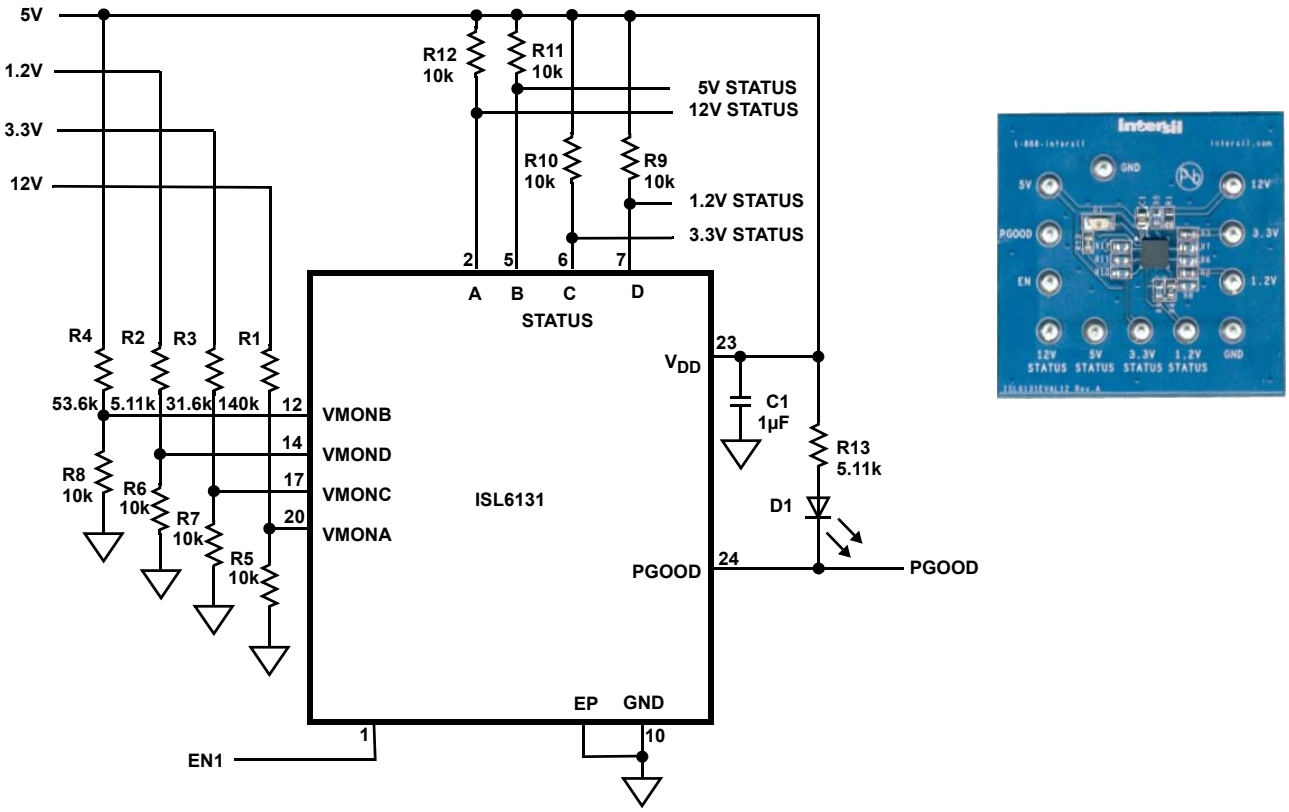


FIGURE 25. ISL6131EVAL1Z SCHEMATIC AND PHOTOGRAPH

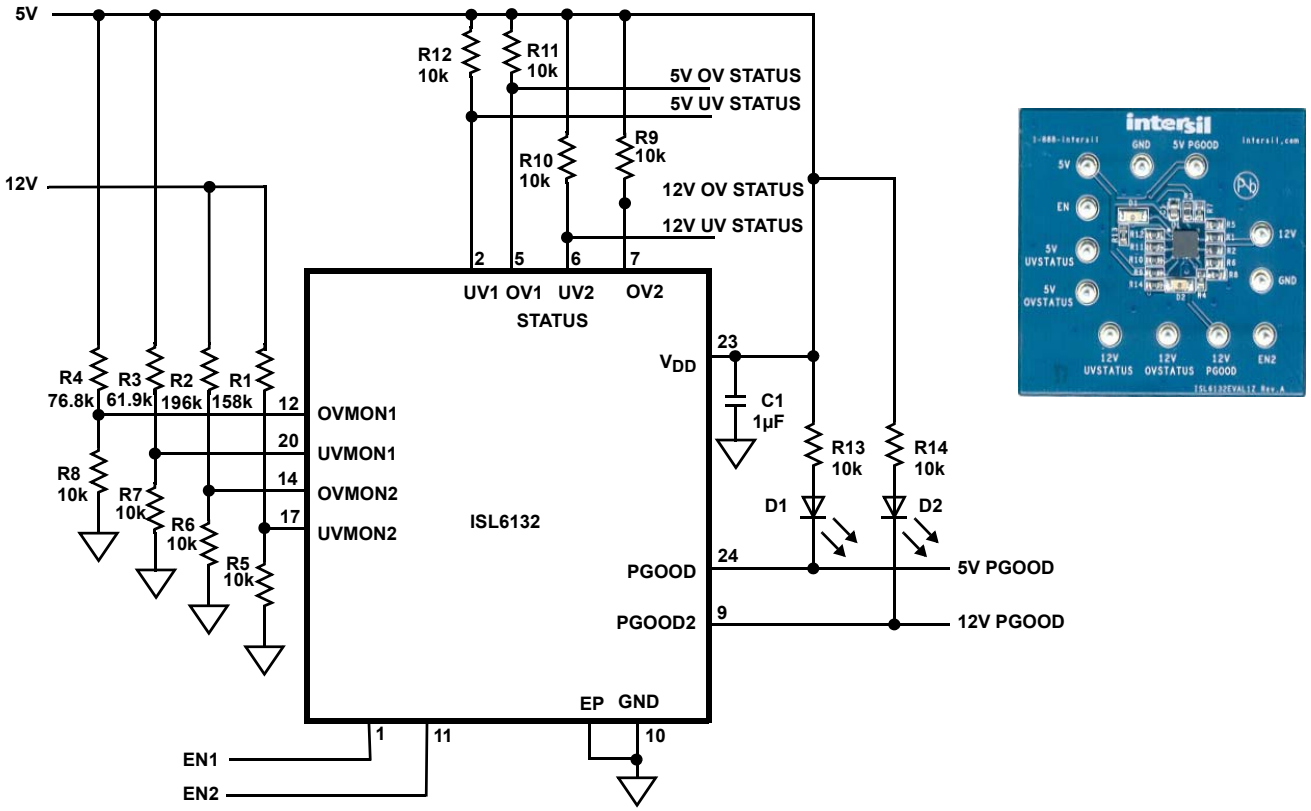


FIGURE 26. ISL6132EVAL1Z SCHEMATIC AND PHOTOGRAPH

TABLE 1. ISL6131EVAL1Z, ISL6132EVAL1Z COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
U1	ISL6131, Quad Undervoltage Supervisor	Intersil, ISL6131IR Quad Undervoltage Supervisor
R1	12V Upper Divider Resistor	140kΩ
R2	1.2V Upper Divider Resistor	5.11kΩ
R3	3.3V Upper Divider Resistor	31.6kΩ
R4	5V Upper Divider Resistor	53.6kΩ
U1	ISL6132, Dual Over & Undervoltage Supervisor	Intersil, ISL6132IR Dual Overvoltage & Undervoltage Supervisor
R1	12V Upper UV Divider Resistor	158kΩ
R2	12V Upper OV Divider Resistor	196kΩ
R3	5V Upper UV Divider Resistor	61.9kΩ
R4	5V Upper OV Divider Resistor	76.8kΩ
R5, R6, R7, R8	Lower Divider Resistors	10kΩ
R9, R10, R11, R12	STATUS Pull-up Resistors	10kΩ
C1	Decoupling Capacitor	1µF
D1, D2	PGOOD# INDICATOR	SMD RED LED

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
February 11, 2014	FN9119.6	• On page 5 - right hand column, paragraph 5 that starts with: "For the ISL6131, two dividers of two resistors each can be employed to monitor the OV and UV levels for each voltage. Otherwise, use a single three-resistor string for each voltage." Changed ISL6131 to ISL6132. • On page 14 - Updated Products section to updated About Intersil verbiage
July 18, 2011	FN9119.5	• On page 2, Ordering Information: added ISL6131EVAL1Z and ISL6132EVAL1Z Evaluation Boards. • On page 7: changed "Using the ISL613XSUPEREVAL2 Platform" section to "Using the ISL6131EVAL1Z and ISL6132EVAL1Z Platforms" and rewrote text. • On page 12: replaced Fig. 25, “ISL613XSUPEREVAL2 PHOTOGRAPH” with “ISL6131EVAL1Z SCHEMATIC AND PHOTOGRAPH.“ • On page 13: replaced Fig. 26, “ISL613XSUPEREVAL2 CHANNEL 1 SCHEMATIC” with “ISL6132EVAL1Z SCHEMATIC AND PHOTOGRAPH.” • Converted to latest datasheet template.
August 17, 2010	FN9119.4	• P1: Removed prenotification part ISL6132IR & Obsolete part ISL6131IR from Order Info. Added Part Marking column to Order Info. Updated Pb-free bullet in Features and Pb-free note in Ordering Information based on lead finish. Added TB347 link to ordering information for reel specifications. • P3: Per customer request, added "PD" label to Pinout and description to Pin Descriptions table, which states "Thermal Pad. Should be electrically connected to GND". • P4: Updated Caution statement in Abs Max. Removed Max Lead Soldering Temp from Thermal Info and replaced with Pb-Free Reflow link. Added standard temp range note to spec table MIN MAX columns. • P13: Updated POD to latest released. Changes were to convert to new QFN format and correct Note 4 (corrected “0.015mm and 0.30mm” to “0.15mm and 0.30mm”).
July 22, 2005	FN9119.3	• Added additional application usage text to clarify component choice. Corrected typographical errors in spec table.
August 18, 2004	FN9119.2	• Added Pb-free parts.
March 5, 2004	FN9119.1	• Added application information.
July 15, 2003	FN9119.0	Initial Release

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

© Copyright Intersil Americas LLC 2003-2014. All Rights Reserved.
All trademarks and registered trademarks are the property of their respective owners.

For additional products, see www.intersil.com/en/products.html

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at www.intersil.com/en/support/qualandreliability.html

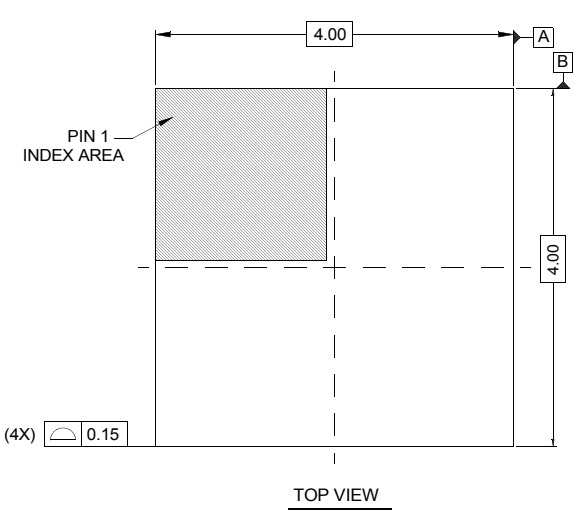
Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com

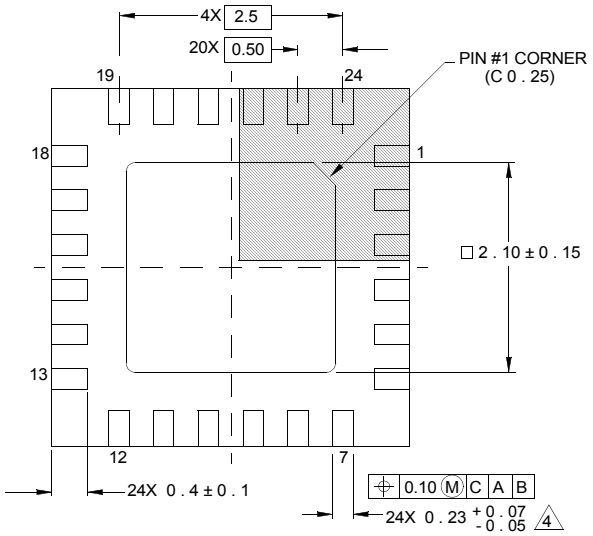
Package Outline Drawing

L24.4x4

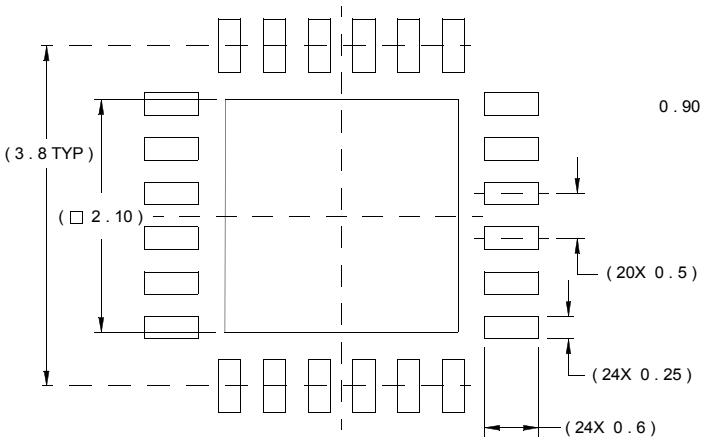
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 10/06



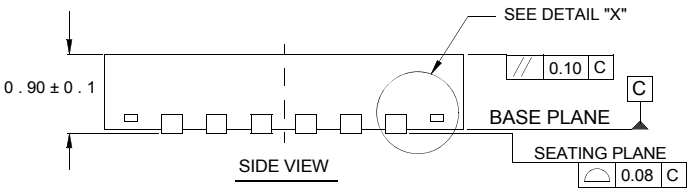
TOP VIEW



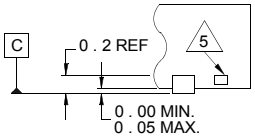
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.