ISL70002SEH, ISL73002SEH

Radiation Hardened and SEE Hardened 22A Synchronous Buck Regulators with Current Sharing

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The ISL70002SEH and ISL73002SEH (ISL7x002SEH) are radiation hardened and SEE hardened high-efficiency monolithic, synchronous buck regulators with integrated MOSFETs. This single chip power solution operates over an input voltage range of 3V to 5.5V and provides a tightly regulated output voltage that is externally adjustable from 0.8V to ~85% of the input voltage. Output load current capability is primarily determined by PVIN voltage with up to 22A for a single IC at PVIN ≤ 5.5V for T_J ≤ +125°C. Two ISL7x002SEH devices, configured to current share, can provide up to 38A of total output current at PVIN ≤ 5.5V for T_J ≤ +125°C assuming ±27% worst-case current share accuracy.

The devices use peak current-mode control with integrated error amp compensation and pin-selectable slope compensation. Switching frequency is also pin selectable to either 1MHz or 500kHz. Two devices can be synchronized 180° out-of-phase to reduce input RMS ripple current.

High integration makes them an ideal choice to power small form factor applications. Two devices can be synchronized to provide a complete power solution for large scale digital ICs, like Field Programmable Gate Arrays (FPGAs) that require separate core and I/O voltages.

The ISL7x002SEH is available in a thermally enhanced heat spreader package (R64.C)

Applications

- FPGA, CPLD, DSP, CPU core, and I/O voltages
- Low-voltage, high-density distributed power systems

Features

- DLA SMD 5962-12202
- Maximum output current ("Single Phase"):
  - 22A with external Schottky (T_J ≤125°C, PVIN ≤5.5V)
  - 18A (T_J ≤125°C, PVIN ≤5.5V)
  - 14A (T_J ≤125°C, PVIN ≤6.2V)
  - 12A (T_J ≤150°C, PVIN ≤6.2V)
- Maximum output current ("Dual Phase")
  - 38A (27% worst case current sharing)
- 1MHz or 500kHz switching frequency
- 3V to 6.2V supply voltage range
- ±1% reference voltage (line, load, temperature, and rad)
- Redundancy/junction isolation: exceptional SET performance
- Excellent transient response
- High efficiency >90%
- Two ISL7x002SEH synchronization, inverted-phase
- Comparator input for enable and power-good
- Input undervoltage, output undervoltage, and adjustable output overcurrent protection
- QML qualified per MIL-PRF-38535
- Full military temperature range operation (-55°C to +125°C)
- Radiation environment - ISL70002SEH
  - HDR (50-300rad(Si)/s): 100krad(Si)
  - LDR (0.01rad(Si)/s): 50krad(Si)
- Radiation environment - ISL73002SEH
  - LDR (0.01rad(Si)/s): 50krad(Si).
- SEE hardness (See the SEE Test report for details)
  - SEL and SEB LET_{TH} . . . . . 86.4MeV/mg/cm^2
  - SEFI LET_{TH}. . . . . 43MeV/mg/cm^2
  - SET LET_{TH} . . . . . 86.4MeV/mg/cm^2

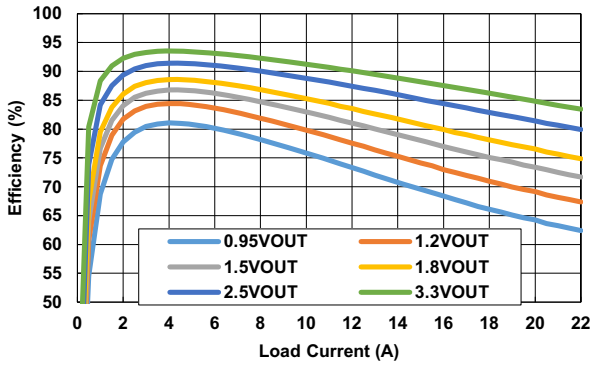

FIGURE 1. EFFICIENCY 5V INPUT, 500kHz, T_{case} = +25°C

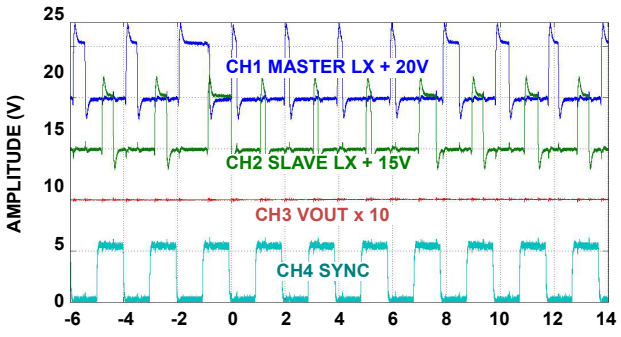

FIGURE 2. 2-PHASE SET PERFORMANCE AT 86.4MeV/mg/cm^2

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Typical Application Schematic

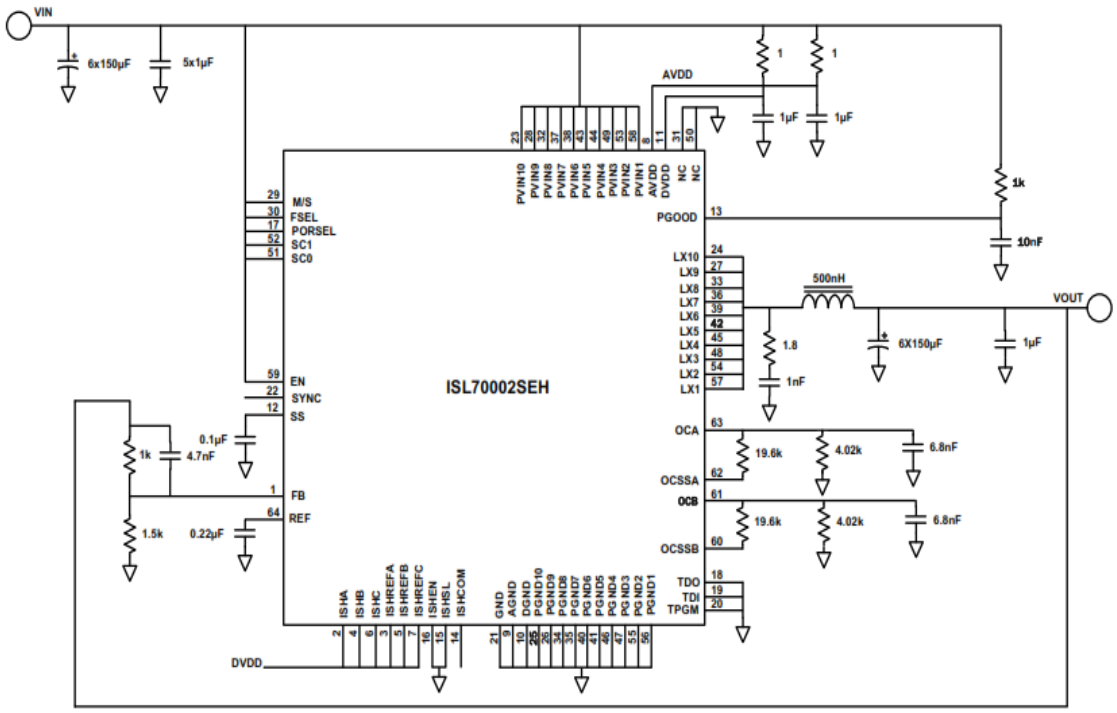


FIGURE 3. SINGLE UNIT OPERATION

Typical Application Schematic (Continued)

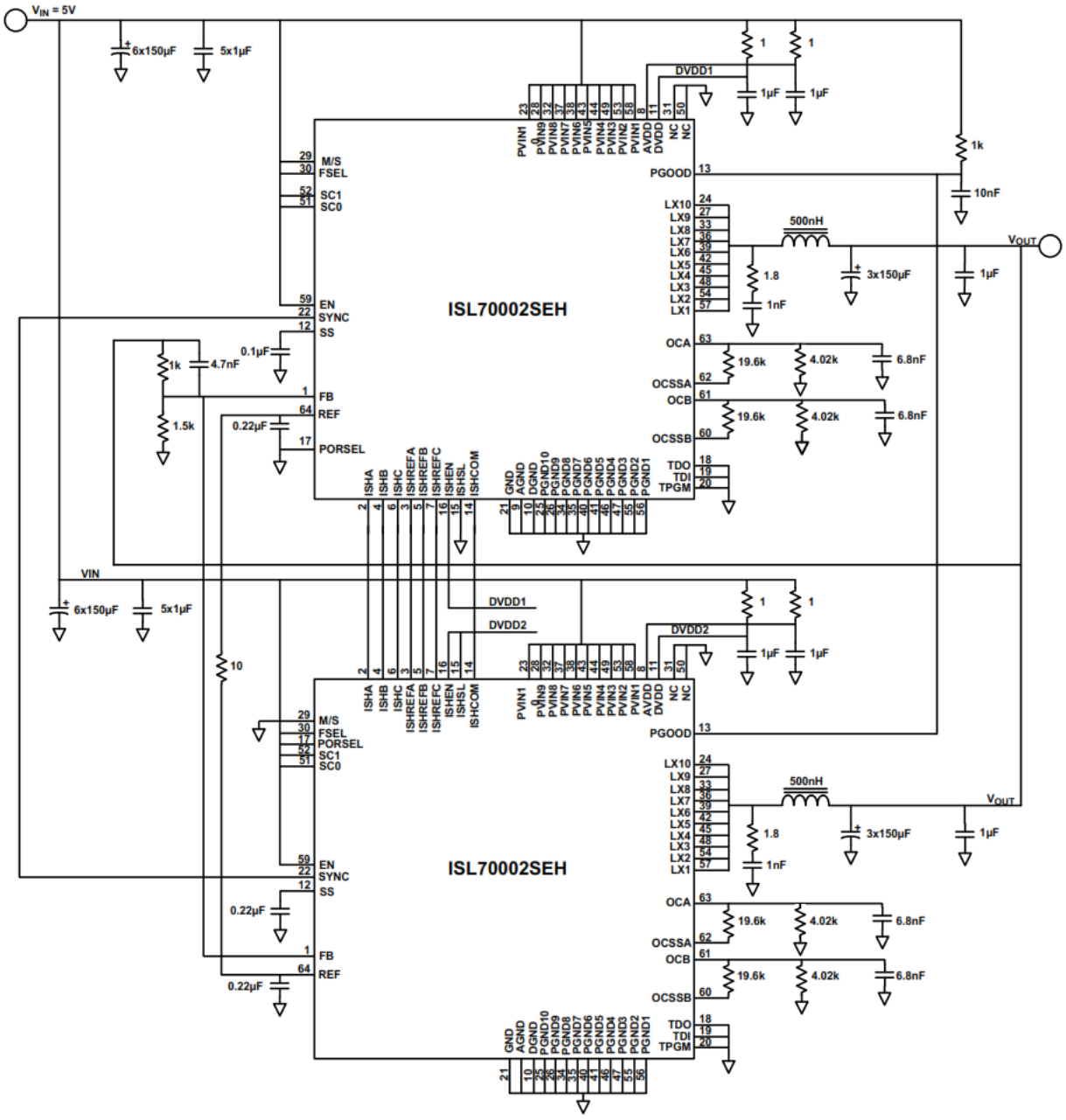


FIGURE 4. TWO-PHASE OPERATION WITH CURRENT SHARING

Functional Block Diagram

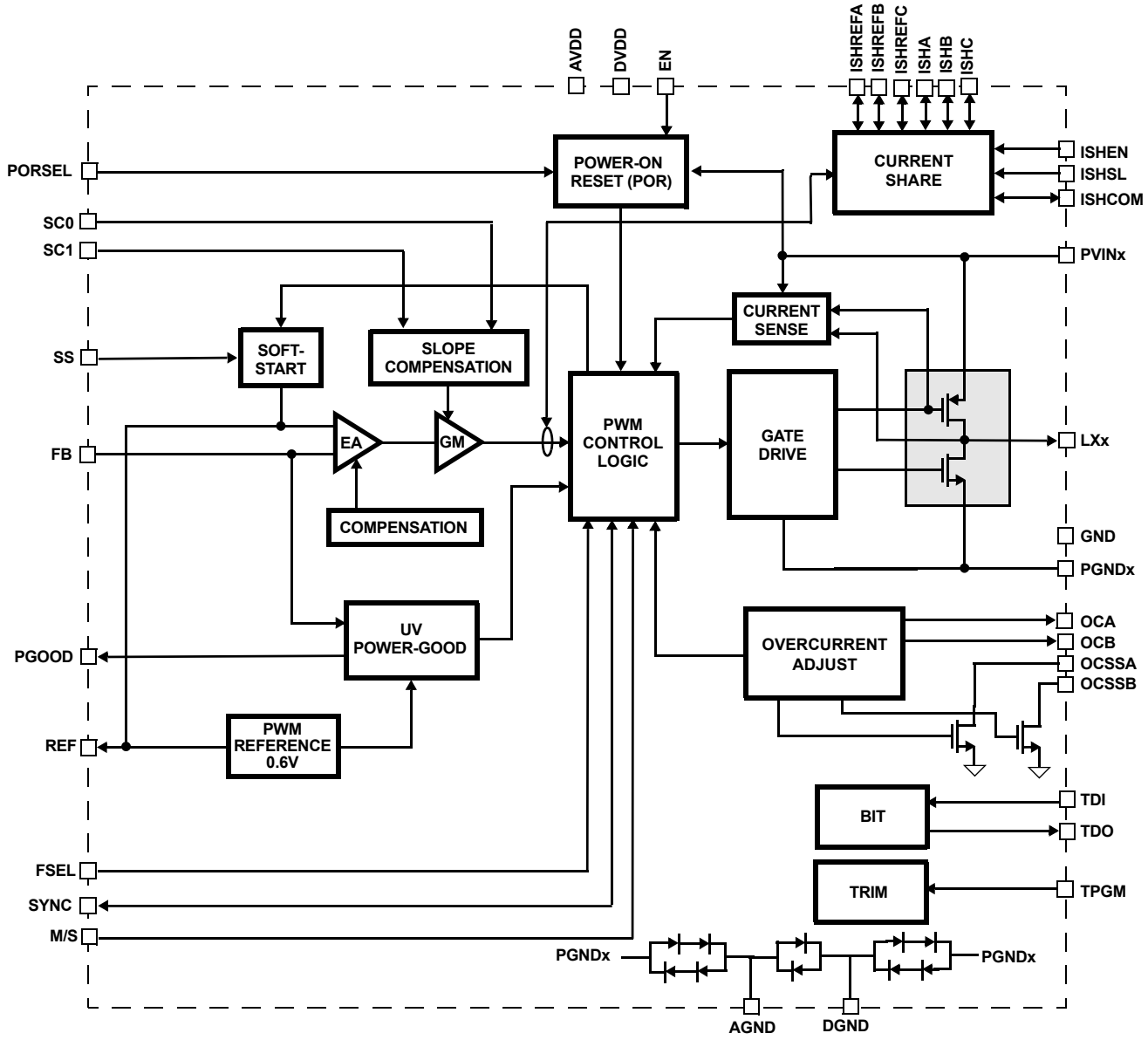


FIGURE 5. FUNCTIONAL BLOCK DIAGRAM

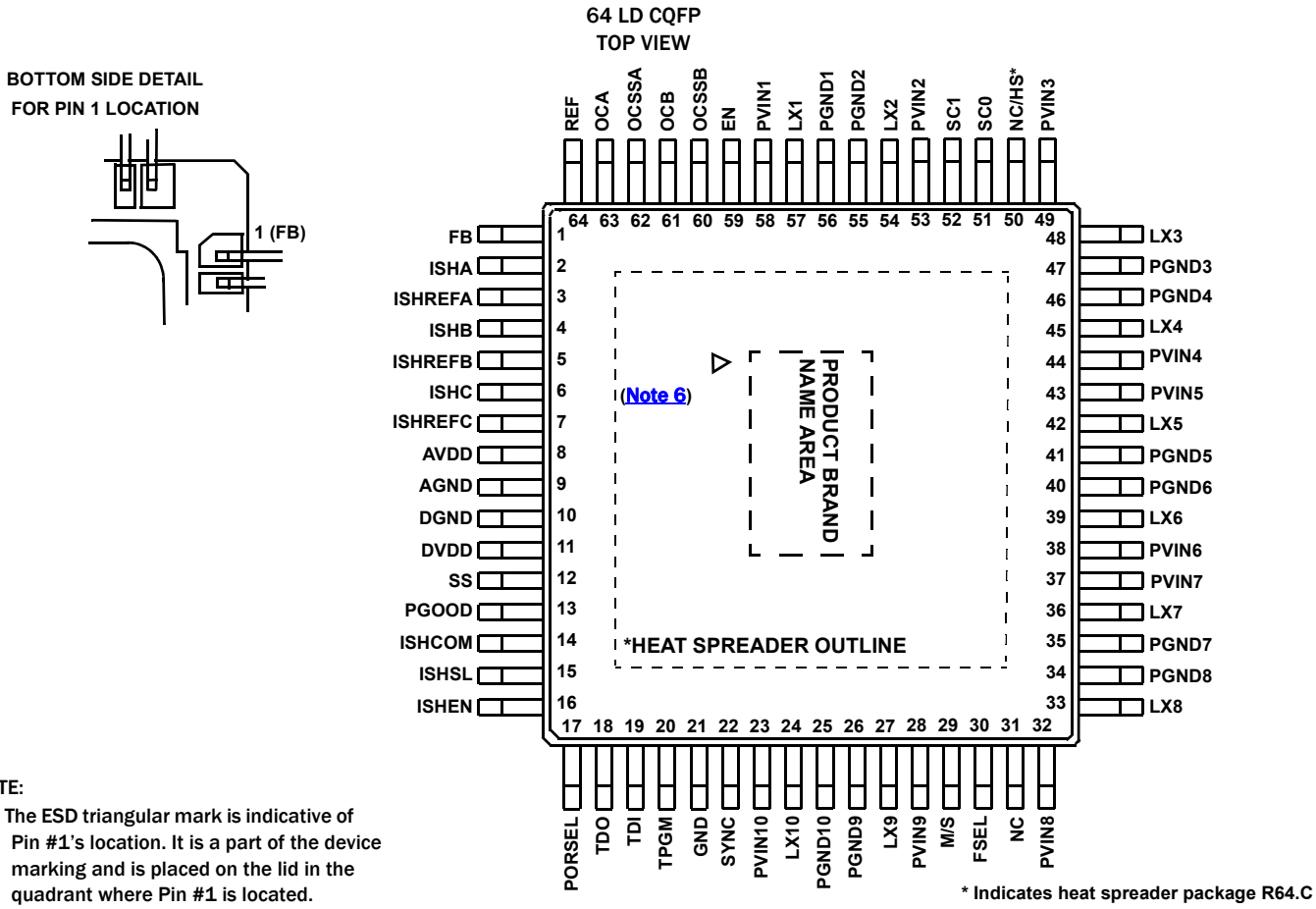
Ordering Information

ORDERING SMD NUMBER (Note 2)	PART NUMBER (Note 1)	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	TEMP. RANGE
5962R1220201VXC	ISL70002SEHVF	HDR to 100krad(Si), LDR to 50krad(Si)	64 Ld CQFP	R64.A	-55 to +125°C
5962R1220201VYC	ISL70002SEHVFE		64 Ld CQFP with heat spreader	R64.C	
5962R1220201V9A	ISL70002SEHVX (Note 3)		Die	N/A	
5962L1220202VXC	ISL73002SEHVF	LDR to 50krad(Si)	64 Ld CQFP	R64.A	
5962L1220202VYC	ISL73002SEHVFE		64 Ld CQFP with heat spreader	R64.C	
5962L1220202V9A	ISL73002SEHVX (Note 3)		Die	N/A	
N/A	ISL70002SEHF/PROTO (Note 4)	N/A	64 Ld CQFP	R64.A	
	ISL70002SEHFE/PROTO (Note 4)		64 Ld CQFP with heat spreader	R64.C	
	ISL70002SEHX/SAMPLE (Notes 3, 4)		Die	N/A	
	ISL73002SEHF/PROTO (Note 4)		64 Ld CQFP	R64.A	
	ISL73002SEHFE/PROTO (Note 4)		64 Ld CQFP with heat spreader	R64.C	
	ISL73002SEHX/SAMPLE (Notes 3, 4)		Die	N/A	
	ISL70002SEHEVAL1Z (Note 5)	Evaluation Board			
	ISL70002SEHEVAL2Z (Note 5)	Current Sharing Evaluation Board			
	ISL70002SEHDEMO1Z (Note 5)	High Current Sharing Demonstration Board			

NOTES:

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in "Electrical Specifications" on page 9.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
5. Evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Pin Configuration



NOTE:

6. The ESD triangular mark is indicative of Pin #1's location. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

Pin Descriptions

R64.A PIN #	R64.C PIN #	PIN NAME	DESCRIPTION
1		FB	Voltage feedback input to the internal error amplifier. Connect a resistor from FB to VOUT and from FB to AGND to adjust the output voltage in accordance with Equation 1: $V_{OUT} = V_{REF} \cdot [1 + (R_T/R_B)]$ (EQ. 1) where: V_{OUT} = output voltage V_{REF} = reference voltage (0.6V typical) R_T = top divider resistor (Must be 1kΩ R_B = bottom divider resistor The top divider resistor must be 1kΩ to mitigate SEE. Connect a 4.7nF ceramic capacitor across R_T to mitigate SEE and to improve stability margins. If using current share, tie FB of the master to FB of the slave.
2, 4, 6		ISHA, ISHB, ISHC	If configured as a current share master (ISHSL = DGND, ISHEN = DVDD), these pins are outputs that provide a current equal to 25 times the redundant A/B/C error amp output currents plus ISHREFA/ISHREFB/ISHREFC (nominally 100µA each). If configured as a current share slave (ISHSL = DVDD, ISHEN = DVDD), the ISHA/ISHB/ISHC pins are inputs that become the slave's redundant A/B/C error amp output current. If using current share, tie ISHA/ISHB/ISHC of the master to ISHA/ISHB/ISHC of the slave. If not using current share, tie ISHA/ISHB/ISHC to DVDD. ISHA/ISHB/ISHC are tri-stated prior to a valid POR and when ISHEN = DGND.

Pin Descriptions (Continued)

R64.A PIN #	R64.C PIN #	PIN NAME	DESCRIPTION
3, 5, 7		ISHREFA, ISHREFB, ISHREFC	If configured as a current share master (ISHSL = DGND, ISHEN = DVDD), these pins provide a reference output current equal to 100µA each. If configured as a current share slave (ISHSL = DVDD, ISHEN = DVDD), the ISHREFA/ISHREFB/ISHREFC pins accept a reference input current. For a current share slave, this input current is used together with the ISHA/ISHB/ISHC current to determine the master's redundant A/B/C error amp output current. If using current share, tie ISHREFA/ISHREFB/ISHREFC of the MASTER to ISHREFA/ISHREFB/ISHREFC of the slave. If not using current share, tie ISHREFA/ISHREFB/ ISHREFC to DVDD. The purpose of the reference current is to reduce the impact of external noise coupling onto ISHA/ISHB/ISHC. ISHREFA/ISHREFB/ISHREFC are tri-stated prior to a valid POR and when ISHEN = DGND.
8		AVDD	Bias supply input to the internal analog control circuitry. Locally filter this pin to AGND using a 1Ω resistor and a 1µF ceramic capacitor. Locate both filter components as close as possible to the IC. AVDD should be the same voltage as DVDD and PVINx (±200mV).
9		AGND	Analog ground associated with the internal analog control circuitry. Connect this pin directly to the PCB ground plane.
10		DGND	Digital ground associated with the internal digital control circuitry. Connect this pin directly to the PCB ground plane.
11		DVDD	Bias supply input to the internal digital control circuitry. Locally filter this pin to DGND using a 1Ω resistor and a 1µF ceramic capacitor. Locate both filter components as close as possible to the IC. DVDD should be the same voltage as AVDD and PVINx (±200mV).
12		SS	Soft-start input. Connect a ceramic capacitor from this pin to DGND to set the soft-start output ramp time in accordance with Equation 2: $t_{SS} = C_{SS} \cdot V_{REF} / I_{SS}$ (EQ. 2) where: t_{SS} = soft-start output ramp time C_{SS} = soft-start capacitor V_{REF} = reference voltage (0.6V typical) I_{SS} = soft-start charging current (23µA typical) Soft-start time is adjustable from approximately 2ms to 200ms. The range of the soft-start capacitor should be 82nF to 8.2µF, inclusive. If using current share, C_{SS} of the slave should be at least twice the C_{SS} of the master.
13		PGOOD	Power-good output. This pin is an open drain logic output that is pulled to DGND when the output voltage is outside a ±11% typical regulation window. This pin can be pulled up to any voltage from 0V to 5.5V, independent of the supply voltage. A nominal 1kΩ to 10kΩ pull-up resistor is recommended. Bypass this pin to DGND with a 10nF ceramic capacitor to mitigate SEE. If using current share, tie PGOOD of the master to PGOOD of the slave.
14		ISHCOM	Bidirectional communication line between a current share master and a current share slave. If using current share, tie ISHCOM of the master to ISHCOM of the slave. The master enables the slave by resistively (~ 8.5kΩ) pulling ISHCOM high. The slave indicates an overcurrent fault condition to the master by pulling ISHCOM low. To mitigate SET, connect a 47pF ceramic capacitor from ISHCOM to the PCB ground plane. If not using current share this pin should be floated or connected to the PCB ground plane. ISHCOM is tri-stated if ISHEN is low.
15		ISHSL	Logic input that configures the IC as a current share master or slave. Tie this pin to DVDD to configure the IC as a current share slave. Tie this pin to the PCB ground plane to configure the IC as a current share master, or if the current share feature is not being used.
16		ISHEN	Input that enables/disables the current share feature. To enable the current share feature, tie this pin to DVDD. To disable the current share feature, tie this pin to the PCB ground plane.
17		PORSEL	Input for selecting the rising and falling POR (Power-On-Reset) thresholds. For a nominal 5V supply, connect this pin to DVDD or PVIN. For a nominal 3.3V supply, connect this pin to DGND. For nominal supply voltages between 5V and 3.3V, connect this pin to DGND. See additional considerations for PORSEL when using an external SYNC clock input on page 17.
18		TDO	Connect this pin to the PCB ground plane.
19		TDI	Connect this pin to the PCB ground plane.
20		TPGM	Connect this pin to the PCB ground plane.
21		GND	This pin is connected to an internal metal die trace that serves as a sensitive node noise shield. Connect this pin to the PCB ground plane.

Pin Descriptions (Continued)

R64.A PIN #	R64.C PIN #	PIN NAME	DESCRIPTION
22		SYNC	When this pin is configured as an output (clock Master Mode, M/S = DVDD), it drives the SYNC input of another ISL7x002SEH with a square wave that is inverted (~180° out-of-phase) from the master clock driving the master PWM circuits. When configured as an input (clock Slave Mode, M/S = DGND), this pin uses the SYNC output from another ISL7x002SEH or an external clock to drive the clock slave PWM circuitry. If synchronizing to an external clock, the clock must be SEE hardened and the frequency must be within the range of 400kHz to 1.2MHz. The master configured SYNC output is active when biased.
23, 28, 32, 37, 38, 43, 44, 49, 53, 58		PVINx	Power supply inputs to the corresponding internal power blocks. These pins must be connected to a common power supply rail, which must fall in the range of 3V to 5.5V. Bypass these pins directly to PGNDx with ceramic capacitors located as close as possible to the IC. PVINx should be the same voltage as DVDD and AVDD (±200mV).
24, 27, 33, 36, 39, 42, 45, 48, 54, 57		LXx	Outputs of the corresponding internal power blocks and should be connected to the output filter inductor. These pins are internally connected to the synchronous MOSFET power switches.
25, 26, 34, 35, 40, 41, 46, 47, 55, 56		PGNDx	Power grounds associated with the corresponding internal power blocks. These pins also provide the ground path for the metal package lid. Connect these pins directly to the PCB ground plane. These pins should also connect to the negative terminals of the input and output capacitors. Place the input and output capacitors as close as possible to the IC.
29		M/S	Clock master/slave input for selecting the direction of the bidirectional SYNC pin. For SYNC = Output (Master Mode), connect this pin to DVDD or PVIN. For SYNC = Input (Slave Mode), connect this pin to the PCB ground plane.
30		FSEL	Oscillator frequency select input. Tie this pin to DVDD or PVIN to select a 1MHz nominal oscillator frequency. Tie this pin to the PCB ground plane to select a 500kHz nominal oscillator frequency.
31, 50	31	NC, HS	No Connect. These pins are not connected to anything internally. They should be connected to the PCB ground plane.
N/A	50	HS	For the R64.C package (heat spreader option), this pin is connected to the heat spreader on the underside of the package. Connect this pin and/or the heat spreader to a thermal plane. This is a floating node.
51, 52		SC0/SC1	Inputs that comprise a 2-bit code to select the slope compensation (SC) current ramp referred to the output as shown below: SC1 = DVDD or PVIN, SC0 = DVDD or PVIN: SC = 6.6A/µs for FSEL = GND SC1 = DVDD or PVIN, SC0 = GND: SC = 3.3A/µs for FSEL = GND SC1 = GND, SC0 = DVDD or PVIN: SC = 1.6A/µs for FSEL = GND SC1 = GND, SC0 = GND: SC = 0.8A/µs for FSEL = GND SC1 = DVDD or PVIN, SC0 = DVDD or PVIN: SC= 13.4A/µs for FSEL = DVDD or PVIN SC1 = DVDD or PVIN, SC0 = GND: SC = 6.7A/µs for FSEL = DVDD or PVIN SC1 = GND, SC0 = DVDD or PVIN: SC = 3.4A/µs for FSEL = DVDD or PVIN SC1 = GND, SC0 = GND: SC = 1.7A/µs for FSEL = DVDD or PVIN If using current share, SC0 and SC1 of the slave MUST match the master SC0 and SC1.
59		EN	Enable input to the IC. This is a comparator type input with a rising threshold of 0.6V and programmable hysteresis. Driving this pin above 0.6V enables the IC. Bypass this pin to the PCB ground plane with a 10nF ceramic capacitor to mitigate SEE. This pin can be tied to DVDD or PVIN
60, 62		OCSSB/ OCSSA	These pins set the redundant A/B peak overcurrent limit threshold during soft-start. Connect a resistor from OCSSx to OCx in accordance with the following equation: ROCSSx (kΩ) = (60 x ROCx)/[(IOCSSx x ROCx) - 60] where ROCx (kΩ) is the resistor value chosen to set the peak overcurrent limit during normal operation and IOCSSx (A) is the desired peak current limit threshold during soft-start.
61, 63		OCB/OCA	These pins set the redundant A/B peak overcurrent limit threshold during normal operation. Connect a resistor from this pin to the PCB ground plane in accordance with the following equation: ROCx (kΩ) = 60/IOC where IOC (A) is the desired peak current limit threshold during normal operation.
64		REF	Internal reference voltage output. Bypass this pin to the PCB ground plane with a 220nF ceramic capacitor located as close as possible to the IC. The bypass capacitor is needed to mitigate SEE. No current (sourcing or sinking) is available from this pin. If using current share, tie REF of the master to REF of the slave through a 10Ω resistor.

Absolute Maximum Ratings in a Heavy Ion Environment (Note 7)

AVDD . . . . . AGND - 0.3V to AGND + 6.2V
DVDD . . . . . DGND - 0.3V to DGND + 6.2V
LXx, PVINx (Note 14) . . . . . PGNDx - 0.3V to PGNDx + 6.2V
- up to 14A at T_J = 125°C, 12A at T_J = 150°C without Schottky Clamp Diode

LXx, PVINx (Note 14) . . . . . PGNDx - 0.3V to PGNDx + 5.5V
- 18A to 22A at T_J = 125°C with Schottky Clamp Diode LX to GND
- 14A to 18A at T_J = 125°C without Schottky Clamp Diode

AVDD - AGND, DVDD - DGND . . . . . PVINx - PGNDx ± 0.3V
Signal Pins (Note 12). . . . . AGND - 0.3V to AVDD + 0.3V
Digital Control Pins (Note 13). . . . . DGND - 0.3V to DVDD + 0.3V
PGOOD . . . . . DGND - 0.3V to DGND + 6.2V
SS. . . . . DGND - 0.3V to DGND + 2.5V
ESD Rating
Human Body Model (Tested per MIL-STD-883 TM3015) 2kV
Machine Model (Tested per JESD22-A115C) 200V
Charged Device Model (Tested per JS-002-2014) 750V

Absolute Maximum Ratings without Heavy Ions

AVDD . . . . . AGND - 0.3V to AGND + 6.5V
DVDD . . . . . DGND - 0.3V to DGND + 6.5V
LXx, PVINx (Note 14) . . . . . PGNDx - 0.3V to PGNDx + 6.5V
AVDD - AGND, DVDD - DGND . . . . . PVINx - PGNDx ± 0.3V
Signal Pins (Note 12). . . . . AGND - 0.3V to AVDD + 0.3V
Digital Control Pins (Note 13). . . . . DGND - 0.3V to DVDD + 0.3V
PGOOD . . . . . DGND - 0.3V to DGND + 6.5V
SS. . . . . DGND - 0.3V to DGND + 2.5V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CQFP Package R64.A (Notes 8, 10)	34	1.5
CQFP Package R64.C (Notes 9, 11)	17	0.7

Operating Junction Temperature Range . . . . . -55°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C

Recommended Operating Conditions

AVDD. . . . . AGND + 3V to 5.5V
DVDD. . . . . DGND + 3V to 5.5V
PVINx. . . . . PGNDx + 3V to 5.5V
AVDD - AGND, DVDD - DGND . . . . . PVINx - PGNDx ± 0.1V
Signal Pins (Note 12) . . . . . AGND to AVDD
Digital Control Pins (Note 13) . . . . . DGND to DVDD
REF, SS . . . . . Internally Set
GND, TDI, TDO, TPGM . . . . . DGND
I_{LXx} (T_J ≤+150°C) . . . . . 0A to 1.2A
I_{LXx} (T_J ≤+125°C) . . . . . 0A to 2.2A
Ambient Temperature Range . . . . . -55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

7. Absolute Maximum Ratings assume operation in a heavy ion environment with LET = 86.4MeV • cm^2/mg.
8. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board. See TB379 for details.
9. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
10. For θ_{JC}, the “case temp” location is the center of the package underside.
11. For θ_{JC}, the “case temp” location is the center of the exposed metal heat spreader on the package underside.
12. EN, FB, ISHx, ISHREFx, OCx, OCSSx, PORSEL, and REF pins.
13. FSEL, GND, ISHCOM, ISHEN, ISHRSL, M/S, SYNC, SC0, SC1, TDI, TDO, and TPGM pins.
14. The 6.2V absolute maximum rating must be met for a 20MHz bandwidth limited observation at the device pins. In addition, for a 600MHz bandwidth limited observation, the peak transient voltage on PVINx (measured to PGNDx) must be less than 7.1V with a duration above 6.2 V of less than 10ns, and the peak transient voltage on LXx (measured to PGNDx) must be less than 7.9V with a duration above 6.2 V of less than 10ns.

Electrical Specifications

Unless otherwise noted, V_{IN} = AVDD = DVDD = PVINx = EN = FSEL = M/S = SC0 = SC1 = 3V to 5.5V; GND = AGND = DGND = PGNDx = ISHx = ISHCOM = ISHEN = ISHREFx = ISHSL = TDI = TDO = TPGM = 0V; FB = 0.65V; PORSEL = V_{IN} for 4.5V ≤ V_{IN} ≤ 5.5V and GND for V_{IN} < 4.5V; LXx = SYNC = Open Circuit; OCx is connected to OCSSx with a 10kΩ resistor; OCx is connected to GND with a 4.99kΩ resistor shunted by a 6.8nF capacitor; PGOOD is pulled up to V_{IN} with a 1kΩ resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; T_A = T_J = -55°C to +125°C; Post 100krad(Si) (Note 12)

PARAMETER	TEST CONDITIONS	MIN (Note 16)	TYP (Note 15)	MAX (Note 16)	UNIT
POWER SUPPLY					
Operating Supply Current (Current Share Disabled)	V_{IN} = 5.5V		70	105	mA
	V_{IN} = 3.6V		43	65	mA
Standby Supply Current (Current Share Disabled)	V_{IN} = 5.5V, EN = GND, ISHEN = GND		2.5	6	mA
	V_{IN} = 3.6V, EN = GND, ISHEN = GND		2	4	mA

Electrical Specifications Unless otherwise noted, V_{IN} = AVDD = DVDD = PVINx = EN = FSEL = M/S = SC0 = SC1 = 3V to 5.5V; GND = AGND = DGND = PGNDx = ISHx = ISHCOM = ISHEN = ISHREFx = ISHSL = TDI = TDO = TPGM = 0V; FB = 0.65V; PORSEL = V_{IN} for 4.5V ≤ V_{IN} ≤ 5.5V and GND for V_{IN} < 4.5V; LXx = SYNC = Open Circuit; OCx is connected to OCSSx with a 10kΩ resistor; OCx is connected to GND with a 4.99kΩ resistor shunted by a 6.8nF capacitor; PGOOD is pulled up to V_{IN} with a 1kΩ resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; T_A = T_J = -55°C to +125°C; Post 100krad(Si) (Note 12) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 16)	TYP (Note 15)	MAX (Note 16)	UNIT
Operating Supply Current (Current Share Enabled, Current Share Master)	V_{IN} = ISHEN = 5.5V, ISHCOM = open circuit		70	120	mA
Operating Supply Current (Current Share Enabled, Current Share Slave)	V_{IN} = ISHEN = ISHSL = 5.5V, ISHCOM pulled to V_{IN} with 1kΩ, M/S = GND, ISHx = ISHREFx = -100µA, SYNC = external 1MHz clock		70	120	mA
Standby Supply Current (Current Share Enabled, Current Share Slave)	V_{IN} = ISHEN = ISHSL = 5.5V, EN = M/S = GND, SYNC = external 1MHz clock		3.0	7	mA
	V_{IN} = ISHEN = ISHSL = 5.5V, M/S = GND, SYNC = external 1MHz clock, ISHCOM = GND		7.3	11	mA
OUTPUT VOLTAGE AND CURRENT					
Reference Voltage		0.594	0.6	0.606	V
Output Voltage Tolerance	V_{OUT} = 0.8V to 2.5V, I_{OUT} = 0A to 12A (Notes 17, 18)	-2		2	%
Error Amp Input Offset Voltage	V_{IN} = 5.5V, V_{REF} = 600mV, test mode	-1		3	mV
Feedback (FB) Input Leakage Current	V_{IN} = 5.5V, V_{FB} = 600mV	-1.5		1.5	µA
Sustained Output Current	V_{IN} = 3V, V_{OUT} = 1.8V, current at which V_{OUT} falls to 98% of set-point with OCA = OCB = PVIN (Note 19)	16	22		A
PWM CONTROL LOGIC					
Internal Oscillator Tolerance	FSEL = V_{IN} or GND	-15		15	%
External Oscillator Range	M/S = GND	0.4		1.2	MHz
Minimum LXx On-Time	V_{IN} = 5.5V, test mode		200	275	ns
Minimum LXx Off-Time	V_{IN} = 5.5V, test mode		0	50	ns
Minimum LXx On-Time	V_{IN} = 3V, test mode		225	300	ns
Minimum LXx Off-Time	V_{IN} = 3V, test mode		0	50	ns
PORSEL, Master/Slave (M/S), SC1, SC0, ISHSL, ISHEN, FSEL Input Voltage	Input high threshold	V_{IN} -0.5	1.3		V
	Input low threshold		1.2	0.5	V
PORSEL, Master/Slave (M/S), SC1, SC0, ISHSL, ISHEN, FSEL Input Leakage Current	V_{IN} = 5.5V	-1		1	µA
Synchronization (SYNC) Input Voltage	Input high threshold, M/S = GND	2.3	1.7		V
	Input Low Threshold, M/S = GND		1.5	1	V
Synchronization (SYNC) Input Leakage Current	V_{IN} = 5.5V, M/S = GND, SYNC = V_{IN} or GND	-1		1	µA
Synchronization (SYNC) Output Voltage	V_{IN} - V_{OH} at I_{OH} = -1mA		0.1	0.4	V
	V_{OL} at I_{OL} = 1mA		0.1	0.4	V
POWER BLOCKS					
Upper Device $r_{DS(ON)}$	V_{IN} = 3V, 4A load, all power blocks in parallel, test mode (Note 15)		20	40	mΩ
Lower Device $r_{DS(ON)}$	V_{IN} = 3V, 4A load, all power blocks in parallel, test mode (Note 15)		15	30	mΩ
LXx Output Leakage	V_{IN} = 5.5V, EN = LXx = GND, single LXx output	-1			µA
	V_{IN} = LXx = 5.5V, EN = GND, single LXx output			10	µA

Electrical Specifications Unless otherwise noted, V_{IN} = AVDD = DVDD = PVINx = EN = FSEL = M/S = SC0 = SC1 = 3V to 5.5V; GND = AGND = DGND = PGNDx = ISHx = ISHCOM = ISHEN = ISHREFx = ISHSL = TDI = TDO = TPGM = 0V; FB = 0.65V; PORSEL = V_{IN} for 4.5V ≤ V_{IN} ≤ 5.5V and GND for V_{IN} < 4.5V; LXx = SYNC = Open Circuit; OCx is connected to OCSSx with a 10kΩ resistor; OCx is connected to GND with a 4.99kΩ resistor shunted by a 6.8nF capacitor; PGOOD is pulled up to V_{IN} with a 1kΩ resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; T_A = T_J = -55°C to +125°C; Post 100krad(Si) (Note 12) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 16)	TYP (Note 15)	MAX (Note 16)	UNIT
Dead Time (Note 18)	Within a single power block or between power blocks	2.2	25		ns
Efficiency (Note 18)	V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 6A, FSEL = GND		88		%
	V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 6A		90		%
POWER-ON RESET					
VIN POR	Rising threshold, PORSEL = V_{IN}	4.1	4.3	4.45	V
	Hysteresis, PORSEL = V_{IN}	225	325	425	mV
	Rising threshold, PORSEL = GND	2.65	2.8	2.95	V
	Hysteresis, PORSEL = GND	70	140	240	mV
Enable (EN) Input Voltage	Rising/falling threshold	0.56	0.6	0.64	V
Enable (EN) Input Leakage Current	V_{IN} = 5.5V, EN = V_{IN} or GND	-3		3	µA
Enable (EN) Sink Current	EN = 0.3V	6.4	11	16.6	µA
SOFT-START					
Soft-Start Source Current	SS = GND	20	23	27	µA
Soft-Start Discharge ON-Resistance			2.2	4.7	Ω
Soft-Start Discharge Time			256		Clock Cycles
POWER-GOOD SIGNAL					
Rising Threshold	V_{FB} as a percentage of V_{REF}, test mode	107	111	115	%
Rising Hysteresis	V_{FB} as a percentage of V_{REF}, test mode	2	3.5	5	%
Falling Threshold	V_{FB} as a percentage of V_{REF}, test mode	85	89	93	%
Falling Hysteresis	V_{FB} as a percentage of V_{REF}, test mode	2	3.5	5	%
Power-Good Drive	V_{IN} = 3V, PGOOD = 0.4V, EN = GND	7.2			mA
Power-Good Leakage	V_{IN} = PGOOD = 5.5V			1	µA
PROTECTION FEATURES					
Undervoltage Monitor					
Undervoltage Trip Threshold	V_{FB} as a percentage of V_{REF}, test mode	71	75	79	%
Undervoltage Recovery Threshold	V_{FB} as a percentage of V_{REF}, test mode	84	88	92	%
Overcurrent Monitor					
Overcurrent Trip Level	I_{OCx} = 60µA, test mode (Note 20)	5.35		7.35	A
	I_{OCx} = 240µA, test mode (Note 20)	23		26	A

Electrical Specifications Unless otherwise noted, V_{IN} = AVDD = DVDD = PVINx = EN = FSEL = M/S = SC0 = SC1 = 3V to 5.5V; GND = AGND = DGND = PGNDx = ISHx = ISHCOM = ISHEN = ISHREFx = ISHSL = TDI = TDO = TPGM = 0V; FB = 0.65V; PORSEL = V_{IN} for 4.5V ≤ V_{IN} ≤ 5.5V and GND for V_{IN} < 4.5V; LXx = SYNC = Open Circuit; OCx is connected to OCSSx with a 10kΩ resistor; OCx is connected to GND with a 4.99kΩ resistor shunted by a 6.8nF capacitor; PGOOD is pulled up to V_{IN} with a 1kΩ resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; T_A = T_J = -55°C to +125°C; Post 100krad(Si) (Note 12) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 16)	TYP (Note 15)	MAX (Note 16)	UNIT
CURENT SHARE					
Slave Load Current	Master load current = 12A, V_{IN} = 3.3V, V_{OUT} = 0.8V, SC1 = ISHSL = M/S = 0, SC0 = ISHEN = FSEL = 1, SYNC = 1MHz external, 500nH inductor (Notes 18, 19)	7	12	17	A
	Master load current = 12A, V_{IN} = 3.3V, V_{OUT} = 1.8V, SC0 = ISHSL= M/S = 0, SC1 = ISHEN = FSEL = 1, SYNC = 1MHz external, 500nH inductor (Notes 18, 19)	7	12	17	A
	Master load current = 12A, V_{IN} = 5.0V, V_{OUT} = 1.8V, SC0 = ISHSL = M/S = 0, SC1 = ISHEN = FSEL = 1, SYNC = 1MHz external, 500nH inductor (Notes 18, 19)	7	12	17	A
	Master load current = 12A, V_{IN} = 5.0V, V_{OUT} = 2.5V, ISHSL = M/S = 0, SC0 = SC1 = ISHEN = FSEL = 1, SYNC = 1MHz external, 500nH inductor (Notes 18, 19)	7	12	17	A
ISHx, ISHREFx, Tri-State Leakage Current	V_{IN} = 5.5V, EN = GND	-1	0	1	µA
Master ISHCOM Pull-Up Resistance	ISHCOM = -50µA	6.5	10	13	kΩ
Slave ISHCOM Input Leakage Current	V_{IN} = ISHSL = 5.5V	-1		1	µA
Slave ISHCOM Pull-Down Resistance	ISHSL = V_{IN}, EN = GND, ISHCOM = 7.2mA	35	75	125	Ω
Slave ISHCOM Input High Voltage	ISHSL = V_{IN}	42	52	62	% of V_{IN}
Slave ISHCOM Input Low Voltage	ISHSL = V_{IN}	26	36	46	% of V_{IN}
Slave ISHCOM Input Voltage Hysteresis	ISHSL = V_{IN}	7	16	24	% of V_{IN}
ISHSL Input Leakage Current		-1		1	µA
ISHSL Input High Voltage		V_{IN} - 0.5	1.3		V
ISHSL Input Low Voltage			1.2	0.5	V
SLOPE COMPENSATION					
	SC1 = SC0 = V_{IN}	5.9	13.4	17.7	A/µs
	SC1 = V_{IN}, SC0 = GND	3.0	6.7	8.8	A/µs
	SC1 = GND, SC0 = V_{IN}	1.5	3.4	4.5	A/µs
	SC1 = SC0 = GND	0.7	1.7	2.2	A/µs
	FSEL = GND, SC1 = SC0 = V_{IN}	2.9	6.6	8.8	A/µs
	FSEL = GND, SC1 = V_{IN}, SC0 = GND	1.4	3.3	4.5	A/µs
	FSEL = GND, SC1 = GND, SC0 = V_{IN}	0.7	1.6	2.2	A/µs
	FSEL = GND, SC1 = SC0 = GND	0.3	0.8	1.2	A/µs

NOTES:

15. Typical values shown reflect T_A = T_J = +25°C operation and are not guaranteed.
16. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C and +125°C, unless otherwise specified.
17. Limits do not include tolerance of external feedback resistors. The 0A to 12A output current range can be reduced by Minimum LXx On-time and Minimum LXx Off-time specifications.
18. Limits established by characterization or analysis and are not production tested.
19. Tested sequentially on LX2, LX6 and LX9.
20. Tested sequentially on LX2 and LX6 at 535mA to 735mA and 2.3A to 2.6A.
21. Tested in accordance with MIL-STD-883, method 1019, condition A.

Typical Performance Curves

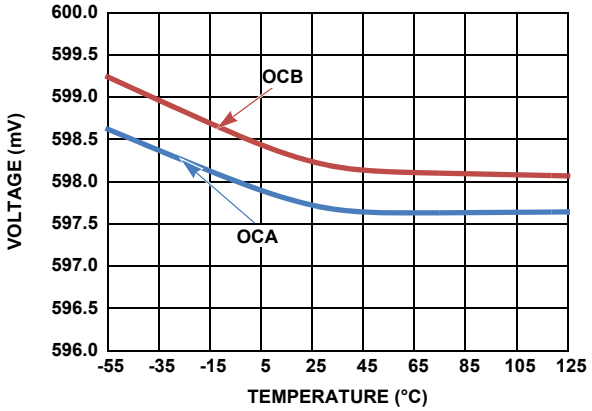


FIGURE 6. OVERCURRENT REFERENCE VOLTAGE

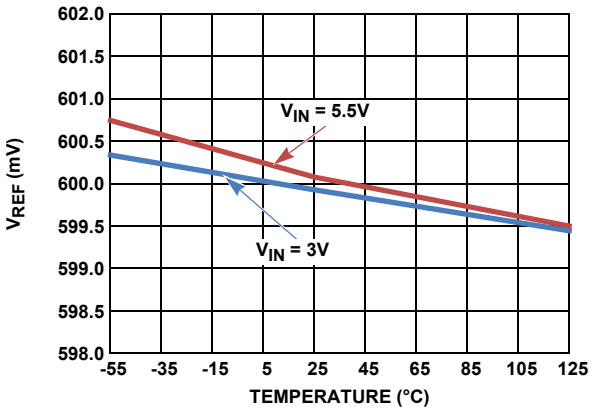


FIGURE 7. REF VOLTAGE vs V_{IN}

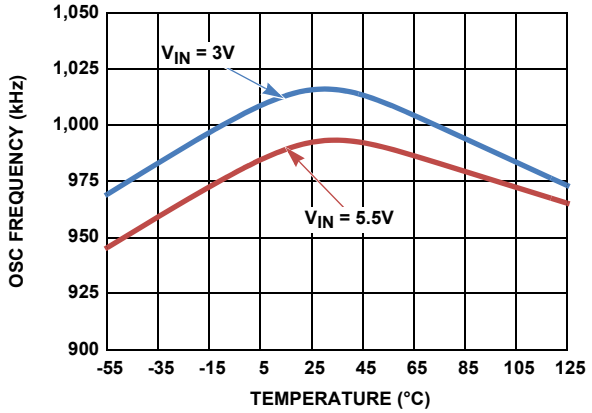


FIGURE 8. OSC FREQUENCY vs V_{IN}

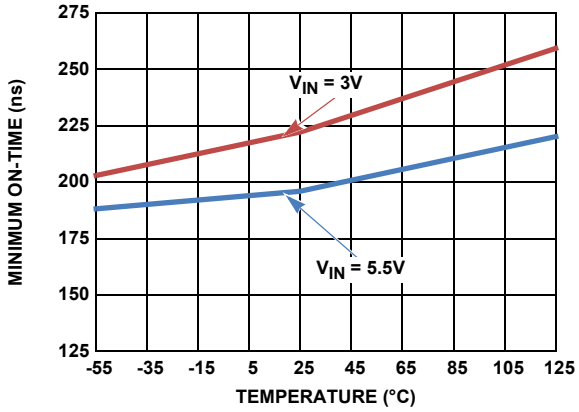


FIGURE 9. LXx MINIMUM ON-TIME vs V_{IN}

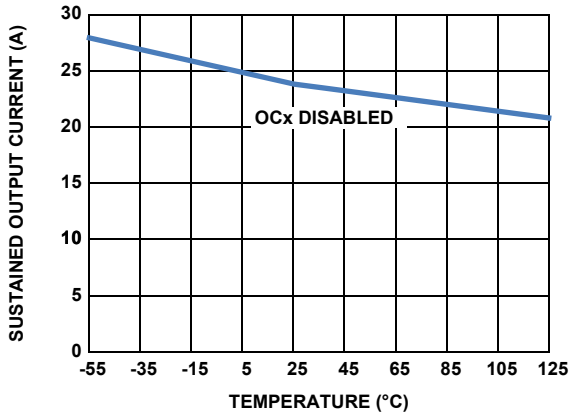


FIGURE 10. SUSTAINED OUTPUT CURRENT WITH OVERCURRENT DISABLED

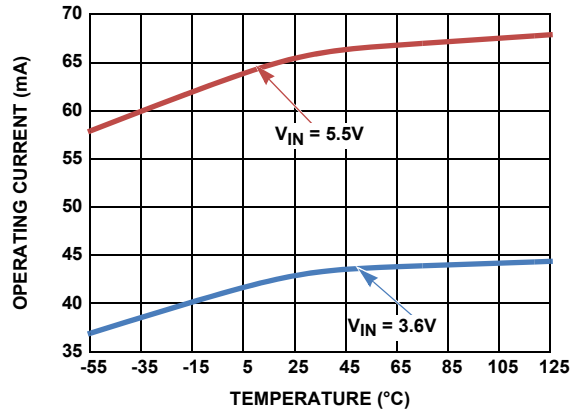


FIGURE 11. OPERATING CURRENT vs V_{IN}

Typical Performance Curves (Continued)

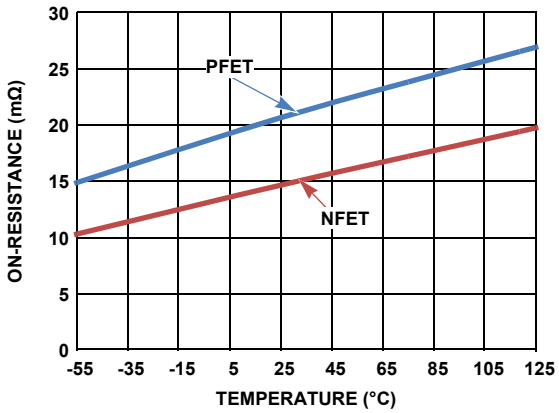


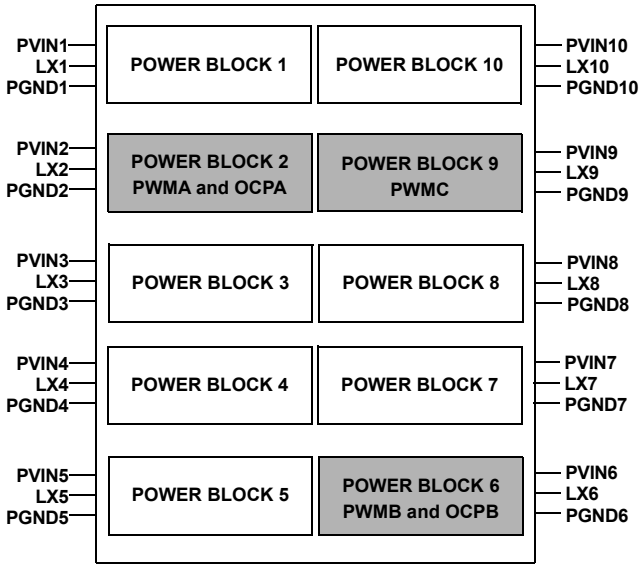
FIGURE 12. LX ON-RESISTANCE, ALL POWER BLOCKS IN PARALLEL, V_{IN} = 3V

Functional Description

The ISL7x002SEH is a monolithic, fixed frequency, current-mode synchronous buck regulator. Two ISL7x002SEH devices can be used to provide a total DC/DC solution for FPGAs, CPLDs, DSPs, and CPUs.

Power Blocks

The power output stage of the regulator consists of ten power blocks that are paralleled to provide up to 18A (22A with an external Schottky diode clamp) output current capability. The block diagram in Figure 13 shows a top level view of the individual power blocks.



Note: Shaded blocks indicate pilot current and overcurrent sensors.

FIGURE 13. POWER BLOCK DIAGRAM

Each power block has a power supply input pin (PVINx), a phase output pin (LXx), and a power supply ground pin (PGNDx). All PVINx pins must be connected to a common power supply rail, and all PGNDx pins must be connected to a common ground. LXx pins should be connected to the output inductor based on the required load current, but must include the LX2, LX6, and LX9 pins. Power Blocks 2, 6, and 9 together comprise a triple redundant with majority voter configuration for the PWM control. This is included to prevent PWM control signal upsets for the internal drive circuitry in the event of SEE ion strikes. In particular applications where all LX pins are not used, LX2, LX6, and LX9 pins must be used without exception. The unused LXx pins should be left unconnected. Connecting all ten LXx pins to the output inductor provides a maximum 12A of output current at +150°C die temperature. See the "Typical Application Schematic" on page 2 for pin connection guidance.

Power Blocks 2 and 6 contain the master pilot current sensing devices, which provide current feedback. These power blocks must be connected to the output inductor. The Overcurrent Protection (OCP) is a redundant AND function of both pilot devices. This redundancy is to avoid a false OC upon an ion strike in the OCP circuitry.

Maximum Current Operation

SINGLE PHASE

The ISL7x002SEH can provide up to 22A of current if specific conditions are met.

If only 12A is needed, PVIN can be as high as 6.2V and the junction temperature may be as high as 150C. For up to 14A operation, PVIN can still be up to 6.2V, but the part must be cooled so the junction temperature does not exceed 125C.

For 14A to 18A operation, maintain a maximum PVIN of 5.5V, and a junction temperature of 125C. 18A to 22A load current can only be supported with the addition of an external Schottky diode clamp. See "Schottky Diode Clamp and RC Snubber" for clamp size and implementation instructions. For additional information about safe operation above 12A, see TB515 section 4 *Extended Output Current Usage Constraints*.

DUAL PHASE

When current sharing two devices, the limits are less than double because of a 27% worse-case current sharing mismatch. 20A can be supplied with a PVIN up to 6.2V and a 150C junction temperature. Cooling the parts' junctions to 125C increases that limit to 24A.

Reducing PVIN to 5.5V and cooling the parts to 125C allows a combined 31A from two devices. The addition of an external Schottky clamp increases that to 38A.

Main Control Loop

During normal operation, the internal top power switch is turned on at the beginning of each clock cycle. Current in the output inductor ramps up until the current comparator trips and turns off the top power MOSFET. Next, the bottom power MOSFET turns on, and the inductor current ramps down for the rest of the cycle.

The current comparator compares the output current at the ripple current peak to the scaled current pilot. The error amplifier monitors V_{OUT} and compares it with an internal reference voltage. The output voltage of the error amplifier creates a proportional current to the pilot. If V_{OUT} is low, both the current level of the pilot is increased and the trip off current level of the output is increased. The increased output current raises V_{OUT} until it is in agreement with the reference voltage.Output Voltage Selection

The output voltage of the ISL7x002SEH can be adjusted using an external resistor divider as shown in Figure 14. RT should be set to 1kΩ to mitigate SEE. RT should be shunted by a 4.7nF ceramic capacitor, CC, to mitigate SEE and to improve loop stability margins. The REF pin should be bypassed to AGND with a 220nF ceramic capacitor to mitigate SEE. Note that no current (sourcing or sinking) is available from the REF pin.

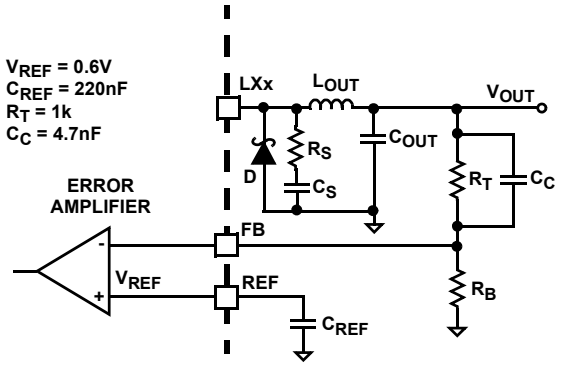


FIGURE 14. OUTPUT VOLTAGE SELECTION

R_B can be determined from Equation 3. You can configure the output voltage from 0.8V to 85% of the input voltage.

$$R_B = R_T \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}} \quad \text{(EQ. 3)}$$

The minimum on-time determines the lowest output voltage, so when V_{IN} = 5.5V and the switching frequency is 500kHz this parameter limits the regulated output voltage to about 0.8V or greater. It increases at the 1MHz switching frequency to about 1.6V or greater. The minimum on-time increases by about 9% at V_{IN} = 3V, but the 500kHz output voltage is not limited by the minimum on-time and the 1MHz minimum V_{OUT} is approximately 0.9V.

Switching Frequency/Synchronization

The ISL7x002SEH features an internal oscillator running at a fixed frequency of either 500kHz or 1MHz ±15% over recommended operating conditions. When the FSEL pin is grounded, the oscillator operates at 500kHz, and if FSEL is connected to DVDD, it operates at 1MHz.

The regulator can be configured to run from the internal oscillator, can be synchronized to another ISL7x002SEH, or can be synchronized to an SEE hardened external clock with a frequency range of 500kHz to 1MHz (±20%).

To run the regulator from the internal oscillator, connect the M/S pin to DVDD. In this case, the output of the internal oscillator appears on the SYNC pin. To synchronize two regulators to the SYNC output of an SEE hardened external clock (or to another ISL7x002SEH regulator, see "Synchronized 2-Phase Operation"), connect the M/S pin to DGND. In this case, the SYNC pin is an input that accepts an external synchronizing signal. When M/S is connected to DGND, the ISL7x002SEH is synchronized 180° out-of-phase with respect to the SYNC input of the external clock. Ideally, two or more regulators operating with individual SYNC inputs should be operated out-of-phase and balanced to reduce input current ripple and to increase the effective switching frequency.

When using an ISL7x002SEH in Slave mode and applying an external clock to SYNC (whether from a master ISL7x002SEH or another external clock), it is imperative that all slave ISL7x002SEH's using that external clock signal have their switching disabled through the EN input prior to any stoppage of the clock on the SYNC input. If the external clock signal on the SYNC pin stops or is otherwise removed while the slave ISL7x002SEH is enabled, the internal lower FET turns on and remains on as the ISL7x002SEH control circuit waits for the next rising edge of the external clock that never arrives, as shown in Figure 15. Current from the load then recirculates through the stuck-on lower FET. Figure 15 shows the SYNC stopping at a low level. If the SYNC stops at a level greater than the SYNC voltage threshold (Vth), and then decreases through the SYNC Vth, there is a solitary LX pulse.

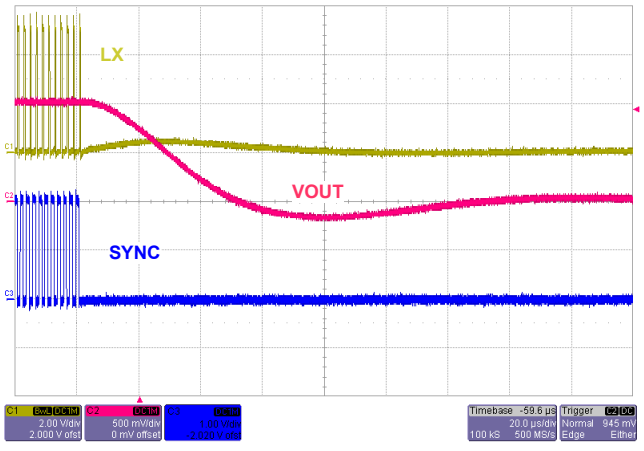


FIGURE 15. SYNC LOSS SHOWING LX PULLED LOW

Synchronized 2-Phase Operation

The ISL7x002SEH can operate two ICs as a single 2-phase regulator with nearly twice the load current capacity. In 2-phase operation mode, a redundant current sharing bus balances the load current between the two devices and communicates any fault conditions. One ISL7x002SEH is designated the master and the other the slave. The master ISHSL pin is connected to DGND and the slave ISHSL pin is connected to DVDD. The ISHEN pins on both master and slave are connected to DVDD. The SYNC, ISHA, ISHB, ISHC, ISHREFA, ISHREFB, ISHREFC, ISHCOM, and FB pins are connected from the master to the slave and the REF pins are tied with a 10Ω resistor. When configured this way, the two-phase regulator nearly doubles the load current capacity, limited only by the current share match tolerance.

In this master/slave configuration, the ISL7x002SEH ICs operate 180° out-of-phase to minimize the input ripple current, effectively operating as a single IC at twice the switching frequency. The master phase uses the falling edge of the SYNC clock to initiate the master switching cycle with the nonoverlap period before the rising edge of LX, while the slave phase internally inverts the SYNC input and uses the falling edge of the inverted copy to start its switching cycle. This is independent of whether the master phase is configured for an external clock (master M/S = DGND) or its internal clock (master M/S = DVDD). The master error amplifier and compensation controls the two-phase regulator while the slave error amplifier is disabled. The schematic in Figure 4 on page 3 shows the complete connections for the master and slave.

Often an enable signal is not provided; instead the PVIN enables the ISL7x002SEH function. In a 2-phase configuration with PVIN = 5V, a method to ensure that slave switching is appropriately enabled and disabled relative to the master switching is to set the clock slave ISL7x002SEH PORSEL high and clock master ISL7x002SEH PORSEL low. As the PVIN voltage is ramped up, the master device is active and producing a clock out to the SYNC input of the slave device before the slave device becomes active. As the PVIN ramps down, the slave device's switching turns off at the higher PORSEL threshold prior to the master device. This method can also be used in a dual single phase application, where the clock master ISL7x002SEH is providing an out-of-phase SYNC signal to the clock slave ISL7x002SEH but not current sharing. This method cannot be used in PVIN = 3.3V applications. Figure 16 illustrates the LX activity with a rising and falling PVIN with PORSEL = 1, which shows the initiation of LX switching activity at PVIN ~ 4.3V and stopping within 5µs of falling below the PORSEL falling threshold at ~4.0V. This is the expected behavior for PVIN droop times >1ms.

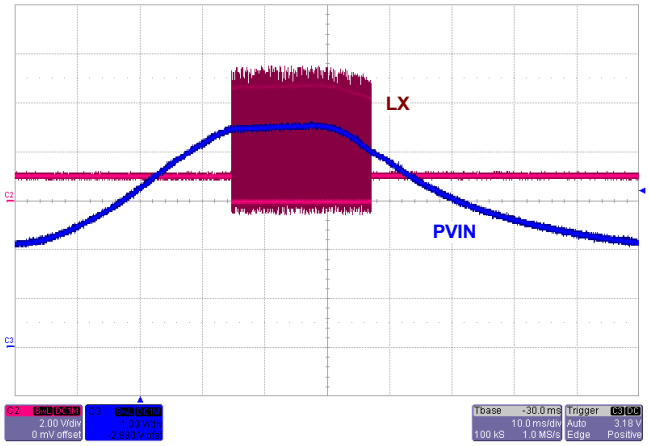


FIGURE 16. PORSEL = 1 PVIN RAMPING AND SYNC ACTIVITY

For PVIN = 3.3V applications, a method must be employed to prevent the lower FET from being left indefinitely in an on state to ensure the slave IC is disabled before the master IC SYNC output is halted by either a falling PVIN or a common disabling signal. In applications where the EN input pin is tied to the PVIN, adding a resistor divider on the slave EN to enable <3V, but greater than the PORSEL maximum of 2.95V is advised. This would ensure that the slave IC is enabled before PVIN = 3V on a rising PVIN and disabled prior to the master entering the POR shutdown on a falling PVIN. As the falling PVIN decreases to the slave enable falling threshold the slave device is disabled prior to the master device being disabled (see Figure 17). Notice the slave LX is tri-stated unlike in Figure 15 on page 15. If a common enable signal is used, the resistor divider on the slave IC ensures a turn-on after and a turn-off before the master IC; thus, preserving the SYNC signal integrity to the slave device and preventing the lower FET stuck in a latched on condition.

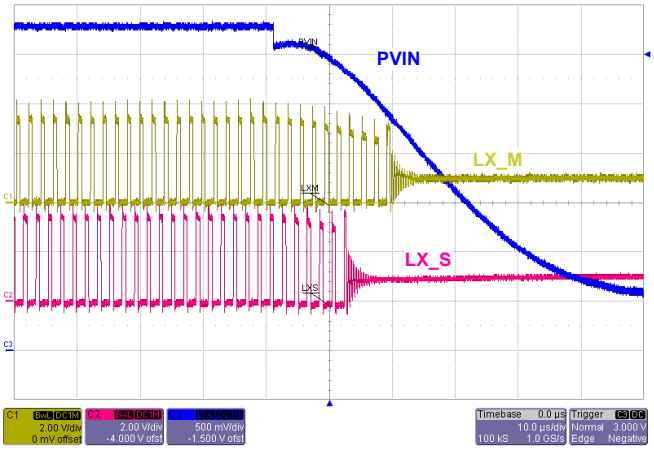


FIGURE 17. FALLING PVIN to M/S DISABLE

Operation Initialization

The ISL7x002SEH initializes based on the state of the Power-On Reset (POR) monitor of the PVINx inputs and the state of the EN input. Successful initialization prompts a soft-start interval and the regulator begins slowly ramping the output voltage. When the commanded output voltage is within the proper window of

operation, the power-good signal changes state from low-to-high, indicating proper regulator operation.

Power-On Reset

The POR circuitry prevents the controller from attempting to soft-start before sufficient bias is present at the PVINx pins.

The POR threshold of the PVINx pins is controlled by the PORSEL pin. For a nominal 5V supply voltage, PORSEL should be connected to the DVDD. For a nominal 3.3V supply voltage, PORSEL should be connected to DGND. For nominal supply voltages between 5V and 3.3V, PORSEL should be connected to DGND. The POR rising and falling thresholds are shown in the "Electrical Specifications" table on page 11.

Hysteresis between the rising and falling thresholds ensures that small perturbations on PVINx seen during regulator turn-on/turn-off do not cause the regulator to inadvertently turn off or turn on. When the PVINx pins are below the POR rising threshold, the internal synchronous power MOSFET switches are turned off, and the LXx pins are held in a high-impedance state.

Enable and Disable

After the POR input requirement is met, the ISL7x002SEH remains in shutdown until the voltage at the enable input rises above the enable threshold. Figure 18 on page 17 shows that the enable circuit features a comparator type input. In addition to simple logic on/off control, the enable circuit allows the level of an external voltage to precisely gate the turn-on/turn-off of the regulator. An internal I_{EN} current sink with a typical value of 11µA is active only when the voltage on the EN pin is below the enable threshold. The current sink pulls the EN pin low. As $V_{CONTROL}$ rises, the enable level is not set exclusively by the resistor divider from $V_{CONTROL}$. With the current sink active, the enable level is defined by Equation 4. R_1 is the resistor from the EN pin to $V_{CONTROL}$ and R_2 is the resistor from the EN pin to the AGND pin.

$$V_{ENABLE} = V_{REF} \cdot \left[1 + \frac{R_1}{R_2}\right] + I_{EN} \cdot R_1 \quad \text{(EQ. 4)}$$

When the voltage at the EN pin reaches the enable threshold, the I_{EN} current sink turns off.

With the part enabled and the I_{EN} current sink off, the disable level is set by the resistor divider. The disable level is defined by Equation 5.

$$V_{DISABLE} = V_{REF} \cdot \left[1 + \frac{R_1}{R_2}\right] \quad \text{(EQ. 5)}$$

The difference between the enable and disable levels provides adjustable hysteresis so that noise on $V_{CONTROL}$ does not interfere with the enabling or disabling of the regulator.

Bypass the EN pin to the AGND pin with a 10nF ceramic capacitor to mitigate SEE.

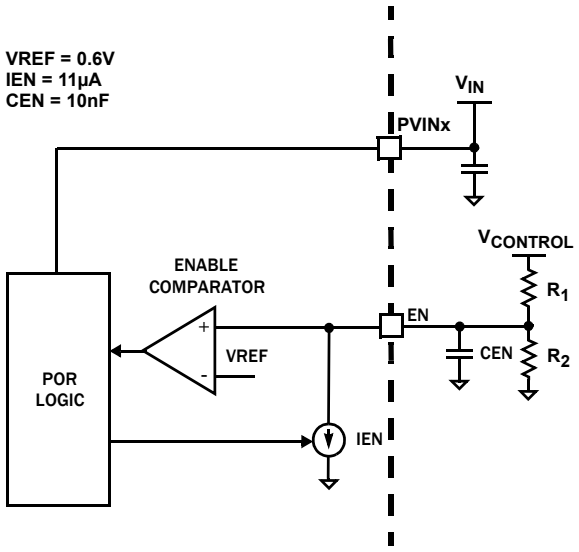


FIGURE 18. ENABLE CIRCUIT

Soft Start

When the POR and enable circuit requirements are met, the regulator initiates a soft-start. Figure 19 shows that the soft-start circuit clamps the error amplifier reference voltage to the voltage on an external soft-start capacitor connected to the SS pin. The soft-start capacitor is charged by an internal I_{SS} current source (23µA typical). As the soft-start capacitor is charged, the output voltage slowly ramps to the set point determined by the reference voltage and the feedback network. When the voltage on the SS pin is equal to the internal reference voltage (600mV), the soft-start interval is complete though the SS pin voltage continues to rise to approximately 1.4V. PGOOD is enabled after SS reaches 1.4V. The controlled ramp of the output voltage reduces the inrush current during start-up. The soft-start output ramp interval is defined in Equation 6 and is adjustable from approximately 2ms to 200ms. The value of the soft-start capacitor (C_{SS}) should range from 82nF to 8.2µF, inclusive. The peak inrush current can be calculated from Equation 7. The soft-start interval should be selected long enough to ensure that the peak inrush current plus the peak output load current does not exceed the SS overcurrent trip level of the regulator.

$$t_{SS} = C_{SS} \cdot \frac{V_{REF}}{I_{SS}} \quad \text{(EQ. 6)}$$

$$I_{INRUSH} = C_{OUT} \cdot \frac{V_{OUT}}{t_{SS}} \quad \text{(EQ. 7)}$$

The soft-start capacitor is immediately discharged by a 2.2Ω resistor whenever POR conditions are not met or EN is pulled low. The soft-start discharge time is equal to 256 clock cycles.

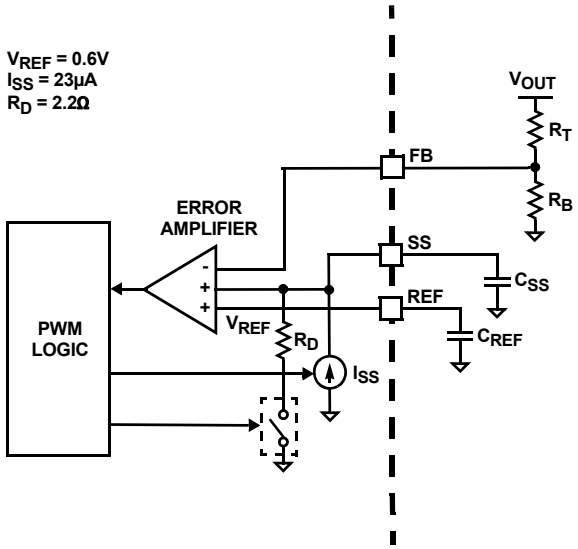


FIGURE 19. SOFT-START CIRCUIT

Power-Good

The power-good (PGOOD) pin is an open-drain logic output that indicates when the output voltage of the regulator is within regulation limits. The PGOOD pin pulls low during shutdown and remains low when the controller is enabled. After a successful soft-start, the PGOOD pin releases and the voltage rises with an external pull-up resistor. The power-good signal transitions low immediately when the EN pin is pulled low.

The power-good circuitry monitors the FB pin and compares it to the rising and falling thresholds shown in the “Electrical Specifications” table on page 11. If the feedback voltage exceeds the typical rising limit of 111% of the reference voltage, the PGOOD pin pulls low. The PGOOD pin continues to pull low until the feedback voltage falls to a typical of 107.5% of the reference voltage. If the feedback voltage drops below a typical of 89% of the reference voltage, the PGOOD pin pulls low. The PGOOD pin continues to pull low until the feedback voltage rises to a typical 92.5% of the reference voltage. The PGOOD pin then releases and signals the return of the output voltage within the power-good window.

The PGOOD pin can be pulled up to any voltage from 0V to 5.5V, independent of the supply voltage. The pull-up resistor should have a nominal value from 1kΩ to 10kΩ. The PGOOD pin is bypassed to DGND with a 10nF ceramic capacitor to mitigate SEE.

Slope Compensation

The SC0 and SC1 pins select four levels of current-mode slope compensation. In current-mode buck regulators, when the duty cycle approaches and exceeds 50%, the regulator operates in sub-harmonic oscillation without slope compensation. Slope compensation is widely considered unnecessary if the duty cycle is held below 40% and provides better phase margin. Transient duty cycles must be taken into consideration when selecting the level of slope compensation. Table 1 describes the amount of effective current that is added the output power stage signal that is used in the PWM modulator.

TABLE 1. SLOPE COMPENSATION

FSEL	SC1	SC0	SLOPE COMPENSATION (A/µs)
DGND	DGND	DGND	0.8
DGND	DGND	DVDD	1.6
DGND	DVDD	DGND	3.3
DGND	DVDD	DVDD	6.6
DVDD	DGND	DGND	1.7
DVDD	DGND	DVDD	3.4
DVDD	DVDD	DGND	6.7
DVDD	DVDD	DVDD	13.4

Fault Monitoring and Protection

The ISL7x002SEH actively monitors output voltage and current to detect fault conditions. Fault conditions trigger protective measures to prevent damage to the regulator and external load device.

Undervoltage Protection

A hysteretic comparator monitors the FB pin of the regulator. The feedback voltage is compared to an undervoltage threshold that is a fixed percentage of the reference voltage. When the comparator trips on two consecutive switching cycles, indicating a valid undervoltage condition, the undervoltage protection logic shuts down the regulator. If the feedback voltage rises back above the undervoltage threshold plus a specified amount of hysteresis (outlined in the “Electrical Specifications” table on page 11) after the first detection and before the second, normal operation continues.

After the regulator shuts down, it enters a delay interval, equivalent to the selected soft-start interval. The undervoltage counter is reset entering the delay interval. The protection logic initiates a normal soft-start when the delay interval ends. If the output successfully soft-starts, the power-good signal goes high and normal operation continues. If undervoltage conditions continue to exist during the soft-start interval, the undervoltage counter must overflow before the regulator shuts down again. This hiccup mode continues indefinitely until the output soft-starts successfully.

Overcurrent Protection

Pilot devices integrated into the PMOS transistor of power block 2 and power block 6 sample the inductor current of each cycle. This current feedback is scaled and compared to an overcurrent (OC) threshold based on the overcurrent resistor connected from OCx to AGND. The Overcurrent Protection (OCP) is a redundant AND function of both pilot devices. This redundancy is to avoid a false OC upon an ion strike in the OCP circuitry.

If the sampled current exceeds the overcurrent threshold, an overcurrent counter increments. If the sampled current falls below

the threshold before the counter overflows, the counter is reset. When the overcurrent counter reaches 2, the regulator shuts down.

After the regulator shuts down, it enters a delay interval equivalent to the soft-start interval, which allows the device to cool. The overcurrent counter is reset entering the delay interval. The protection logic initiates a normal soft-start when the delay interval ends. If the output successfully soft-starts, the power-good signal goes high and normal operation continues. If overcurrent conditions continue to exist during the soft-start interval, the overcurrent counter must overflow before the regulator shut downs the output again. This hiccup mode continues indefinitely until the output soft-starts successfully.

Component Selection Guide

This design guide provides a high-level explanation of the steps necessary to create a power converter. It is assumed the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Renesas provides an evaluation board, schematic, Bill of Materials (BOM), and an example PCB layout.

Output Filter Design

The output inductor and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase node. The filter must also provide the transient energy until the regulator can respond. Because the filter has low bandwidth relative to the switching frequency, it limits the system transient response. The output capacitors must supply or sink current while the current in the output inductor increases or decreases to meet the load demand.

OUTPUT CAPACITOR SELECTION

The critical load parameters in choosing the output capacitors are the maximum size of the load step (ΔI_{STEP}), the load-current slew rate (di/dt), and the maximum allowable output voltage deviation under transient loading (ΔV_{MAX}). Capacitors are characterized according to their capacitance, ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance).

At the beginning of a load transient, the output capacitors supply all of the transient current. The output voltage initially deviates by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by an amount shown in Equation 8.

$$\Delta V_{MAX} \approx \left[ESL \times \frac{di}{dt}\right] + [ESR \times \Delta I_{STEP}] \quad \text{(EQ. 8)}$$

The filter capacitors selected must have sufficiently low ESL and ESR so that the total output voltage deviation is less than the maximum allowable ripple.

Most capacitor solutions rely on a mixture of high frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but larger ESR. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

Ceramic capacitors with an X7R dielectric are recommended. Alternately, a combination of low ESR solid tantalum capacitors and ceramic capacitors with an X7R dielectric can be used.

The ESR of the bulk capacitors is responsible for most of the output voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current, a voltage, $V_{P-P(MAX)}$, develops across the bulk capacitor according to Equation 9.

$$V_{P-P(MAX)} = ESR \times \left[\frac{(V_{IN} - V_{OUT})V_{OUT}}{L_{OUT} \times f_s \times V_{IN}}\right] \quad \text{(EQ. 9)}$$

OUTPUT INDUCTOR SELECTION

When the output capacitors are selected, the maximum allowable ripple voltage, $V_{P-P(MAX)}$, determines the lower limit on the inductance as shown in Equation 10.

$$L_{OUT} \geq ESR \times \left[\frac{(V_{IN} - V_{OUT})V_{OUT}}{f_s \times V_{IN} \times V_{P-P(MAX)}}\right] \quad \text{(EQ. 10)}$$

Because the output capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductor must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 11 gives the upper limit on output inductance for the case when the trailing edge of the current transient causes the greater output voltage deviation than the leading edge.

$$L_{OUT} \leq \frac{2 \cdot C_{OUT} \cdot V_{OUT}}{(\Delta I_{STEP})^2}\left[\Delta V_{MAX} - (\Delta I_{L(P-P)} \cdot ESR)\right] \quad \text{(EQ. 11)}$$

Equation 12 addresses the leading edge. Normally, the trailing edge controls the inductance selection because duty cycles are usually <50%. However, both inequalities should be evaluated, and inductance should be governed based on the lower of the two results. In each equation, L_{OUT} is the output inductance, C_{OUT} is the total output capacitance, and $\Delta I_{L(P-P)}$ is the peak-to-peak ripple current in the output inductor.

$$L_{OUT} \leq \frac{2 \cdot C_{OUT}}{(\Delta I_{STEP})^2}\left[\Delta V_{MAX} - (\Delta I_{L(P-P)} \cdot ESR)\right]\left(V_{IN} - V_{OUT}\right) \quad \text{(EQ. 12)}$$

The other concern when selecting an output inductor is to ensure there is adequate slope compensation when the regulator is operated above 40% duty cycle. In most cases, the maximum slope compensation setting (SC1 = DVDD, SC0 = DVDD) provides sufficient phase margin, so this is the recommended configuration.

Input Capacitor Selection

Input capacitors are responsible for sourcing the AC component of the input current flowing into the switching power devices. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the switching power devices,

which is related to duty cycle. The maximum RMS current required by the regulator is closely approximated by Equation 13.

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}}} \sqrt{1 + \frac{1}{3} \times \left(\frac{V_{IN} - V_{OUT}}{I_{OUT} \times L_{OUT} \times f_s} \times \frac{V_{OUT}}{V_{IN}} \right)^2} \quad \text{(EQ. 13)}$$

The important parameters to consider when selecting an input capacitor are the voltage rating and the RMS ripple current rating. For reliable operation, select capacitors with voltage ratings at least 1.5 times greater than the maximum input voltage. The capacitor RMS ripple current rating should be higher than the largest RMS ripple current required by the circuit.

A combination of low ESR tantalum capacitors and ceramic capacitors with an X7R dielectric are recommended. The ISL7x002SEH requires a minimum effective input capacitance of 100µF for stable operation.

PCB Design

PCB design is critical to high-frequency switching regulator performance. Careful component placement and trace routing are necessary to reduce voltage spikes and minimize undesirable voltage drops. Select a suitable thermal interface material for optimum heat dissipation and to provide lead strain relief.

PCB Plane Allocation

Four layers of 2-oz. copper are recommended. Layer 2 should be a dedicated ground plane with all critical component ground connections made with vias to this layer. Layer 3 should be a dedicated power plane split between the input and output power rails. Layers 1 and 4 should be used primarily for signals, but can also provide additional power and ground islands as required.

PCB Component Placement

Place components as close as possible to the IC to minimize stray inductance and resistance. Prioritize the placement of bypass capacitors on the pins of the IC in the following order: REF, SS, AVDD, DVDD, PVINx (high frequency capacitors), EN, PGOOD, PVINx (bulk capacitors).

Locate the output voltage resistive divider as close as possible to the FB pin of the IC. Connect the top leg of the divider directly to the POL (Point of Load) and the bottom leg of the divider directly to AGND. Connect the junction of the resistive divider directly to the FB pin.

A small series RC snubber connected from the LXx pins to the PGNDx pins can be used to damp high frequency ringing on the LXx pins if desired.

PCB Layout

Use a small island of copper to connect the LXx pins of the IC to the output inductor on layers 1 and 4. To minimize capacitive coupling to the power and ground planes, void the copper on layers 2 and 3 adjacent to the island. Place most of the island of layer 4 to minimize the amount of copper that must be voided from the ground plane (layer 2).

Keep all other signal traces as short as possible. For an example layout, see AN1732.

Schottky Diode Clamp and RC Snubber

Implement the Schottky diode clamp at the LX node to GND as close as possible to the IC when output current is 18A or greater per phase. A diode rated for an average forward current of 3A at the maximum operating temperature is adequate.

The diode shunts current at the switching transient edges to reduce the Si die temperature approximately 22% more at an output current level of 18A than without the diode in place. It is imperative to implement adequate thermal relief in the hardware design, as the Si temp is ~135°C at an output current level of 24A with the diode clamp in place at a room ambient.

A small series RC snubber connected from the LXx pins to the PGNDx pins can be used to damp high-frequency ringing on the LXx pins. See Figure 14 on page 15.

Thermal Management for Ceramic Package

For optimum thermal performance, place a pattern of vias on the top layer of the PCB directly underneath the IC. Connect the vias to the plane that serves as a heat spreader. To ensure good thermal contact, use thermal interface material such as a Sil-Pad or thermally conductive epoxy to fill the gap between the vias and the bottom of the IC of the ceramic package.

Lead Strain Relief

Because the package leads protrude from the bottom of the package, the leads need forming to provide strain relief. On the ceramic bottom package R64.A, the Sil-pad or epoxy can be used to fill the gap left between the PCB board and the bottom of the package when lead forming is completed. On the heat spreader option of the package R64.C, the formed leads should be flush.

Heat Spreader Mounting Guidelines

The R64.C package option has a heat spreader mounted on the underside of the package. Use the following JESD-51x series guidelines to mount the package:

- Place a thermal land on the PCB under the heat spreader.
- The land should be approximately the same size as to 1mm larger than the 10.16x10.16mm heat spreader.
- Place an array of thermal vias below the thermal land.
  - Via array size: ~9x9 = 81 thermal vias.
  - Via diameter: ~0.3mm drill diameter with plated copper on the inside of each via.
  - Via pitch: ~1.2mm.
  - Vias should drop to and contact as much buried metal area as feasible to provide the best thermal relief.

Heat Spreader Electrical Potential

The heat spreader is connected to Pin 50 within the package; therefore, the PCB design and potential applied to Pin 50 define the heat spreader potential. If unconnected, the heat spreader is a floating node.

Heat Spreader Mounting Materials

When using electrically conductive mounting methods (conductive epoxy, solder, etc) the thermal land, vias, and connected plane(s) below must be the same potential as Pin 50.

When using electrically nonconductive mounting methods (nonconductive epoxy), the heat spreader and Pin 50 can have a different electrical potential than the thermal land, vias, and connected plane(s) shown in the following layout.

Weight Characteristics

Weight of Packaged Device

1.43g typical - R64.A Package

2.65g typical - R64.C Package

Die Characteristics

Die Dimensions

8300µmx8300µm (327 mils x 327 mils)
Thickness: 300µm ±25.4µm (12 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Silicon oxide and Silicon nitride
Thickness: 0.3µm ±0.03µm and 1.2µm ±0.12µm

TOP METALLIZATION

Type: AlCu (0.5%)
Thickness: 2.7µm ±0.4µm

SUBSTRATE

Type: Silicon
Isolation: Junction

BACKSIDE FINISH

Silicon

ASSEMBLY RELATED INFORMATION

Substrate and Metal Lid Potential

PGND

Heat Spreader Potential R64.C Package

Connected to Pin 50, electrically isolated

ADDITIONAL INFORMATION

Worst Case Current Density

$< 2 \times 10^5$ A/cm^2

Transistor Count

28,160

Layout Characteristics

Step and Repeat

8300µmx8300µm

Metallization Mask Layout

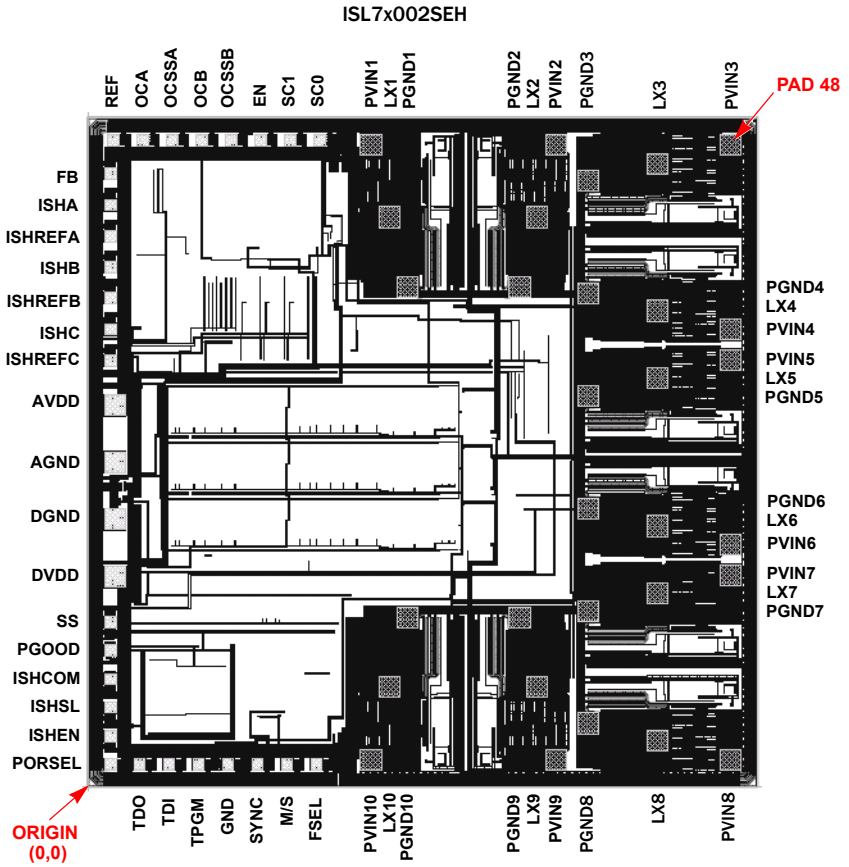


TABLE 2. LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES SIZE (0.001")
FB	1	275	7497	135	135	1.5
ISHA	2	275	7117	135	135	1.5
ISHREFA	3	275	6737	135	135	1.5
ISHB	4	275	6357	135	135	1.5
ISHREFB	5	275	5977	135	135	1.5
ISHC	6	275	5597	135	135	1.5
ISHREFC	7	275	5217	135	135	1.5
AVDD	8	335	4672	254	254	3
AGND	9	335	3972	254	254	3
DGND	10	335	3272	254	254	3
DVDD	11	335	2572	254	254	3
SS	12	275	2021	135	134	1.5
PGOOD	13	275	1671	135	135	1.5
ISHCOM	14	275	1321	135	135	1.5

TABLE 2. LAYOUT X-Y COORDINATES (Continued)

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES SIZE (0.001")
ISHSL	15	275	971	135	135	1.5
ISHEN	16	275	621	135	135	1.5
PORSEL	17	275	275	135	135	1.5
TDO	18	635	275	135	135	1.5
TDI	19	995	275	135	135	1.5
TPGM	20	1355	275	135	135	1.5
GND	21	1715	275	135	135	1.5
SYNC	22	2075	275	135	135	1.5
M/S	23	2435	275	135	135	1.5
FSEL	24	2795	275	135	135	1.5
PVIN10	25	3463	336	254	254	3
LX10	26	3693	1222	254	254	3
PGND10	27	3905	2074	254	254	3
PGND9	28	5281	2074	254	254	3
LX9	29	5494	1222	254	254	3
PVIN9	30	5723	336	254	254	3
PGND8	31	6115	778	254	254	3
LX8	32	6967	566	254	254	3
PVIN8	33	7853	336	254	254	3
PGND7	34	6115	2154	254	254	3
LX7	35	6967	2366	254	254	3
PVIN7	36	7853	2596	254	254	3
PVIN6	37	7853	2965	254	254	3
LX6	38	6967	3195	254	254	3
PGND6	39	6115	3408	254	254	3
PGND5	40	6115	4784	254	254	3
LX5	41	6967	4996	254	254	3
PVIN5	42	7853	5226	254	254	3
PVIN4	43	7853	5595	254	254	3
LX4	44	6967	5825	254	254	3
PGND4	45	6115	6037	254	254	3
PGND3	46	6115	7413	254	254	3
LX3	47	6967	7625	254	254	3
PVIN3	48	7853	7855	254	254	3
PVIN2	49	5723	7855	254	254	3
LX2	50	5494	6969	254	254	3
PGND2	51	5281	6117	254	254	3
PGND1	52	3905	6117	254	254	3
LX1	53	3693	6969	254	254	3

TABLE 2. LAYOUT X-Y COORDINATES (Continued)

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES SIZE (0.001")
PVIN1	54	3463	7855	254	254	3
SC0	55	2836	7914	135	135	1.5
SC1	56	2476	7914	135	135	1.5
EN	57	2116	7914	135	135	1.5
OCSSB	58	1756	7914	135	135	1.5
OCB	59	1396	7914	135	135	1.5
OCSSA	60	1036	7914	135	135	1.5
OCA	61	676	7914	135	135	1.5
REF	62	316	7914	135	135	1.5

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Mar 31, 2022	12.01	Added ISL73002SEH information throughout the document.
Sep 10, 2021	12.00	Updated Title changed 18A to 22A. Updated 2nd Feature bullet. Updated supply voltage range feature bullet changed max value from 5.5V to 6.2V. Added Note 3 and updated Note 4. Added ILXx (TJ ≤+125°C) to the Recommended Operating Conditions section. Added Maximum Current Operation section.
Jun 11, 2019	11.00	Updated Figure 1. Updated Power Blocks section. Updated Synchronized 2-Phase Operation section. Updated Overcurrent Protection section.
Apr 5, 2019	10.00	Updated links throughout document. Updated Features section. Updated Figure 4 on page 3. Added last paragraph in the "Switching Frequency/Synchronization" and "Synchronized 2-Phase Operation" sections. Added Figure 15 in the "Switching Frequency/Synchronization" section. Updated Disclaimer
May 31, 2018	9.00	Applied new Header/Footer. Updated Related Literature section. Added ISL70002SEHDEMO1Z to Ordering Information Table on page 4 Added ESD ratings (Human Body Model, Charged Device Model, and Machine Model) to Absolute Maximum Ratings on page 10. Updated Figure 1 on page 2. Clarified the Maximum Output Current constraints and recommendations on page 1 and in the Absolute Maximum Ratings on page 10. Added test condition clarification for Output Sustained Current on page 11. Added Schottky Diode Clamp and Snubber section on page 20. Removed About Intersil section and updated disclaimer.
Oct 1, 2015	8.00	On page 20 in "Metallization Mask Layout", clarified pad labels for PVIN3, LX8, PGND3, PVIN8, LX8, PGND8. Corrected XY coordinates for PVIN3, PGND3, PVIN8, PGND8 in Table 2 on page 22.
Oct 9, 2014	7.00	On "EFFICIENCY 5V INPUT, 500kHz, Tcase = +25°C" on page 1: changed Figure 1 to reflect latest testing results. Pin descriptions on page 8: Clarified pin descriptions for pins 60 through 63. Figures 3 and 4 on pages 7 and 8 corrected pin numbers for PVINx, LXx AND PGNDx.
Jul 11, 2014	6.00	Absolute Maximum Ratings on page 9: updated Heading by adding "Ratings in a Heavy Ion Environment". Absolute Maximum Ratings on page 9: added: Absolute Maximum Ratings without Heavy Ions values to the table section.

Revision History

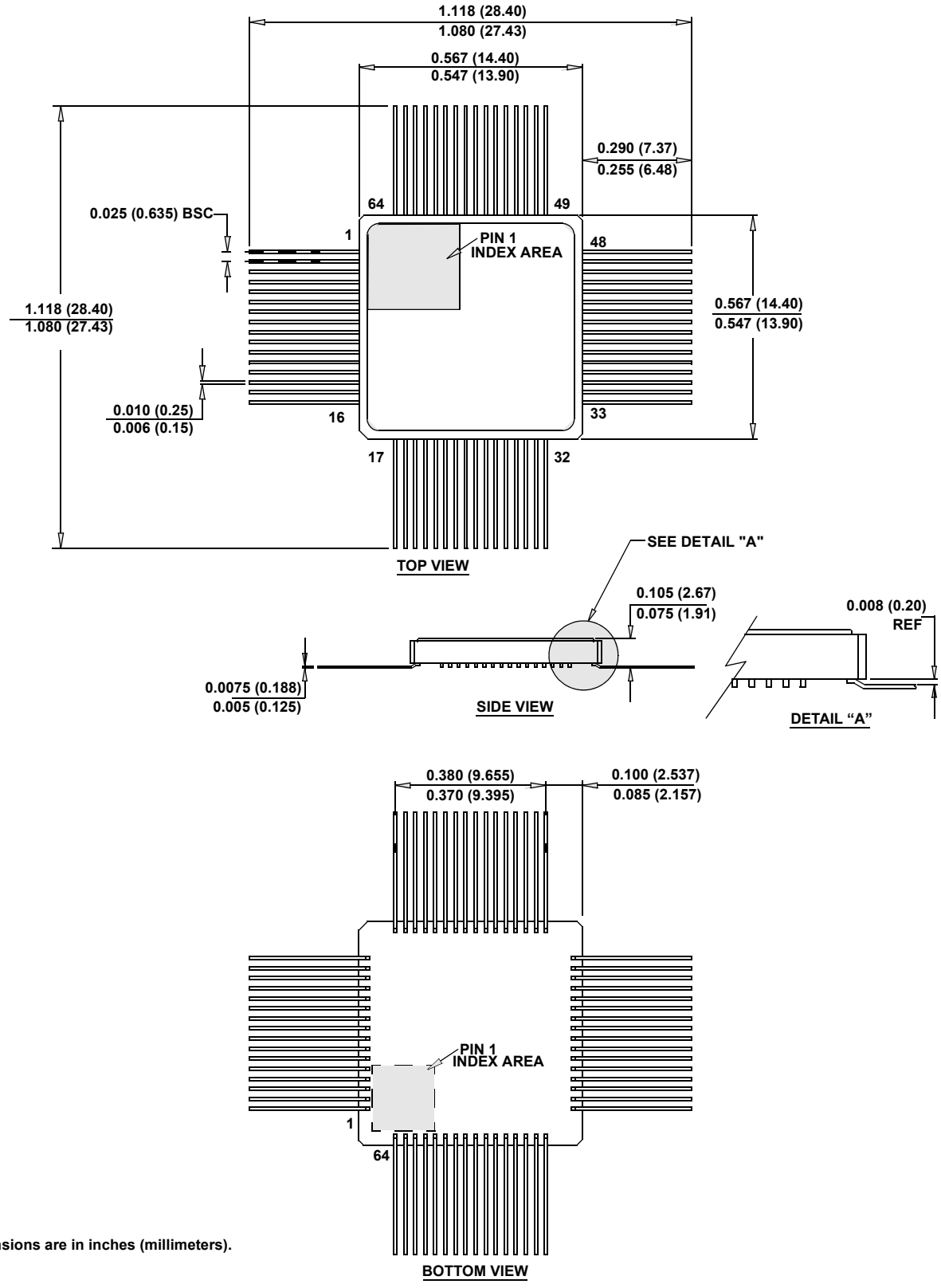
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision. **(Continued)**

DATE	REVISION	CHANGE
May 20, 2014	5.00	Page 1: Added Related Literature, Updated bullets under Features section as below: • From "12A output current for a single device (at TJ = +150°C)" to "Output current for a single device 14A at TJ = +125°C; 12A at TJ = +150°C" • From "• 14A output current for a single device (at TJ = +125°C) • 19A output current for two paralleled devices" to "Output current for two paralleled devices 22A at TJ = +125°C; 19A at TJ = +150°C"
Feb 11, 2014	4.00	On page 6 modified the pin configuration diagram to explicitly identify PIN 1. Updated POD R64.A from Rev 4 to Rev 5 to show larger corner chamfer in pin #16/17 corner. Updated POD R64.C from Rev 0 to Rev 1 to show larger corner chamfer in pin #16/17 corner. "Switching Frequency and Synchronization" on page 15 - Added text to third paragraph.
Jul 12, 2013	3.00	On page 6 modified the pin configuration, and changed note from indicates changes heat spreader package R64.C to indicates heat spreader package R64.C. On page 6 modified pin 50 description from: ..."the heat spreader to the power plane which offers the best thermal relief", to...."the heat spreader to a thermal plane". Made correction to Equations in pin description table on page 8 matching SMD for pins 60, 62 and 61, 63.
Jun 27, 2013	2.00	On page 1: Added bullet, "14A output current for a single device (at TJ = +125°C)" to Feature list. Ordering information table on page 5: Added new part number ISL70002SEHVFE and ISL70002SEHFE/PROTO. Thermal Information table on page 9: Added CQFP Package R64.C θ_{JA}17, θ_{JC}0.7. Ordering information table on page 5: Added R46.C package outline drawing. Added POD "R46.C" to datasheet.
Apr 5, 2012	1.00	Added the heat spreader package option to the ordering table. Also added mounting guidelines, electrical potential and mounting material sections to the datasheet. Figure 2 on page 1changed "Slave" to "Master" to CH1 and added "at 86.4MeV/mg/cm2" to Figure Title. "" on page 17 changed in 2nd to last sentence "...range from 8.2nF..." to "...range from 82nF..." "LAYOUT X-Y COORDINATES" on page 22 changed in Bond Wires column for "ISHB" from "1.51" to "1.5"
Mar 27, 2012	0.00	Initial Release

Package Outline Drawings

For the most recent package outline drawing, see R64.A.

R64.A
64 CERAMIC QUAD FLATPACK PACKAGE (CQFP)
Rev 5, 10/13

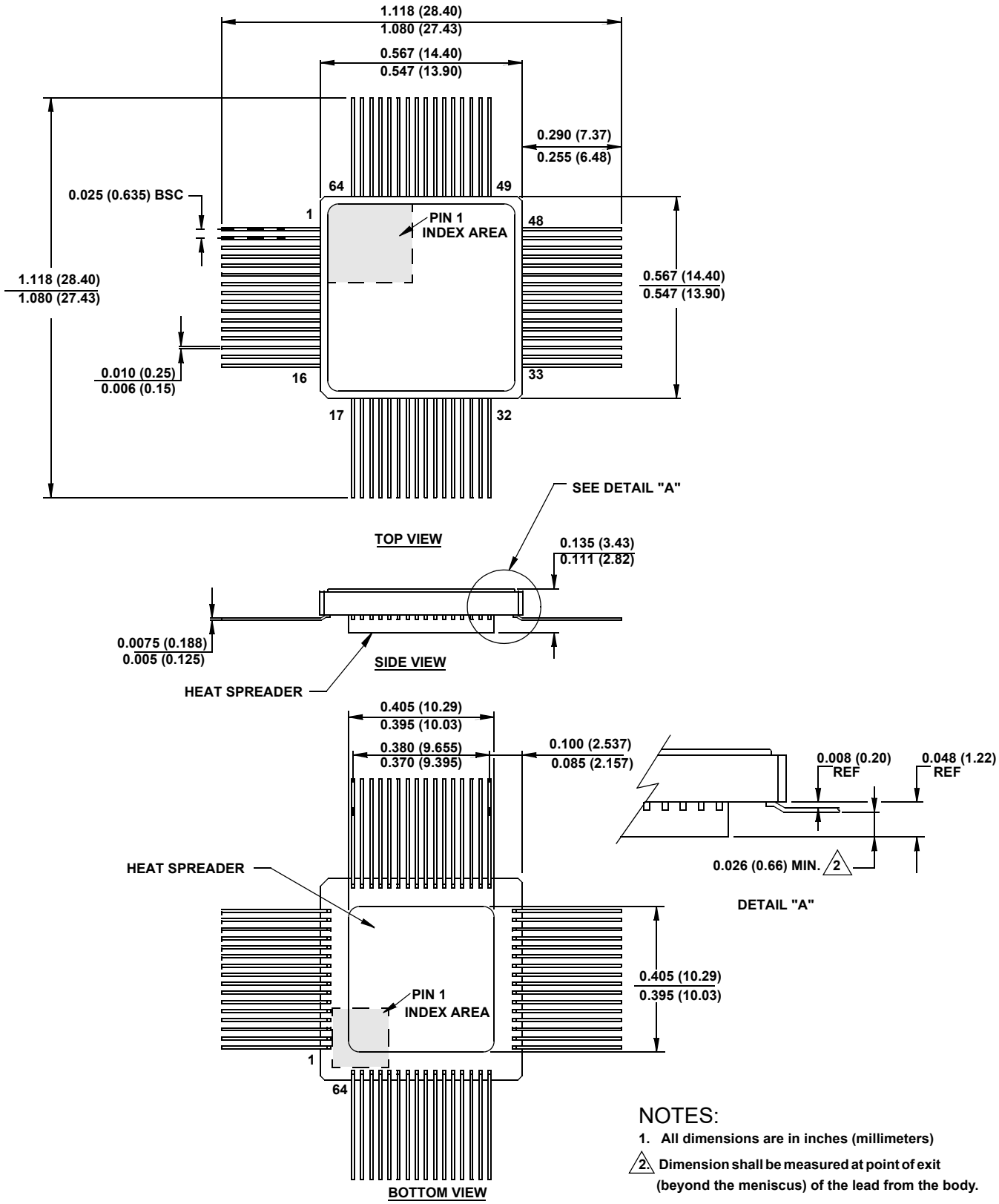


NOTE:

1. All dimensions are in inches (millimeters).

For the most recent package outline drawing, see R64.C.

R64.C
64 CERAMIC QUAD FLATPACK PACKAGE (CQFP) WITH BOTTOM HEAT SPREADER
Rev 1, 10/13



NOTES:

1. All dimensions are in inches (millimeters)
2. Dimension shall be measured at point of exit (beyond the meniscus) of the lead from the body.

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