ISL7119RH, ISL7119EH

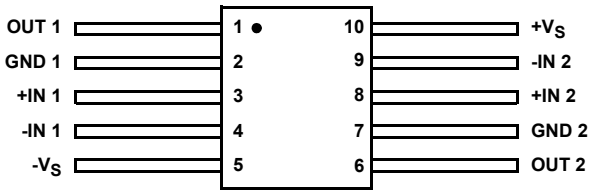
Radiation Hardened High Speed Dual Voltage Comparators

The ISL7119RH, ISL7119EH are radiation hardened, high speed, dual voltage comparators fabricated on a single monolithic chip. They are designed to operate over a wide dual supply voltage range as well as a single 5V logic supply and ground. The open collector output stage facilitates interfacing with a variety of logic devices and has the ability to drive relays and lamps at output currents up to 25mA.

The ISL7119RH, ISL7119EH are fabricated on our dielectrically isolated Radiation Hardened Silicon Gate (RSG) process, which provides immunity to Single Event Latch-Up (SEL) and highly reliable performance in the natural space environment.

Pin Configuration

ISL7119RH, ISL7119EH
(10 LD FLATPACK GDFP1-F10 OR CDFP2-F10)
TOP VIEW



Features

- Electrically screened to DLA SMD # 5962-07215
- QML qualified per MIL-PRF-38535 requirements
- Radiation acceptance testing - ISL7119RH
  - HDR (50-300rad(Si)/s) . . . . . 300krad(Si)
- Radiation acceptance testing - ISL7119EH
  - HDR (50-300rad(Si)/s) . . . . . 300krad(Si)
  - LDR (0.01rad(Si)/s) . . . . . 50krad(Si)
- SEE hardness (see SEE report for details)
  - SEL/SEB . . . . . Immune
- Input offset voltage (V_{IO}) . . . . . 8mV (max)
- Input bias current (I_{BIAS}) . . . . . 1000nA (max)
- Input offset current (I_{IO}) . . . . . 150nA (max)
- Saturation voltage at I_{SINK} = 3.2mA (V_{SAT}) . . . . 0.65V (max)
- Saturation voltage at I_{SINK} = 25mA (V_{SAT}) . . . . . 1.8V (max)
- Response time (t_{PD}) . . . . . .160ns (max)

Applications

- Window detector
- Level shifter
- Relay driver
- Lamp driver

Ordering Information

ORDERING SMD NUMBER (Note 2)	PART NUMBER (Note 1)	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #	TEMP. RANGE
5962F0721501QXC	ISL7119RHQF	LDR to 50krad(Si)	10 Lead Ceramic Metal Seal Flatpack	K10.A	-55 to +125°C
5962F0721501VXC	ISL7119RHVF				
5962F0721502VXC	ISL7119EHVF	HDR to 300krad(Si), LDR to 50krad(Si)			
5962F0721501V9A	ISL7119RHVX (Note 3)	LDR to 50krad(Si)	Die	N/A	
5962F0721502V9A	ISL7119EHVX (Note 3)	HDR to 300krad(Si), LDR to 50krad(Si)			
ISL7119RHF/PROTO	ISL7119RHF/PROTO (Note 4)	N/A	10 Lead Ceramic Metal Seal Flatpack	K10.A	
ISL7119RHX/SAMPLE	ISL7119RHX/SAMPLE (Notes 3, 4)		Die	N/A	

NOTES:

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the table must be used when ordering.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in the DLA SMD.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

Die Characteristics

DIE DIMENSIONS:

2030µm x 2030µm (~80 mils x 80 mils)
Thickness: 483µm ± 25.4µm (19 mils ±1 mil)

INTERFACE MATERIAL:

Glassivation:

Type: PSG (Phosphorous Silicon Glass)
Thickness: 8.0kÅ ±1.0kÅ

Top Metallization:

Type: AlSiCu
Thickness: 16.0kÅ ±2kÅ

Substrate:

Radiation Hardened Silicon Gate, Dielectric Isolation

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential:

Unbiased (DI)

ADDITIONAL INFORMATION:

Worst Case Current Density:

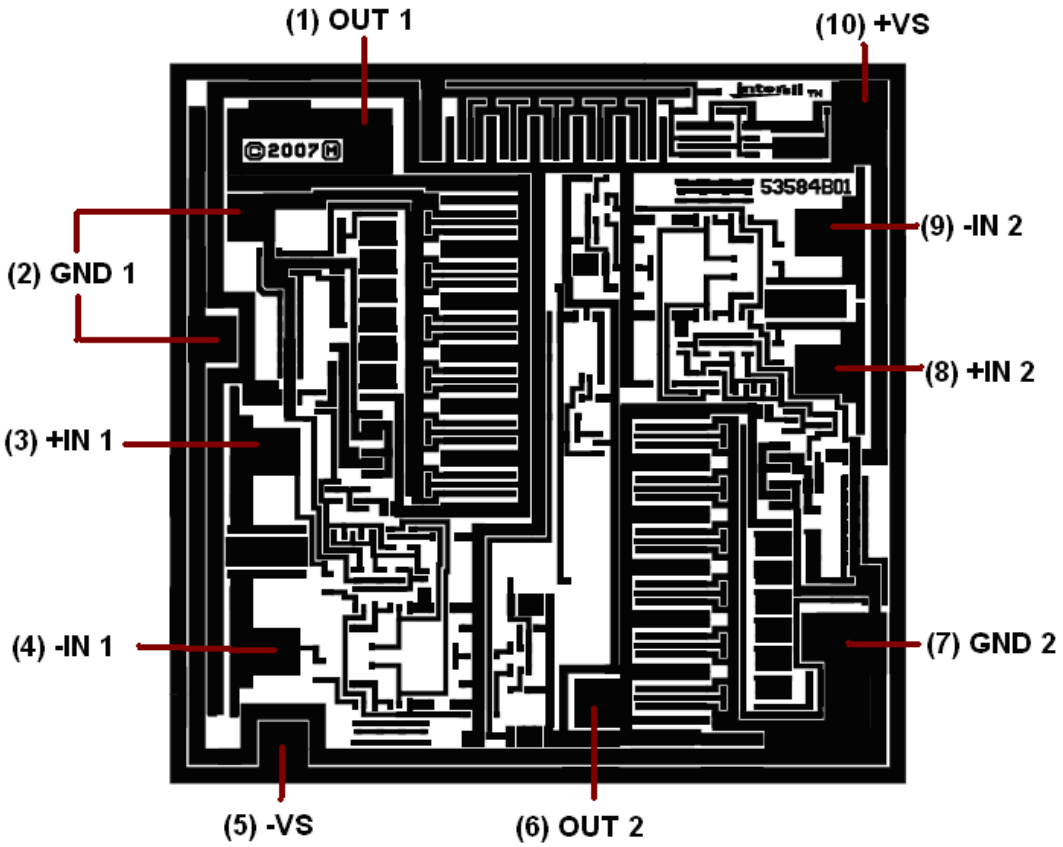
$<2.0 \times 10^5$ A/cm^2

Transistor Count:

66

Metallization Mask Layout

ISL7119RH, ISL7119EH



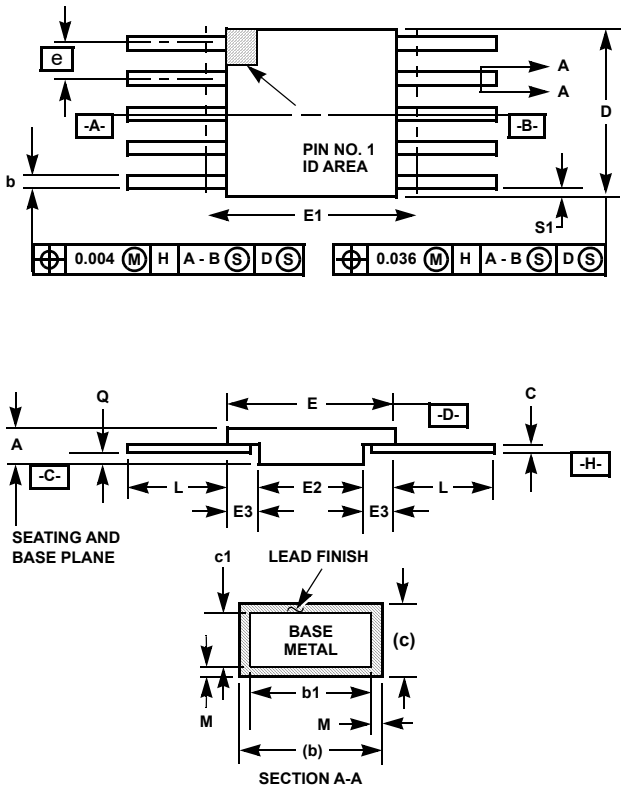
Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Feb 9, 2023	5.01	Fixed links. Updated Radiation Acceptance feature bullets. Updated Ordering Information table. Removed About Intersil section.
Apr 15, 2016	5.00	Updated package info in ordering information for parts ending in X from 10 Lead Ceramic Metal Seal Flatpack to Die. Added Revision History and About Intersil sections. Added POD K10.A.

Package Outline Drawing

For the most recent package outline drawing, see K10.A.



K10.A MIL-STD-1835 CDFP3-F10 (F-4A, CONFIGURATION B)
10 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.290	-	7.37	3
E	0.240	0.260	6.10	6.60	-
E1	-	0.280	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	10		10		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

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