ISL80030, ISL80030A, ISL80031, ISL80031A

3A Synchronous Buck Converter in 2x2 DFN Package

FN8766
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The ISL80030, ISL80030A, ISL80031, and ISL80031A are highly efficient, monolithic, synchronous step-down DC/DC converters that can deliver up to 3A of continuous output current from a 2.7V to 5.5V input supply. They use peak current mode control architecture to allow very low duty cycle operation. These devices operate at either a 1MHz or 2MHz switching frequency, thereby providing superior transient response and allowing for the use of small inductors. They also have excellent stability.

The ISL80030, ISL80030A, ISL80031, and ISL80031A integrate very low $r_{DS(ON)}$ MOSFETs to maximize efficiency. In addition, because the high-side MOSFET is a PMOS, the need for a Boot capacitor is eliminated, thereby reducing external component count. The devices can operate at 100% duty cycle.

The ISL80030 and ISL80030A are configured for PWM pulse width modulation operation and provide a fast transient response, which helps reduce the output noise and RF interference.

The ISL80031 and ISL80031A are configured for PFM discontinuous conduction operation and provide high efficiency by reducing switching losses at light loads.

These devices are offered in a space saving 8 Ld 2mmx2mm DFN Pb-free package with exposed pad for improved thermal performance. The complete converter occupies an area less than $64mm^2$.

Features

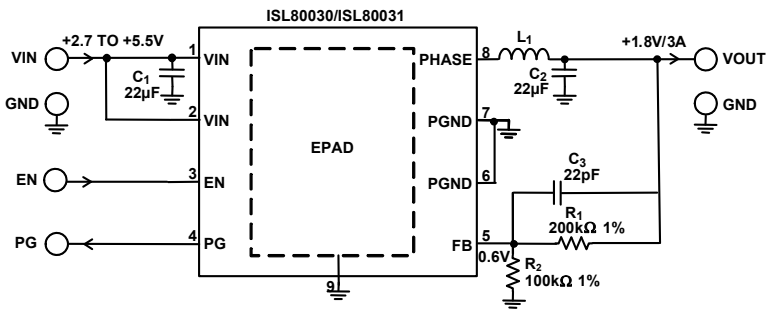
- V_{IN} range 2.7V to 5.5V
- Up to 3A of output current
- Switching frequency of 1MHz or 2MHz (see Table 1 on page 3)
- 35µA quiescent current (ISL80031 and ISL80031A)
- Overcurrent and short-circuit protection
- Over-temperature/thermal protection
- Negative current protection
- Power-good and enable
- 100% duty cycle
- Internal soft-start and soft-stop
- V_{IN} undervoltage lockout and V_{OUT} overvoltage protection
- Up to 95% peak efficiency

Applications

- General purpose POL
- Industrial, instrumentation, and medical equipment
- Telecom and networking equipment
- Game consoles

Related Literature

- For a full list of related documents, visit our website
  - ISL80030, ISL80030A, ISL80031, ISL80031A product pages



(EQ. 1) $$R_1 = R_2\left(\frac{V_O}{VFB} - 1\right)$$

FIGURE 1. TYPICAL APPLICATION CIRCUIT CONFIGURATION

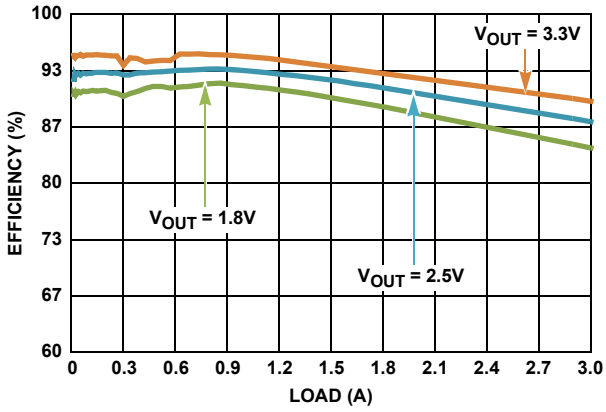


FIGURE 2. EFFICIENCY vs LOAD, ISL80031, V_{IN} = 5V, T_A = +25°C

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TABLE 1. SUMMARY OF KEY DIFFERENCES

PART#	PWM/PFM MODE	f_{SW} (MHz)	V_{IN} RANGE (V)	I_{OUT} (MAX) (A)	PACKAGE SIZE
ISL80030	PWM	1	2.7 to 5.5	3	8 pin 2mmx2mm DFN
ISL80030A	PWM	2			
ISL80031	PFM	1			
ISL80031A	PFM	2			

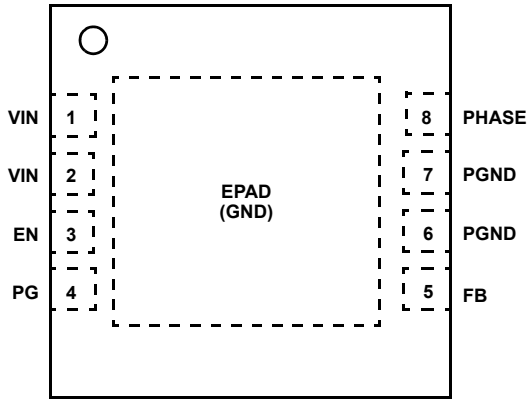
NOTE: In this datasheet, the parts in this table are collectively called “device”.

TABLE 2. COMPONENT VALUE SELECTION TABLE

V_{OUT} (V)	C_1 (µF)	C_2 (µF)	C_3 (pF)	L_1 (µH)	R_1 (kΩ)	R_2 (kΩ)
0.8	22	22	22	1.0~2.2	33	100
1.2	22	22	22	1.0~2.2	100	100
1.5	22	22	22	1.0~2.2	150	100
1.8	22	22	22	1.0~3.3	200	100
2.5	22	22	22	1.5~3.3	316	100
3.3	22	22	22	1.5~4.7	450	100

Pin Configuration

ISL80030, ISL80030A, ISL80031, ISL80031A
(8 LD 2x2 DFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1, 2	VIN	The input supply for the power stage of the PWM regulator and the source for the internal linear regulator that provides bias for the IC. Place a minimum of 10µF ceramic capacitance from VIN to GND and as close as possible to the IC for decoupling.
3	EN	Device enable input. When the voltage on this pin rises above 1.4V, the device is enabled. The device is disabled when the pin is pulled to ground. When the device is disabled, a 100Ω resistor discharges the output through the PHASE pin. See Figure 3, "Functional Block Diagram" on page 5 for details.
4	PG	The power-good output is pulled to ground during the soft-start interval and also when the output voltage is below regulation limits. This pin has an internal 5MΩ internal pull-up resistor.
5	FB	Feedback pin for the regulator. FB is the negative input to the voltage loop error amplifier. The output voltage is set by an external resistor divider connected to FB. In addition, the power-good PWM regulator's power-good and undervoltage protection circuits use FB to monitor the output voltage.
6, 7	PGND	Power and analog ground connections. Connect directly to the board GROUND plane.
8	PHASE	Power stage switching node for output voltage regulation. Connect to the output inductor. This pin is discharged by a 100Ω resistor when the device is disabled. See Figure 3, "Functional Block Diagram" on page 5 for details.
-	EPAD	The exposed pad must be connected to the PGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to the PGND plane for optimal thermal performance.

Functional Block Diagram

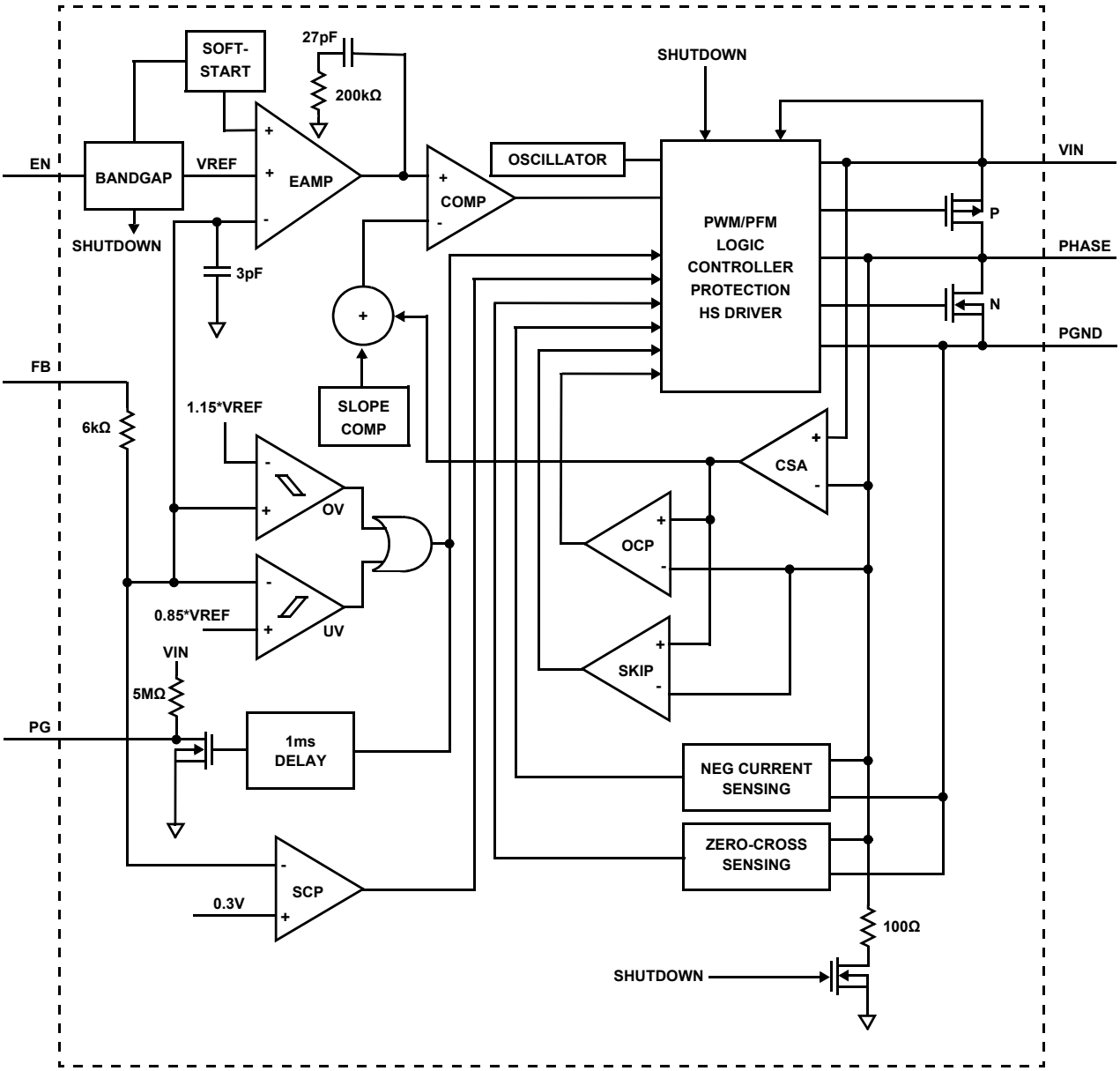


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Ordering Information

PART NUMBER (Notes 1, 2, 3)	TAPE AND REEL QUANTITY	PART MARKING	TECHNICAL SPECIFICATIONS	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL80030FRZ-T	1000	030	1MHz, PWM	-40 to +125	8 Ld DFN	L8.2x2E
ISL80030FRZ-T7A	250	030	1MHz, PWM	-40 to +125	8 Ld DFN	L8.2x2E
ISL80030AFRZ-T	1000	30A	2MHz, PWM	-40 to +125	8 Ld DFN	L8.2x2E
ISL80030AFRZ-T7A	250	30A	2MHz, PWM	-40 to +125	8 Ld DFN	L8.2x2E
ISL80031FRZ-T	1000	031	1MHz, PFM	-40 to +125	8 Ld DFN	L8.2x2E
ISL80031FRZ-T7A	250	031	1MHz, PFM	-40 to +125	8 Ld DFN	L8.2x2E
ISL80031AFRZ-T	1000	31A	2MHz, PFM	-40 to +125	8 Ld DFN	L8.2x2E
ISL80031AFRZ-T7A	250	31A	2MHz, PFM	-40 to +125	8 Ld DFN	L8.2x2E
ISL80030DEMO1Z	Demonstration Board for the ISL80030					
ISL80031DEMO1Z	Demonstration Board for the ISL80031					
ISL80030ADEMO1Z	Demonstration Board for the ISL80030A					
ISL80031ADEMO1Z	Demonstration Board for the ISL80031A					

NOTES:

1. Refer to TB347 for details on tape and reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL80030, ISL80030A, ISL80031, ISL80031A product information pages. For more information on MSL, refer to TB363.

Absolute Maximum Ratings

VIN . . . . . -0.3V to 6V (DC) or 7V (20ms)
PHASE . . . . . -1.5V (100ns)/-0.3V (DC) to 6V (DC) or 7V (20ms)
EN, PG . . . . . -0.3V to VIN + 0.3V
FB . . . . . -0.3V to 2.7V
Junction Temperature Range at 0A . . . . . +150°C
ESD Rating
Human Body Model (Tested per JESD22-JS-001). 4kV
Machine Model (Tested per JESD22-A115C) 300V
Charged Device Model (Tested per JESD22-C101D) 2kV
Latch-Up (Tested per JESD78D, Class 2, Level A). . . . ±100mA at +125°C

Thermal Information

Thermal Resistance (Typical, Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
2x2 DFN Package	70	7

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Ambient Temperature Range . . . . . -40°C to +125°C
Operating Junction Temperature Range . . . . . -40°C to +125°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

V_{IN} Supply Voltage Range . . . . . 2.7V to 5.5V
Load Current Range . . . . . 0A to 3A
Junction Temperature Range . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

T_A= -40°C to +125°C, V_{IN} = 2.7V to 5.5V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the junction operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
INPUT SUPPLY						
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising, no load		2.5	**2.7**	V
		Falling, no load	**2.2**	2.4		V
Quiescent Supply Current	I_{VIN}	ISL80031A, no load at the output		35	**60**	µA
		ISL80030, no load at the output		7	**15**	mA
		ISL80030A, no load at the output		10	**22**	mA
Shutdown Supply Current	I_{SD}	ISL80031, ISL80031A, V_{IN} = 5.5V, EN = low		1.2	**10**	µA
OUTPUT REGULATION						
Feedback Voltage	V_{FB}	T_J = -40°C to +85°C	0.594	0.600	0.606	V
		T_J = -40°C to +125°C	**0.589**		**0.606**	V
VFB Bias Current	I_{VFB}	V_{FB} = 2.7V. T_J = -40°C to +125°C	**-120**	50	**350**	nA
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V (minimal 2.7V) Nominal = 3.6V	**-0.32**	-0.05	**0.28**	%/V
Soft-Start Ramp Time Cycle		V_{IN} = 5.5V	**0.39**	1	**1.36**	ms
PROTECTIONS						
Positive Peak Current Limit	I_{PLIMIT}		**3.6**	4.5	**5.4**	A
Peak Skip Limit	I_{SKIP}	ISL80031, ISL80031A V_{IN} = 3.6, V_{OUT} = 1.8V (See "Applications Information" on page 17 for details)		450		mA
Zero Cross Threshold		ISL80031, ISL80031A	**-170**	-70	**30**	mA
Negative Current Limit	I_{NLIMIT}		**-2.6**	-2	**-1**	A
Thermal Shutdown		Temperature rising		150		°C
Thermal Shutdown Hysteresis		Temperature falling		25		°C

Electrical Specifications T_A= -40°C to +125°C, V_{IN} = 2.7V to 5.5V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the junction operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
COMPENSATION						
Error Amplifier Transconductance				40		µA/V
Transresistance	RT		**0.20**	0.25	**0.30**	Ω
PHASE						
P-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA		70		mΩ
N-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA		60		mΩ
PHASE Maximum Duty Cycle				100		%
PHASE Minimum On-Time		ISL80030, ISL80030A		60	**80**	ns
OSCILLATOR						
Nominal Switching Frequency	f_{SW}	ISL80030, ISL80031	**850**	1000	**1150**	kHz
		ISL80030A, ISL80031A	**1700**	2000	**2300**	kHz
PG						
Output Low Voltage		1mA sinking current			**0.3**	V
Delay Time (Rising Edge)			**0.5**	1	**2**	ms
PGOOD Delay Time (Falling Edge)				5		µs
PG Pin Leakage Current		PG = V_{IN}		0.01	**0.1**	µA
OVP PG Rising Threshold			**110**	117	**125**	%
OVP PG Hysteresis				2		%
UVP PG Rising Threshold			**80**	85	**90**	%
UVP PG Hysteresis				2		%
EN LOGIC						
Logic Input Low					**0.4**	V
Logic Input High			**1.4**			V
Logic Input Leakage Current	I_{EN}	Pulled up to 5.5V		0.1	**1**	µA

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

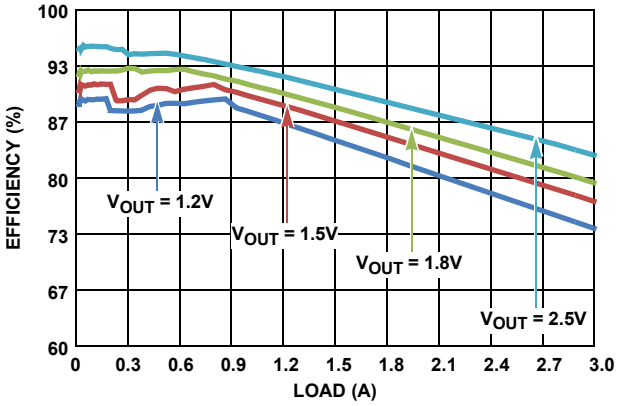


FIGURE 4. EFFICIENCY vs LOAD (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 3.3V, PFM, T_A = +25°C

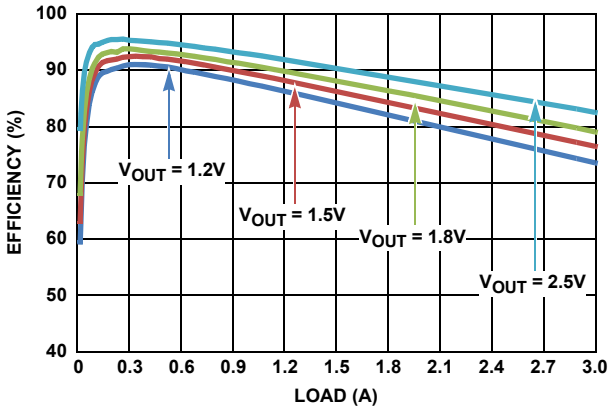


FIGURE 5. EFFICIENCY vs LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 3.3V, PWM, T_A = +25°C

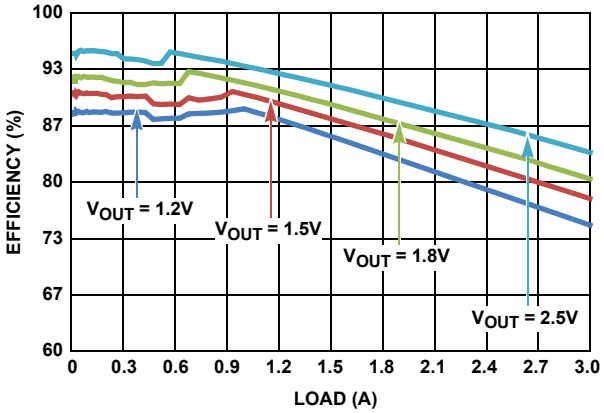


FIGURE 6. EFFICIENCY vs LOAD (ISL80031)
f_{SW} = 1MHz, V_{IN} = 3.3V, PFM, T_A = +25°C

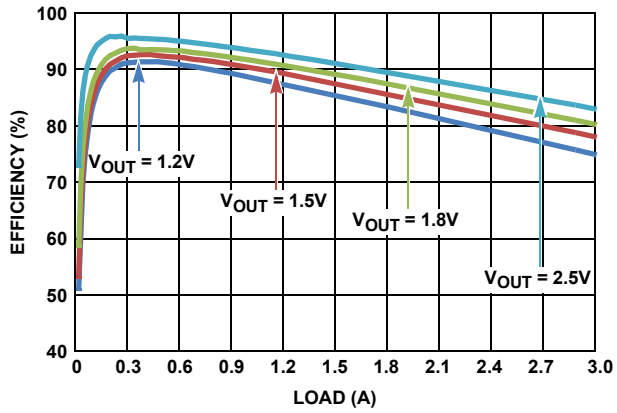


FIGURE 7. EFFICIENCY vs LOAD (ISL80030)
f_{SW} = 1MHz, V_{IN} = 3.3V, PWM, T_A = +25°C

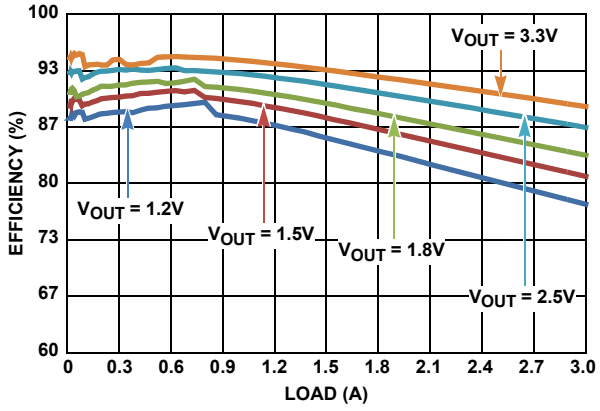


FIGURE 8. EFFICIENCY vs LOAD (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 5V, PFM, T_A = +25°C

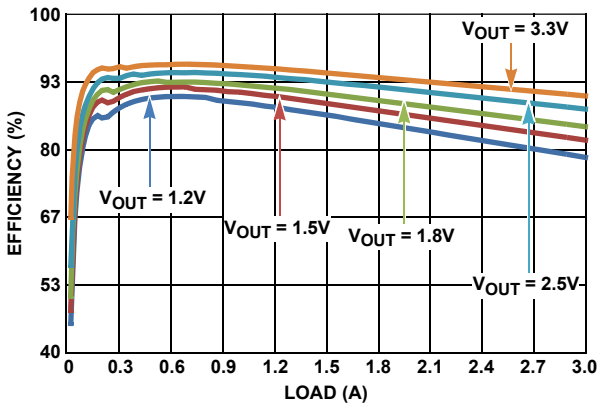


FIGURE 9. EFFICIENCY vs LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

Typical Performance Curves (Continued)

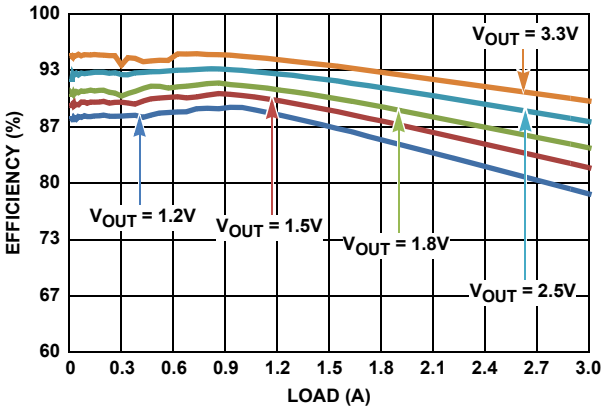


FIGURE 10. EFFICIENCY vs LOAD (ISL80031)
f_{SW} = 1MHz, V_{IN} = 5V, PFM, T_A = +25°C

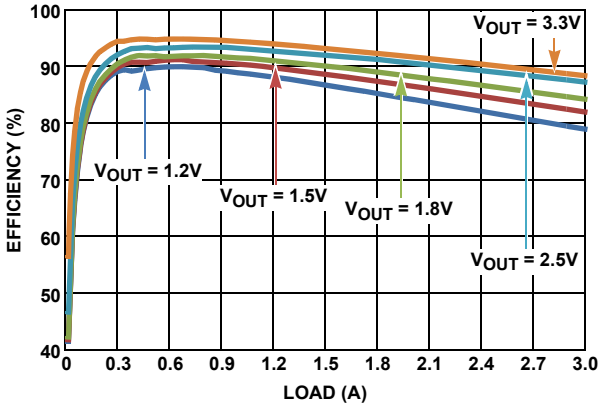


FIGURE 11. EFFICIENCY vs LOAD (ISL80030)
f_{SW} = 1MHz, V_{IN} = 5V, PWM, T_A = +25°C

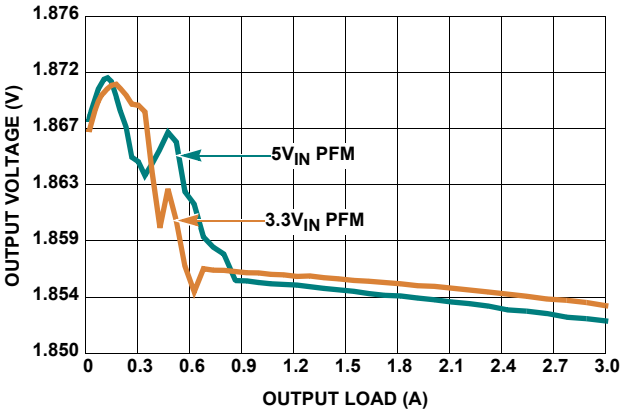


FIGURE 12. V_{OUT} REGULATION vs LOAD (ISL80031)
f_{SW} = 1MHz, V_{OUT} = 1.8V, PFM, T_A = +25°C

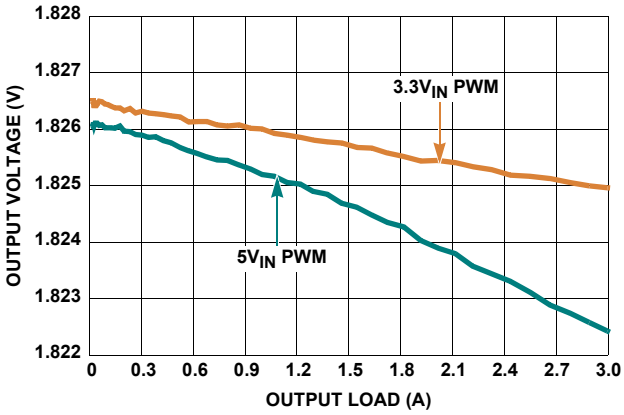


FIGURE 13. V_{OUT} REGULATION vs LOAD (ISL80030)
f_{SW} = 1MHz, V_{OUT} = 1.8V, PWM, T_A = +25°C

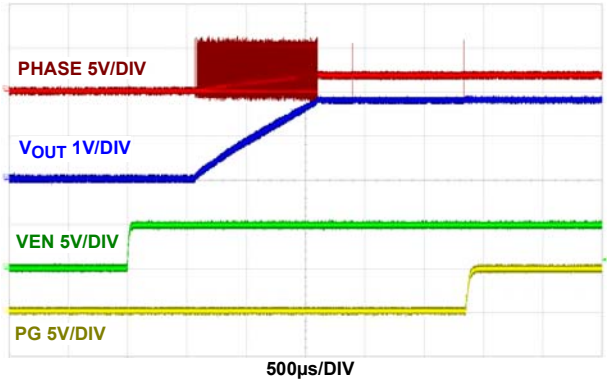


FIGURE 14. START-UP AT NO LOAD (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 5V, PFM, T_A = +25°C

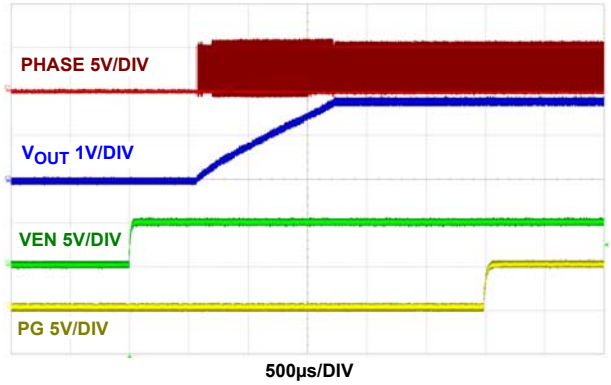


FIGURE 15. START-UP AT NO LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

Typical Performance Curves (Continued)

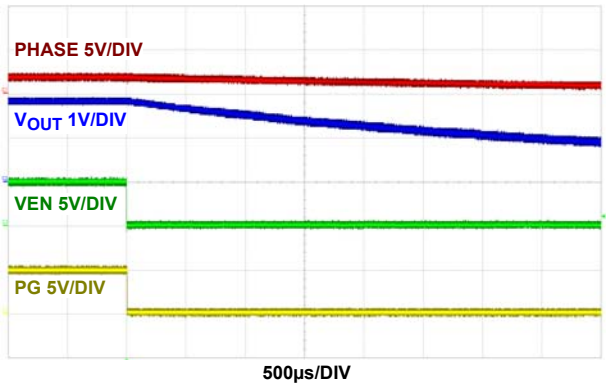


FIGURE 16. SHUTDOWN AT NO LOAD (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 5V, PFM, T_A = +25°C

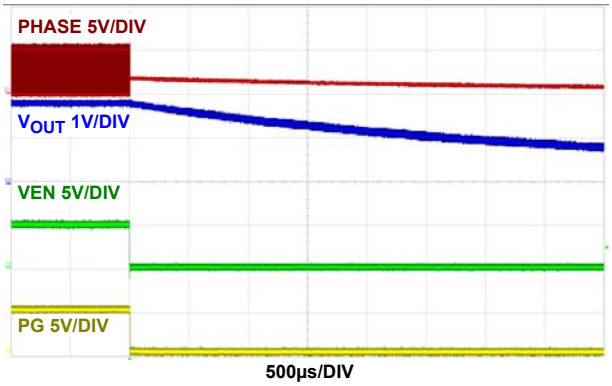


FIGURE 17. SHUTDOWN AT NO LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

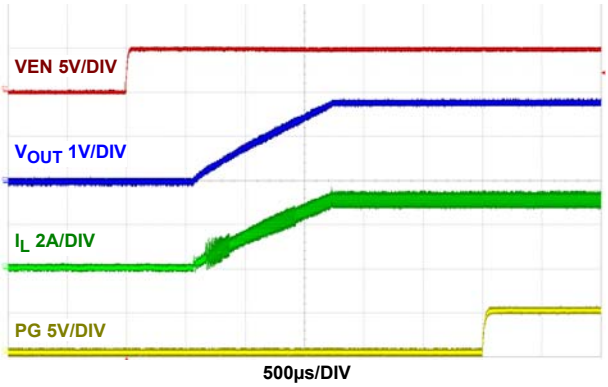


FIGURE 18. START-UP AT 3A LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

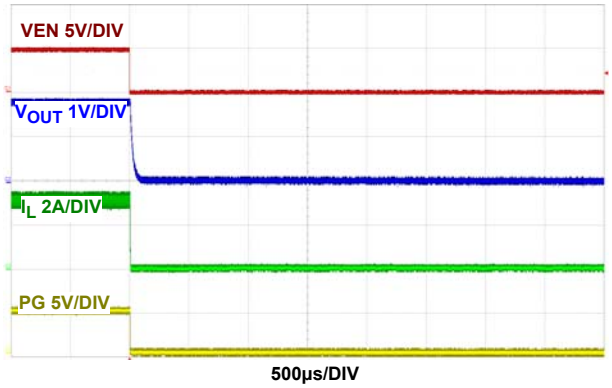


FIGURE 19. SHUTDOWN AT 3A LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

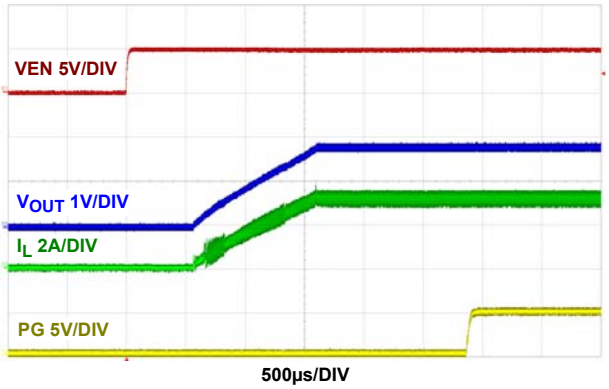


FIGURE 20. START-UP AT 3A LOAD (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 5V, PFM, T_A = +25°C

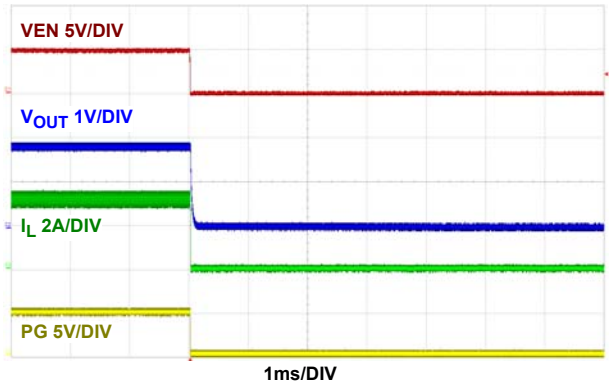


FIGURE 21. SHUTDOWN AT 3A LOAD (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 5V, PFM, T_A = +25°C

Typical Performance Curves (Continued)

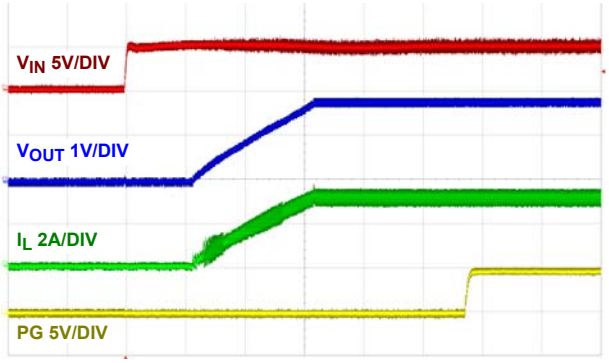


FIGURE 22. START-UP V_{IN} AT 3A LOAD (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 5V, PFM, T_A = +25°C

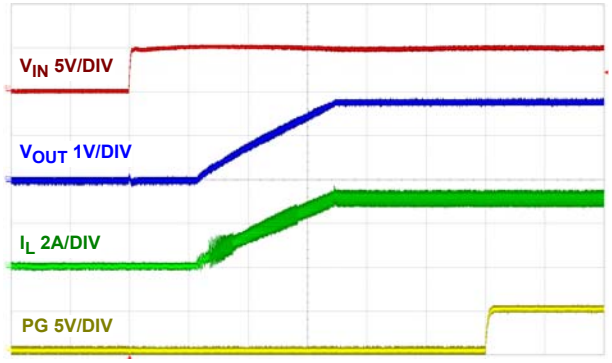


FIGURE 23. START-UP V_{IN} AT 3A LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

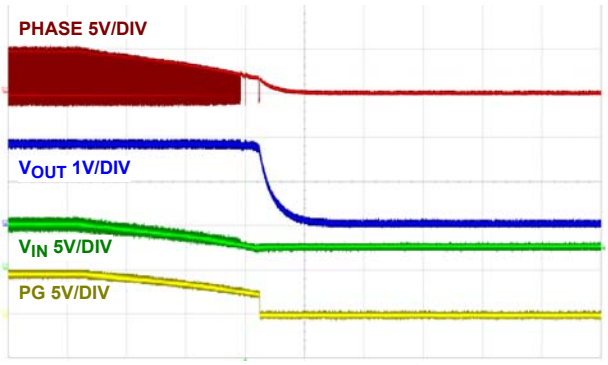


FIGURE 24. SHUTDOWN V_{IN} AT 3A LOAD (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 5V, PFM, T_A = +25°C

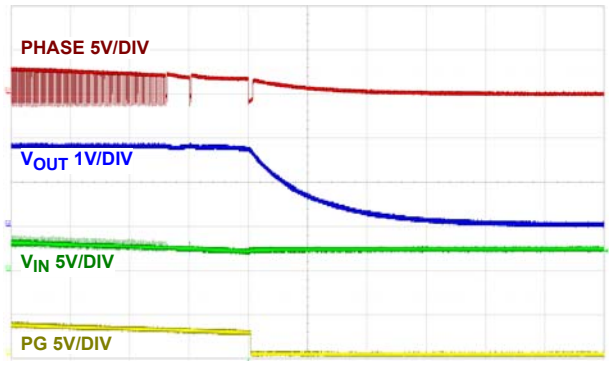


FIGURE 25. SHUTDOWN V_{IN} AT 3A LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

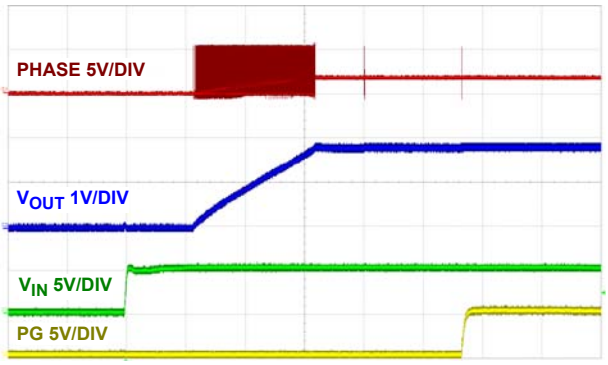


FIGURE 26. START-UP V_{IN} AT NO LOAD (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 5V, PFM, T_A = +25°C

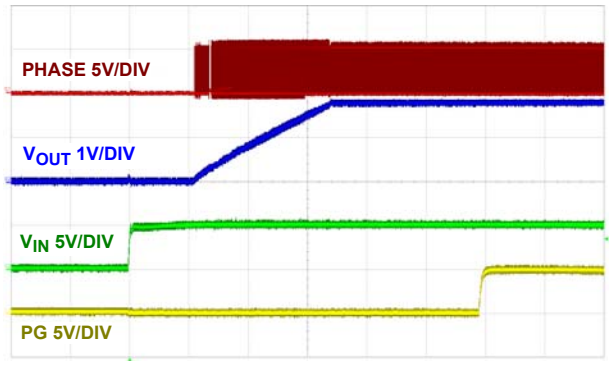


FIGURE 27. START-UP V_{IN} AT NO LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

Typical Performance Curves (Continued)

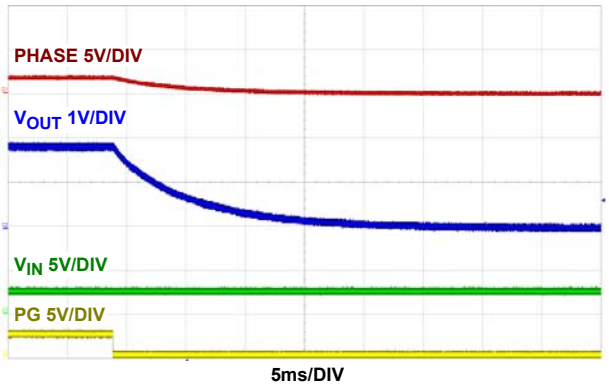


FIGURE 28. SHUTDOWN V_{IN} AT NO LOAD (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 5V, PFM, T_A = +25°C

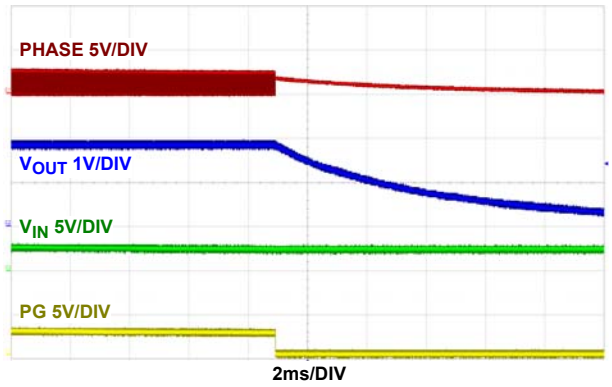


FIGURE 29. SHUTDOWN V_{IN} AT NO LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

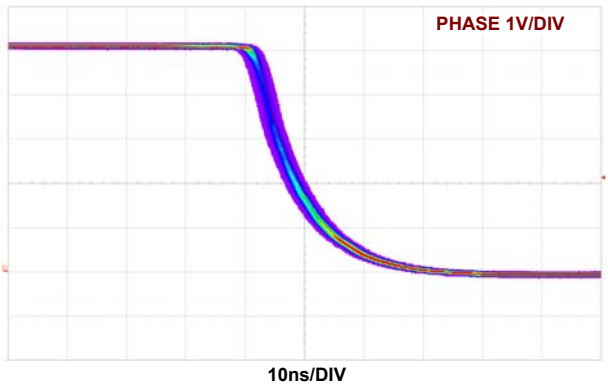


FIGURE 30. JITTER AT NO LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

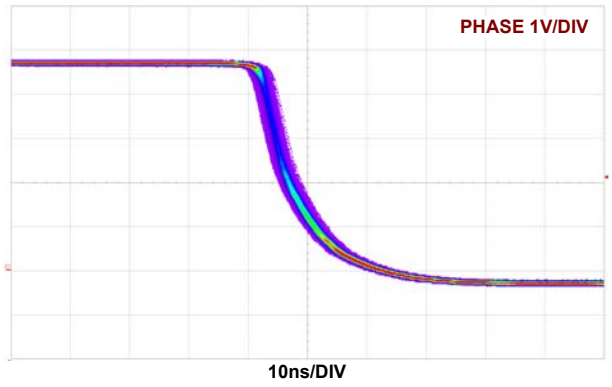


FIGURE 31. JITTER AT FULL LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

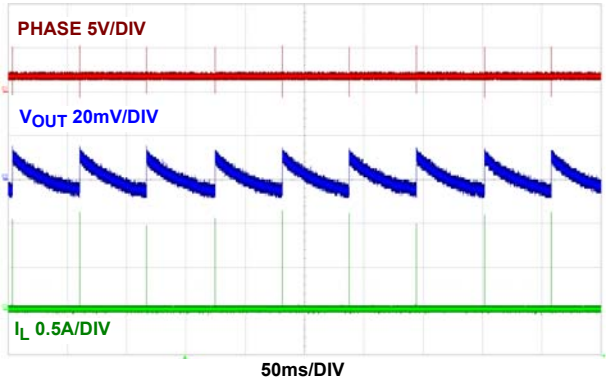


FIGURE 32. STEADY STATE AT NO LOAD (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 5V, PFM, T_A = +25°C

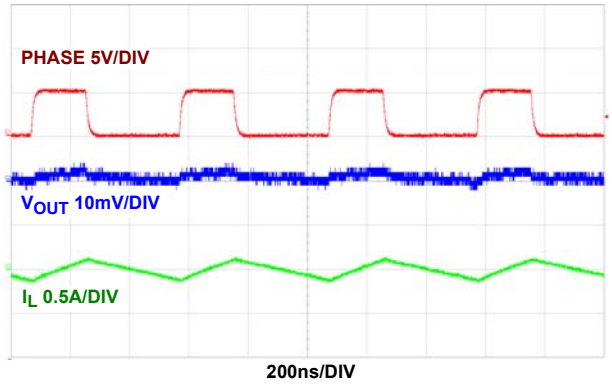


FIGURE 33. STEADY STATE AT NO LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

Typical Performance Curves (Continued)

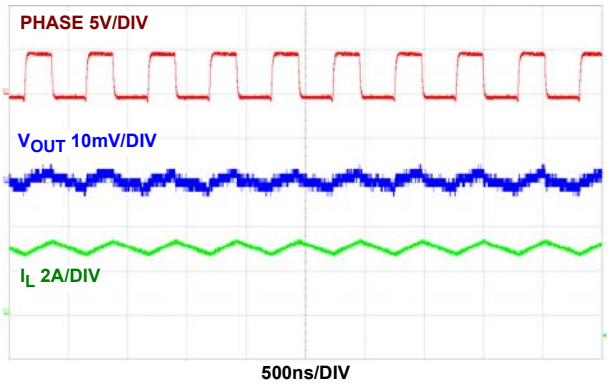


FIGURE 34. STEADY STATE AT 3A LOAD (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 5V, PFM, T_A = +25°C

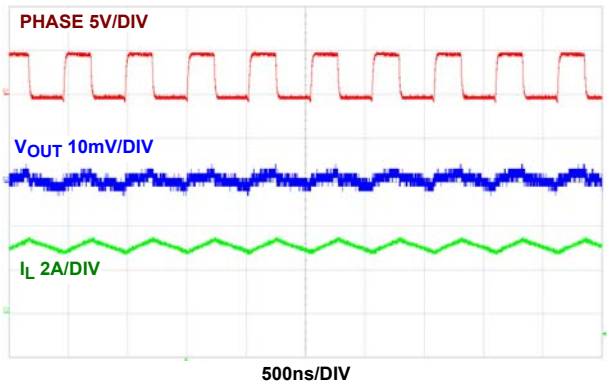


FIGURE 35. STEADY STATE AT 3A LOAD (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

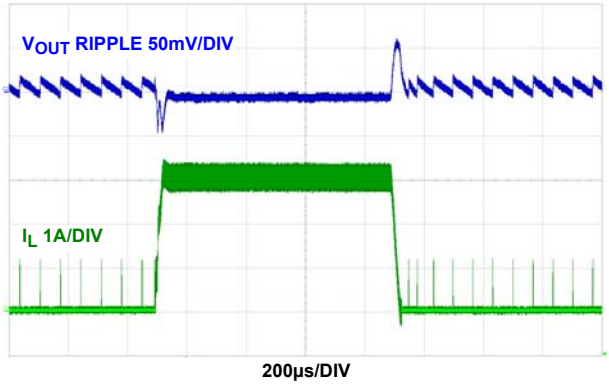


FIGURE 36. LOAD TRANSIENT (ISL80031A)
f_{SW} = 2MHz, V_{IN} = 5V, PFM, T_A = +25°C

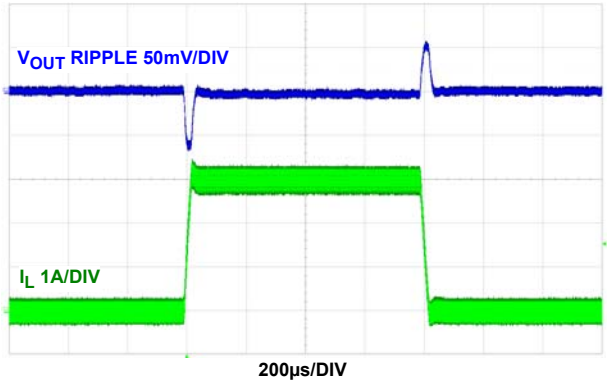


FIGURE 37. LOAD TRANSIENT (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

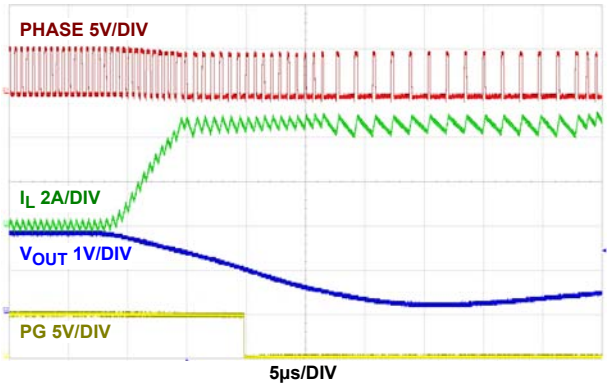


FIGURE 38. OUTPUT SHORT-CIRCUIT (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

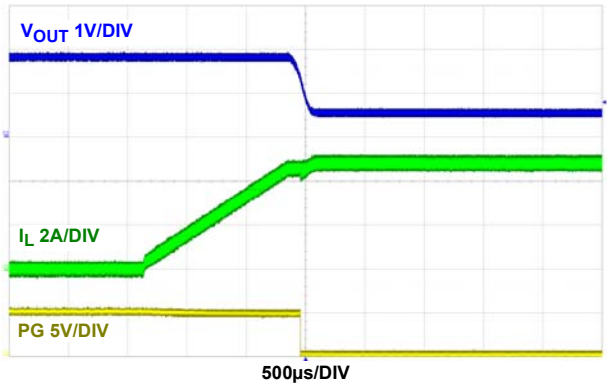


FIGURE 39. OVERCURRENT PROTECTION (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

Typical Performance Curves (Continued)

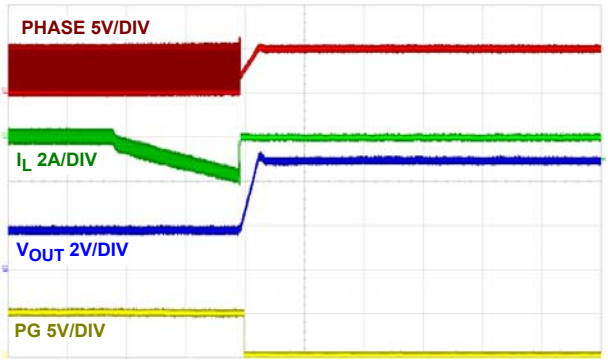


FIGURE 40. OVERVOLTAGE PROTECTION (ISL80030A)
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +25°C

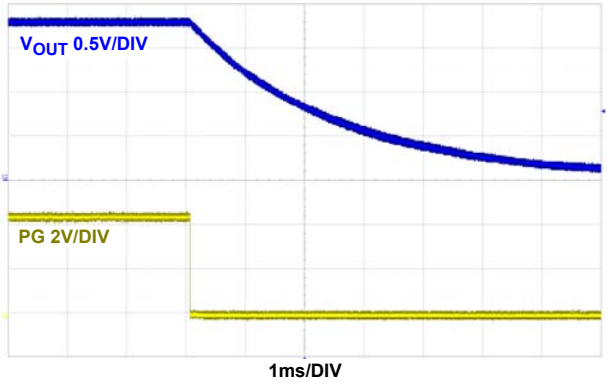


FIGURE 41. OVER-TEMPERATURE PROTECTION
f_{SW} = 2MHz, V_{IN} = 5V, PWM, T_A = +150°C

Theory of Operation

The device is a step-down switching regulator optimized for battery powered applications. It operates at a high switching frequency (1MHz or 2MHz), which enables the use of smaller inductors resulting in a small form factor, while also providing excellent efficiency. The quiescent current is typically only 1.2µA when the regulator is shut down.

PWM Control Scheme

The ISL80030 and ISL80030A employ the current-mode Pulse-Width Modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting (see "Functional Block Diagram" on page 5). The current loop consists of the oscillator, PWM comparator, current sensing circuit, and the slope compensation for current loop stability. The slope compensation is 900mV/Ts, which changes with frequency. The gain for the current sensing circuit is typically 250mV/A. The control reference for the current loop comes from the error amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-FET and turn on the N-channel MOSFET. The N-FET stays on until the end of the PWM cycle. Figure 42 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the current-sense amplifier's CSA output.

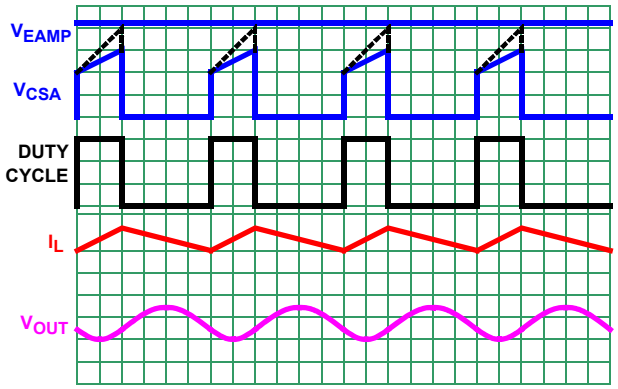


FIGURE 42. PWM OPERATION WAVEFORMS

The reference voltage is 0.6V, which is used by feedback to adjust the output of the error amplifier, V_{EAMP}. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 27pF and 200kΩ RC network. The maximum EAMP voltage output is precisely clamped to 1.6V.

PFM Operation

The ISL80031 and ISL80031A employ a pulse-skipping mode to minimize the switching loss at light load by reducing the switching frequency. Figure 43 on page 16 illustrates the skip-mode operation. A zero-cross sensing circuit shown in Figure 43 monitors the N-FET current for zero crossing. When 16 consecutive cycles of the inductor current crossing zero are detected, the regulator enters the skip mode. During the eight detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

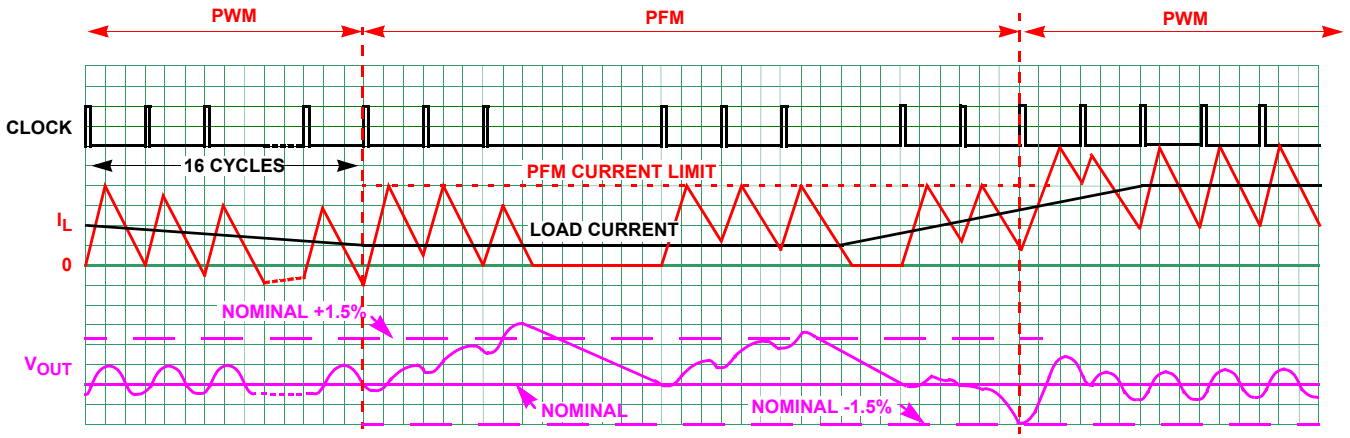


FIGURE 43. PFM MODE OPERATION WAVEFORMS

When the device enters skip mode, the SKIP comparator starts controlling pulse modulation as shown in the "Functional Block Diagram" on page 5. Each pulse cycle is still synchronized by the PWM clock. The P-FET is turned on at the clock's rising edge and turned off when the output is higher than 1.5% of the nominal regulation or when its current reaches the peak skip current limit value. Then, the inductor current discharges to 0A and stays at zero. The internal clock is disabled. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-FET will be turned on again at the rising edge of the internal clock as it repeats the previous operations.

Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in the "Functional Block Diagram" on page 5. The current sensing circuit has a gain of 300mV/A, from the P-FET current to the CSA output. When the CSA output reaches a threshold, the OCP comparator is tripped to turn off the P-FET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. If the overcurrent condition goes away, the output will resume back into the regulation point.

Short-Circuit Protection

The Short-Circuit Protection (SCP) comparator monitors the VFB pin voltage for output short-circuit protection. When the VFB is lower than 0.3V, the SCP comparator forces the PWM oscillator frequency to drop to 1/3 of the normal operation value. This comparator is effective during start-up or an output short-circuit event.

Negative Current Protection

Similar to the overcurrent, the negative current protection is realized by monitoring the current across the low-side N-FET, as shown in the "Functional Block Diagram" on page 5. When the valley point of the inductor current reaches -2A for two consecutive cycles, both P-FET and N-FET shut off. The 100Ω in parallel to the N-FET will activate discharging the output into regulation. The control will begin to switch when output is within regulation. The regulator will be in PFM for 20µs before switching to PWM if necessary.

PG

PG is an output of a window comparator that continuously monitors the buck regulator output voltage. PG is actively held low when EN is low and during the buck regulator soft-start period. After a 1ms delay of the soft-start period, PG becomes high impedance as long as the output voltage is within nominal regulation voltage set by VFB. When VFB drops 15% below or raises 15% above the nominal regulation voltage, the device pulls PG low. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start. There is an internal 5MΩ pull-up resistor to fit most applications. An external resistor can be added from PG to VIN for more pull-up strength.

UVLO

When the input voltage is below the Undervoltage Lockout (UVLO) threshold, the regulator is disabled.

Enable, Disable and Soft-Start Up

After the VIN pin exceeds its rising POR trip point (nominal 2.5V), the device begins operation. If the EN pin is held low externally, nothing happens until this pin is released. When the EN is released and above the logic threshold, the internal default soft-start time is 1ms.

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs or the VIN UVLO is set, the outputs discharge to GND through an internal 100Ω switch.

100% Duty Cycle

The device features 100% duty cycle operation to maximize the battery life. When the battery voltage drops below a level at which the device can no longer maintain the regulation at the output, the regulator completely turns on the P-FET. The maximum dropout voltage under the 100% duty cycle operation is the product of the load current and the ON-resistance of the P-FET.

Thermal Shutdown

The device has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shut down. As the temperature drops to +125°C, the device resumes operation by stepping through the soft-start.

Power Derating Characteristics

To prevent the device from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by Equation 2:

$$T_{RISE} = (PD)(\theta_{JA}) \quad \text{(EQ. 2)}$$

where PD is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by Equation 3:

$$T_j = (T_A + T_{RISE}) \quad \text{(EQ. 3)}$$

where T_A is the ambient temperature. For the DFN package, the θ_{JA} is +70°C/W.

The actual junction temperature should not exceed the absolute maximum junction temperature of +125°C when considering the thermal design.

The device delivers full current at ambient temperatures up to +85°C; if the thermal impedance from the thermal pad maintains the junction temperature below the thermal shutdown level, depending on the input voltage/output voltage combination and the switching frequency. The device power dissipation must be reduced to maintain the junction temperature at or below the thermal shutdown level. Figure 44 illustrates the approximate output current derating versus ambient temperature for the ISL80030EVAL1Z board.

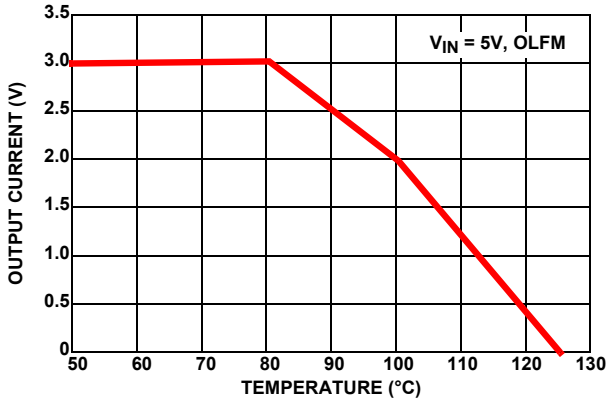


FIGURE 44. DERATING CURVE vs TEMPERATURE

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operations, the device typically requires a 1µH output inductor. Higher or lower inductor values can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V applications, to decrease the inductor ripple current and output voltage ripple, the output inductor value can be increased. It is recommended to set the inductor ripple current to approximately 30% of the maximum output current for optimized performance. The inductor ripple current can be expressed as shown in Equation 4:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet f_{SW}} \quad \text{(EQ. 4)}$$

The inductor's saturation current rating needs to be larger than the peak current.

The device uses an internal compensation network and the output capacitor value is dependent on the output voltage. An X5R or X7R ceramic capacitor is recommended.

Output Voltage Selection

The output voltage of the regulator can be programmed from an external resistor divider that scales the output voltage relative to the internal reference voltage and feeds it back to the inverting input of the error amplifier.

The output voltage programming resistor, R_1, will depend on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor is typically between 10kΩ and 100kΩ, as shown in Equation 5.

$$R_1 = R_2\left(\frac{V_O}{VFB} - 1\right) \quad \text{(EQ. 5)}$$

If the output voltage desired is 0.6V, then R_2 is left unpopulated and R_1 is shorted. There is a leakage current from VIN to LX. It is recommended to preload the output with 10µA minimum. For better performance, add 22pF in parallel with R_1.

Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. At least two 22µF X5R or X7R ceramic capacitors are a good starting point for the input capacitor selection.

Output Capacitor Selection

An output capacitor is required to filter the inductor current. Output ripple voltage and transient response are two critical factors when considering output capacitance choice. The current mode control loop allows for the usage of low ESR ceramic capacitors and thus smaller board layout. Electrolytic and polymer capacitors can also be used.

Although ceramic capacitors offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturer's datasheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction will generally suffice. The result of these considerations can easily result in an effective capacitance 50% lower than the rated value. Nonetheless, they are a very good choice in many applications due to their reliability and extremely low ESR.

Use the following equations to calculate the required capacitance to meet a desired ripple voltage level. Additional capacitance can be used.

For the ceramic capacitors (low ESR):

$$V_{OUTripple} = \frac{\Delta I}{8 * f_{SW} * C_{OUT}} \quad \text{(EQ. 6)}$$

where ΔI is the inductor's peak-to-peak ripple current, f_{SW} is the switching frequency and C_{OUT} is the output capacitor.

If using electrolytic capacitors:

$$V_{OUTripple} = \Delta I * ESR \quad \text{(EQ. 7)}$$

To determine transient response needs, a good starting point is to determine the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor will be transferred to C_{OUT} causing its voltage to rise. After calculating capacitance required for both ripple and transient needs, choose the larger of the calculated values. The following equation determines the required output capacitor value to achieve a desired overshoot relative to the regulated voltage.

$$C_{OUT} = \frac{I_{OUT}^2 * L}{V_{OUT}^2 * (V_{OUTMAX}/V_{OUT})^2 - 1)} \quad \text{(EQ. 8)}$$

where V_{OUTMAX}/V_{OUT} is the relative maximum overshoot allowed during the removal of the load. For an overshoot of 5%, Equation 9 becomes as follows:

$$C_{OUT} = \frac{I_{OUT}^2 * L}{V_{OUT}^2 * (1.05^2 - 1)} \quad \text{(EQ. 9)}$$

Layout Considerations

PCB layout is a very important converter design step to make sure the designed converter works well. The power loop is composed of the output inductor Ls, the output capacitor C_{OUT}, the PHASE's pins, and the PGND pin. Make the power loop as small as possible and the connecting traces among them direct, short, and wide. The switching node of the converter, the PHASE pins, and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as closely as possible to the VIN pin and the ground of the input and output capacitors should be connected as closely as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least four vias ground connection within the pad for the best thermal relief.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Nov 16, 2017	FN8766.2	Added Related Literature section on page 1. Added the ISL80030ADEMO1Z and ISL80031ADEMO1Z to Ordering Information on page 6. Added test conditions, minimum value, and maximum value for the Soft-Start Ramp Time Cycle specification on page 7. Applied new header/footer.
Dec 24, 2015	FN8766.1	Added Related Literature section on page 1. Added Demonstration boards to the ordering information on page 6. Feedback Voltage parameter on page 7. -Added test conditions “TJ = -40°C to +85°C” to the first line and unbolded the min and max specs. -The second line (TJ = -40°C to +125°C) bolded the min and max specs. VFB Bias Current parameter on page 7, bolded the min and max specs.
Jul 20, 2015	FN8766.0	Initial release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit www.intersil.com/glossary.

You can report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

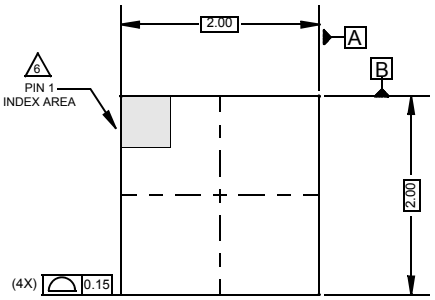
Package Outline Drawing

For the most recent package outline drawing, see L8.2x2E.

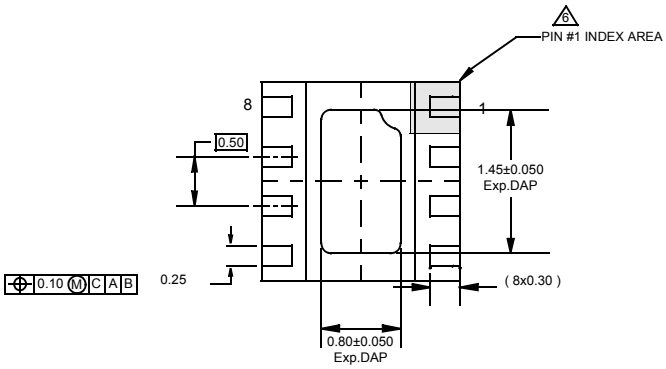
L8.2x2E

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE (DFN) WITH E-PAD

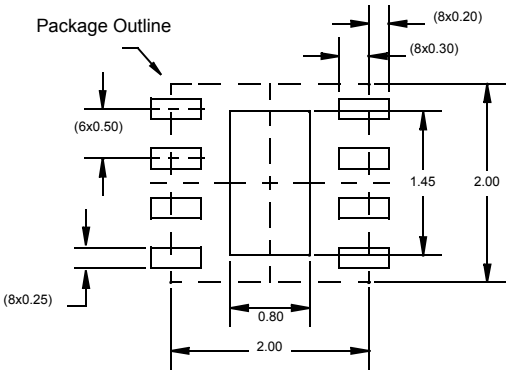
Rev 0, 5/15



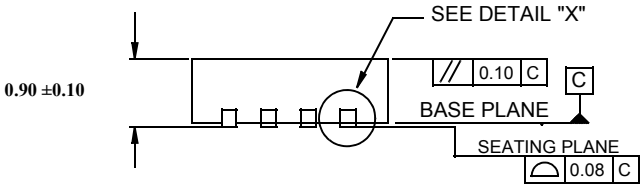
TOP VIEW



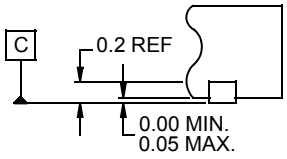
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.