ISL9116B

Ultra-Low IQ Boost Regulator With Bypass

The ISL9116B is a highly integrated boost switching regulator capable of supplying output voltage up to 5.375V. The device features an extremely low input quiescent current consumption of 250nA and output quiescent current consumption of 1200nA. The Shutdown mode input current is 80nA. It supports input voltages from 0.8V to 5.5V.

The ISL9116B has automatic bypass functionality for situations where the input voltage is close to or above the output voltage.

This device is capable of delivering up to 500 × (V_{IN}/V_{OUT})mA of output current (V_{OUT} > 2.5V) and provides excellent efficiency due to its adaptive frequency hysteretic control architecture.

The ISL9116B is designed for stand-alone applications and supports a default output voltage at Power-On Reset (POR). After POR, the output voltage can be adjusted in the range of 1.8V to 5.375V by using the I²C interface bus. Specific default output voltages are available on request.

The ISL9116B requires only a single EIA 0603 size inductor and a minimum of two external capacitors. The power supply solution size is minimized by a 3.0mm×2.0mm 8 Lead plastic DFN.

Features

- 250nA input quiescent current
- 86% efficiency at 100µA load (V_{IN} = 3.6V, V_{OUT} = 5V)
- 91% peak efficiency (V_{IN} = 3.6V, V_{OUT} = 5V)
- Input voltage range: 0.8V to 5.5V
- Output voltage range: 1.8V to 5.375V
- Output current: up to 500 × (V_{IN}/V_{OUT})mA (V_{OUT} > 2.5V)
- Auto Bypass power saving mode
- PFM and PWM modes with seamless transition
- I²C Control and voltage adjustability
- Hysteretic controller
- Small 3.0mm×2.0mm 8 Lead DFN

Applications

- Smart watches and wristband devices
- Wireless earphones
- Internet of Things (IoT) devices
- Water, gas, and oil meters
- Portable medical devices
- Hearing aid devices

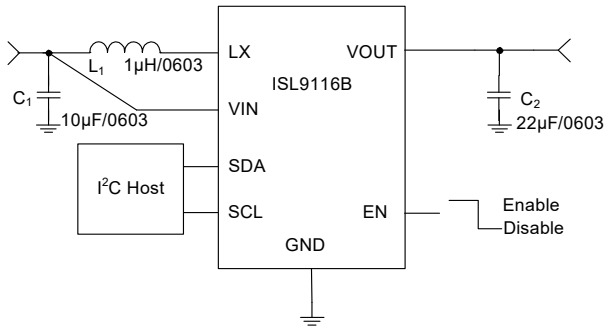


Figure 1. Typical Application (Minimum De-Rated C_2 = 6µF)

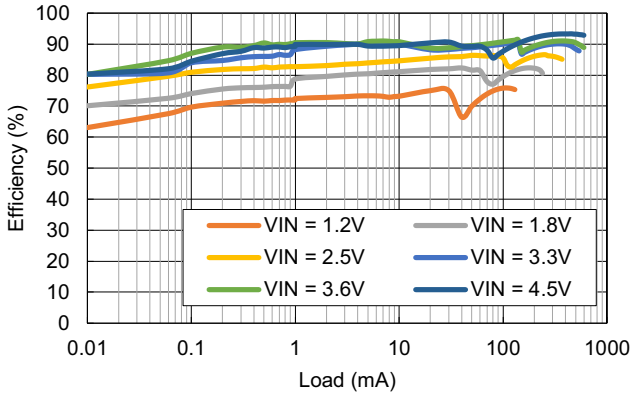


Figure 2. Efficiency vs Load Current: V_{OUT} = 5V, T_A = +25°C

Contents

1. Overview

1.1 Block Diagram

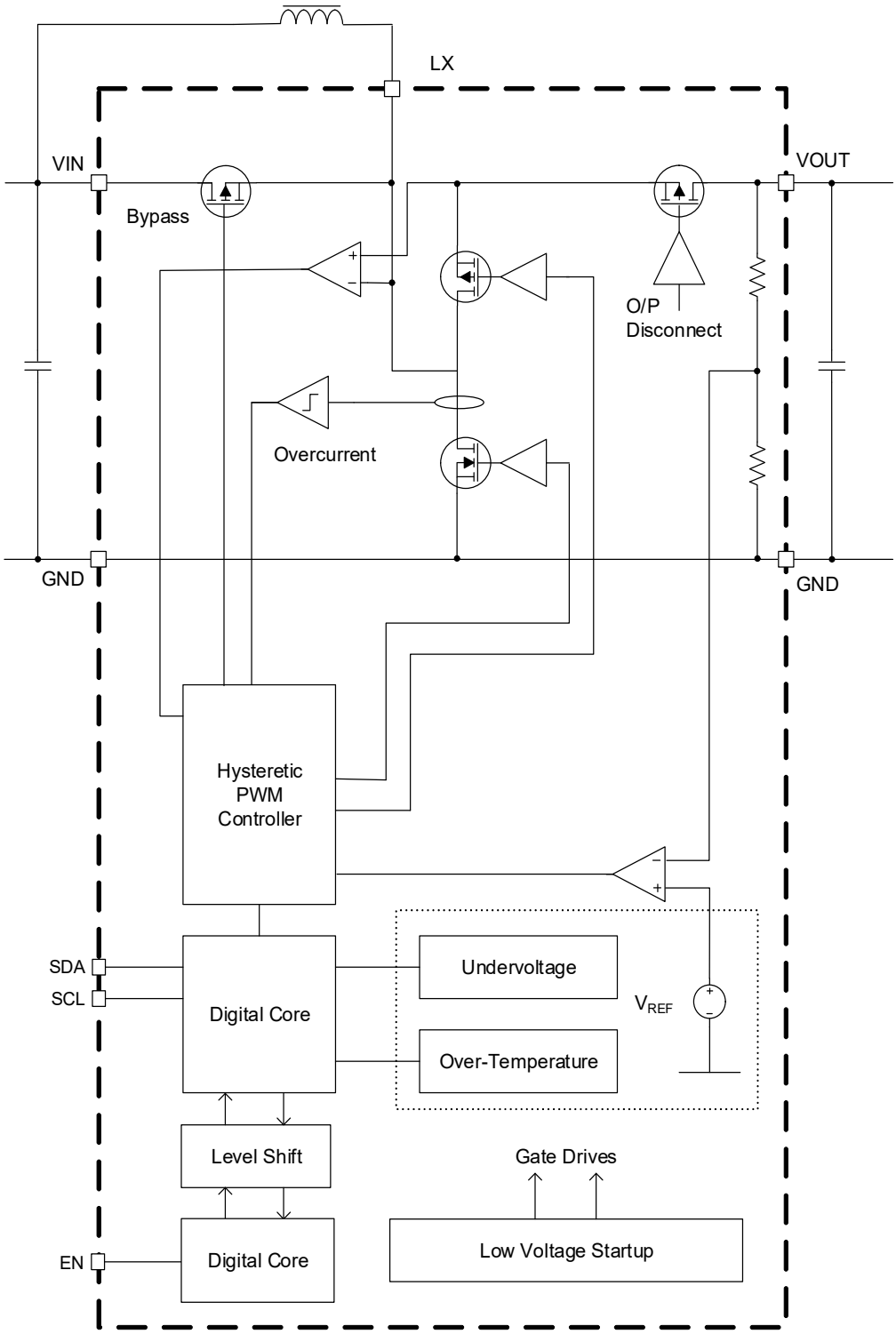
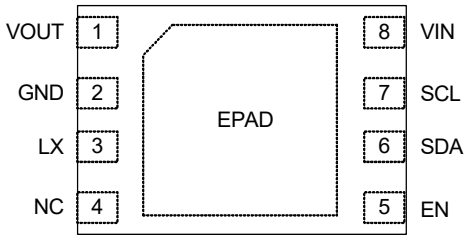


Figure 3. Block Diagram

2. Pin Information

2.1 Pin Assignments



8 Ld DFN - Top View

2.2 Pin Descriptions

Pin Number	Pin Names	Description
1	VOUT	Boost output
2	GND	Ground connection
3	LX	Inductor connection
4	NC	Not connected internally. Acceptable to leave pin floating.
5	EN	Logic input, drive HIGH to enable device. Do not leave floating.
6	SDA	I^2C data input. Pull down to GND if not being used. Do not leave floating
7	SCL	I^2C clock input. Pull down to GND if not being used. Do not leave floating
8	VIN	Power supply input
-	EPAD	Exposed pad. Must be soldered to PCB GND.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN, VOUT	-0.3	6.5	V
LX	-0.3	6.5	V
LX (less than 10ns)	-2	8.0	V
All Other Pins	-0.3	6.5	V
Maximum Junction Temperature	-	+125	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2023)	-	2	kV
Charged Device Model (Tested per JS-002-2022)	-	1	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

3.2 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance (Typical)	8 Ld 2x3 DFN Package	θ_{JA}[1]	Junction to air	72	°C/W
		θ_{JC}[2]	Junction to case	21	

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For $\theta_{JC,}$ the case temperature location is the center of the exposed metal pad on the package underside. See TB379.

3.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature (T_A) Range	-40	+85	°C
Supply Voltage (V_{IN}) Range	0.8	5.5	V
Output Voltage (V_{OUT}) Range	1.8	5.375	V
Load Current (I_{OUT}) Range (DC)	0	See Figure 15	mA
Effective Output Capacitance (C_{OUT})[1]	6	-	µF
Effective Input Capacitance (C_{IN})[1]	5	-	µF

1. Refer to *ISL9116B Evaluation Board Manual* for the reference design and recommended components.

3.4 Analog Specifications

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 5V, I^2C pull-up voltage = V_{OUT}, L_1 = 1µH, C_1 = 10µF, C_2 = C_{OUT} (effective) = 6µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range (-40°C to +85°C) and input voltage range (0.8V to 5.5V) unless specified otherwise.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Power Supply						
Input Voltage Range	V_{IN}	-	**0.8**	-	**5.5**	V
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	-	-	**0.79**	V
V_{UVLO} Hysteresis	$HYST_{UVLO}$	-	-	150	-	mV
V_{IN} Quiescent Current[2]	I_{QVIN}	V_{IN} = 3.0V, V_{OUT} = 3.5V	-	250	**700**	nA
V_{OUT} Quiescent Current[2]	I_{QVOUT}	V_{IN} = 3.0V, V_{OUT} = 3.5V	-	1150	**2750**	nA
V_{IN} Switching Current	I_{SW}	V_{IN} = 3.0V, V_{OUT} = 3.3V, I_{OUT} = 0A	-	1500	-	nA
V_{IN} Supply Current, Shutdown	I_{SD}	V_{IN} = 3.6V, V_{EN} pulled to GND	-	80	**1500**	nA
Output Voltage Regulation						
Output Voltage Range	V_{OUT}	V_{IN} < V_{SET}, I_{OUT} = 1mA	**1.8**	-	**5.375**	V
Output Voltage Accuracy						
ISL9116BIRNZ	V_{OUT_ACC}	V_{IN} = 3.0V, V_{OUT} = 3.3V, I_{OUT} = 0A, forced PWM	-2.5	-	+2.5	%
		V_{IN} = 3.0V, V_{OUT} = 3.3V, I_{OUT} = 1mA, PFM	-3.6	-	+3.6	
Soft-Start						
Time to Read OTP	t_{OTP}	Time from when V_{IN} > 1.8V and EN signal asserts until switching starts, and I^2C interface enabled	-	700	-	µs
V_{OUT} Ramp Rate for Soft-Start and During Dynamic Voltage Scaling (applicable only for V_{OUT} ramp-up, not ramp-down)	DVSRATE	Default at POR	-	3.125	-	mV/µs
		Programmable using I^2C after POR	-	6.25 0.78125 1.5625	-	

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 5V, I^2C pull-up voltage = V_{OUT}, L_1 = 1µH, C_1 = 10µF, C_2 = C_{OUT} (effective) = 6µF, T_A = +25°C. **Boldface limits apply across the recommended operating temperature range (-40°C to +85°C) and input voltage range (0.8V to 5.5V) unless specified otherwise.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Power MOSFET						
P-Channel MOSFET + Isolation Switch ON-Resistance	r_{DSON_P}	V_{IN} = 3.6V, V_{OUT} = 3.6V	-	200	-	mΩ
N-Channel MOSFET ON-Resistance	r_{DSON_N}		-	135	-	mΩ
P-Channel Bypass Switch MOSFET ON-Resistance	r_{DSON_PBYP}		-	1.5	**2**	Ω
Bypass Mode						
Auto Bypass Thresholds	V_{IN_BYP}	Auto bypass exit threshold - V_{IN} offset below regulated output voltage V_{OUT}. I_{OUT} = 10mA	-	30	-	mV
		Auto bypass entry threshold - V_{IN} offset below regulated output voltage V_{OUT}. I_{OUT} = 10mA	-	20	-	mV
Inductor Peak Current Limit						
Peak Current Limit	I_{LIM}	2.5V < V_{OUT} < 5.5V	-	2.5	-	A
		1.8V < V_{OUT} < 2.5V	-	2.5× (V_{OUT}/ 2.5)	-	A
Efficiency						
Efficiency	η	V_{IN} = 3.6V, V_{OUT} = 5.0V, I_{OUT} = 50mA	-	91	-	%
		V_{IN} = 3.6V, V_{OUT} = 5.0V, I_{OUT} = 100µA	-	86	-	
Switching Frequency						
Switching Frequency	f_{SW}	V_{IN} = 1.8V, V_{OUT} = 3.6V, I_{OUT} = 1mA, Forced PWM	-	2.0	-	MHz
Hiccup Mode						
Hiccup Time	t_{FLT_WAIT}	Fault occurrence, time from shutdown to restart	-	100	-	ms
Thermal Protection						
Thermal Shutdown Threshold	T_{SD}	Rising temperature	-	135	-	°C
Logic Levels						
Input Leakage	I_{LEAK}	EN pin	-	20	**300**	nA
		SCL pin	-	8	**300**	nA
		SDA pin	-	8	**300**	nA
EN Input HIGH Voltage	EN_{IH}	V_{IN} = 3.6V	**0.7**	-	-	V
EN Input LOW Voltage	EN_{IL}		-	-	**0.2**	V
SCL/SDA Input HIGH Voltage	SCL/SDA_{IH}		**1.55**	-	-	V
SCL/SDA Input LOW Voltage	SCL/SDA_{IL}		-	-	**0.45**	V

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

2. Quiescent current measurements are taken when the output is not switching.

3.5 I²C Interface Timing Specifications

Applicable to SCL and SDA in the Fast mode I²C operation, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
I²C Frequency Capability	f_{I2C}		0	-	400	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{SP}	Any pulse narrower than the maximum specification is suppressed	-	-	50	ns
Data Valid Time	$t_{VD:DAT}$	Time from SCL falling edge crossing SCL_{IL} to SDA exiting the SDA_{IL} to SDA_{IH} window	-	-	900	ns
Data Valid Acknowledge Time	$t_{VD:ACK}$	Time from SCL falling edge crossing SCL_{IL} to SDA exiting the SDA_{IL} to SDA_{IH} window, during acknowledgment	-	-	900	ns
Bus Free Time Between a STOP and START Condition	t_{BUF}	Time from SDA crossing SDA_{IH} at STOP to SDA crossing SDA_{IH} at the following START	1300	-	-	ns
SCL Low Time	t_{LOW}	Measured at the SCL_{IL} crossing	1300	-	-	ns
SCL High Time	t_{HIGH}	Measured at the SCL_{IH} crossing	600	-	-	ns
START Condition Set-Up Time	$t_{SU:STA}$	Time from SCL rising edge crossing SCL_{IH} to SDA falling edge crossing SDA_{IH}	600	-	-	ns
START Condition Hold Time	$t_{HD:STA}$	Time from SDA falling edge crossing SDA_{IL} to SCL falling edge crossing SCL_{IH}	600	-	-	ns
Data Set-Up Time	$t_{SU:DAT}$	Time from SDA exiting the SDA_{IL} to SDA_{IH} window to SCL rising edge crossing SCL_{IL}	100	-	-	ns
Data Hold Time	$t_{HD:DAT}$	Time from SCL falling edge crossing SCL_{IL} to SDA entering the SDA_{IL} to SDA_{IH} window	50	-	-	ns
STOP Condition Set-Up Time	$t_{SU:STO}$	Time from SCL rising edge crossing SCL_{IH} to SDA rising edge crossing SDA_{IL}	600	-	-	ns
SCL/SDA Capacitive Loading	C_b	Capacitive load for each bus line	-	-	400	pF

1. Limits established by design and are not production tested.

4. Typical Performance Graphs

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 5.0V, I^2C pull-up voltage = 3.6V, L1 = 1µH/0603, C_1 = C_{IN} =10µF/0603, C_2 = C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated.

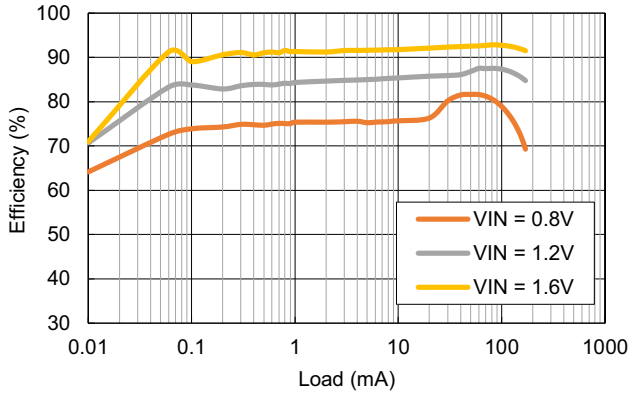


Figure 4. Efficiency vs Load Current: V_{OUT} = 1.8V

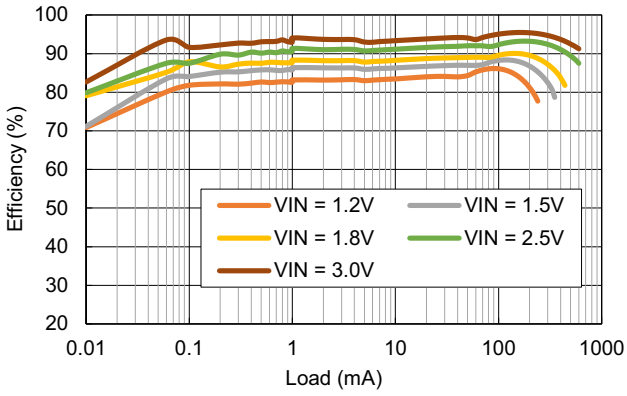


Figure 5. Efficiency vs Load Current: V_{OUT} = 3.3V

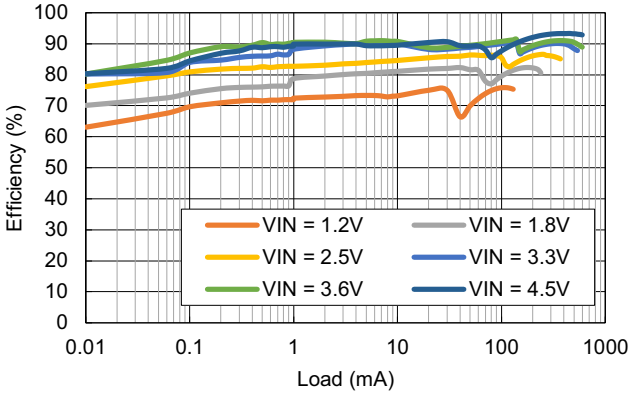


Figure 6. Efficiency vs Load Current: V_{OUT} = 5.0V

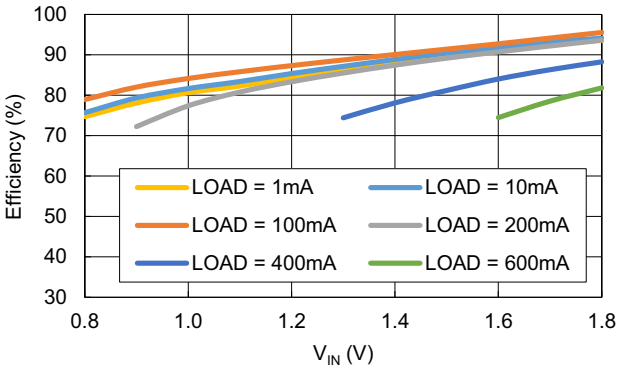


Figure 7. Efficiency vs Input Voltage: V_{OUT} = 1.8V

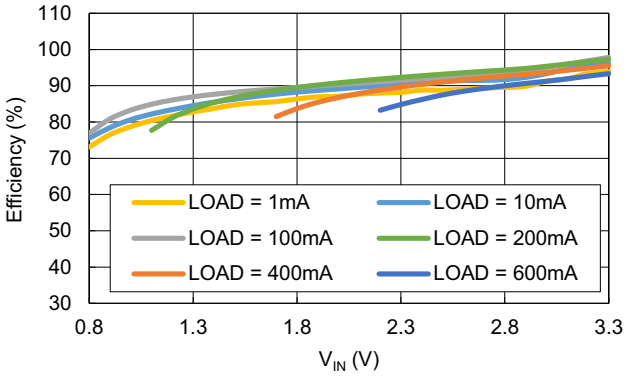


Figure 8. Efficiency vs Input Voltage: V_{OUT} = 3.3V

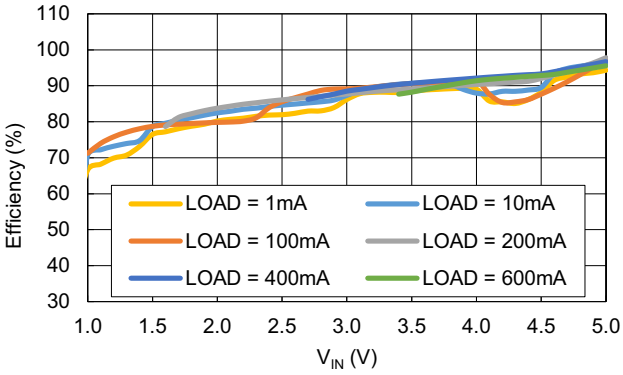


Figure 9. Efficiency vs Input Voltage: V_{OUT} = 5V

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 5.0V, I^2C pull-up voltage = 3.6V, L1 = 1µH/0603, C_1 = C_{IN} =10µF/0603, C_2 = C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated. (Cont.)

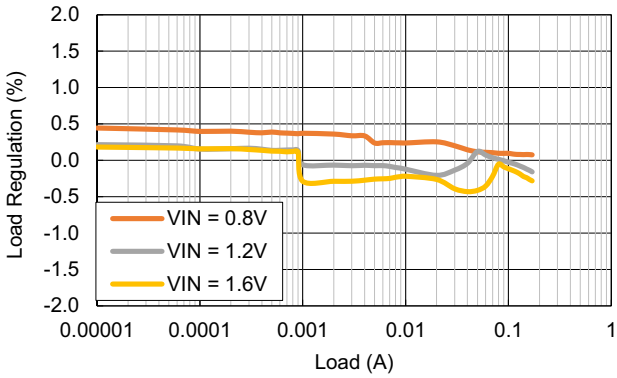


Figure 10. Output Voltage Accuracy vs Load Current: V_{OUT} = 1.8V

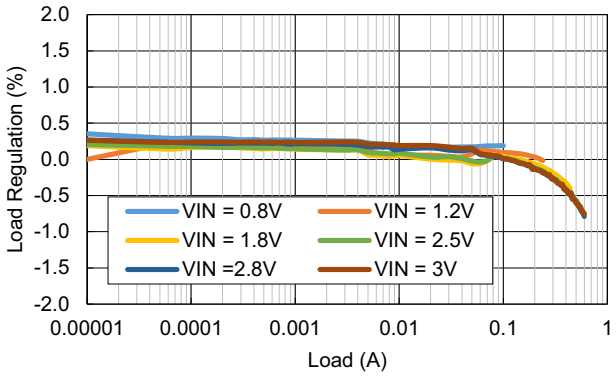


Figure 11. Output Voltage Accuracy vs Load Current: V_{OUT} = 3.3V

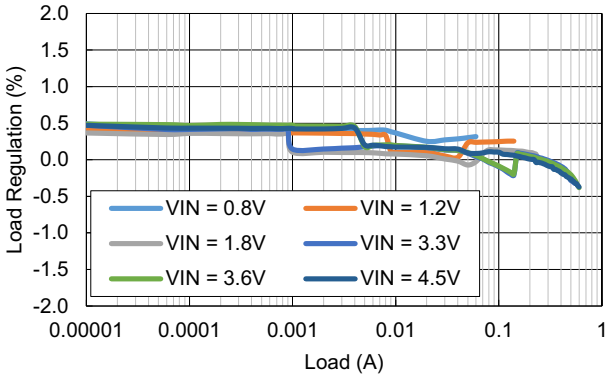


Figure 12. Output Voltage Accuracy vs Load Current: V_{OUT} = 5V

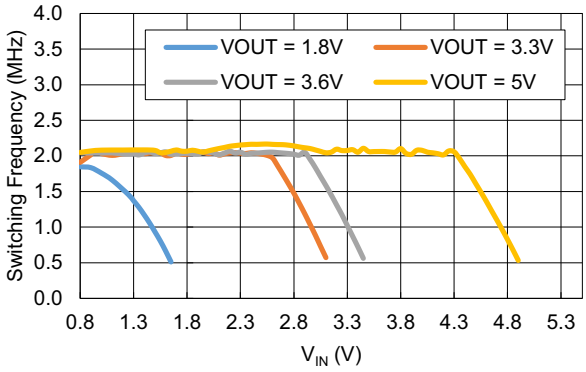


Figure 13. Switching Frequency vs Input Voltage: I_{OUT} = 1mA

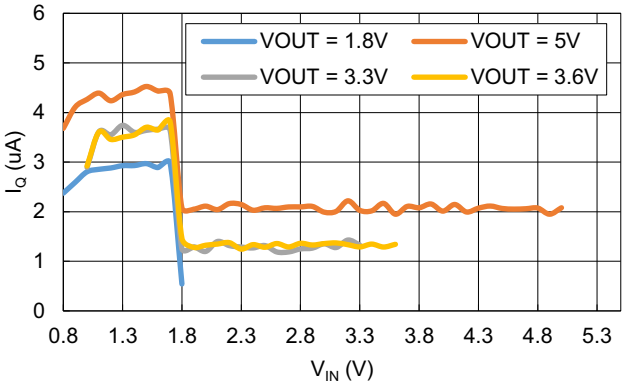


Figure 14. Quiescent Current vs Input Voltage (Device not Switching)

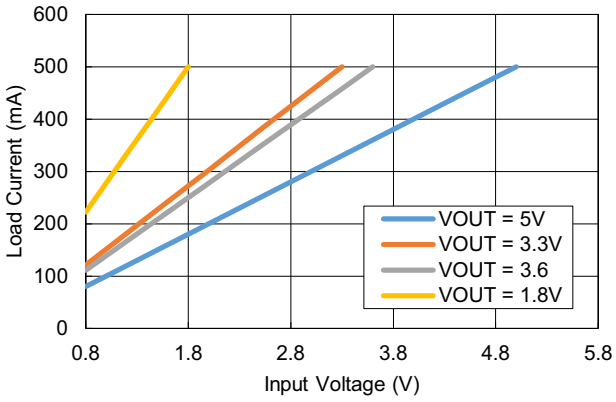


Figure 15. Maximum Load Current vs Input Voltage

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 5.0V, I^2C pull-up voltage = 3.6V, L1 = 1µH/0603, C_1 = C_{IN} =10µF/0603, C_2 = C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated. (Cont.)

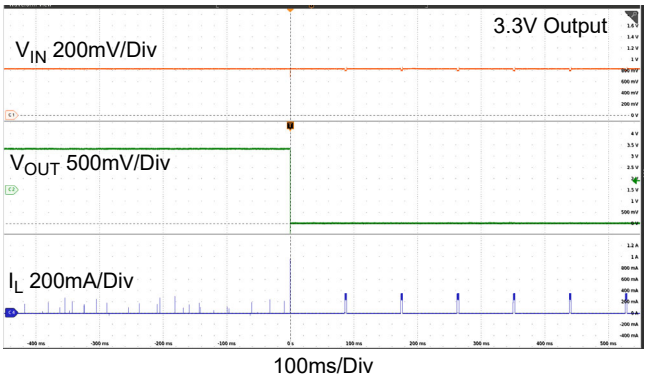


Figure 16. Output Short-Circuit Behavior (Hiccup Mode) (V_{IN} = 0.8V)

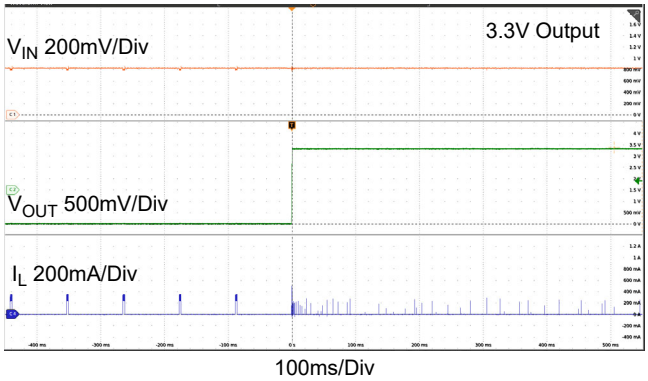


Figure 17. Output Short-Circuit Behavior (Normal Mode after removal short at Output) (V_{IN} = 0.8V)

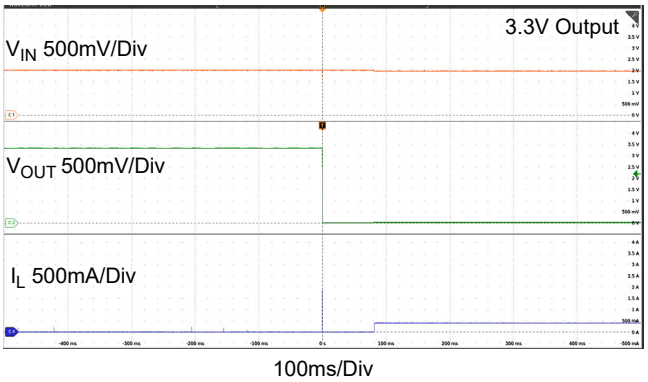


Figure 18. Output Short-Circuit Behavior (Current Limit Mode) (V_{IN} = 2.0V)

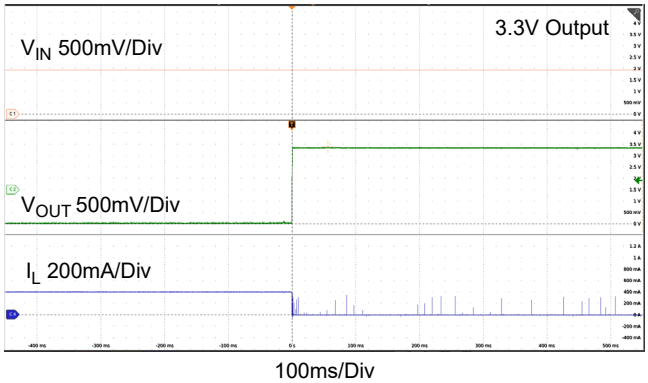


Figure 19. Output Short-Circuit Behavior (Normal Mode after Removal Short at Output) (V_{IN} = 2.0V)

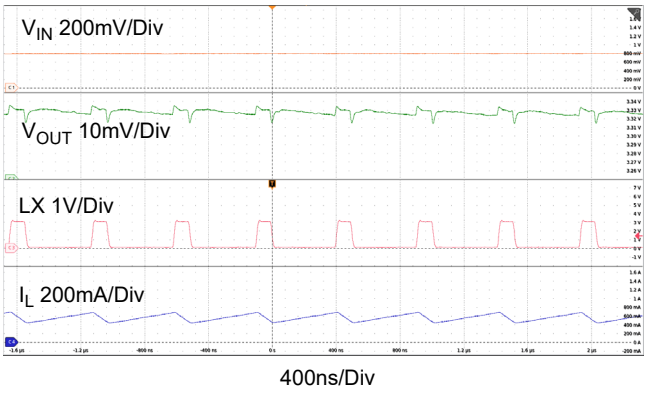


Figure 20. Steady-State Operation in PWM: V_{IN} = 0.8V, V_{OUT} = 3.3V, I_{OUT} = 200mA

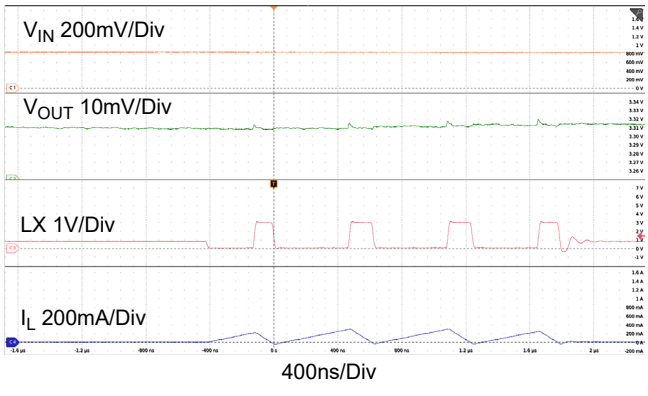


Figure 21. Steady-State Operation in PFM: V_{IN} = 0.8V, V_{OUT} = 3.3V, I_{OUT} = 10mA

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 5.0V, I^2C pull-up voltage = 3.6V, L1 = 1µH/0603, C_1 = C_{IN} =10µF/0603, C_2 = C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated. (Cont.)

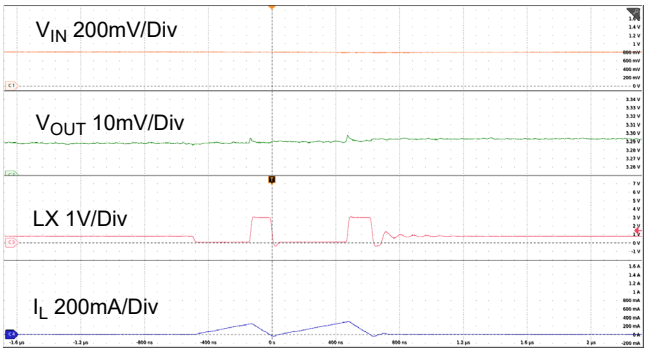


Figure 22. Steady-State Operation in PFM: V_{IN} = 0.8V, V_{OUT} = 3.3V, NO LOAD

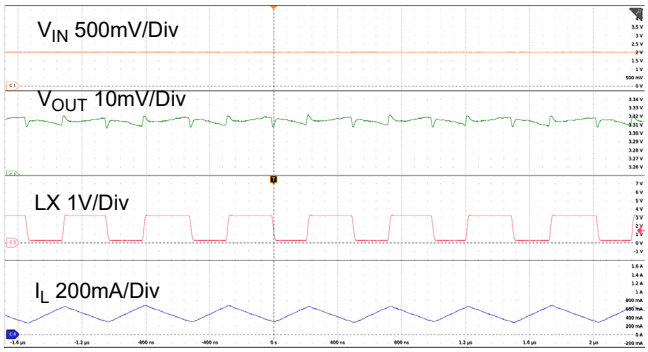


Figure 23. Steady-State Operation in PWM: V_{IN} = 2.0V, V_{OUT} = 3.3V, I_{OUT} = 250mA

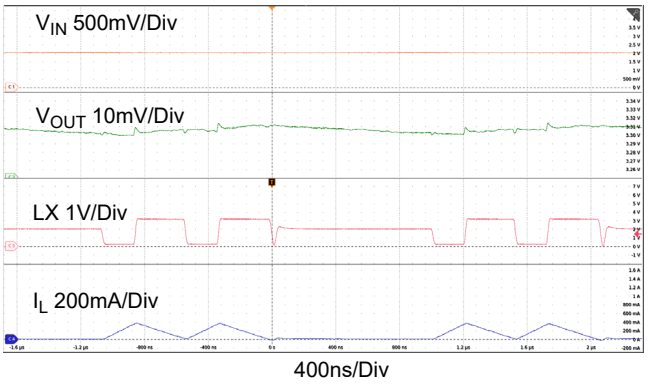


Figure 24. Steady-State Operation in PFM: V_{IN} = 2.0V, V_{OUT} = 3.3V, I_{OUT} = 50mA

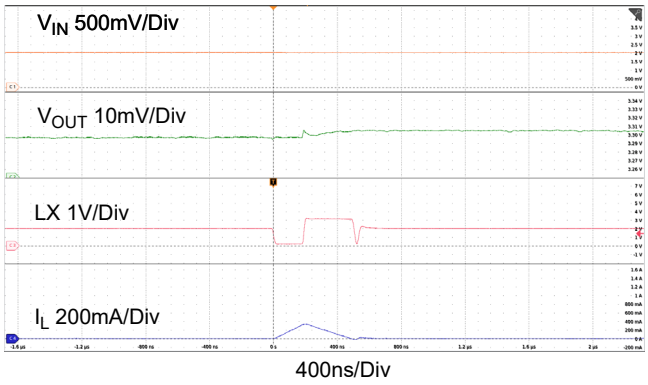


Figure 25. Steady-State Operation in PFM: V_{IN} = 2.0V, V_{OUT} = 3.3V, NO LOAD

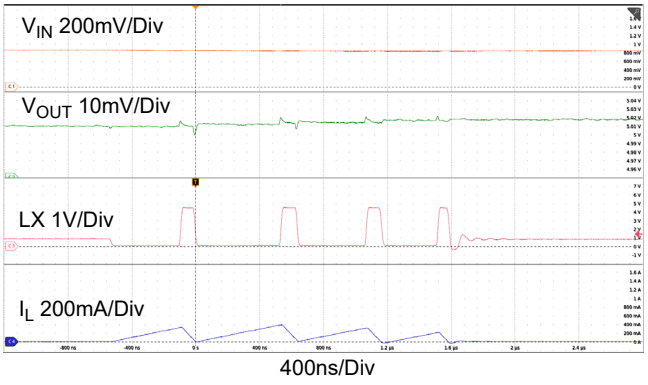


Figure 26. Steady-State Operation in PFM: V_{IN} = 0.8V, V_{OUT} = 5.0V, NO LOAD

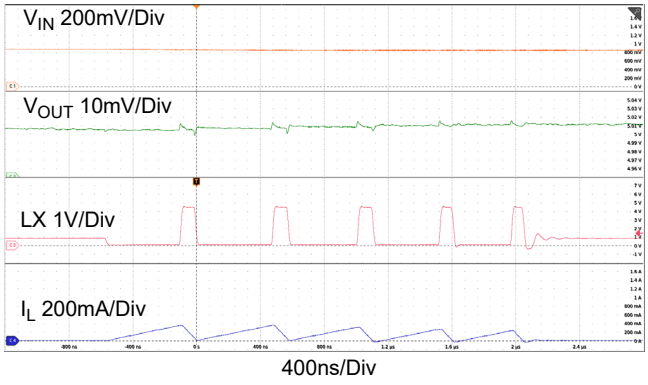


Figure 27. Steady-State Operation in PFM: V_{IN} = 0.8V, V_{OUT} = 5.0V, I_{OUT} = 5mA

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 5.0V, I^2C pull-up voltage = 3.6V, L1 = 1µH/0603, C_1 = C_{IN} =10µF/0603, C_2 = C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated. (Cont.)

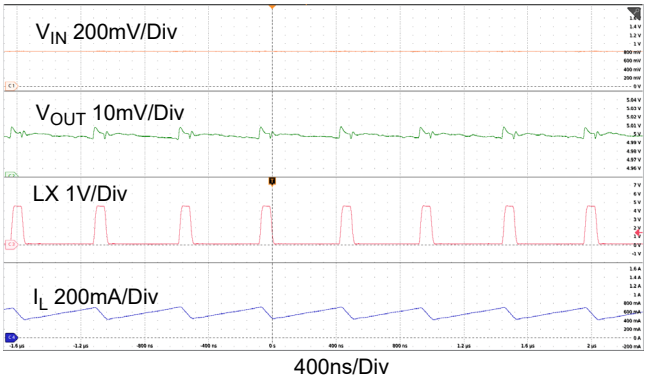


Figure 28. Steady-State Operation in PWM: V_{IN} = 0.8V, V_{OUT} = 5.0V, I_{OUT} = 65mA

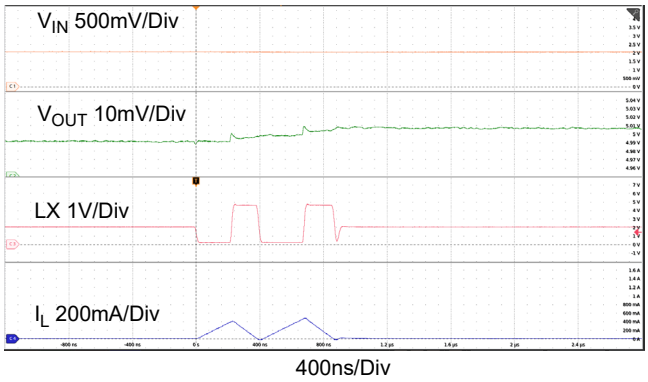


Figure 29. Steady-State Operation in PFM: V_{IN} = 2.0V, V_{OUT} = 5.0V, NO LOAD

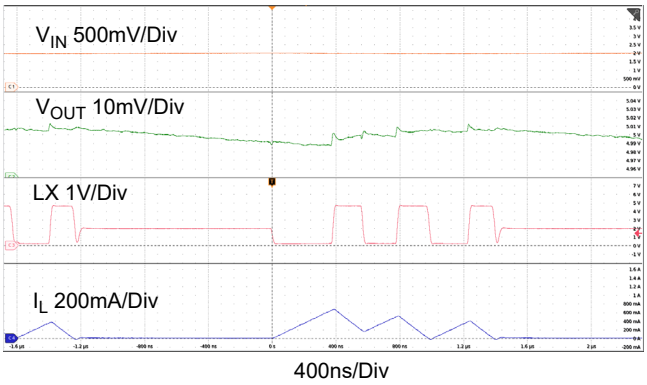


Figure 30. Steady-State Operation in PFM: V_{IN} = 2.0V, V_{OUT} = 5.0V, I_{OUT} = 50mA

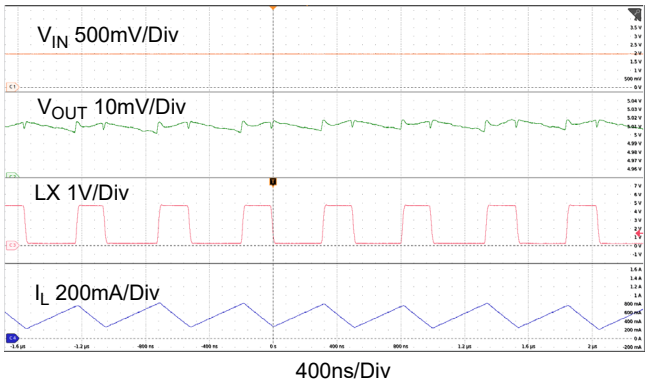


Figure 31. Steady-State Operation in PWM: V_{IN} = 2.0V, V_{OUT} = 5.0V, I_{OUT} = 165mA

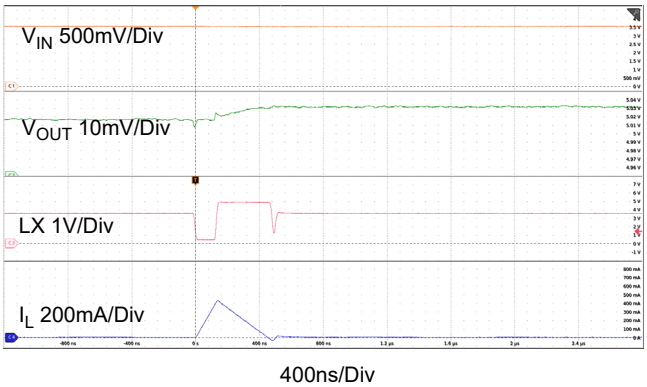


Figure 32. Steady-State Operation in PFM: V_{IN} = 3.6V, V_{OUT} = 5.0V, NO LOAD

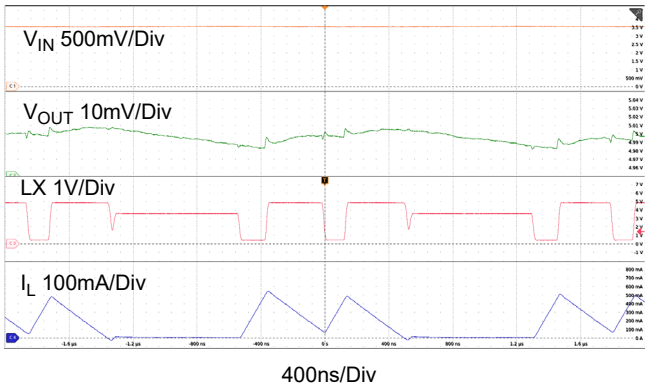


Figure 33. Steady-State Operation in PFM: V_{IN} = 3.6V, V_{OUT} = 5.0V, I_{OUT} = 100mA

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 5.0V, I^2C pull-up voltage = 3.6V, L1 = 1µH/0603, C_1 = C_{IN} =10µF/0603, C_2 = C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated. (Cont.)

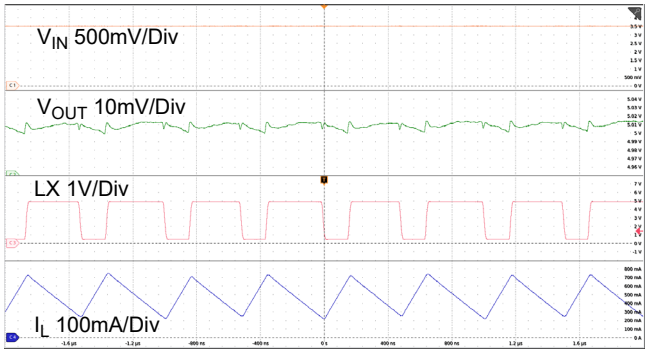


Figure 34. Steady-State Operation in PWM: V_{IN} = 3.6V, V_{OUT} = 5.0V, I_{OUT} = 300mA

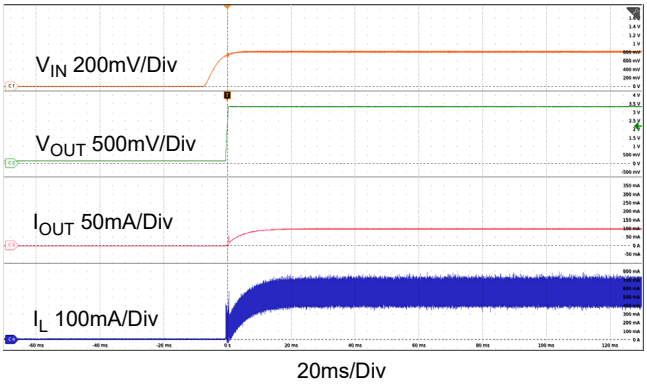


Figure 35. Output Voltage Startup: V_{IN} = 0.8V, V_{OUT} = 3.3V, I_{OUT} = 100mA

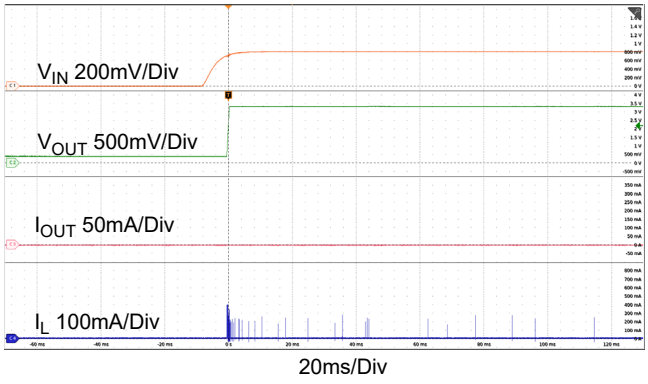


Figure 36. Output Voltage Startup: V_{IN} = 0.8V, V_{OUT} = 3.3V, No Load

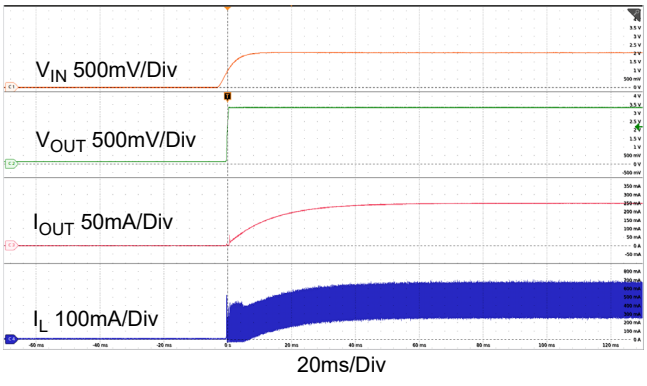


Figure 37. Output Voltage Startup: V_{IN} = 2V, V_{OUT} = 3.3V, I_{OUT} = 250mA

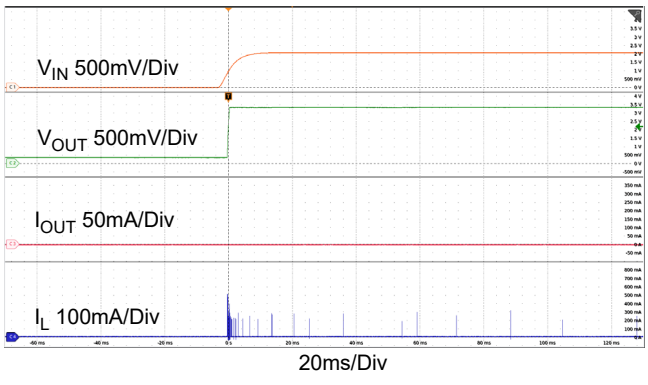


Figure 38. Output Voltage Startup: V_{IN} = 2V, V_{OUT} = 3.3V, No Load

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 5.0V, I^2C pull-up voltage = 3.6V, L1 = 1µH/0603, C_1 = C_{IN} =10µF/0603, C_2 = C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated. (Cont.)

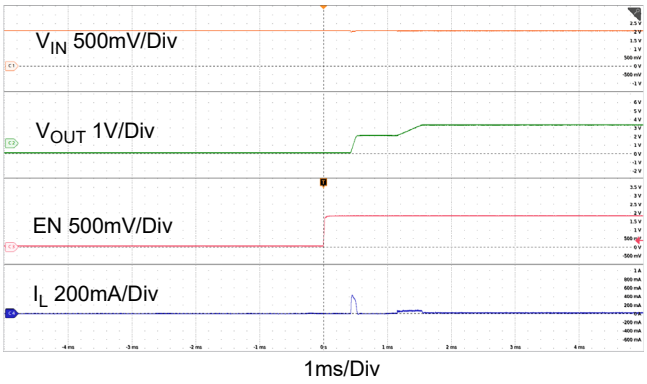


Figure 39. Output Voltage Startup with EN: V_{IN} = 2V, V_{OUT} = 3.3V, No Load

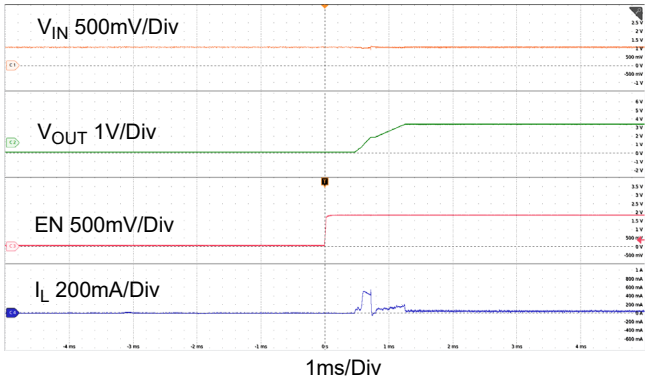


Figure 40. Output Voltage Startup with EN: V_{IN} = 1V, V_{OUT} = 3.3V, No Load

4.1 Line/Load Transient Waveforms

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 5V, I^2C pull-up voltage = 3.6V, Type II Error Amplifier L1 = 1µH/0603, C_1 = C_{IN} =10µF/0603, C_2 = C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated.

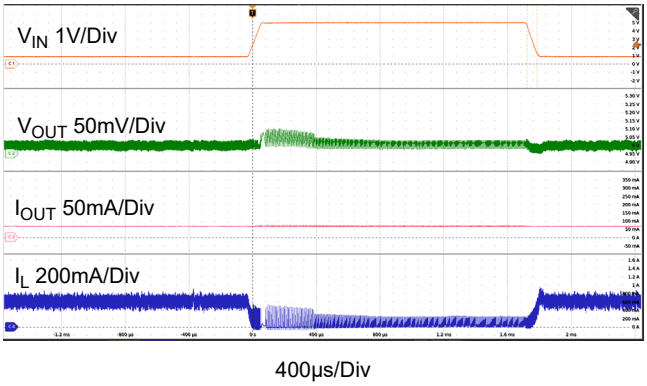


Figure 41. Line Transient: V_{IN} = 0.8V to 5.0V, Slew Rate = 0.5V/µs, V_{OUT} = 5V, I_{OUT} = 60mA

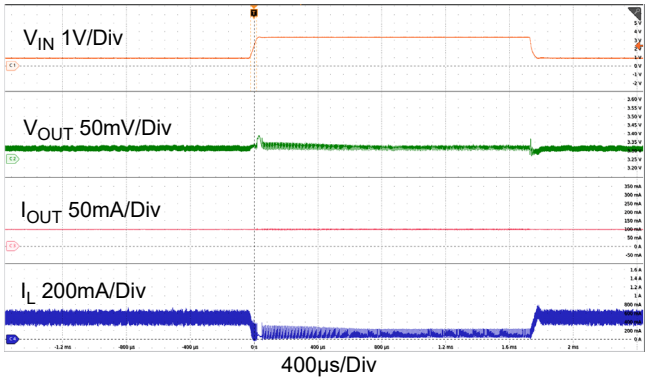


Figure 42. Line Transient: V_{IN} = 0.8V to 3.3V, Slew Rate = 0.5V/µs, V_{OUT} = 3.3V, I_{OUT} = 100mA

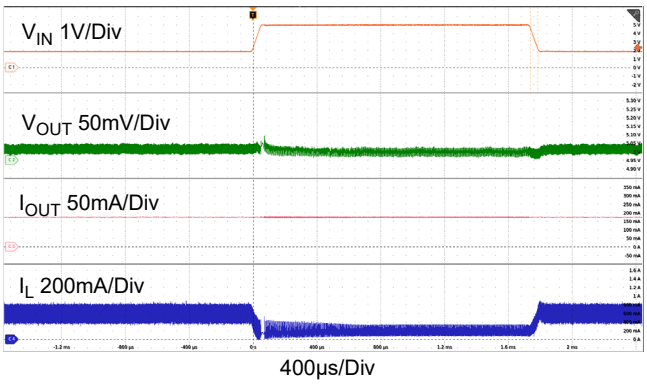


Figure 43. Line Transient: V_{IN} = 2.0V to 5.0V, Slew Rate = 0.5V/µs, V_{OUT} = 5.0V, I_{OUT} = 165mA

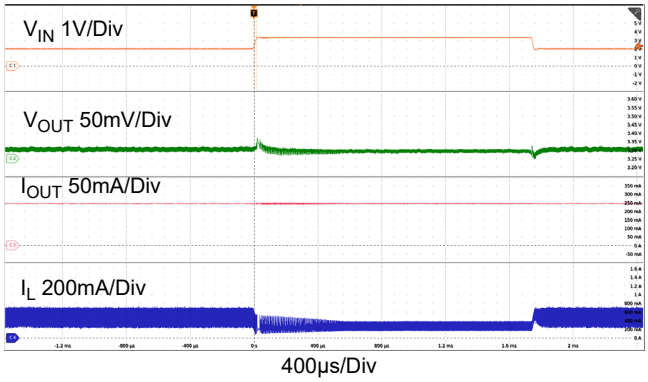


Figure 44. Line Transient: V_{IN} = 2.0V to 3.3V, Slew Rate = 0.5V/µs, V_{OUT} = 3.3V, I_{OUT} = 250mA

V_{IN} = V_{EN} = 3.6V, V_{OUT} = 5V, I^2C pull-up voltage = 3.6V, Type II Error Amplifier L1 = 1µH/0603, C_1 = C_{IN} =10µF/0603, C_2 = C_{OUT} = 22µF/0603, T_A = +25°C, unless otherwise stated. (Cont.)

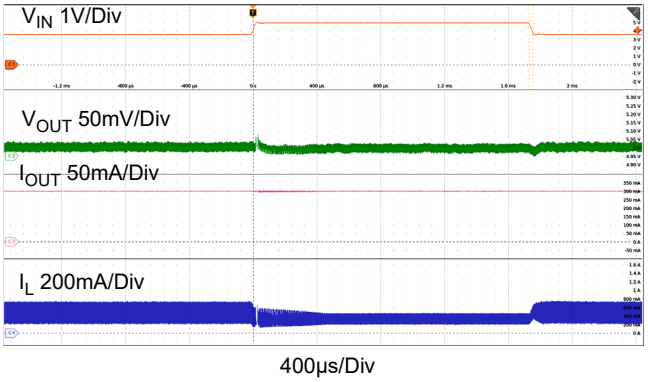


Figure 45. Line Transient: V_{IN} = 3.6V to 5.0V, Slew Rate = 0.5V/µs, V_{OUT} = 3.3V, I_{OUT} = 300mA

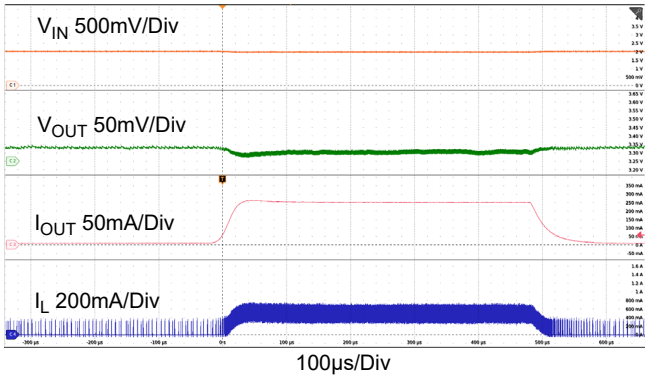


Figure 46. Load Transient: V_{IN} = 2.0V, V_{OUT} = 3.3V, I_{OUT} = 0.01A to 0.250A

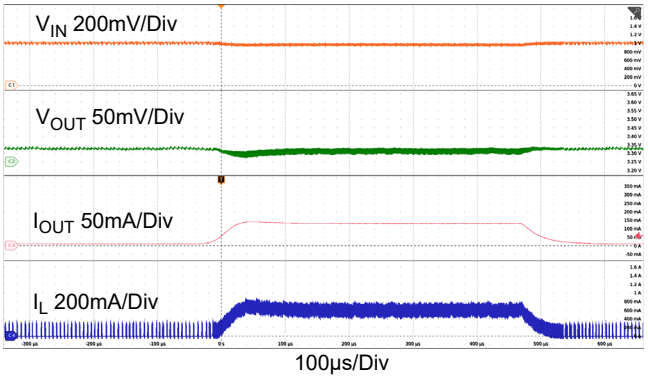


Figure 47. Load Transient: V_{IN} = 1.0V, V_{OUT} = 3.3V, I_{OUT} = 0.01A to 0.125A

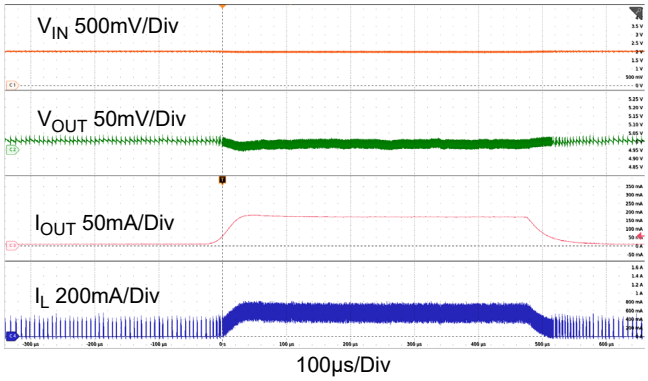


Figure 48. Load Transient: V_{IN} = 2.0V, V_{OUT} = 5.0V, I_{OUT} = 0.01A to 0.165A

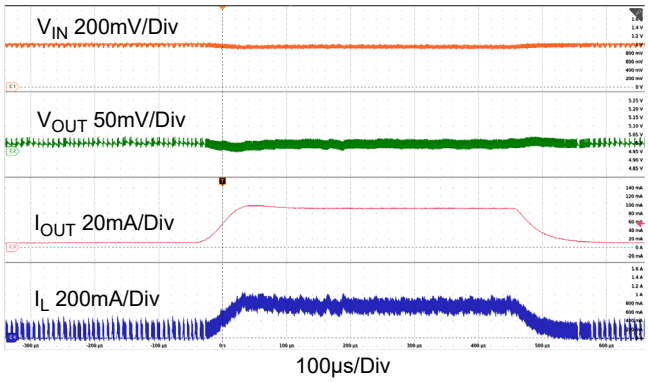


Figure 49. Load Transient: V_{IN} = 1.0V, V_{OUT} = 5.0V, I_{OUT} = 0.01A to 0.08A

5. Functional Description

The ISL9116B implements a complete boost switching regulator with a PWM controller, internal switches, references, protection circuitry, and control inputs. For more information, see the Block Diagram.

5.1 Enable Input

The device is enabled by asserting the EN pin high. Driving the EN LOW invokes Power-Down mode, in which most internal device functions are disabled. EN must remain LOW for at least 50µs for the device to be disabled. When the device is disabled by driving EN LOW, the output discharges naturally based on the load current.

Note: The I^2C interface is disabled when EN is LOW.

5.2 Startup

When the input voltage rises above the undervoltage lockout threshold, and EN is asserted HIGH, the power-on sequence starts. There are two startup phases, low and high voltage, which are determined by the V_{IN} voltage. Cycling of the EN pin, while VIN remains valid, restarts the power-on sequence.

5.2.1 Low-Voltage Startup

The low-voltage startup sequence occurs when V_{IN} < 1.8V (typical). The following outlines the sequence of behavior during low-voltage startup:

- A low-voltage startup circuit controls the power switch gates to boost V_{OUT} to an internal threshold voltage.
- One-Time Programmable (OTP) memory is read and loaded to registers.
- Switching starts, programmed soft-start begins, and V_{OUT} ramps to the target output voltage (V_{OUT} ≥ 1.8V)

5.2.2 High-Voltage Startup

The high-voltage startup sequence occurs when V_{IN} ≥ 1.8V (typical). The following outlines the sequence of behavior during high-voltage startup:

- The device always starts with the low-voltage startup phase but rapidly transitions into the high-voltage startup when V_{IN} ≥ 1.8V.
- One-Time Programmable (OTP) memory is read and loaded to registers.
- Pre-charge mode – V_{OUT} is raised to the V_{IN} level with a constant current source (no switching)
- Programmed soft-start begins. An internal reference (V_{REF}) begins ramping. Until it reaches the V_{IN} level, V_{OUT} is static. When it reaches the V_{IN} level, the controller begins normal switching, and V_{OUT} ramps to the target output voltage (V_{OUT} ≥ 1.8V).

5.3 Fault Protection

5.3.1 Fault Response

The device uses a Hiccup mode response to define fault scenarios. Hiccup mode behavior includes output shutdown (stops switching), I^2C is disabled, waiting for a 100ms hiccup timer (t_{FLT_WAIT}), and (re)starting through the normal start-up sequences that include reloading OTP. Hiccup mode may occur when in either low-voltage or high-voltage V_{IN} operation. The I^2C interface is unavailable when the device enters hiccup mode.

5.3.2 Overcurrent/Short-Circuit Protection

The ISL9116B provides overcurrent protection by monitoring the inductor current. The device enters Hiccup mode when the peak inductor current hits its current limit. During Hiccup mode, the device shuts down for 100ms and then tries to restart through the start-up sequences.

- Low-voltage phase – If it encounters the overcurrent condition again, it shuts down and tries to restart after another 100ms. This cycle repeats until there is no overcurrent, and V_{OUT} can return (≥ 1.8V).
- High-voltage phase – If it encounters the overcurrent condition again, it shuts down and tries to restart after another 100ms. *Note:* If the output cannot rise (for example, an output short), the device remains in pre-charge mode and delivers a constant current; see High-Voltage Startup.

OTP memory is read every time the part restarts, which overwrites any pre-existing register settings.

5.3.3 Thermal Shutdown

The ISL9116B features a thermal shutdown that protects the device from damage caused by overheating. An integrated temperature sensor circuit monitors the internal IC temperature. When the temperature exceeds the shutdown threshold (T_{SD}), the device enters Hiccup mode. During Hiccup mode, the device shuts down for 100ms and then tries to restart through the start-up sequences. OTP memory is read every time the part restarts, which overwrites any pre-existing register settings. The temperature is rechecked after the OTP is read. If the over-temperature condition remains, the device hiccups. If the condition has subsided, it starts up.

Note: The part only has a T_{SD} threshold and no hysteresis.

5.4 Boost Conversion Topology

The ISL9116B operates in either Boost or Bypass mode. When operating in conditions in which V_{IN} is close to V_{OUT}, the ISL9116B automatically switches from Boost mode to Bypass mode. For other conditions, the device performs Boost regulation.

Figure 50 shows a simplified diagram of the internal switches and the external inductor.

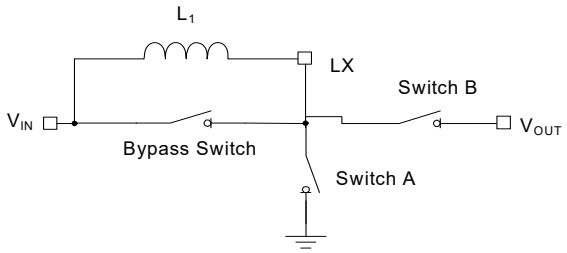


Figure 50. Boost Topology

5.5 Pulse Width Modulation (PWM) Operation

In Boost PWM mode, Switches A and B operate as a synchronous boost converter. Initially, Switch A is turned ON, and this ramps up the inductor current with a slope of V_{IN}/L. When the inductor current hits the upper threshold, as dictated by the hysteretic controller, Switch A is turned OFF. This is followed by a small dead time where both the switches are OFF. During this interval, the inductor current keeps flowing, finding its path through the body diode of Switch B. When the dead time is over, Switch B is turned ON, and the inductor current ramps down with a slope of $(V_{IN} - V_{OUT})/L$ (in boost mode, $V_{IN} < V_{OUT}$). When it hits the lower hysteretic threshold, Switch B is turned OFF, followed by another dead-time interval. After this, Switch A is turned ON again, and the entire sequence repeats.

The converter operates in PWM mode under two conditions:

- Load is sufficiently high in the Normal Mode (Auto PFM/PWM mode)
- Forced PWM mode is enabled by setting the FMODE bits in CONV_CFG register to 0x2.

The optimal switching frequency is determined by the hysteretic controller and is centered around 2.0MHz, for V_{IN} = 1.8V and V_{OUT} = 3.6V.

5.6 Pulse Frequency Modulation (PFM) Operation

During PFM operation in Boost mode, Switches A and B operate in discontinuous mode (DCM). Switch A is turned ON, followed by a dead-time, and then Switch B is turned ON. The inductor current ramps up and down, respectively, and the energy contained in this current pulse charges up V_{OUT}. After Switch B turns OFF, there is a period where both the switches remain OFF until V_{OUT} discharges down to the lower threshold of the hysteretic controller. The switching cycle repeats after that.

Multiple switching pulses are needed in most operating conditions to charge up the output capacitor. These pulses continue until V_{OUT} has achieved the upper threshold of the PFM hysteretic controller. Switching then stops and remains stopped until V_{OUT} decays to the lower threshold. As load increases, the frequency of PFM pulses increases as V_{OUT} gets discharged faster and needs to be recharged more often. This continues until the PFM pulses start bunching together, and the part then enters sustained PWM operation. The converter operates in PFM mode under only one condition: load is light enough in the Normal Mode (Auto PFM/PWM mode).

The PFM-PWM transition, going from light to heavy load and then back to light load, has a hysteretic band, allowing for a seamless PFM to PWM and PWM to PFM transition.

5.7 Operation with V_{IN} Close to V_{OUT}

When the output voltage is close to the input voltage, the ISL9116B rapidly and smoothly switches between Boost and Bypass modes to maintain the regulated output voltage. This behavior provides excellent efficiency and very low output voltage ripple. There is no overcurrent limit protection in auto-bypass mode.

5.8 Forced Operating Modes

Forced PWM mode is the only forced operating mode, and it is selected using the FMODE bits in the CONV_CFG register (See Table 5 for details). The power-up default mode is Normal operation with automatic transitions to optimize efficiency. If V_{IN} approaches V_{OUT}, switching instances reduce and smoothly transition from switching to Bypass mode.

Forced PWM mode can be selected to minimize the switching frequency variation and to obtain a tight V_{OUT} accuracy, although this comes at the expense of increased input current.

5.9 I^2C Serial Interface

The ISL9116B supports a bidirectional bus-oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master, and the device being controlled is the slave. The master always initiates data transfers and provides the clock for transmitting and receiving operations. Therefore, the device operates as a slave in all applications.

The IC supports the following data transfer rates and modes as defined in the I^2C specification:

- Up to 100kbit/s in Standard mode
- Up to 400kbit/s in Fast mode

All communication over the I^2C interface is conducted by sending the MSB of each data byte first.

The I^2C pull-up voltage may be from 1.8V to 5.5V. However, input quiescent current increases by up to 1µA (typical) and 3µA (maximum) if the I^2C pull-up voltage is less than the larger of V_{IN} and V_{OUT}. There is no increase in the quiescent current if the I^2C pins are pulled down to ground.

5.9.1 Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. The SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 51). At power-up, the SDA pin is in input mode.

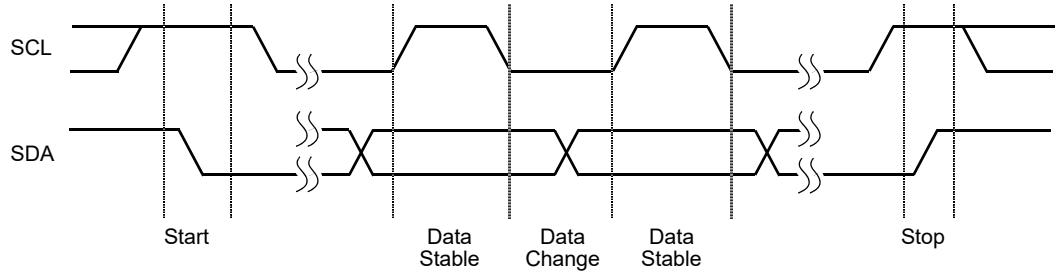


Figure 51. Valid Data Changes, Start, and Stop Conditions

All I^{2}C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA, while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 51). A START condition is ignored during the power-up sequence and when EN input is low.

All I^{2}C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 51).

An acknowledge (ACK) is a software convention that indicates a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 52), and the data is latched in and responded to by the device.

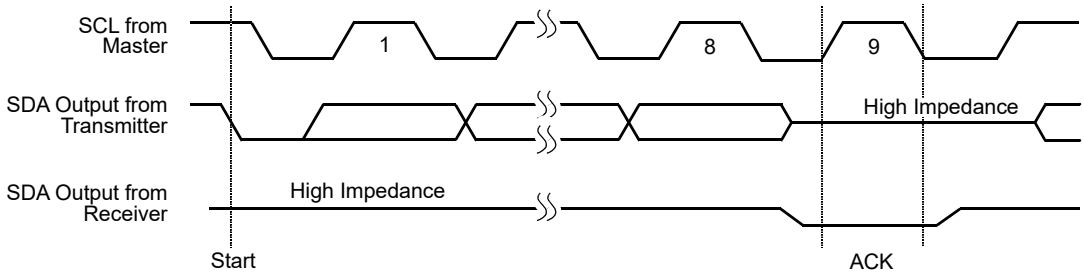


Figure 52. Acknowledge Response from Receiver

The device responds with an ACK after recognizing a START condition followed by a valid 7-bit slave address and once again after successfully receiving a register address byte. The device also responds with an ACK after receiving a data byte of a write operation. The master must respond with an ACK after receiving a data byte of a read operation.

For the base version of ISL9116B, the 7-bit slave address is set in trim to 0x1B. The 7-bit address is followed by a Read/$\overline{\text{Write}}$ bit whose value is 1 for a Read operation and 0 for a Write operation (see Table 1).

Table 1. 7-Bit Address Format

0	0	1	1	0	1	1	R/$\overline{\text{W}}$
(MSB)							(LSB)

5.9.2 Write Operation

Write operations are shown in Figure 53. A write operation requires a START condition followed by a valid 7-bit slave address with the R/$\overline{W}$ bit set to 0, a valid register address byte, one or more data bytes, and a STOP condition. After each of the bytes, the device responds with an ACK. After each data byte is acknowledged, the device increments its register address to support block writes. The master sends a STOP to complete the command.

The master must send STOP conditions that terminate write operations after sending at least one full data byte and its associated ACK signal. If a STOP condition is issued in the middle of a data byte or before one full data byte + ACK is sent, the device ignores the command and does not change the output voltage or other settings.

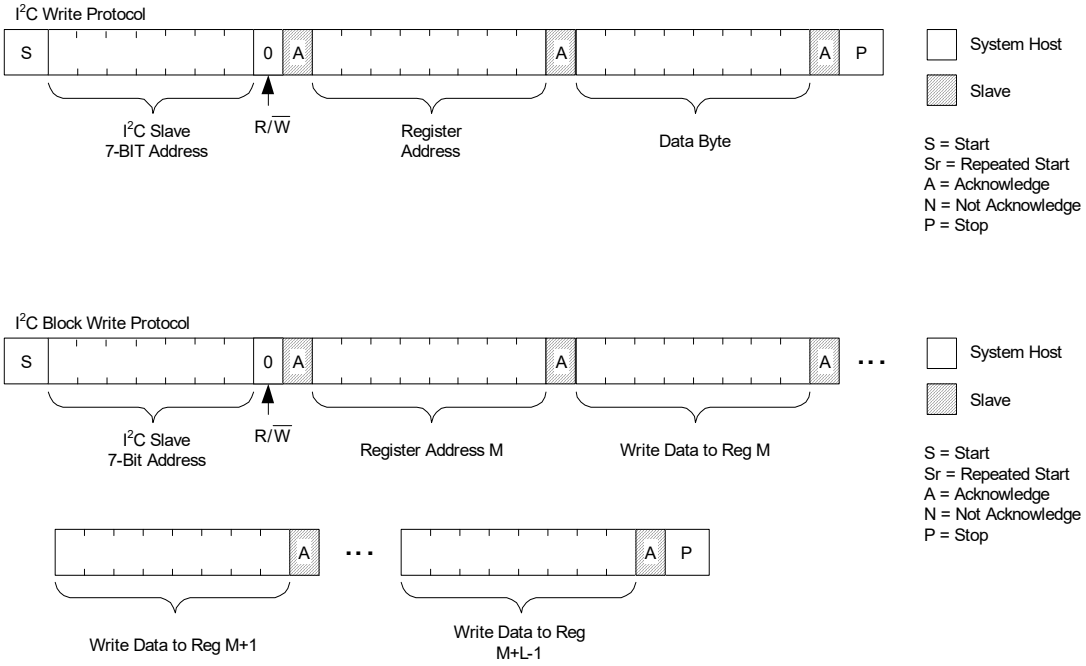


Figure 53. I^{2}C Register Write Protocols

5.9.3 Read Operation

Read operations are shown in Figure 54. They consist of four or more bytes. The host generates a START condition and then transmits the 7-bit slave address with the R/$\overline{W}$ bit set to 0. The device responds with an ACK. The host then transmits the register address byte, and the device responds with another ACK.

The host then generates a repeat START condition and transmits the 7-bit slave address with the R/$\overline{W}$ bit set to 1. The device responds with an ACK, indicating it is ready to provide the requested data.

The device then transmits the data byte by asserting control of the SDA pin while the host generates clock pulses on the SCL pin. After each data byte is complete, the host generates an ACK condition. After every successfully transmitted data byte, the ISL9116B automatically increments its internal register address to support block reads. The host terminates the Read operation by issuing a NACK and sending a STOP condition.

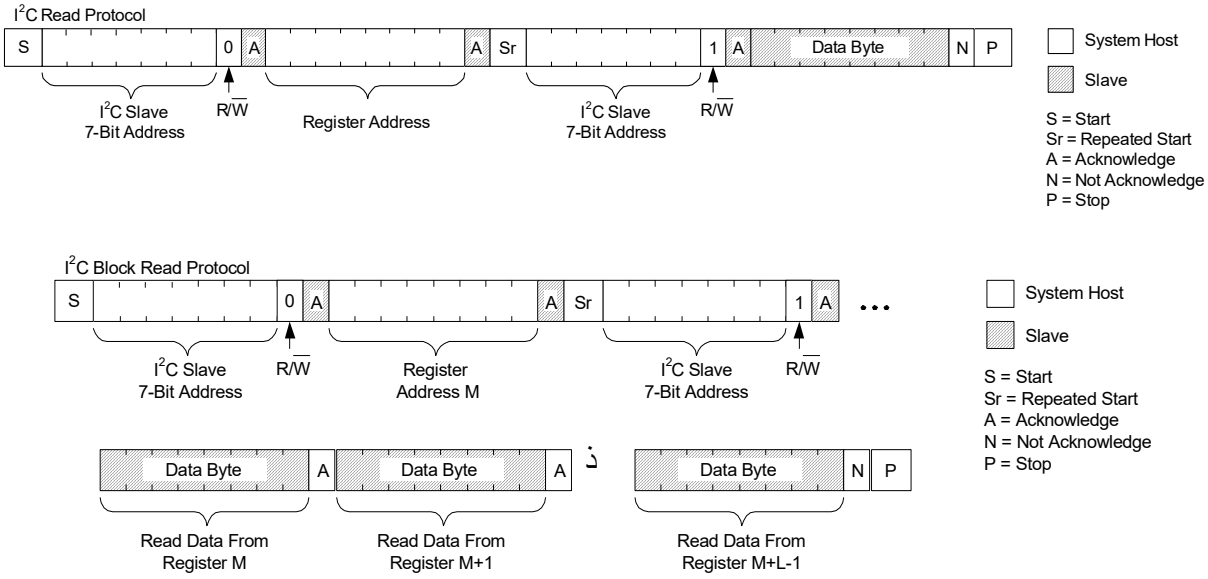


Figure 54. I²C Register Read Protocols

6. Register Descriptions

The ISL9116B has I²C accessible control registers whose functions are described in Table 3 through Table 5. These registers can be accessed any time the device is enabled. When the ISL9116B is disabled (EN = LOW), in hiccup mode, or loading OTP, attempts to communicate through its I²C interface are not supported.

6.1 RO_REG1

The RO_REG1 register contains the hardware identification bits as described in Table 2.

Table 2. Register Address 0x02: RO_REG1

Bit	Name	Type	Reset	Description
7:6	FAMILY_ID[1:0]	R	0x0	Chip family identifier 0x0 = ISL9122 stand-alone converter family
5:3	HW_REV[2:0]	R	0x3	Chip revision level 0x3 = Hardware revision D
2:0	RAIL_VAR[2:0]	R	0x3	Converter variant identifier 0x3 = Low voltage input Boost (ISL9116B)

6.2 INTFLG_REG

The INTFLG_REG register contains fault flags. Each bit represents a different type of fault, as described in Table 3. A 0 indicates no fault, and a 1 indicates a fault. Each bit is set by a fault event and is cleared when read. When a fault flag is read back and asserted (1), it indicates a fault occurred in the past. Read the flag again to examine the current IC status – occurring in the time between the first and second I²C read. Continuing to poll the flags provides period updates of the IC status relative to the previous read-back.

Table 3. Register Address 0x03: INTFLG_REG

Bit	Name	Type	Reset	Description
3	INT3	R	0x0	Voltage setting under-range. Sets to 1 when VSET changes from within the 0x48-0xD7 range to below 0x48.
2	INT2	R	0x0	Voltage setting over-range. Sets to 1 when VSET changes from within the 0x48-0xD7 range to above 0xD7.

6.3 VSET

The VSET register contains the output voltage setting in 25mV steps, as shown in Equation 1.

(EQ. 1) $V_{OUT} = VSET \times 0.025V$

VSET can be changed after the IC is enabled and operating. When the output voltage is changed, it ramps at the rate set in the DVSRATE bits of the CONV_CFG register.

The output voltage range is digitally limited to be between the minimum and maximum values shown in Table 4. Setting values above or below the limits results in the output voltage ramping to the limit and the appropriate overvoltage or undervoltage interrupt flag in INTFLG_REG being set. The limits described in the Recommended Operating Conditions should be followed while setting the output voltage.

Table 4. Register Address 0x11: VSET

Bit	Name	Type	Reset[1]	Description
7:0	VSET[7:0]	R/W	-	Output voltage setting (25mV steps): Minimum limit = 1.8V (0x48) Maximum limit = 5.375V (0xD7)

1. For part specific default output voltage, see the Ordering Information table.

6.4 CONV_CFG

The CONV_CFG register settings are described in Table 5.

Table 5. Register Address 0x12: CONV_CFG

Bit	Name	Type	Reset	Description
7	Reserved	RW	0x1	Reserved. Do not use.
6	Reserved	RW	0x0	Reserved. Do not use.
5:4	DVSRATE[1:0]	RW	0x0	Dynamic Voltage Scaling slew rate is applied when the output voltage setting is changed. 0x0 = 3.125mV/µs 0x1 = 6.25mV/µs 0x2 = 0.78125mV/µs 0x3 = 1.5625mV/µs
3:2	FMODE[1:0]	RW	0x0	Forced operating modes. 0x0 = Normal operation with automatic mode transitions. 0x1 = Reserved. **DO NOT USE** this combination 0x2 = Forced PWM mode with no PFM operation. 0x3 = Reserved. **DO NOT USE** this combination

Table 5. Register Address 0x12: CONV_CFG (Cont.)

1	CONV_RSVD	RW	0x1	Reserved. Do not use.
0	TYPE1	RW	0x1	0x0 = Type I error amplifier for best transient response with voltage positioning 0x1 = Type II error amplifier for best steady state voltage accuracy.

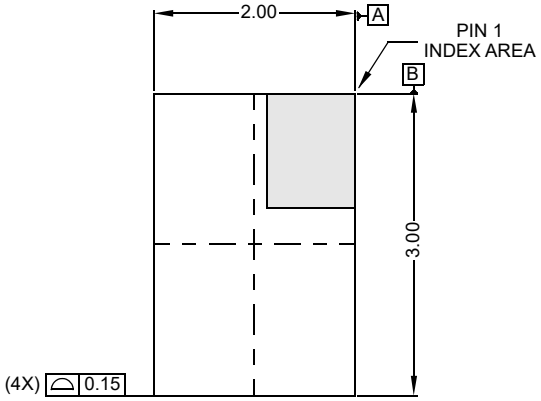
7. Package Outline Drawing

For the most recent package outline drawing, see L8.2x3

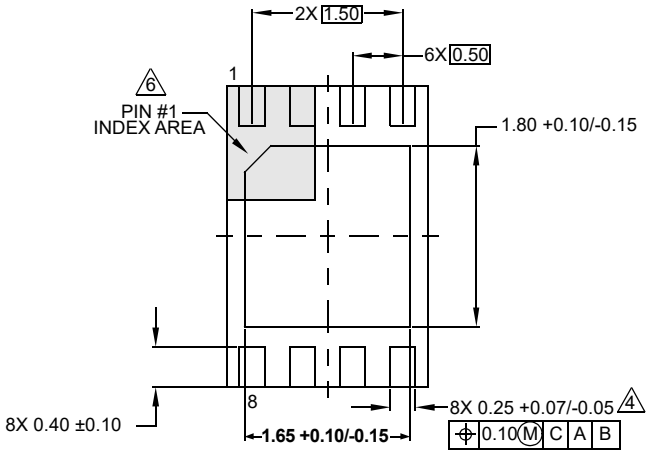
L8.2x3

8 Lead Dual Flat No-Lead Plastic Package

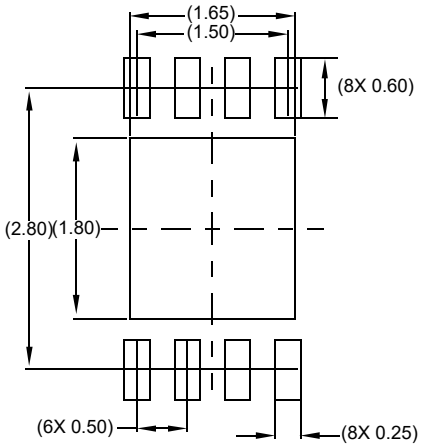
Rev 2, 3/15



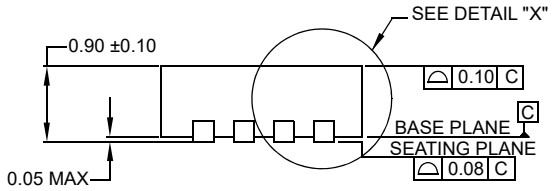
TOP VIEW



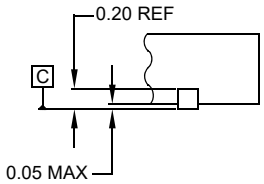
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. **Dimensions are in millimeters.**
   Dimensions in ( ) for Reference Only.
2. **Dimensioning and tolerancing conform to ASME Y14.5m-1994.**
3. **Unless otherwise specified, tolerance : Decimal ± 0.05**
4. **Dimension applies to the metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip.**
5. **Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).**
6. **The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.**
7. **Complies to JEDEC MO-229 VCED-2.**

8. Ordering Information

Part Number[1]	Part Marking	Default V_{OUT} (V)	I^2C Address	Package Description[2] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp Range
ISL9116BIRNZ-T[4]	B16	3.3	0x1B	8 Lead DFN	L8.2x3	Reel, 6k	-40 to +85°C
ISL9116BIRN-EVZ	Evaluation Board for ISL9116BIRNZ						

1. For Moisture Sensitivity Level (MSL), see the ISL9116B device page. For more information about MSL, see TB363.
2. For the Pb-Free Reflow Profile, see TB493.
3. See TB347 for details on reel specifications.
4. Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

9. Revision History

Rev.	Date	Description
1.01	Jan 12, 2024	Update labels on Figures 19, 33, 34, and 38. Updated titles for Figures 46 through 49.
1.00	Dec 18, 2023	Initial release

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