To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Renesas Technology Corp.

DESCRIPTION

M66011 Semiconductor Integrated Circuit is a serial bus controller. It converts 2-byte parallel data that arrives from microcomputer into serial and outputs it to serial bus. It also converts serial data input from serial bus into parallel and outputs it to microcomputer.

The M66011 is used for the extension of microcomputer I/O ports and two-way communication with peripheral equipment connected with serial buses.
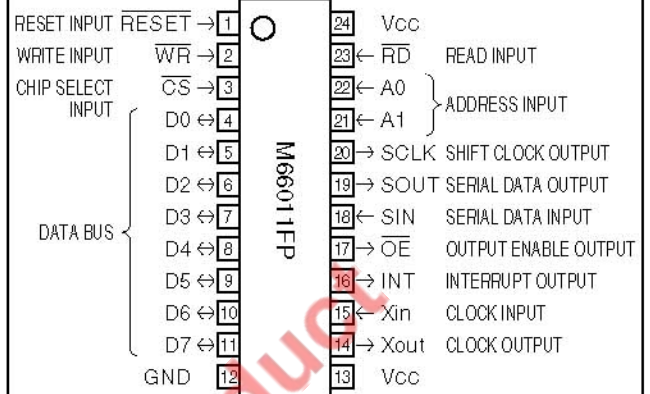
FEATURES

* Compatible with general-purpose 8-bit microprocessor busses
* TTL level input (one microcomputer side)
* Interrupt output
* Schmitt input ($\overline{RESET}$, $\overline{CS}$, SIN)
* Low power dissipation
* Wide operating temperature range (Ta = −20 to 75˚C)

APPLICATION

Microcomputer I/O port extension, etc.

PIN CONFIGURATION (TOP VIEW)

RESET INPUT	$\overline{RESET}$ →	1	24	Vcc
WRITE INPUT	$\overline{WR}$ →	2	23	← $\overline{RD}$ READ INPUT
CHIP SELECT INPUT	$\overline{CS}$ →	3	22	← A0
	D0 ↔	4	21	← A1 ADDRESS INPUT
	D1 ↔	5	20	→ SCLK SHIFT CLOCK OUTPUT
	D2 ↔	6	19	→ SOUT SERIAL DATA OUTPUT
DATA BUS	D3 ↔	7	18	← SIN SERIAL DATA INPUT
	D4 ↔	8	17	→ $\overline{OE}$ OUTPUT ENABLE OUTPUT
	D5 ↔	9	16	→ INT INTERRUPT OUTPUT
	D6 ↔	10	15	← Xin CLOCK INPUT
	D7 ↔	11	14	→ Xout CLOCK OUTPUT
	GND	12	13	Vcc

M66011FP

Outline 24P2N-B

BLOCK DIAGRAM

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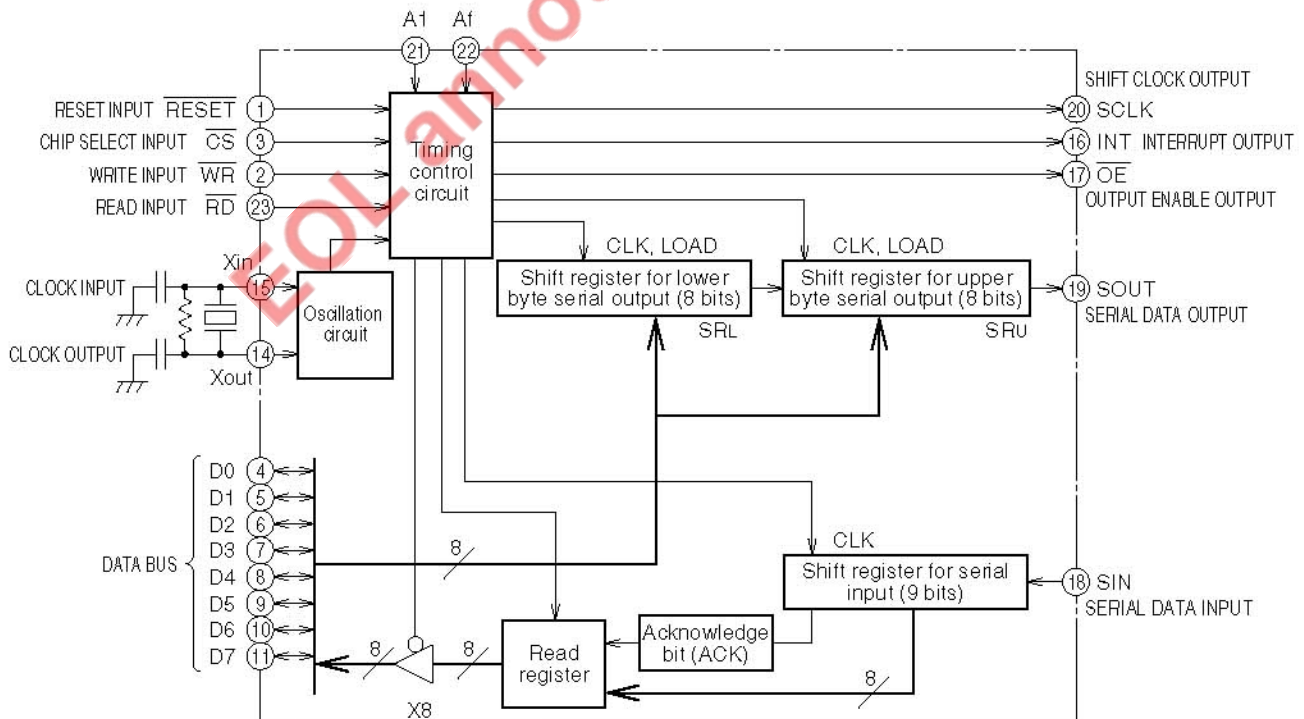
FUNCTION

M66011 integrated circuit is a serial bus controller. It is equipped with two 8-bit shift registers used to convert parallel input data into serial for output, as well as with one 9-bit shift register used to convert serial input data into parallel for output.

This IC receives and sends 8-bit parallel in communication with microcomputer. In communication with serial bus, it outputs 16-bit data and receives 9-bit data.

Serial data input/output uses four signal lines: shift clock output SCLK, serial data output SOUT, serial data input SIN and output enable output $\overline{OE}$.

Serial data is output synchronously with shift clock fall edges, while input of serial data is synchronous with shift clock rise edges.

Serial communication data consists of one prefixed acknowledge bit and 8 data bits.

PIN DESCRIPTIONS

Pin	Name	Input/Output	Functions
$\overline{RESET}$	Reset input	Input	"L" level: M66011 is reset to initial state.
$\overline{CS}$	Chip select input	Input	"L" level: M66011 becomes accessible.
$\overline{WR}$	Write input	Input	"L" level: 8-bit parallel data is input from data bus and written on M66011.
$\overline{RD}$	Read input	Input	"L" level: Serial-input 8-bit data or internal status data is output in parallel to data bus.
D0~D7	Data bus	Input/Output	Bi-directional 8-bit bus buffer. Used for communication with microcomputer (data write and read).
SCLK	Shift clock output	Output	Outputs clock to serial bus. Active ("H") status normally.
SOUT	Serial date output	Output	Outputs serial data to serial bus. Active ("H") status normally.
SIN	Serial data input	Input	Inputs serial data from serial bus.
$\overline{OE}$	Output enable output	Output	"L" when serial data communication is executed. Active ("H") otherwise.
INT	Interrupt output	Output	Outputs interrupt command signal to microcomputer when serial data communication is finished.
A0, A1	Address input	Input	Selects register on which data is written during write operation. Designates data to be read during read operation.
Xin	Clock input	Input	Connected to ceramic resonator, generates M66011 activation clock and SCLK output clock.
Xout	Clock output	Output	If clock is input from outside, use pin Xin and keep pin Xout open.
Vcc	Positive supply pin	—	Connected positive supply (5V).
GND	Grounding pin	—	Used for grounding (0V).

OPERATION

1. Write operation

(1) Serial output data setting

The M66011 has two built-in 8-bit shift registers. They are used to set serial output data.

When the address setting is (A1, A0) = (0, 1), 8-bit data on data bus is written on the upper byte serial output shift register (SRU). When the address setting is (A1, A0) = (0, 0), the data is written on the lower byte serial output shift register (SRL). In either case, data write starts when $\overline{WR}$ is on the "L" level.

(2) Status register setting

When the address setting is (A1, A0) = (1, 1), written data becomes the setting of status register in M66011. (Refer to the table below.)

Write Operation Basic Functions (Note 1)

$\overline{CS}$	A1	A0	$\overline{RD}$	$\overline{WR}$	Functions		
0	0	0	1	0	• Lower byte serial output shift register	←	Data bus data
0	0	1	1	0	• Upper byte serial output shift register	←	Data bus data
0	1	1	1	0	• Shift clock divider ratio register • Interrupt output control register	←	(Note 2) Data bus data

Note 1: Figure "0" indicates "L" level, while "1" indicates "H" level.

Note 2:

D7	D6	D5	D4	D3	D2	D1	D0

Don't care

Don't care

D1	D0	Divider ratio
0	0	1/2
0	1	1/4
1	0	1/8
1	1	1/16
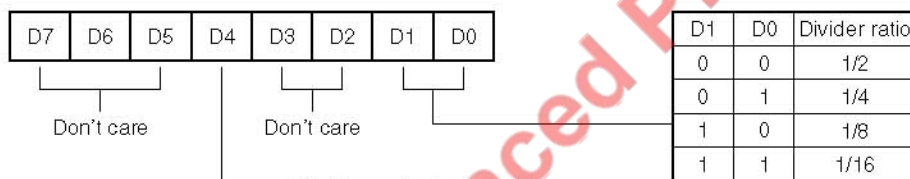
"0": Interrupt output disable
(INT output is fixed to "L".)
"1": Interrupt output enable
(INT output shifts from "L" to "H" when serial communication is completed.)
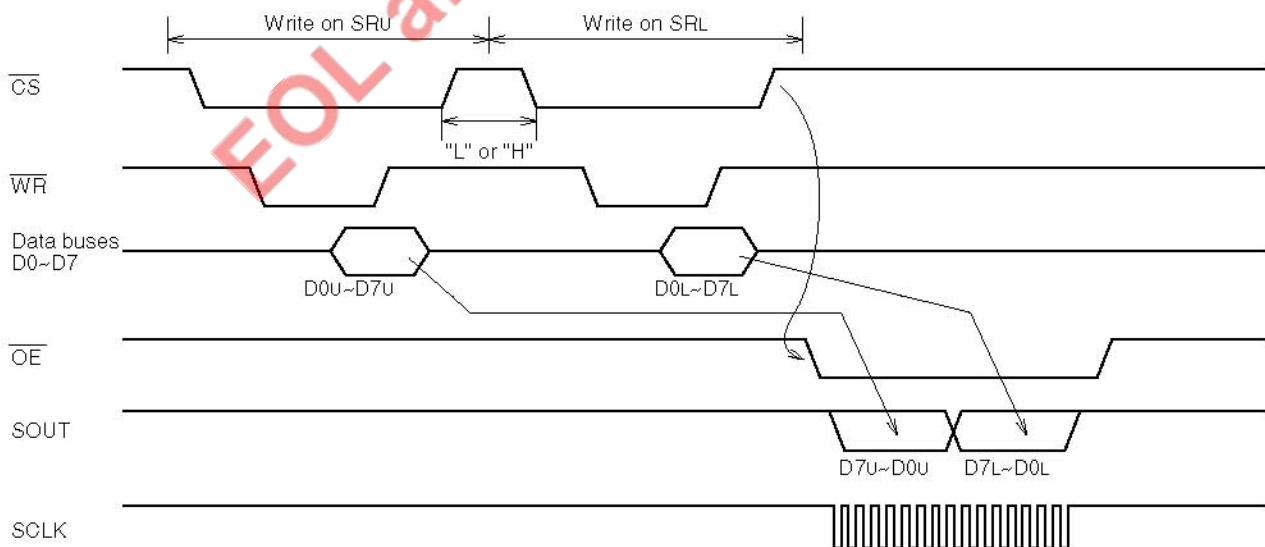
Write Operation Basic Timing (Serial Output Data Setting)

2. Read operation

When a read access arrives, M66011 outputs data in parallel to data bus. The data output at this moment may be serial input data, or data on internal status resister.

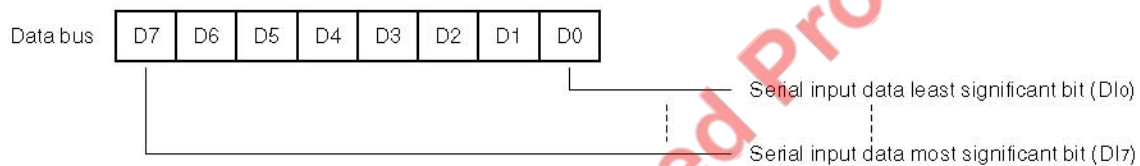When a read access arrives when the address setting is (A1, A0) = (1, 0), 8-bits of 9-bit serial input data, excluding the acknowledge bit, is output to data bus While $\overline{RD}$ is "L".

When a read access arrives when the address setting is (A1, A0) =(1, 1), interrupt control register, busy flag, serial-input acknowledge bit and clock dividing ratio register are output to data bus while $\overline{RD}$ is "L".
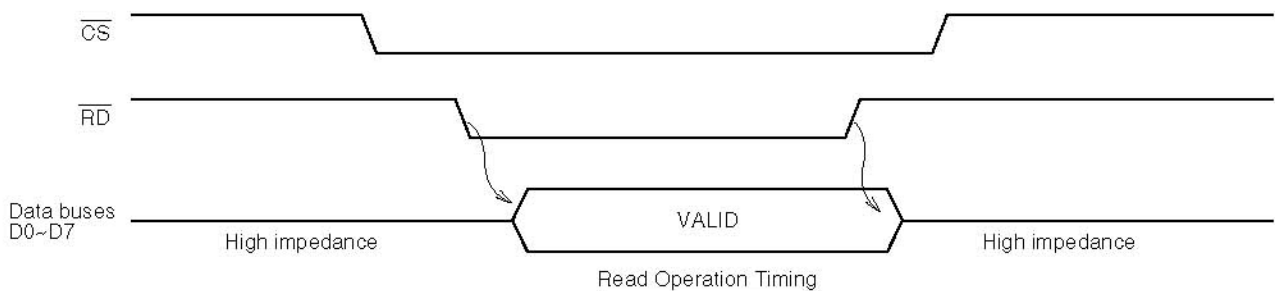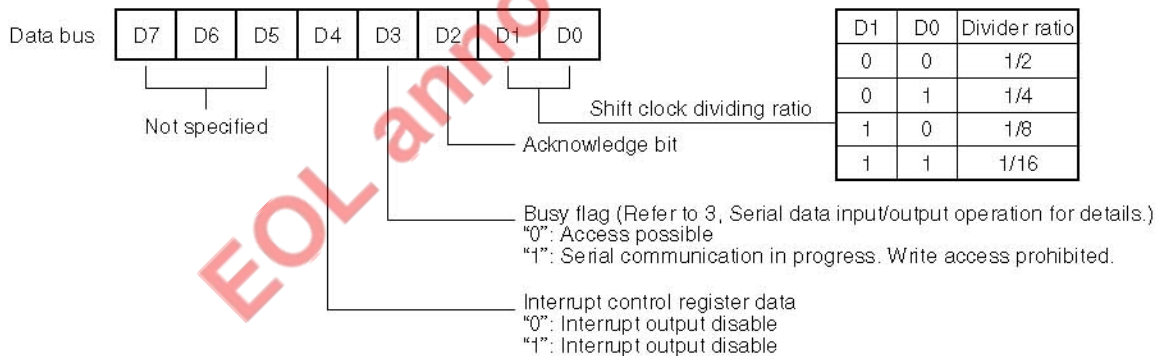
Read Operation Basic Function

$\overline{CS}$	A1	A0	$\overline{RD}$	$\overline{WR}$	Functions		
0	1	0	0	1	Date bus	←	Serial input shift register
0	1	1	0	1	Data bus	←	Status register

Read Output Data Details
(1)When (A1, A0) is (1, 0):

(2)When (A1, A0) is (1, 1):

D1	D0	Divider ratio
0	0	1/2
0	1	1/4
1	0	1/8
1	1	1/16

Not specified

Shift clock dividing ratio

Acknowledge bit

Busy flag (Refer to 3, Serial data input/output operation for details.)
"0": Access possible
"1": Serial communication in progress. Write access prohibited.

Interrupt control register data
"0": Interrupt output disable
"1": Interrupt output disable

Read Operation Timing

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3. Serial data input/output operation

A cycle of 16-bit serial output data setting and serial data communication starts with a write access given by microcomputer to transmission shift registers in M66011.

M66011 has two 8-bit shift registers, on for upper byte (SR∪), the other for lower byte (SRL). If the $\overline{CS}$ status rises from "L" to "H" after a write access is given to SRL, serial data communication is started. SR∪ 8-bit data and SRL, 8-bit data are output in series in this order. Output of each data starts from its most significant bit.

At the $\overline{CS}$ rise edge, busy flag in M66011 is set, and $\overline{OE}$ output shifts from "H" to "L". Shift clock SCLK and serial data SOUT are then output.

At SCLK fall edges, serial output shift register executes shifting operation, and data on shift register is output in series from pin SOUT. Serial input data from pin SIN is taken into input shift register at SCLK 8T thru 16T rise edges. However, data taken in at 8T rise edge is processed as acknowledge bit, while data taken in at 9T thru 16T rise edges are processed as data bits.

After the SCLK 16T rise edge, the status of SOUT and $\overline{OE}$ shifts to "H" after one bit's delay of SCLK, and busy flag is reset. When interrupt output is being set to enable, INT output is set.

(Remarks)
(1) If $\overline{CS}$ rises after write operation is executed on SRL only and not on SR∪, SR∪ data is unstable.
(2) When write operations executed on SRL, M66011 becomes ready for start of serial communication and stands by for detection of $\overline{CS}$ rise. However, if a read access is given after data is written on SRL while $\overline{CS}$ is maintained on "L" level, this standby status is canceled. To resume serial communication in this case, rewrite data on SRL and raise $\overline{CS}$.
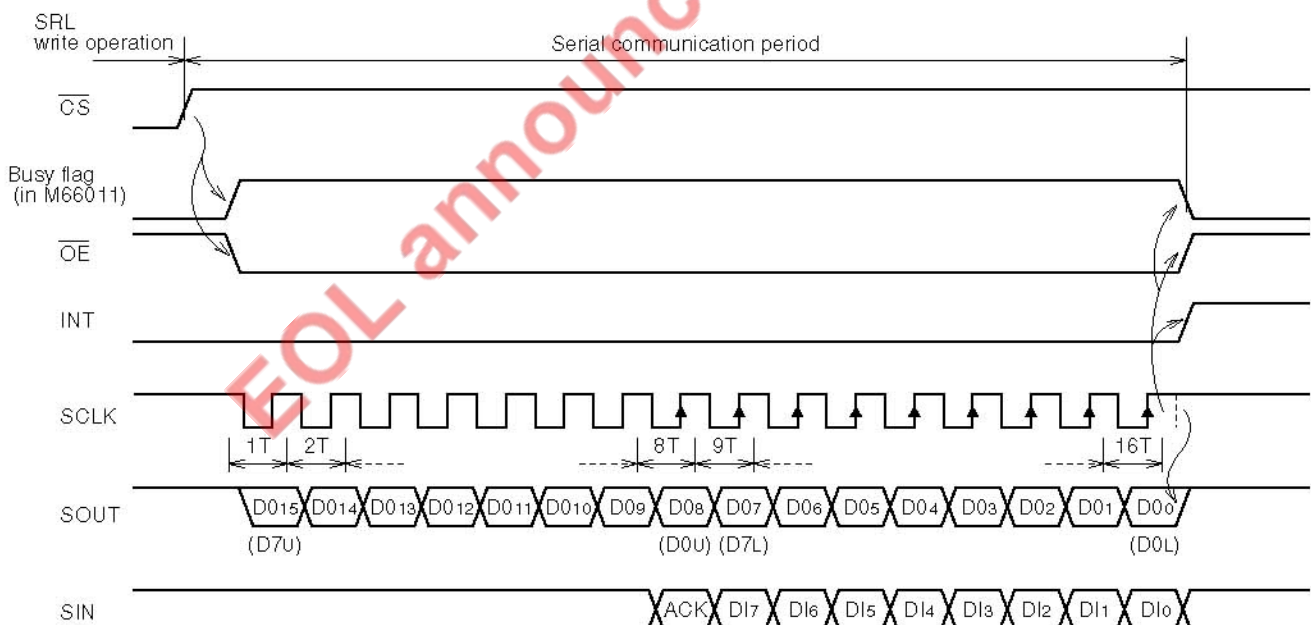
Serial Communication Timing Chart

4. Shift clock output

Shift clock output pin (SCLK) outputs clock pulses generated by ceramic resonator oscillation circuit connected between pins X_{in} and X_{out}, or divided clock pulses input via pin X_{in} from external clock. The dividing ratio can be selected from among 1/2, 1/4, 1/8 and 1/16.

5. Interrupt output

When interrupt output control register is set to "1" (interrupt output enable), the status of this output shifts from "L" to "H" at the end of a serial communication cycle, and an interrupt command is given to microcomputer. Interrupt output "H" is reset when read accessed.

When interrupt output control register is set to "0" (interrupt output disable), the status of this output is retained on the "L" level.

6. Conditions when reset

If "L" is input to RESET, M66011 are put under the conditions as specified below:

Pin name	Status
OE, SCLK and SOUT outputs	Active ("H")
Internal busy flag	Reset ("L")
Acknowledge bit register	Set ("H")
INT output	Disable (continuous "L" output)
Divider ratio	1/2

7. Oscillation circuit

An example of circuit connection and circuit constants are given below for the case where a ceramic resonator is used.
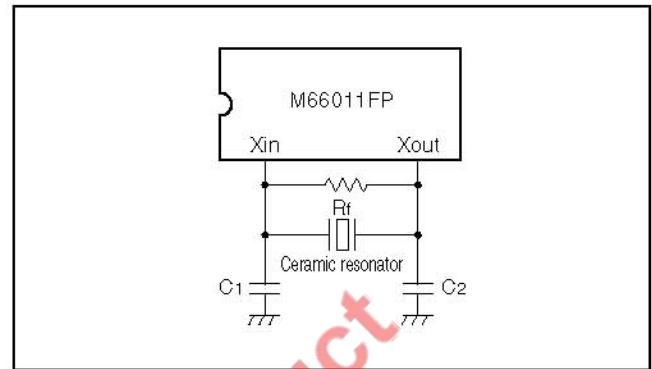
Clock Oscillation Circuit

Maker	Ceramic resonator	Frequency (MHz)	C1 (pF)	C2 (pF)	Rf (MΩ)
Murata Mfg.	CSA4.00MG 040	4.0	100	100	1.0
	CST4.00MGW 040	4.0	100 (built-in)	100 (built-in)	1.0
	CSA8.00MT	8.0	30	30	1.0
	CSA8.00MTW	8.0	30 (built-in)	30 (built-in)	1.0

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
Vcc	supply voltage	−0.5 ~ +7.0	V
VI	Input voltage	−0.5 ~ Vcc + 0.5	V
Vo	Output voltage	−0.5 ~ Vcc + 0.5	V
Pd	Power dissipation	500	mW
Tstg	Storage temperature	−60 ~ 150	°C

RECOMMENDED OPERATIONAL CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vcc	Supply voltage	4.5	5.0	5.5	V
VI	Input voltage	0		Vcc	V
Vo	Output voltage	0		Vcc	V
Topr	Operating temperature	−20		75	°C

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ 75°C, Vcc = 5V ± 10% and GND = 0V unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
VIH	"H" input voltage	$\overline{WR}$, $\overline{RD}$, A0, A1,		2.0			V
VIL	"L" input voltage	D0~D7				0.8	V
VIH	"H" input voltage	Xin		Vcc×0.8			V
VIL	"L" input voltage					Vcc×0.2	V
VT+	Positive threshold voltage					2.4	V
VT−	Negative threshold voltage	$\overline{RESET}$, $\overline{CS}$, SIN		0.7			V
Vh	Hysteresis width				0.6		V
VOH	"H" output voltage	D0~D7, SCLK,	IOH=−4mA	Vcc−0.8			V
VOL	"L" output voltage	INT, SOUT, $\overline{OE}$	IOL=4mA			0.4	V
II	Input leak current		VI=0~Vcc			±10	μA
Ioz	Output leak current in off state	D0~D7	Vo=0~Vcc			±10	μA
Icc	Quiescent supply current		VI=Vcc, GND output open			200	μA
CI/O	Input/output pin capacitance	D0~D7				20	pF

Note 3: Standard value measuring conditions: Ta = 25°C and Vcc =5V

## TIMING CONDITIONS (Ta = −20 ~ 75°C, Vcc = 5V ± 10%, GND = 0V)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_c(\phi)$	Clock cycle		120		520	ns
$tWH(\phi)$	Clock "H" pulse width			$t_c(\phi)/2$		ns
$tWL(\phi)$	Clock "L" pulse width			$t_c(\phi)/2$		ns
$tr(\phi)$	Clock rise time				20	ns
$tf(\phi)$	Clock fall time				20	ns
$tW(\overline{R})$	Read pulse width		100			ns
$tW(\overline{W})$	Write pulse width		100			ns
$tsu(\overline{CS}-\overline{R})$	Chip select setup time before read		0			ns
$tsu(A-\overline{R})$	Address setup time before read		0			ns
$tsu(\overline{CS}-\overline{W})$	Chip select setup time before write		0			ns
$tsu(A-\overline{W})$	Address setup time before write		0			ns
$tsu(D-\overline{W})$	Data setup time before write		40			ns
$th(\overline{R}-CS)$	Chip select hold time after read		0			ns
$th(\overline{R}-A)$	Address hold time after read		0			ns
$th(\overline{W}-\overline{CS})$	Chip select hold time after write		0			ns
$th(\overline{W}-A)$	Address hold time after write		0			ns
$th(\overline{W}-D)$	Data hold time after write		0			ns
$tsu(SI-CK)$	Serial data setup time		100			ns
$th(CK-SI)$	Serial data hold time		100			ns
$tBUSY$	Internal processing time after write				$5t_c(\phi)$	ns
$tWH(\overline{CS})$	Chip select "H" time at serial communication start up		$5t_c(\phi)$			ns

SWITCHING CHARACTERISTICS (Ta = −20 ~ 75°C, Vcc = 5V ± 10%, GND = 0V)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
$tPZH(\overline{R}-D)$ $tPZL(\overline{R}-D)$	Data output enable time after read					80	ns
$tPHZ(\overline{R}-D)$ $tPLZ(\overline{R}-D)$	Data output disable time after read		CL=150pF RL=2KΩ (Note 4)	5		50	ns
$tPLH$, $tPHL$	Serial output propagation delay time	SCLK-SOUT				60	ns
		$\overline{OE}$-SCLK		$t_c(\phi)+20$			ns
		SCLK-$\overline{OE}$			$\dfrac{n \cdot t_c(\phi)}{2}$		ns

n: Divider ratio

NOTE 4: TEST CIRCUIT
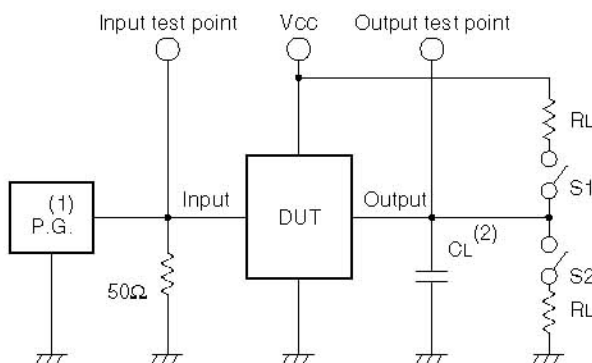
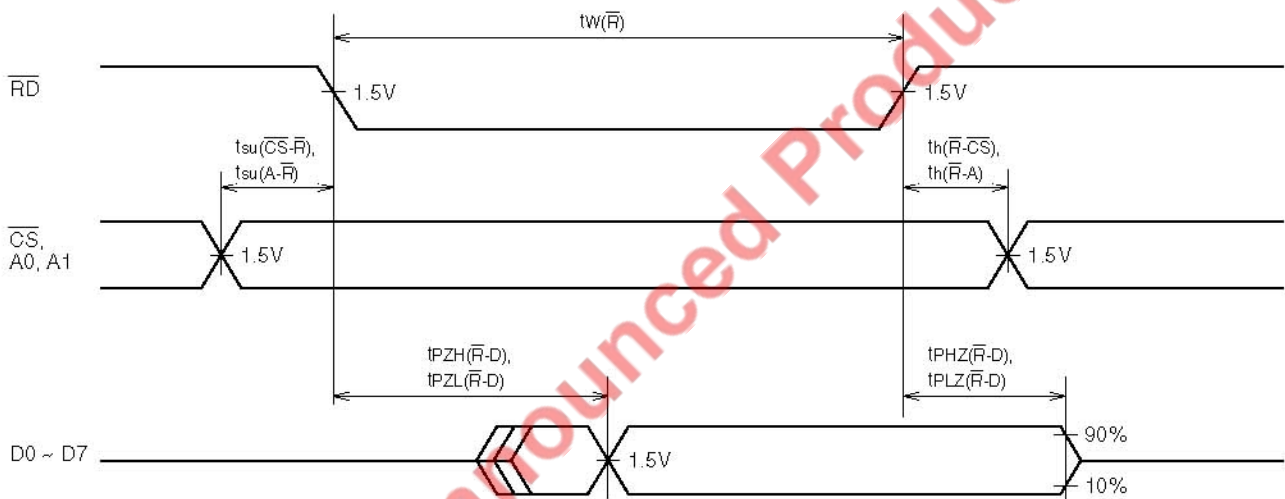| Symbol	S1	S2
$tPZH(\overline{R}-D)$	Open	Closed
$tPZL(\overline{R}-D)$	Closed	Open
$tPHZ(\overline{R}-D)$	Open	Closed
$tPLZ(\overline{R}-D)$	Closed	Open
$tPLH$, $tPHL$	Open	Open

(1) Pulse generator (PG) characteristics: tr=tf=6ns, Zo=50Ω
(2) Capacitance CL includes connection floating capacitance and probe input capacitance.

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TIMING CHARTS
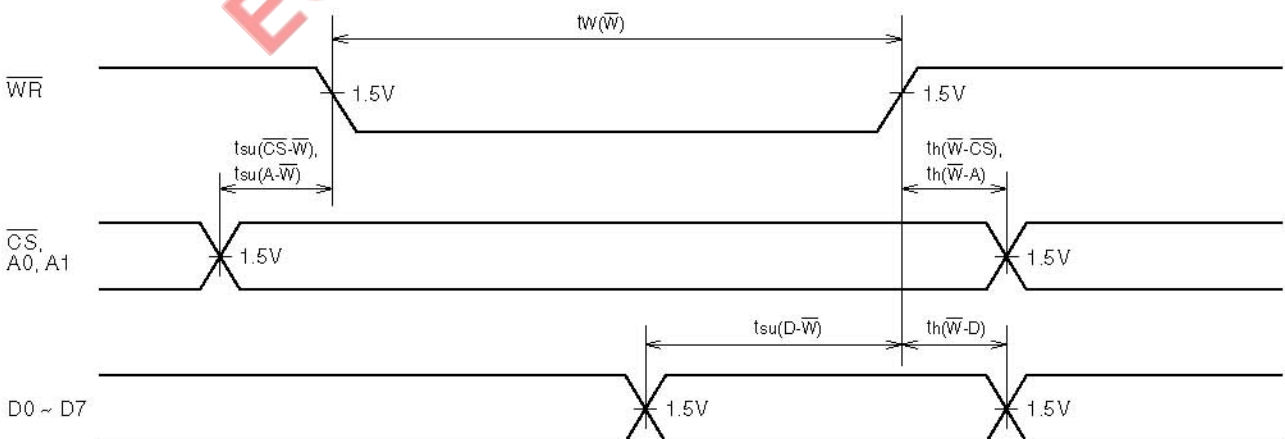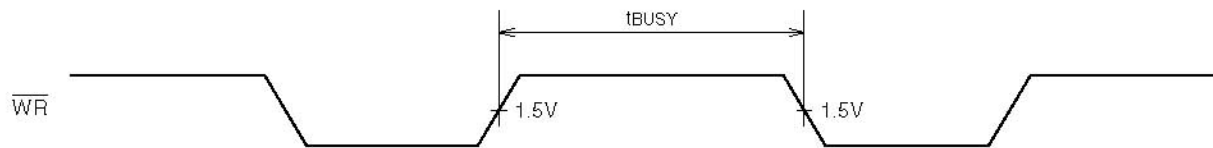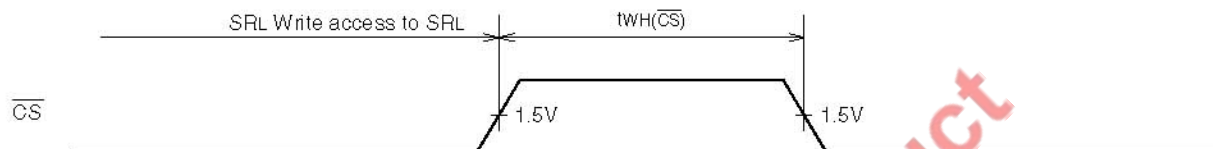
Clock timing
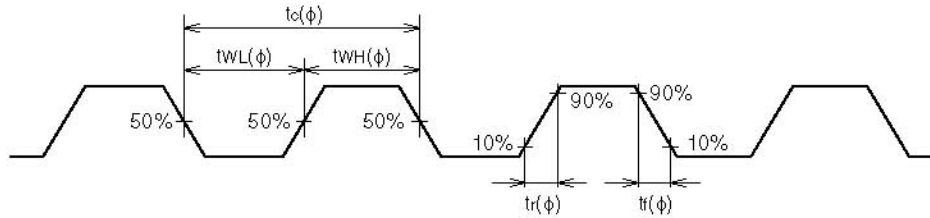
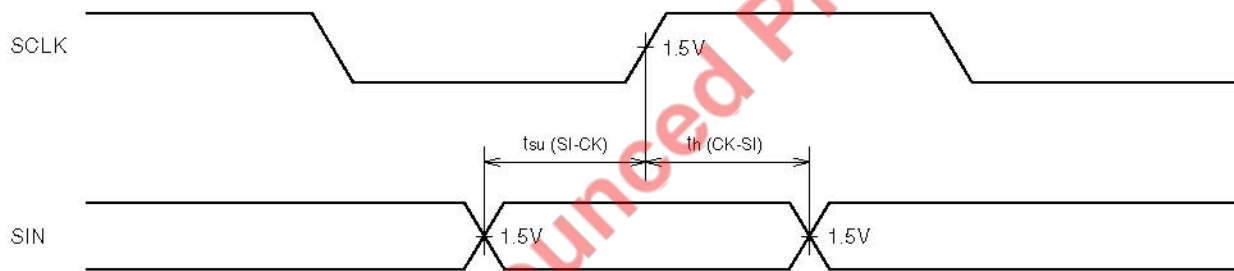### Read operation timing

Write operation timing

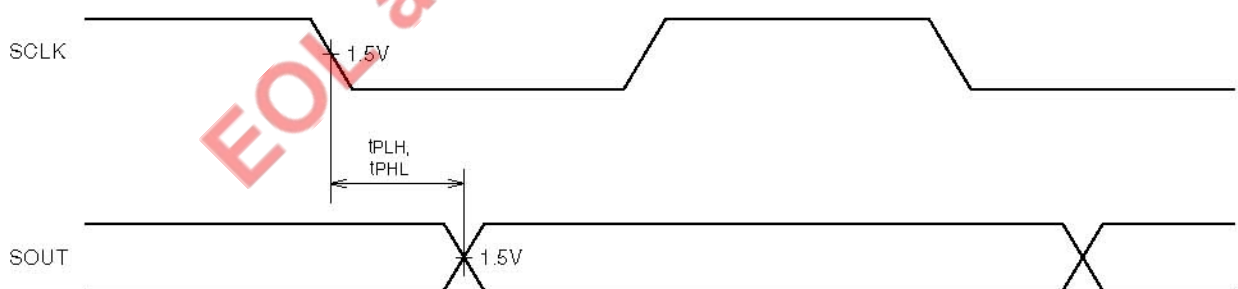## Write operation internal processing time

tBUSY

$\overline{WR}$ 1.5V   1.5V

Serial input communication start timing

SRL Write access to SRL   tWH($\overline{CS}$)

$\overline{CS}$ 1.5V   1.5V

Serial input operation

SCLK   1.5V

tsu (SI-CK)   th (CK-SI)

SIN   1.5V   1.5V

Serial output operation

SCLK   1.5V

tPLH,
tPHL

SOUT   1.5V

$\overline{OE}$ 1.5V   1.5V

tPHL   tPLH

SCLK   1.5V   1.5V

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Operation Flow Chart

When Busy Flag Is Used

When INT Output Is Used

APPLICATION EXAMPLE