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April 1st, 2010
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M66239FP

High Speed Standard Clock Generator With Frequency Synthesizer

REJ03E0002-0100
Rev.1.00
Mar 16, 2005

Description

M66239FP is high speed synchronizing clock generator with frequency synthesizer which is fabricated by high performance silicon gate CMOS process technology.

It is able to output clock in sync with external trigger. And it features excellent synchronizing precision (sync accuracy: jitter) over a wide range frequency band.

Also, it has frequency synthesizer function which is able to modulate input frequency by resister setting before normal operation. Frequency modulation resolution is high accuracy 0.01%.

And in order to process the Y/M/C/K printing signal processing by 1 chip, M66239FP integrate fore synchronizing clock generator macro with frequency synthesizer function.

Also, this part can use various applications as frequency synthesizer LSI.

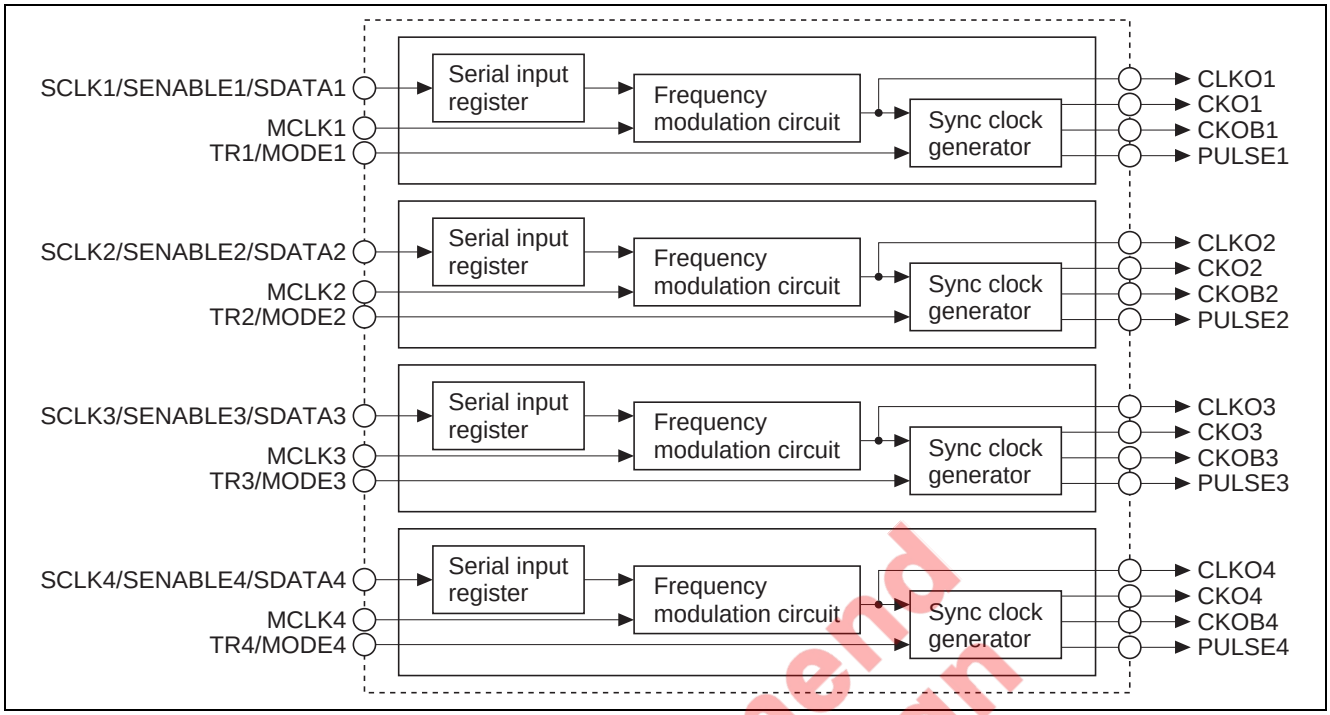
Features

- Power supply voltage: Single 3.3 V
- Frequency band: 28 MHz to 100 MHz
- Synchronizing precision (jitter): $\Delta T = \pm 1.5$ ns
- Output clock type
  (1) Sync clock output (CKO)
  (2) Sync clock output inverted CKO (CKOB)
  (3) One-shot pulse output (PULSE)
  (4) Continuous clock output (CLKO: asynchronous to trigger)
- Trigger edge: Polarity (positive/negative) selectable
- Output clock phase control: T/8 step resolution (T: clock period)
- Frequency synthesizer type
  (1) Offset type modulation
  (2) Triangle type modulation
  (3) Polygon type modulation
- Frequency modulation resolution: 0.01%
- Output clock center frequency modulation: 0.01% step/Maximum ±2.55%
- Output clock peak frequency modulation: 0.01% step/Maximum ±2.55%
- Output clock modulation period: 16 bit resister setting
- Output clock modulation start position: 10 bit resister setting
- Output clock disable function: Disable CKOB and PULSE by OE pin control
- Integrated 4 synchronizing clock generator macro with frequency synthesizer function

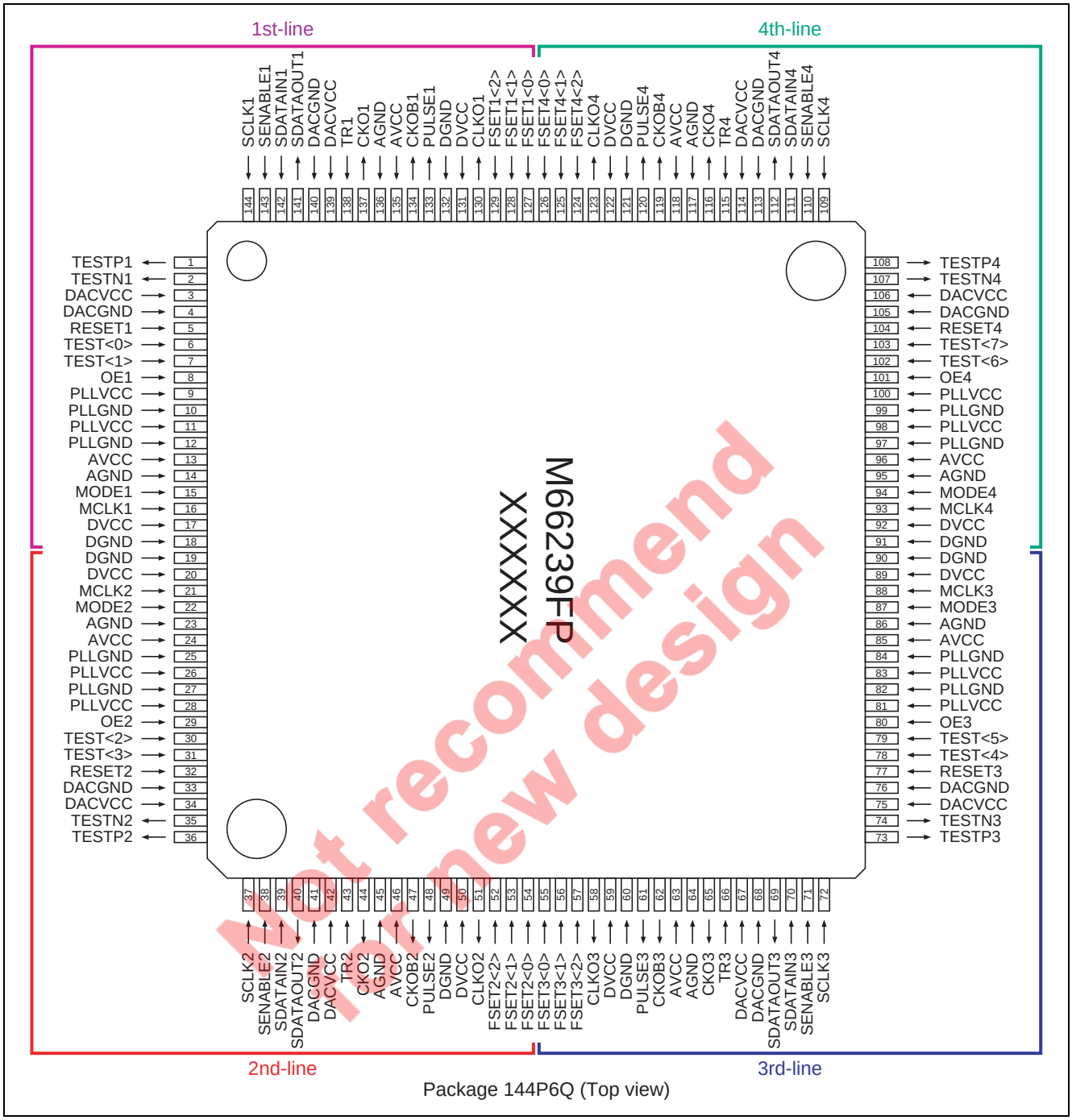
Application

Digital color copier/Digital color laser beam printer

Block Diagram



Pin Configuration

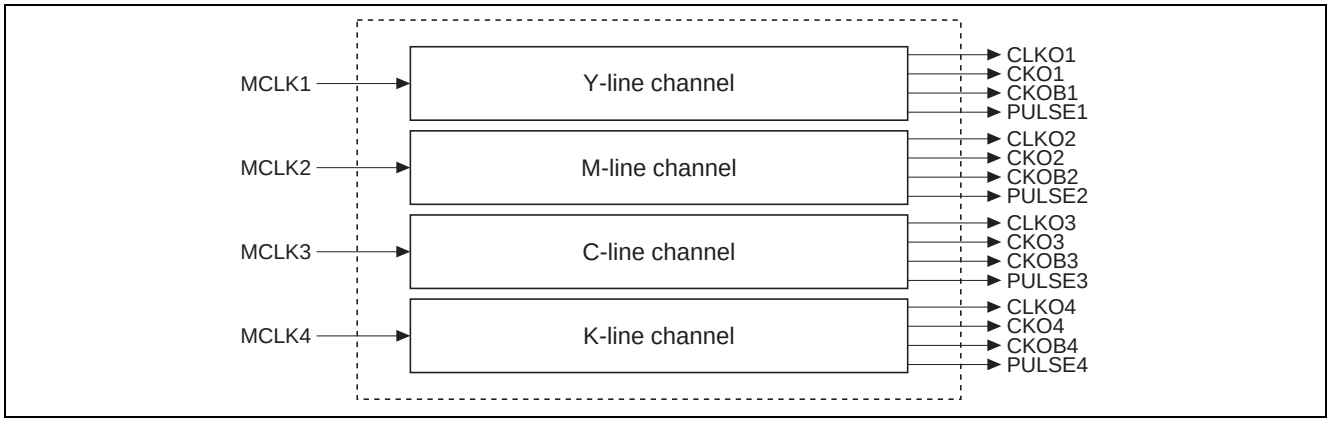


Package 144P6Q (Top view)

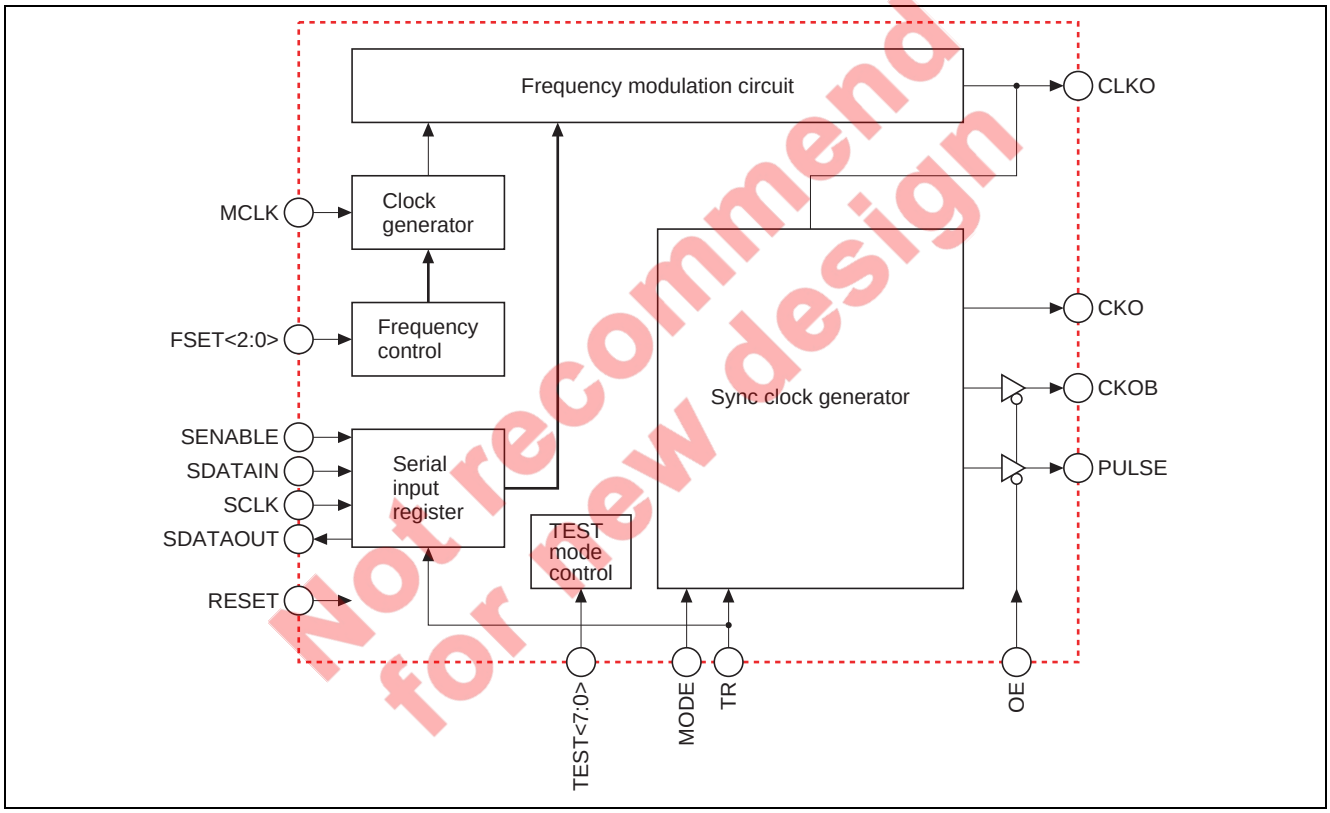
Pin Description

Pin Name	I/O	Function
MCLK	I	Input clock.
SCLK	I	Serial resister clock input.
SENABLE	I	Serial resister enable input. H level: disable, L level: enable
SDATAIN	I	Serial resister data input.
RESET	I	System reset input. When set to "L", system reset function. Reset function initialize all resister data to the default settings.
FSET<2:0>	I	Frequency range settings correspond to MCLK frequency.
MODE	I	Trigger edge polarity (positive/negative) select. H level: negative edge mode, L level: positive edge mode
TR	I	Trigger input for clock outputs.
CLKO	O	Continuous clock output. CLKO is asynchronous clock output to trigger.
CKO	O	Sync. clock output. Synchronized with trigger signal.
CKOB	O	Sync. clock output. Synchronized with trigger signal. CKOB is inverted clock of CKO.
PULSE	O	Sync. clock output. Synchronized with trigger signal. PULSE is one-shot pulse synchronized with CKO.
SDATAOUT	O	Serial resister data output.
OE	I	Output enable control. H level: CKOB and PULSE will be disabled. L level: All clock outputs will be enabled.
TEST<7:0>	I	Test control input. Set to "L".
TESTP<4:1> TESTN<4:1>	O	Test control input. Set to open.
DVCC DGND	I	Digital block VDD and GND.
AVCC AGND	I	Analog block VDD and GND.
PLL VCC PLL GND	I	PLL block VDD and GND.
DAC VCC DAC GND	I	DA converter VDD and GND.

Whole Block Diagram



Unit Channel Block Diagram



Function Summary

Sync Clock Generation Function

M66239FP has standard clock generator function, it is able to output clock in sync with external trigger TR. And it features excellent synchronizing precision (sync accuracy: jitter) over a wide range frequency band.

Sync clock output timing is determined by trigger input signal edge. Trigger edge polarity (positive/negative) is selectable by MODE input.

Time-lag between trigger input signal edge and sync clock output equals the sum of clock input signal "L" pulse width and M66239FP internal delay.

Variation in this lag (Δt) is ±1.5ns, ensuring excellent synchronizing accuracy.

There are three types of outputs: synchronous clock output (CKO), synchronous clock inverted output (CKOB), and one-shot pulse output (PULSE).

Synchronous clock output CKO is the same frequency as clock input signal MCLK. Synchronous clock inverted output CKOB is inverted signal of sync clock CKO. PULSE is one-shot pulse output which is almost equal to two cycles. All three sync outputs are suspended when trigger input signal is on "H" level when MODE is "H", and "L" level when MODE is "L" level. During these period, CKO and PULSE stay on "L" level, CKOB stay on "H" level.

Also, start phase of 3 sync. clocks are controlled by T/8 steps (T: Clock Period).

T/8 steps resolution is controlled by serial resister setting.

M66239FP integrate four synchronizing clock generator macro with frequency synthesizer function.

Frequency Modulation Function

M66239FP is able to modulate sync. clock frequency.

Frequency modulation profile is controlled by serial resister. Serial resister is controlled by serial input clock (SCLK), serial input enable (SENABLE) and serial input data (SDATAIN).

When SENABLE is "L" level, SDATAIN is able to write to serial input resister by SCLK. SDATAIN is composed by 4 bit address + 3 bit W/R distinction + 16 bit resister data.

After write operation completed, it can be able to confirm the resister status using read operation to serial input resister.

Resister setting is as follows.

(1) Operation mode : Resister 1
(2) Frequency modulation period (Trate) : Resister 2
(3) Frequency modulation start position (Tstart) : Resister 3
(4) Output center frequency (fcenter) : Resister 4
(5) Output peak frequency (fpeak) : Resister 5
(6) 1st.pole position (1stPole) : Resister 6
(7) 2nd.pole position (2ndPole) : Resister 7
(8) 3rd.pole position (3rdPole) : Resister 8
(9) 4th.pole position (4thPole) : Resister 9
(10) 1st.Pole frequency (f1stPole) : Resister 10
(11) 3rd.Pole frequency (f3rdPole) : Resister 11

There are four operation modes, center frequency offset type modulation (mode1), triangle type modulation (mode2 and 3), and polygon type modulation (mode4).

Sync. Clock Generation Operation Timing

Trigger Mode 1 (Negative edge operation: MODE = "H")

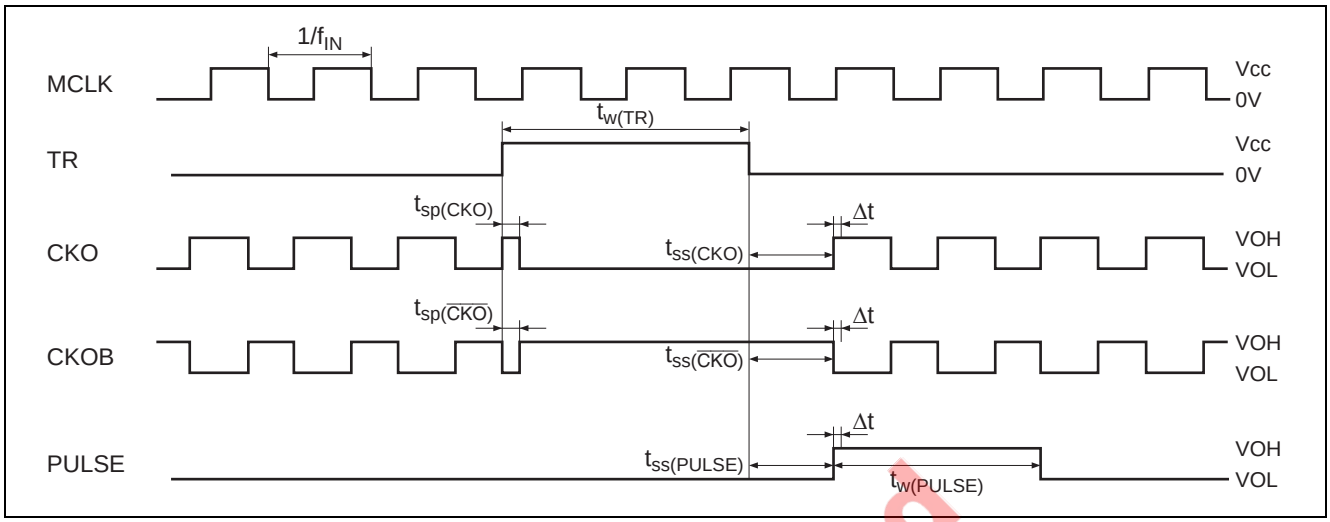


Figure 1 Trigger Mode 1

Trigger Mode 2 (Positive edge operation: MODE = "L")

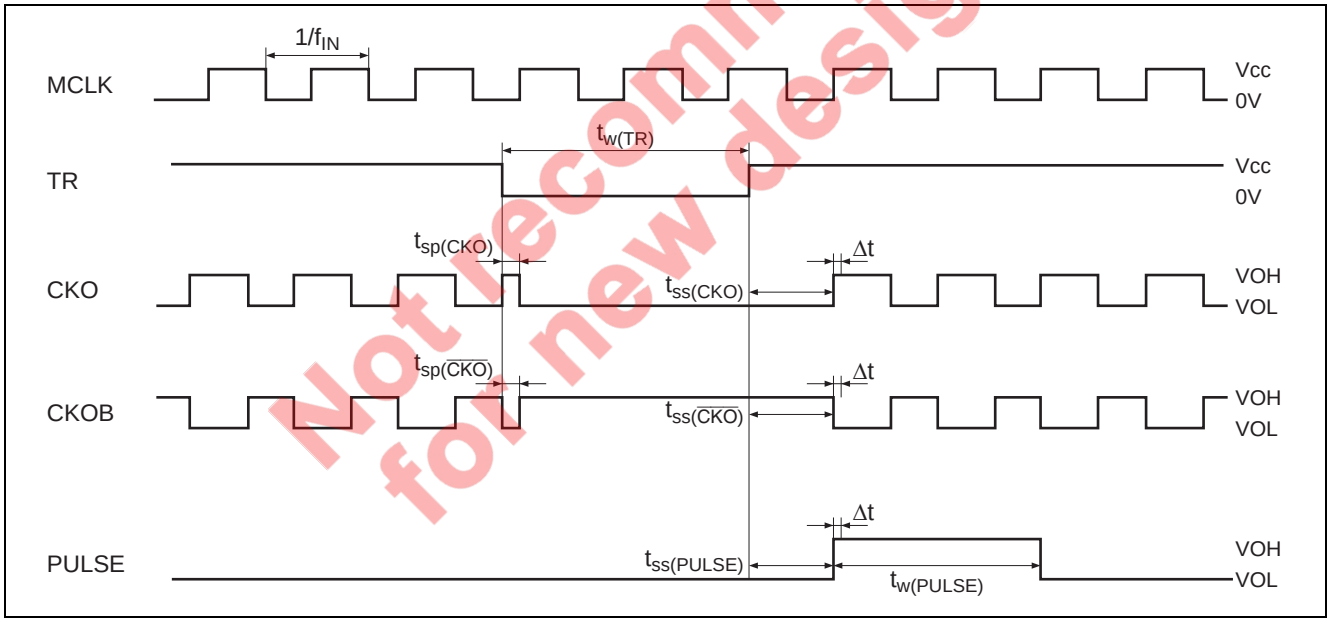


Figure 2 Trigger Mode 2

Notes: 1. t_{ss} (CKO, CKOB and PULSE) equals the sum of input clock "L" width and α.
Value α refers to internal delay in M66239FP. Under environment where temperature and VCC do not change, value α and t_{ss} are kept constant approximately.
Dispersion of t_{ss} under such conditions is defined as Δt (synchronizing precision: jitter).
2. Outputs (CKO, CKOB and PULSE) are unknown until twice trigger pulse input TR reaches after power-on.
3. Internal trigger signal is generated by EXOR of TR and MODE signal.

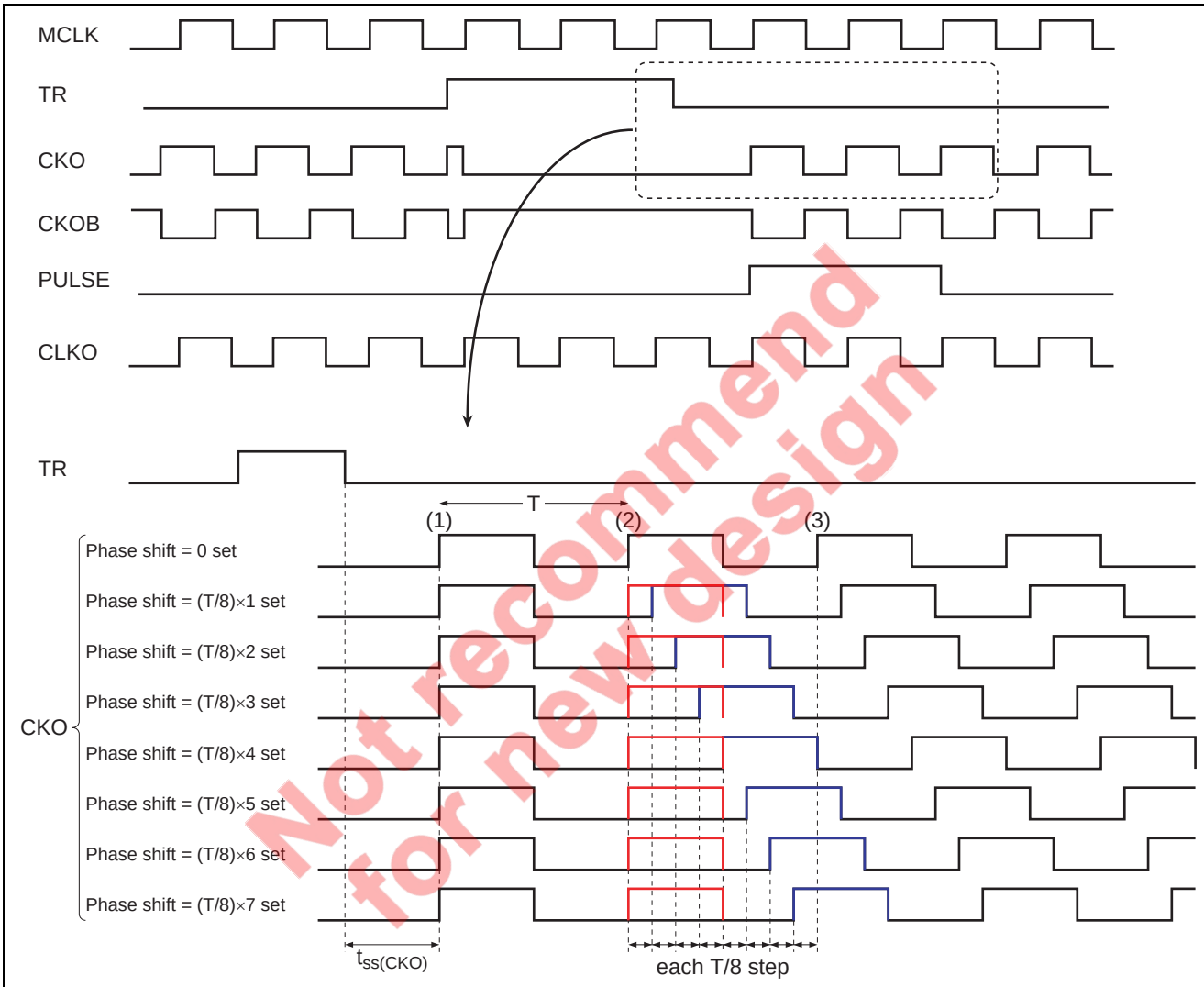
Sync. Clock Phase Timing

M66239FP is able to control the phase of sync clock outputs (CKO, CKOB, PULSE) as each T/8 step. (T: clock period)

This phase shift control is set up by serial input resister No. 13.

Also, 1st edge phase (= (1) position) of sync clock outputs is not shifted, and 2nd edge phase (= (2) position) of sync clock outputs is either not shifted position or resister set position, after 3rd edge phase (= (3) position) of sync clock outputs is shift as resister settings.

CLKO output can not use this phase shift function because CLKO is asynchronous clock output to trigger.



Notes: 1. 1st edge phase of sync clock output is not shifted.
2nd edge phase of sync clock output is either not shifted position or resistor set position,
3rd edge phase of sync clock output is shift as resistor settings.
2. It can set T/8 step resolution, but if T/8 is less than synchronizing precision (jitter)
+/– 1.5 ns, it may be not able to realize such high step resolution.
T/8 is not guarantee value which is taken into account the jitter and noise.

Figure 3 Sync. Clock Phase Timing

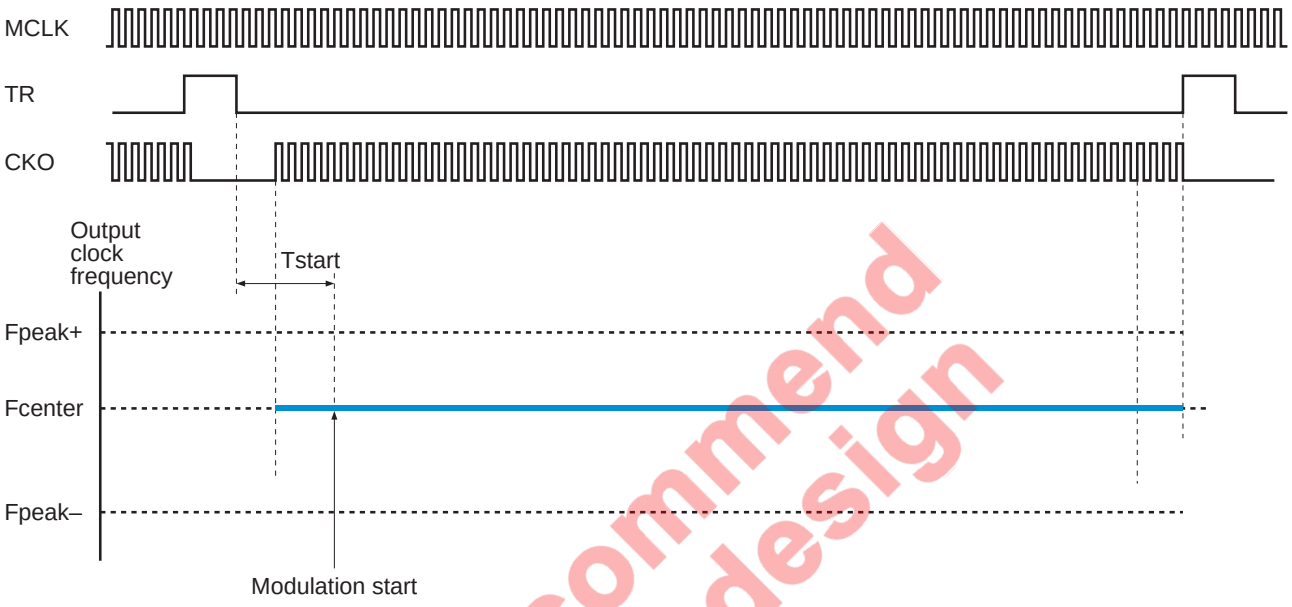
Frequency Modulation Operation Timing

Function Mode 1

Mode 1 is frequency offset type modulation. Output clock frequency keep Fcenter-freqency.

Frequency modulation is set by serial input resister.

(1) Operation mode : Resister 1
(2) Frequency modulation start position (Tstart) : Resister 3
(3) Output center frequency (fcenter) : Resister 4



Note: 1. Until next TR input, output clock frequency keep "Fcenter".

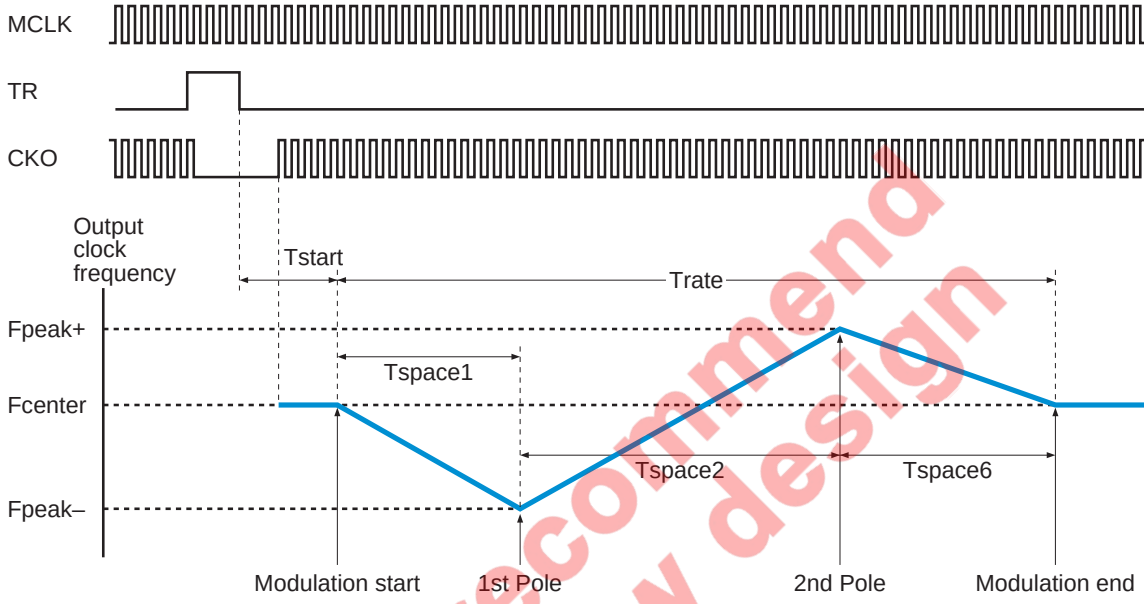
Figure 4 Operation Timing of Mode 1

Function Mode 2

Mode 2 is triangle modulation type as following.

Frequency modulation is set by serial input resister.

(1) Operation mode : Resister 1
(2) Frequency modulation period (Trate) : Resister 2
(3) Frequency modulation start position (Tstart) : Resister 3
(4) Output center frequency (fcenter) : Resister 4
(5) Output peak frequency (fpeak) : Resister 5
(6) 1st.pole position (1stPole) : Resister 6
(7) 2nd.pole position (2ndPole) : Resister 7



Notes: 1. Each Pole position (cycle number) is defined by Tstart position.
2. Until next TR input, output clock frequency keep "Fcenter".

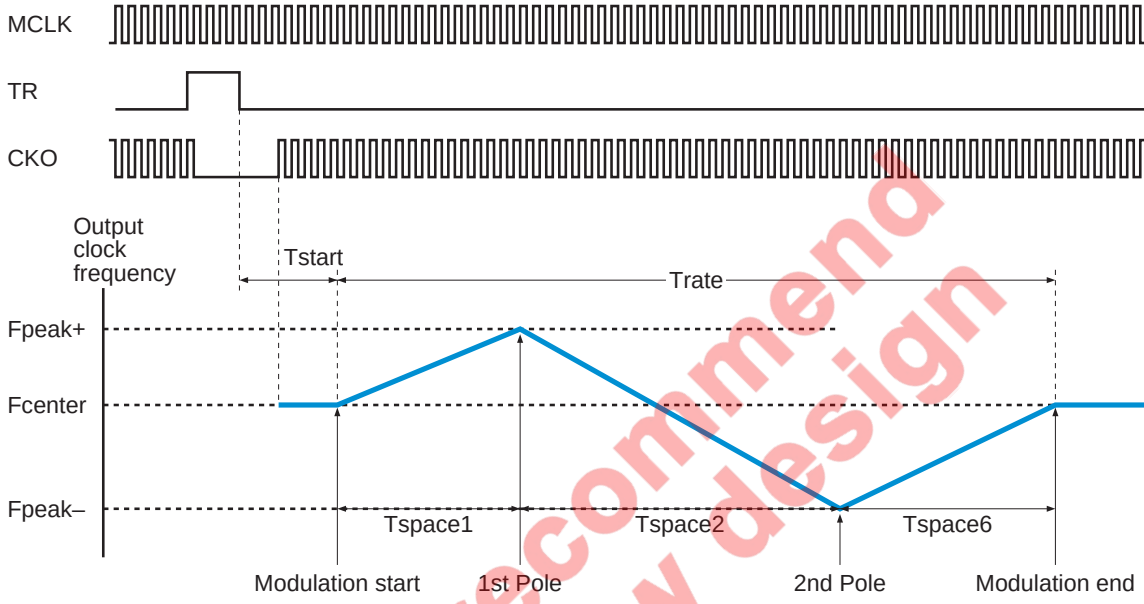
Figure 5 Operation Timing of Mode 2

Function Mode 3

Mode 3 is triangle modulation type as following.

Frequency modulation is set by serial input resister.

(1) Operation mode : Resister 1
(2) Frequency modulation period (Trate) : Resister 2
(3) Frequency modulation start position (Tstart) : Resister 3
(4) Output center frequency (fcenter) : Resister 4
(5) Output peak frequency (fpeak) : Resister 5
(6) 1st.pole position (1stPole) : Resister 6
(7) 2nd.pole position (2ndPole) : Resister 7



Notes: 1. Each Pole position (cycle number) is defined by Tstart position.
2. Until next TR input, output clock frequency keep "Fcenter".

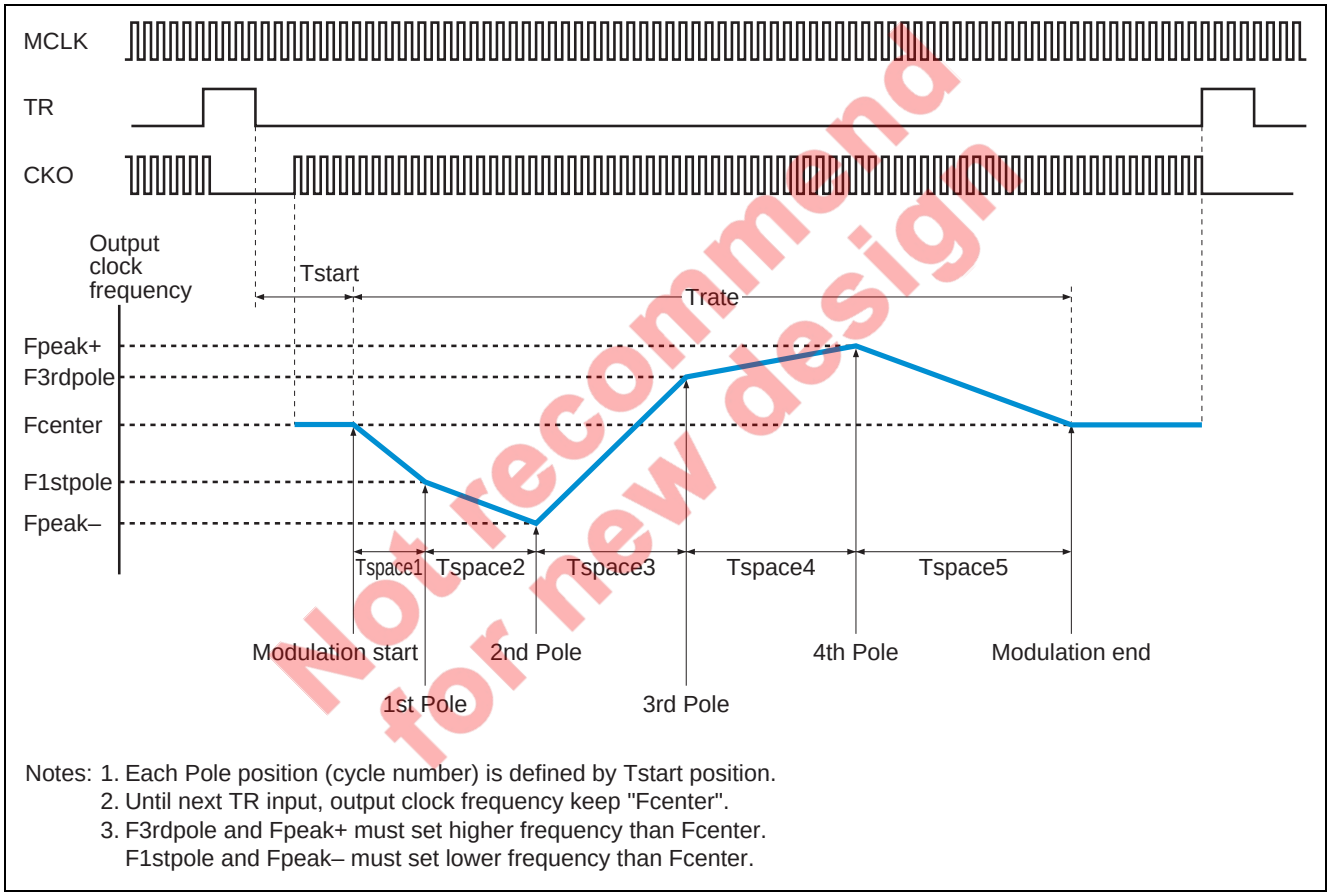
Figure 6 Operation Timing of Mode 3

Function Mode 4

Mode 4 is polygon modulation type as following.

Frequency modulation is set by serial input resister.

(1) Operation mode : Resister 1
(2) Frequency modulation period (Trate) : Resister 2
(3) Frequency modulation start position (Tstart) : Resister 3
(4) Output center frequency (fcenter) : Resister 4
(5) Output peak frequency (fpeak) : Resister 5
(6) 1st.pole position (1stPole) : Resister 6
(7) 2nd.pole position (2ndPole) : Resister 7
(8) 3rd.pole position (3rdPole) : Resister 8
(9) 4th.pole position (4thPole) : Resister 9
(10) 1st.Pole frequency (f1stPole) : Resister 10
(11) 3rd.Pole frequency (f3rdPole) : Resister 11



Notes: 1. Each Pole position (cycle number) is defined by Tstart position.
2. Until next TR input, output clock frequency keep "Fcenter".
3. F3rdpole and Fpeak+ must set higher frequency than Fcenter.
F1stpole and Fpeak– must set lower frequency than Fcenter.

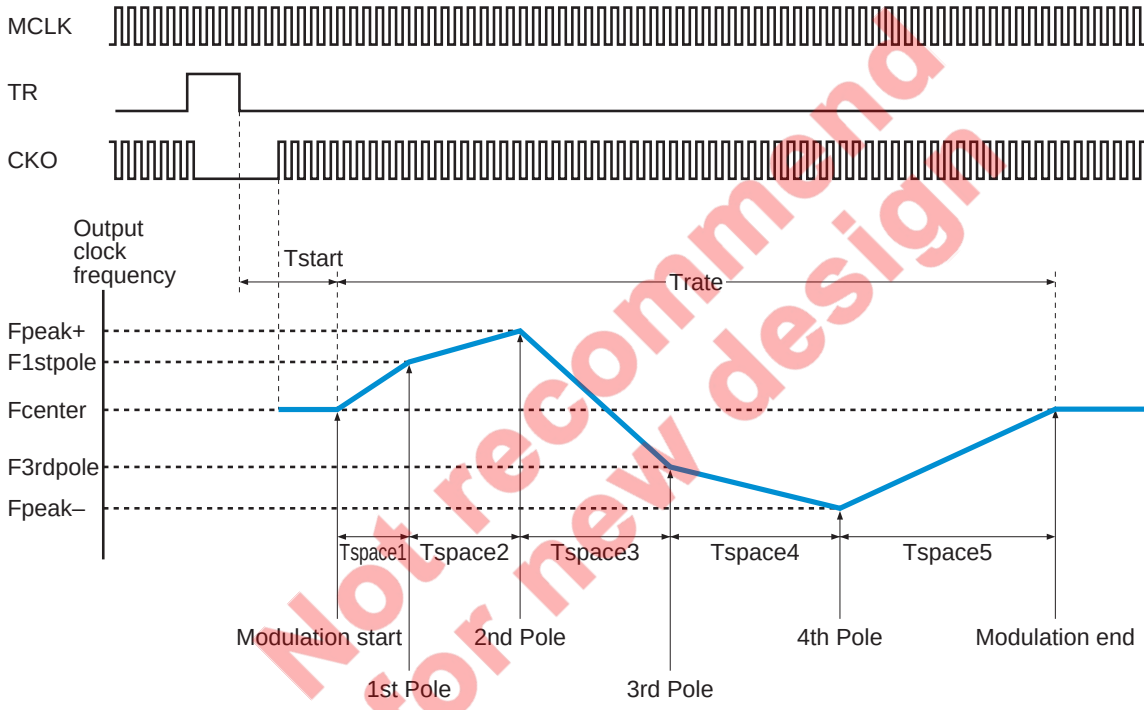
Figure 7.1 Operation Timing of Mode 4 (1)

Function Mode 4 (cont.)

Mode 4 is polygon modulation type as following.

Frequency modulation is set by serial input resister.

(1) Operation mode : Resister 1
(2) Frequency modulation period (Trate) : Resister 2
(3) Frequency modulation start position (Tstart) : Resister 3
(4) Output center frequency (fcenter) : Resister 4
(5) Output peak frequency (fpeak) : Resister 5
(6) 1st.pole position (1stPole) : Resister 6
(7) 2nd.pole position (2ndPole) : Resister 7
(8) 3rd.pole position (3rdPole) : Resister 8
(9) 4th.pole position (4thPole) : Resister 9
(10) 1st.Pole frequency (f1stPole) : Resister 10
(11) 3rd.Pole frequency (f3rdPole) : Resister 11



Notes: 1. Each Pole position (cycle number) is defined by Tstart position.
2. Until next TR input, output clock frequency keep "Fcenter".
3. F1stpole and Fpeak+ must set higher frequency than Fcenter.
F3rdpole and Fpeak– must set lower frequency than Fcenter.

Figure 7.2 Operation Timing of Mode 4 (2)

CLKO Operation Timing

The CLKO output is the continuation clock output that frequency modulation is worked like CKO but to be in the asynchronous relation with TR. Of the operation timing specified in operation mode 4 in the figure below by it but the other operation mode is same.

Also, because CLKO is continuation clock output before synchronous clock generation circuit, phase relation during 4 channel is not guaranteed.

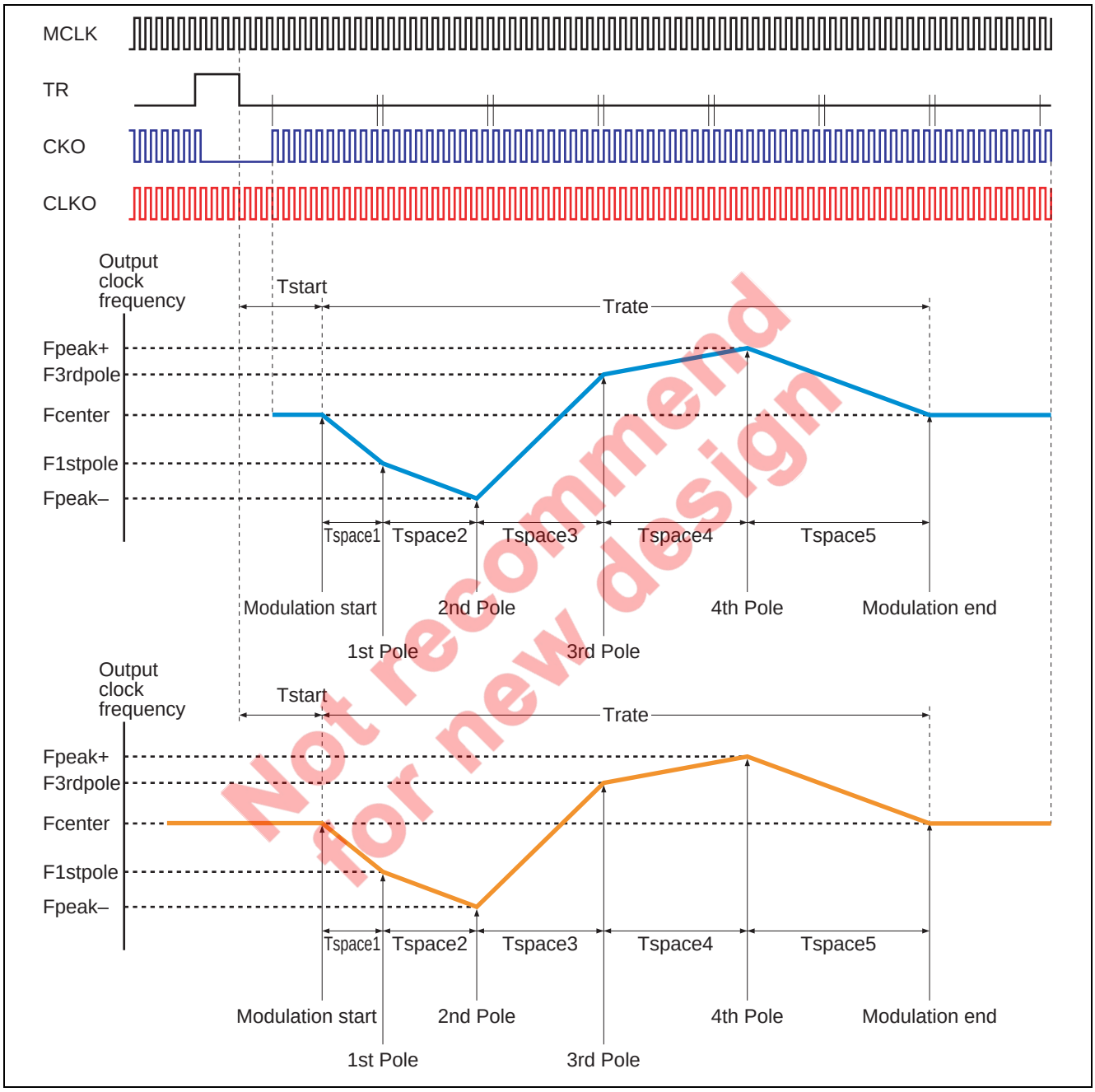


Figure 8 CKO (upper) and CLKO (lower)

Frequency Modulation Resister Setting (Write Operation)

Write Operation

Frequency modulation is set by serial input resister. Serial input resister is controlled by serial input clock (SCLK), serial input enable (SENABLE) and serial input data (SDATAIN).

When SENABLE is "L" level, SDATAIN is written to serial input resister by SCLK. SDATAIN is composed by 4 bit address + 3 bit W/R distinction data + 16 bit resister data.

After SENABLE change to "H", more than 20 dummy SLCK cycle is needed.

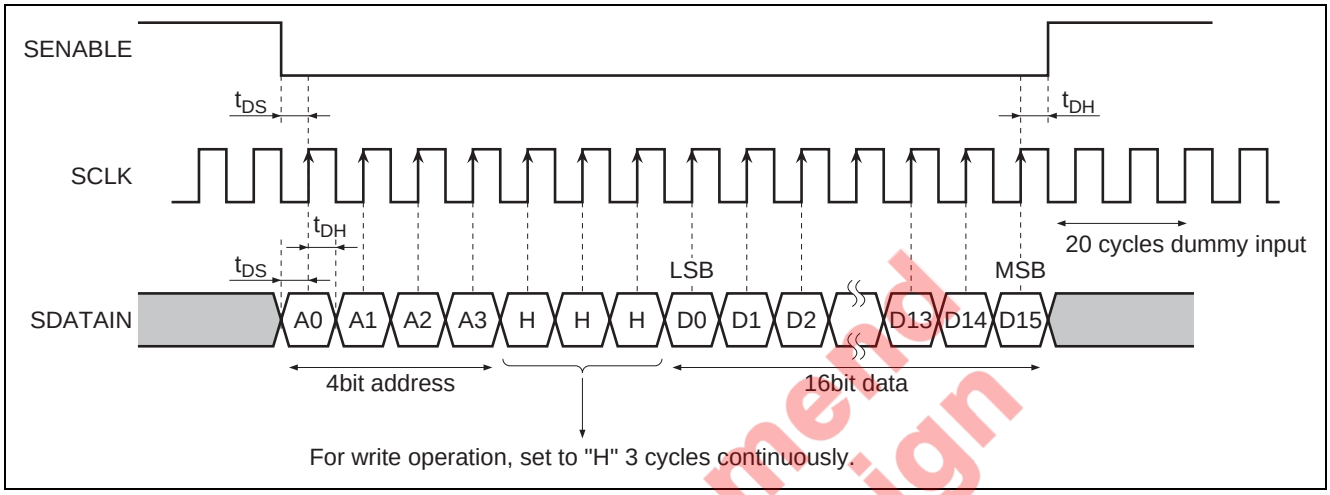


Figure 9 Frequency Modulation Resister Setting (Write Operation)

Frequency Modulation Resister

Resister Name	Function	Address A3 A0	Bit Number	Setting Range D15 · · · D0	Default Value D15 · · · D0	Unit 1LSB
Resister 1	Operation mode	0 0 0 0	3 bit	min 0000000000000001 max 0000000000000100	0000000000000001(1 dec) * Mode1 when 1 dec	—
Resister 2	Modulation period	0 0 0 1	16 bit	min 0000010111011100 max 1111111111111111	0010000000000000(8192 dec)	MCLK cycle
Resister 3	Modulation start position	0 0 1 0	10 bit	min 0000000001100100 max 0000001111111111	0000000100000000(256 dec)	MCLK cycle
Resister 4	Center frequency	0 0 1 1	9 bit	min 0000000000000000 max 0000000111111111 * –2.55% when min. value * +2.55% when max. value	0000000100000000(256 dec) * 0% when 256 dec * Modulate to + side more than 256 dec * Modulate to – side less than 256 dec	MCLK frequency ×0.01%
Resister 5	Peak frequency	0 1 0 0	8 bit	min 0000000000011110 max 0000000011111111 * ±0.30% when min. value * ±2.55% when max. value	0000000011111111(255 dec) * ±2.55% when 255 dec	MCLK frequency ×0.01%
Resister 6	1st-pole position	0 1 0 1	16 bit	min 0000000111110100 max 1001111111111111	0000011001100110(1638 dec)	MCLK cycle
Resister 7	2nd-pole position	0 1 1 0	16 bit	min 0000000111110100 max 1001111111111111	0000110011001100(3276 dec)	MCLK cycle
Resister 8	3rd-pole position	0 1 1 1	16 bit	min 0000000111110100 max 1001111111111111	0001001100110010(4914 dec)	MCLK cycle
Resister 9	4th-pole position	1 0 0 0	16 bit	min 0000000111110100 max 1001111111111111	0001100110011000(6552 dec)	MCLK cycle
Resister 10	1st-pole frequency (Mode 4)	1 0 0 1	9 bit	min 0000000000000000 max 0000000111111111 * –2.55% when min. value * +2.55% when max. value	0000000010000000(128 dec) * –1.28% when 128 dec	MCLK frequency ×0.01%
Resister 11	3rd-pole frequency (Mode 4)	1 0 1 0	9 bit	min 0000000000000000 max 0000000111111111 * –2.55% when min. value * +2.55% when max. value	0000000110000000(384 dec) * +1.28% when 384 dec	MCLK frequency ×0.01%
Resister 12	Modulation resolution	1 0 1 1	1 bit	min 0000000000000000 max 0000000000000001 * ±0.01% mode when min. * ±0.005% mode when max.	0000000000000000(0 dec) * 0.01% mode when 0 dec	—
Resister 13	Output phase control	1 1 0 0	3 bit	min 0000000000000000 max 0000000000000111 * Delay 0 when min. * Delay 7T/8 when max.	0000000000000000(0 dec) * Delay 0 when 0 dec	T/8 (Clock cycle)

Notes: 1. Set to the following value for resister 1.
- For operation mode 1: "0000000000000001"
- For operation mode 2: "0000000000000010"
- For operation mode 3: "0000000000000011"
- For operation mode 4: "0000000000000100"

2. Resister 12 must not change.
3. Above table intend to setting available value of resister, practical limits are described in page 20.
4. Resister 13 is for phase control of sync clock output.
5. If the default value of above resister use, write operation to all resister must be done.
6. Resister 6 to 9 refer to following.
- 1st Pole = Tspace1
- 2nd Pole = Tspace1 + Tspace2
- 3rd Pole = Tspace1 + Tspace2 + Tspace3
- 4th Pole = Tspace1 + Tspace2 + Tspace3 + Tspace4

Frequency Modulation Resister Setting (Read Operation)

Read Operation

After write operation completed, it can confirm the resister status using read operation to serial input resister.

When SENABLE is "L" level, SDATAIN is written to serial input resister by SCLK. SDATAIN is composed by 4 bit address + 3 bit W/R distinction data. After SENABLE change to "H", more than 20 dummy SLCK cycle is needed.

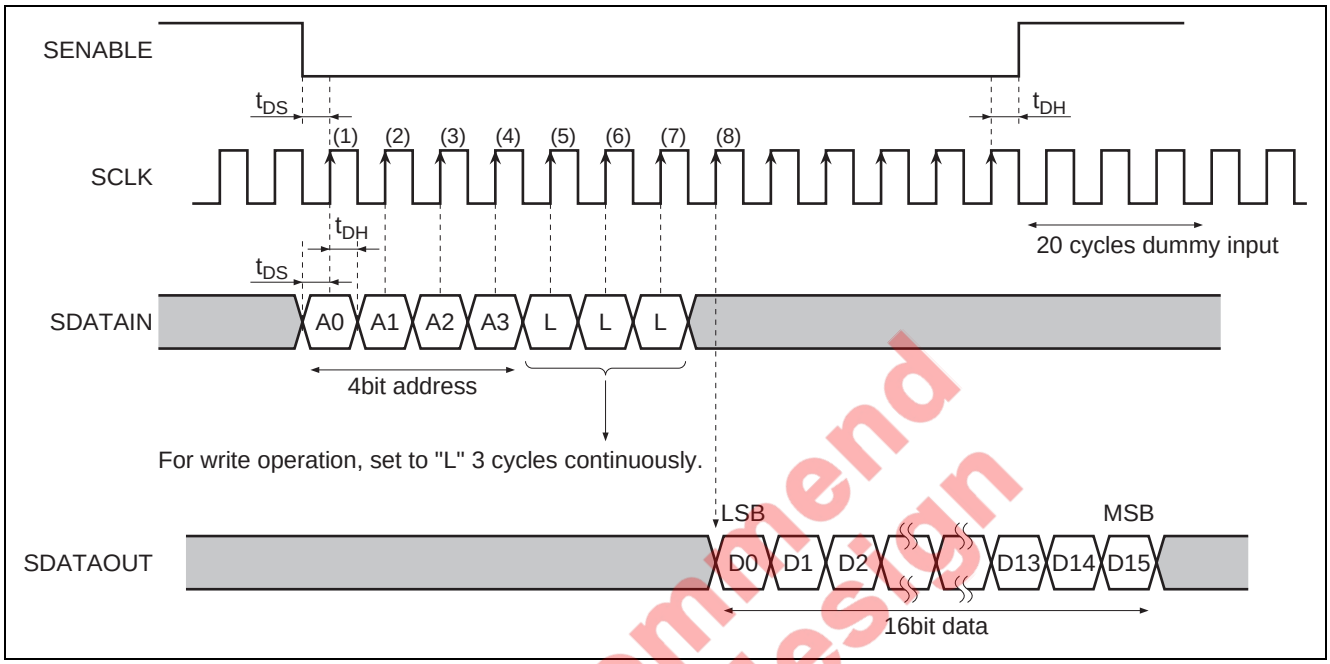


Figure 10 Frequency Modulation Resister Setting (Read Operation)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	Vcc	–0.3 to +4.6	V	
Input voltage	V_I	–0.3 to Vcc+0.3	V	
Output voltage	V_O	–0.3 to Vcc+0.3	V	
Storage temperature	Tstg	–55 to +150	°C	
Power dissipation	Pd	2500 *1	mW	θja = 30°C/W, Ta = 50°C

Note: 1. θja should be less than 30°C/W, Tjmax should be less than 125°C.
When θja = 30°C/W and Tjmax is 125°C, Ta(max) will be 50°C.
PCB needs over 4 layers, over 100 mm × 100 mm size, over 70% Cu occupied ratio (average value of each layer) roughly.
Please contact to our sales division when you design PCB layout.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	Vcc	3.15	3.3	3.46	V	
Supply voltage	GND	—	0	—	V	
Input voltage	V_I	0	—	Vcc	V	
Output voltage	V_O	0	—	Vcc	V	
Operating temperature	Topr	0	—	50	°C	

DC Characteristics

(Ta = 0 to +50°C, Vcc = 3.15 to 3.46V, GND = 0V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
"H" input voltage	V_{IH}	2.0	—	—	V	
"L" input voltage	V_{IL}	—	—	0.8	V	
"H" output voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4 mA
"L" output voltage	V_{OL}	—	—	0.4	V	I_{OH} = 4 mA
Supply current (static)	Icc (s)	—	55	100	mA	V_I = Vcc or GND
Supply current (active)	Icc (a)	—	480	700	mA	f_{MCLK} = 100 MHz, f_{SCLK} = 20 MHz, C_L = 10 pF, OE = L
		—	440	—		f_{MCLK} = 80 MHz, f_{SCLK} = 20 MHz, C_L = 10 pF, OE = L
		—	350	—		f_{MCLK} = 40 MHz, f_{SCLK} = 20 MHz, C_L = 10 pF, OE = L
		—	250	—		f_{MCLK} = 20 MHz, f_{SCLK} = 20 MHz, C_L = 10 pF, OE = L
"H" input current	I_{IH}	—	—	10	µA	V_I = Vcc
"L" input current	I_{IL}	—	—	–10	µA	V_I = GND
Input capacitance	C_I	—	—	10	pF	

Note: The direction of current flowing to the circuit is specified to be positive. (No sign)

Timing Requirements

(Ta = 0 to +50°C, Vcc = 3.15 to 3.46V, GND = 0V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
MCLK frequency	f_{MCLK}	28	—	100	MHz	C_L = 10 pF
MCLK and SCLK clock duty	f_{DUTY}	45	—	55	%	
TR input pulse width	$t_{w(TR)}$	500	—		ns	
MCLK and SCLK input rising time	t_r	—	—	5	ns	
MCLK and SCLK input falling time	t_f	—	—	5	ns	
SDATA, SENABLE set-up time	t_{DS}	5	—	—	ns	
SDATA, SENABLE hold time	t_{DH}	5	—	—	ns	
SCLK frequency	f_{SCLK}	—	—	20	MHz	
Internal PLL lock up time	Tpllock	—	—	10	ms	
RESET pulse width	$t_{w(RESET)}$	1	—	—	µs	

Switching Characteristics

(Ta = 0 to +50°C, Vcc = 3.15 to 3.46V, GND = 0V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Synchronizing precision (jitter)	Δt	—	—	±1.5	ns	C_L = 10 pF
Sync. clock CKO output start time	$t_{ss(CKO)}$	—	—	t_{Lp}+50	ns	
Sync. clock CKOB output start time	$t_{ss(CKOB)}$					
One-shot pulse output start time	$t_{ss(PULSE)}$	—	—	t_{Lp}+50	ns	
Sync clock CKO output stop time	$t_{sp(CKO)}$	—	—	40	ns	
Sync. clock CKOB output stop time	$t_{sp(CKOB)}$					
One-shot pulse width	$t_{w(PULSE)}$	2 t_p–10	—	2 t_p+10	ns	
Sync. clock CKO output duty	$f_{oDUTY(CKO)}$	40	—	60	%	
Sync. clock CKOB output duty	$f_{oDUTY(CKOB)}$					

Notes: 1. $t_p = 1/f_{IN}$, $t_{Lp} = t_p \times (100 - f_{DUTY})/100$

2. Switching test waveform
   Input pulse level MCLK: 0 to Vcc, TR: 0 to Vcc
   Input clock rising time: 3 ns
   Input clock falling time: 3 ns
   Criteria Voltage MCLK: Vcc/2, TR: 1.3 V, Sync. clock: Vcc/2

Frequency Modulation Characteristics

(Ta = 0 to +50°C, Vcc = 3.15 to 3.46V, GND = 0V)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Frequency modulation start position	Tstart	100	256	1023	Cycle	C_L = 10 pF
Frequency modulation period	Trate	1500	8192	65535	Cycle	
Center frequency	Fcenter	±0	—	±2.55	%	
Center frequency resolution	Fstep1	0.01	—	—	%	
Peak frequency (+ side)	Fpeak+	+0.3	—	+2.55	%	
Peak frequency (– side)	Fpeak–	–0.3	—	–2.55	%	
Peak frequency resolution	Fstep2	0.01	—	—	%	
1st.pole position	1stPole	Tstart+500	—	40959	Cycle	
2nd.pole position	2ndPole	1stPole+500	—	40959	Cycle	
3rd.pole position	3rdPole	2ndPole+500	—	40959	Cycle	
4th.pole position	4thPole	3rdPole+500	—	40959	Cycle	
Min cycle between 1stPole and Tstart	Tspace1	500	—	—	Cycle	
Min cycle between 2ndPole and 1stPole	Tspace2	500	—	—	Cycle	
Min cycle between 3rdPole and 2ndPole	Tspace3	500	—	—	Cycle	
Min cycle between 4thPole and 3rdPole	Tspace4	500	—	—	Cycle	
Min cycle between modulation end-4thPole	Tspace5	500	—	—	Cycle	
Min cycle between modulation end-2ndPole (In case of mode 2 or mode 3)	Tspace6	500	—	—	%	
1st.Pole frequency (In case of page 12)	F1stpole	Fcenter–0.1	—	–Fpeak+0.1	%	
1st.Pole frequency (In case of page 13)		Fcenter+0.1	—	+Fpeak–0.1	%	
3rd.Pole frequency (In case of page 12)	F3rdpole	Fcenter+0.1	—	+Fpeak–0.1	%	
3rd.Pole frequency (In case of page 13)		Fcenter–0.1	—	–Fpeak+0.1	%	

Notes: 1. Regarding Fpeak+/–, F1stpole, F3rdpole higher frequency than Fcenter is specified to be positive (+ sign), lower frequency than Fcenter is specified to be negative (– sign).
2. The above limitations of Fcenter, Fstep1, Fpeak+/–, Fstep2, F1stpole, F3rdpole, 1stPole, 2ndPole, 3rdPole, and 4thPole are setting available vale.
Actual output clock is affected PLL jitter, above limitations are not guarantee value which is taken into account the jitter and noise.
3. Minimum specification of modulation period is 1500 cycles, operation mode 4 needs over 2500 cycles.

Frequency Range Setting of Input Clock

FEST<2:0> pins need to set correspond to following table.

Table 1 Frequency Range Setting of Input Clock

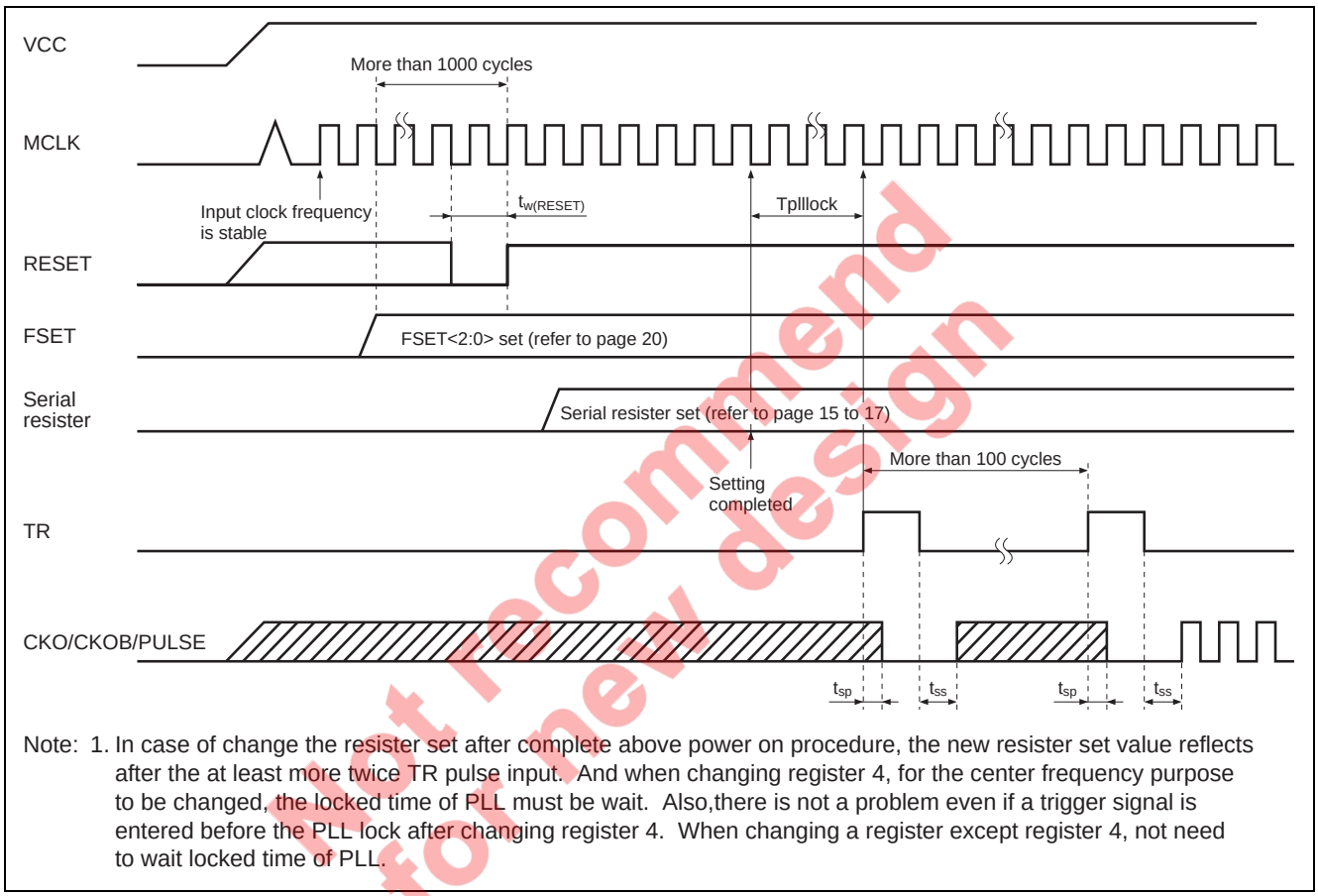
Input Clock Frequency (MHz)	FSET<2>	FSET<1>	FSET<0>
28 to 60	H	L	L
60 to 80	H	L	H
80 to 100	H	H	L

Notes: 1. If MCLK frequency change under operating, it should need to start power on procedure again.
2. If FSET<2:0> setting are changed, reset function is needed again.
By the reset operation, all serial resisters are set to default settings, so it should set serial resister again.

After Power-On Procedure

After power-on, M66239FP status is unknown. Following procedure must be done.

1. VCC power-on
2. After Vcc and input clock frequency is stable, set the FSET[2:0].
3. Reset pulse input.
   Input more than MCLK 1000 clock cycle from FSET setting is completed to RESET set to "H" level.
4. Serial resister set.
5. After input MCLK clock till PLL lockup time (Tplllock), input twice TR pulse.
   Input more than 100 cycle MCLK clocks between 1st. TR and 2nd. TR.
6. After that, sync clock will be outputted from M66239FP.

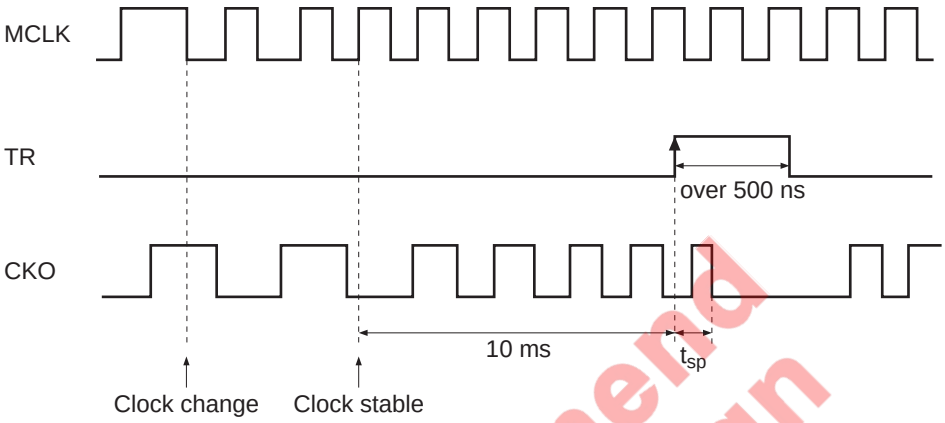


Note: 1. In case of change the resister set after complete above power on procedure, the new resister set value reflects after the at least more twice TR pulse input. And when changing register 4, for the center frequency purpose to be changed, the locked time of PLL must be wait. Also,there is not a problem even if a trigger signal is entered before the PLL lock after changing register 4. When changing a register except register 4, not need to wait locked time of PLL.

Figure 11 After Power-On Procedure

Input Clock Change Sequence

When changing the frequency of the input clock, if being the inside of each range in the frequency range which is specified in page 20, the change of the FSET is unnecessary but the lock of PLL sometimes comes when a frequency is changed even if it is the inside of each range in the frequency range. When the frequency of the input clock changes in each range in the frequency range and PLL comes off the lock condition, it adds that it takes time by locking 10 ms once again. To get a stable output clock, after passing in the PLL lock time in the frequency of input clock or it after phase change, enter TR signal. The output clock which was stable after entry is gotten in the TR signal. About the change of the frequency which exceeds the frequency range which is specified in page 20, for the purpose of FSET[2:0] to be changed, the sequence of power on must be done.

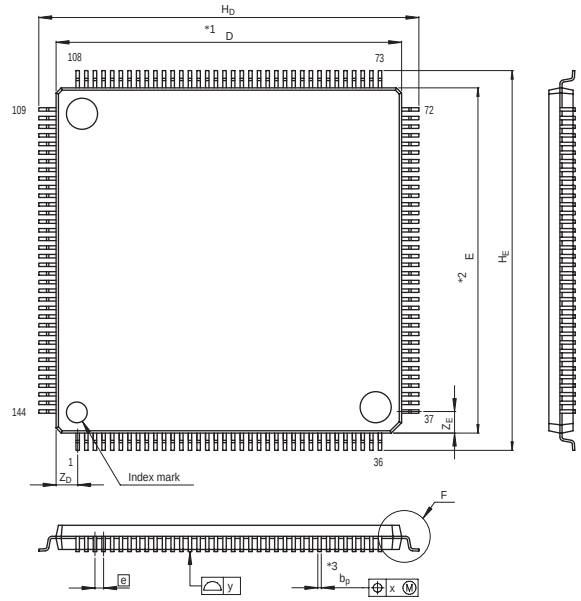


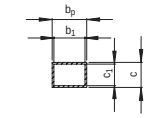
The sequence when changing an entry frequency in each range in the frequency range

Figure 12 Input Clock Change Sequence

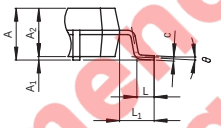
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	——	1.4	——
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	——	——	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	——	0.20	——
c	0.09	0.145	0.20
c_1	——	0.125	——
θ	0°	——	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.10
Z_D	——	1.25	——
Z_E	——	1.25	——
L	0.35	0.5	0.65
L_1	——	1.0	——

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