2.5 VOLT LOW EMI CLOCK GENERATOR

MK1728A-01

Description

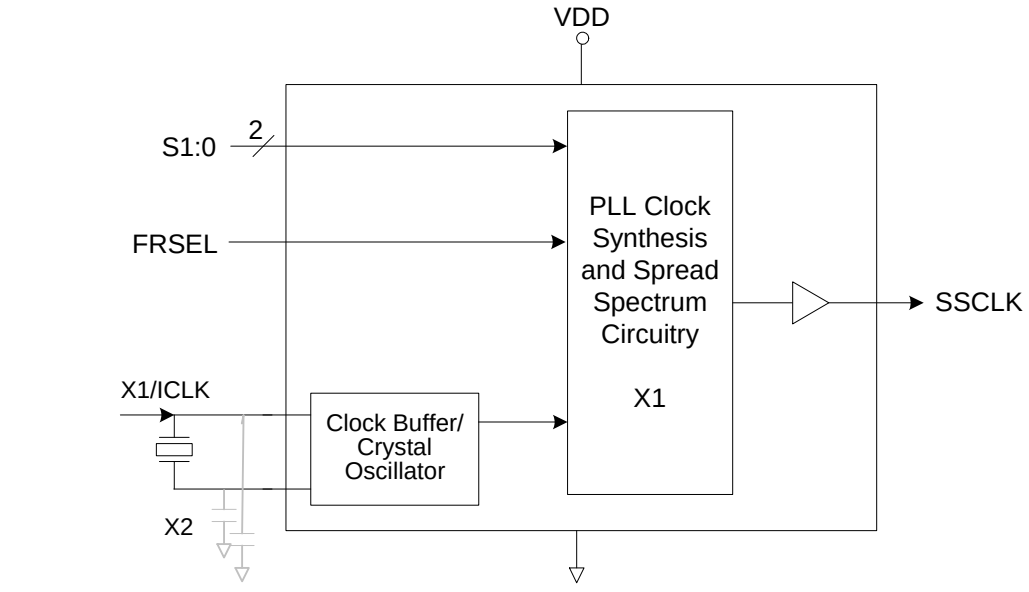
The MK1728A-01 generates a low EMI output clock from a clock or crystal input. Operating at 2.5 V, the part is designed to dither the LCD interface clock for PDAs, printers, scanners, modems, copiers, and other applications. Using IDT's proprietary mix of analog and digital Phase-Locked Loop (PLL) technology, the device spreads the frequency spectrum of the output, reducing the frequency amplitude peaks by several dB. The MK1728A-01 offers both centered and down spread from a high-speed crystal or clock input.

IDT offers many other clocks for computers and computer peripherals. Consult IDT when you need to remove crystals and oscillators from your board.

Features

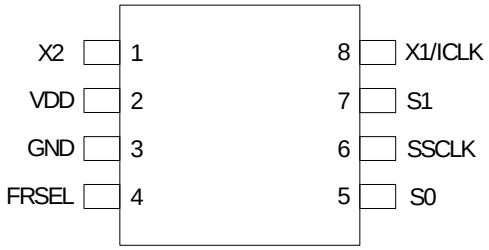
- Operating voltage of 2.5 V
- Packaged in 8-pin SOIC/TSSOP
- Provides a spread spectrum (Center and down spread) clock output
- Accepts a clock or crystal input (provides same frequency dithered output)
- Input frequency range of 4 to 36 MHz
- Output frequency range of 4 to 36 MHz (1X Multiplier)
- Peak reduction by 8 dB to 16 dB typical on 3rd through 19th odd harmonics
- Low EMI feature can be disabled
- 3.3 V tolerant inputs (S0,S1, FRSEL, X1)
- Advanced, low-power CMOS process

Block Diagram



External caps required with crystal for accurate tuning of the clock

Pin Assignment



8 pin (150 mil) SOIC/TSSOP

Spread Direction and Percentage Select Table

S1 Pin 7	S0 Pin 5	Spread Direction	Typical Spread Percentage (%)
0	0	Center	±0.5
0	M	Center	±1.0
0	1	Center	±1.5
M	0	Center	±2.0
M	M	No Spread	-
M	1	Down	-0.5
1	0	Down	-1.0
1	M	Down	-1.5
1	1	Down	-2.0

FRSEL (pin 4)	Input Freq. Range	Multiplier	Output Freq. Range
0	4.0 to 8.0 MHz	X1	4.0 to 8.0 MHz
1	8.0 to 16.0MHz	X1	8.0 to 16.0MHz
M	16.0 to 36.0MHz	X1	16.0 to 36.0MHz

0 = connect to GND
M = unconnected (floating)
1 = connect directly to VDD

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X2	XO	Crystal connection to a 4 to 36 MHz crystal. Leave unconnected for clock.
2	VDD	Power	Connect to +2.5 V.
3	GND	Power	Connect to ground.
4	FRSEL	Input	Function select for input frequency range. Default to mid-level “M”.
5	S0	Input	Function select 0 input. Selects spread amount and direction per table above (default-internal mid-level).
6	SSCLK	Output	Clock output with spread spectrum.
7	S1	Input	Function select 1 input. Selects spread amount and direction per table above (default-internal mid-level).
8	X1/ICLK	Input	Connect to a 4 to 36 MHz crystal or clock.

External Components

The MK1728A-01 requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD and GND on pins 2 and 3, as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock output and the load is over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω.

Tri-level Select Pin Operation

The S1, S0, and FRSEL select pins are tri-level, meaning they have three separate states to make the selections shown in the table on page 2. To select the M (mid) level, the connection to these pins must be eliminated by either floating them originally, or tri-stating the GPIO pins which drive the select pins.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between the decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

3) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the MK1728A-01. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Crystal Information

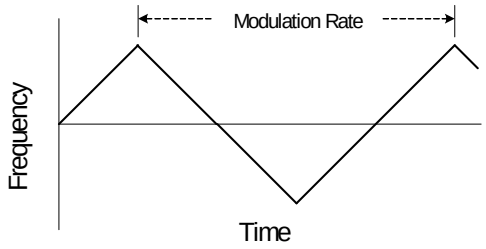
The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation:

$$\text{Crystal caps (pF)} = (C_L - 6) \times 2$$

In the equation, C_L is the crystal load capacitance. So, for a crystal with a 16 pF load capacitance, two 20 pF [(16-6) x 2] capacitors should be used.

Spread Spectrum Profile

The MK1728A-01 low EMI clock generator uses an optimized frequency slew rate algorithm to facilitate down stream tracking of zero delay buffers and other PLL devices. The frequency modulation amplitude is constant with variations of the input frequency.



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1728A-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Outputs	-0.5 V to VDD+0.5 V
All Inputs	-0.5 V to 3.6 V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+2.375	2.5	2.625	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 2.5 V**, Ambient Temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375	2.5	2.625	V
Supply Current	IDD	No load, at 2.5 V, Fin=32 MHz		10	15	mA
Input High Voltage	V_{IH}	FRSEL, S1:S0	VDD-0.6			V
Input High Voltage	V_{IH}	ICLK	1.7			V
Input Middle Voltage	V_{IM}	FRSEL, S1:S0	VDD-1.8		VDD-0.7	V
Input Low Voltage	V_{IL}	FRSEL, S1:S0			0.6	V
Input Low Voltage	V_{IL}	ICLK			0.7	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -10 mA	2.0			V
Output Low Voltage	V_{OL}	I_{OL} = 10 mA			0.4	V
Input Capacitance	C_{IN1}	S0, S1, FRSEL pins		4	6	pF
	C_{IN2}	X1, X2 pins		6	9	pF
Short Circuit Current	I_{OS}			±50		mA

AC Electrical Characteristics

Unless stated otherwise, **VDD = 2.5 V**, C_L=15 pF, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency		Crystal or Clock	4		36	MHz
Output Clock Frequency			4		36	MHz
Input Clock Duty Cycle		Time above VDD/2	45		55	%
Output Clock Duty Cycle		Time above 1.25 V	40	50	60	%
Cycle to Cycle Jitter				200	300	ps
Output Rise Time	t_R	20% to 80% of VDD	1.6	2.8	4	ns
Output Fall Time	t_F	80% to 20% of VDD	1.6	2.8	4	ns
Modulation Rate	F_{MOD}	Fin=24 MHz		32		kHz
EMI Peak Frequency Reduction				8 to 16		dB

Thermal Characteristics – 8 SOIC

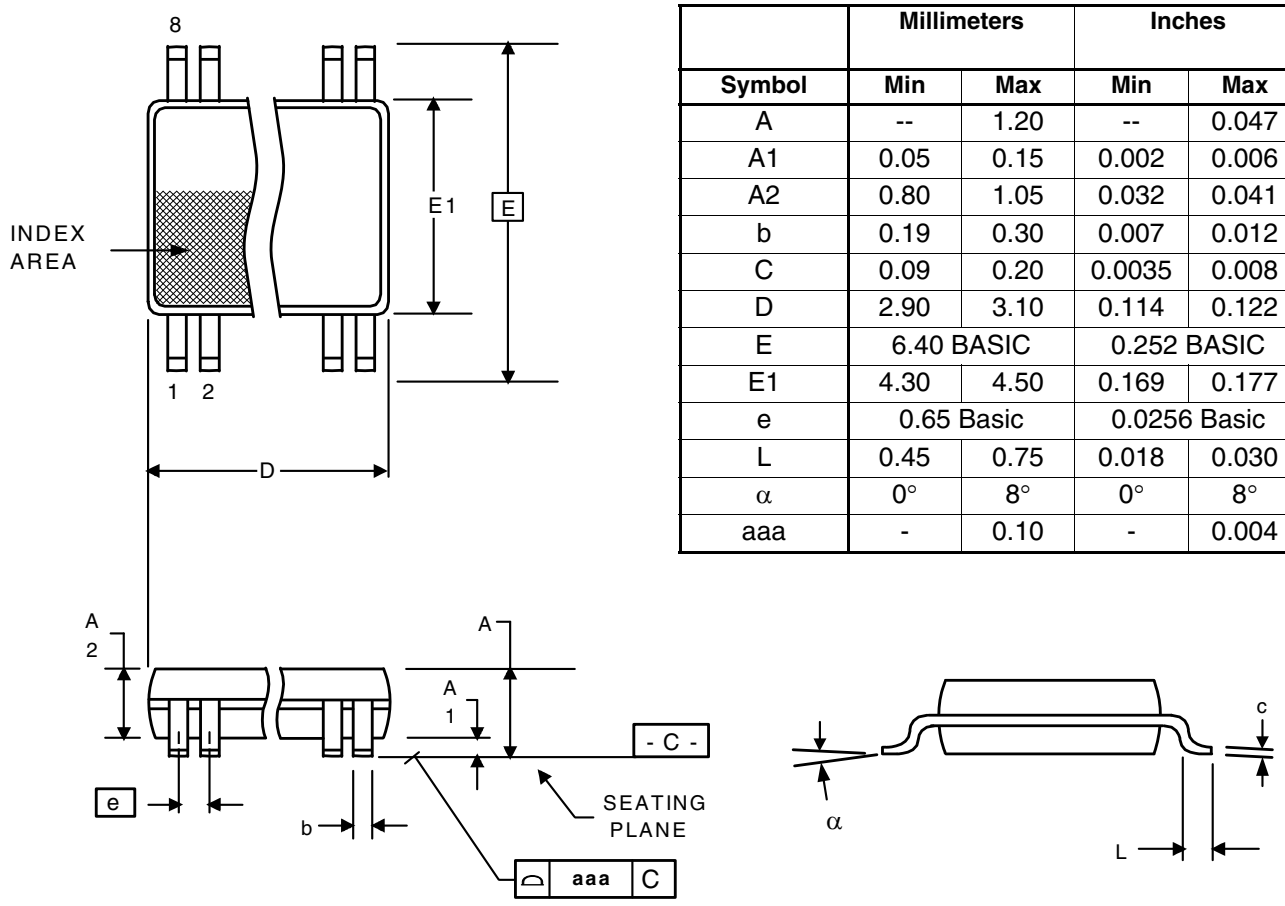
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Thermal Characteristics – 8 TSSOP

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		110		°C/W
	θ_{JA}	1 m/s air flow		100		°C/W
	θ_{JA}	3 m/s air flow		80		°C/W
Thermal Resistance Junction to Case	θ_{JC}			35		°C/W

Package Outline and Package Dimensions (8-pin TSSOP)

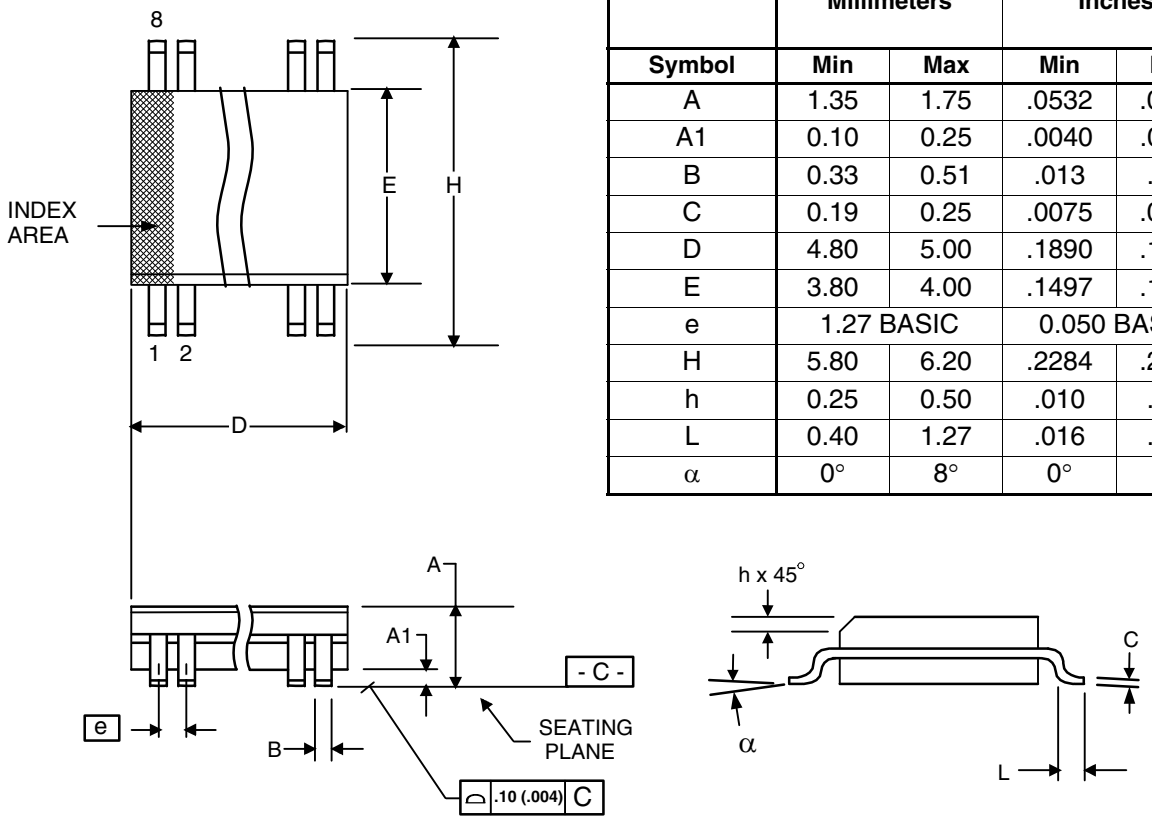
Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	2.90	3.10	0.114	0.122
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	-	0.10	-	0.004

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK1728AG-01LF	28A1L	Tubes	8-pin TSSOP	0 to +70° C
MK1728AG-01LFT	28A1L	Tape and Reel	8-pin TSSOP	0 to +70° C
MK1728AM-01LF	28AM01LF	Tubes	8-pin SOIC	0 to +70° C
MK1728AM-01LFT	28AM01LF	Tape and Reel	8-pin SOIC	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Originator	Date	Description of Change
A	P. Griffith	05/17/06	New device; added seperate voltage ratings for all inputs and all outputs.
B	D. Chan	12/14/10	Updated Rise/Fall Time specs from 1/1.82/2.62 ns to 1.6/2.8/4 ns.
C	J. Chao	08/14/13	Corrected top-side marking information; changed from 1728AG1L to 28A1L (8 TSSOP).

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