

## Description

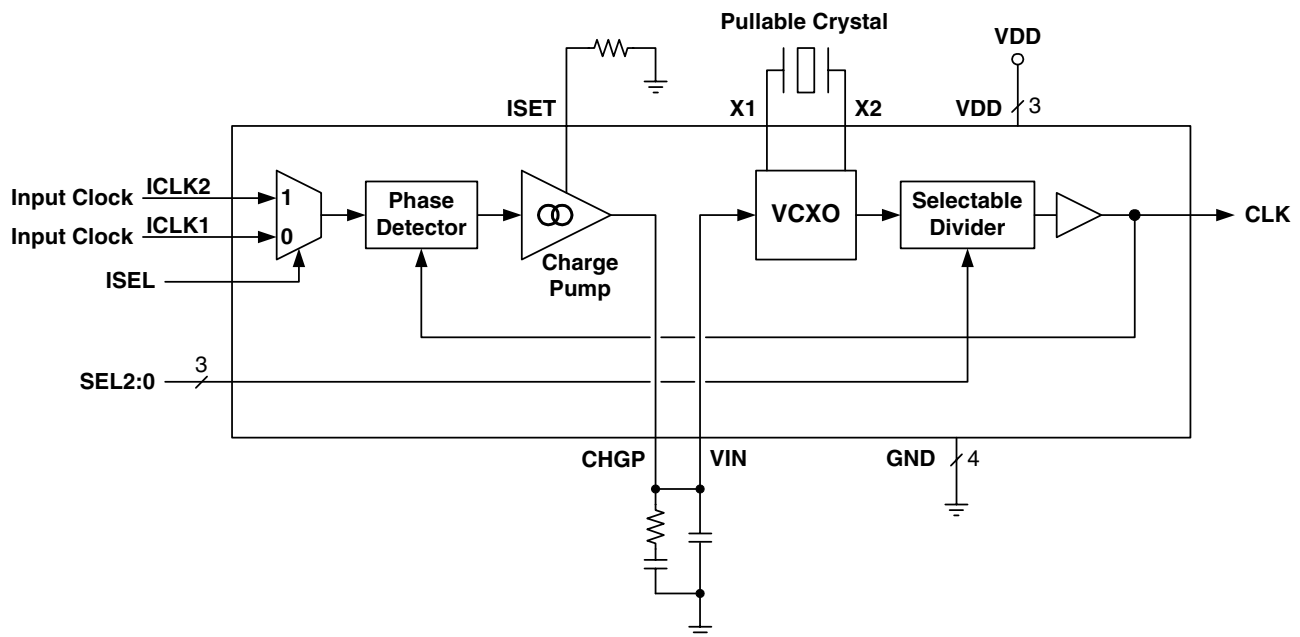
The MK2058-01 is a VCXO (Voltage Controlled Crystal Oscillator) based clock jitter attenuator designed for system clock distribution applications. This monolithic IC, combined with an external inexpensive quartz crystal, can be used to replace a more costly hybrid VCXO retiming module. The device accepts and outputs the same clock frequency in selectable ranges covering 4 kHz to 27 MHz. A dual input mux is also provided.

By controlling the VCXO frequency within a phase-locked loop (PLL), the output clock is phase and frequency locked to the input clock. Through selection of external loop filter components, the PLL loop bandwidth and damping factor can be tailored to meet system clock requirements. A loop bandwidth down to the Hz range is possible.

## Features

- Excellent jitter attenuation for telecom clocks
- Also serves as a general purpose clock jitter attenuator for distributed system clocks and recovered data or video clocks
- 2:1 Input MUX for input reference clocks
- No switching glitches on output
- VCXO-based clock generation offers very low jitter and phase noise generation
- Output clock is phase and frequency locked to the selected input reference clock
- Fixed input to output phase relationship
- $\pm 115\text{ppm}$  minimum crystal frequency pullability range, using recommended crystal
- Industrial temperature range
- Low power CMOS technology
- 20-pin SOIC package
- Pb (lead) free package
- Single 3.3 V power supply

## Block Diagram



## Pin Assignment

|      |      |    |         |
|------|------|----|---------|
| X1   | □ 1  | 20 | □ X2    |
| VDD  | □ 2  | 19 | □ GND   |
| VDD  | □ 3  | 18 | □ ISEL  |
| VDD  | □ 4  | 17 | □ ICLK1 |
| VIN  | □ 5  | 16 | □ ICLK2 |
| GND  | □ 6  | 15 | □ SEL0  |
| GND  | □ 7  | 14 | □ CLK   |
| GND  | □ 8  | 13 | □ NC    |
| CHGP | □ 9  | 12 | □ SEL1  |
| ISET | □ 10 | 11 | □ SEL2  |

20-pin 300 mil SOIC

## Output Clock Selection Table

| SEL2 | SEL1 | SEL0 | Input / Output Range | Crystal Frequency |
|------|------|------|----------------------|-------------------|
| 0    | 0    | 0    | 3.3 to 8.7 kHz       | 3072 x ICLK       |
| 0    | 0    | 1    | 0.64 to 1.68 MHz     | 16 x ICLK         |
| 0    | 1    | 0    | 1 to 2.7 MHz         | 10 x ICLK         |
| 0    | 1    | 1    | 1.7 to 4.5 MHz       | 6 x ICLK          |
| M    | 0    | 0    | 5 to 13 kHz          | 2048 x ICLK       |
| M    | 0    | 1    | 6 to 15.75 kHz       | 1716 x ICLK       |
| M    | 1    | 0    | 26 to 70 kHz         | 384 x ICLK        |
| M    | 1    | 1    | 70 to 210 kHz        | 128 x ICLK        |
| 1    | 0    | 0    | 2.5 to 6.75 MHz      | 4 x ICLK          |
| 1    | 0    | 1    | 3.4 to 9 MHz         | 3 x ICLK          |
| 1    | 1    | 0    | 5 to 13.5 MHz        | 2 x ICLK          |
| 1    | 1    | 1    | 10 to 27 MHz         | 1 x ICLK          |

Note: For SEL input pin programming:  
0 = GND, 1 = VDD, M = Floating

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description  |
|------------|----------|----------|--|
| 1          | X1       | —        | Crystal Input. Connect this pin to the specified crystal.  |
| 2          | VDD      | Power    | Power Supply. Connect to +3.3 V.   |
| 3          | VDD      | Power    | Power Supply. Connect to +3.3 V.   |
| 4          | VDD      | Power    | Power Supply. Connect to +3.3 V.   |
| 5          | VIN      | Input    | VCXO Control Voltage Input. Connect this pin to CHGP pin and the external loop filter as shown in this data sheet.   |
| 6          | GND      | Power    | Connect to ground.   |
| 7          | GND      | Power    | Connect to ground.   |
| 8          | GND      | Power    | Connect to ground.   |
| 9          | CHGP     | Output   | Charge Pump Output. Connect this pin to the external loop filter and to pin VIN.   |
| 10         | ISET     | —        | Charge pump current setting node, connection for setting resistor.   |
| 11         | SEL2     | Input    | Output Frequency Selection Pin 2. Determines output frequency as per table above. Internally biased to VDD/2.  |
| 12         | SEL1     | Input    | Output Frequency Selection Pin 1. Determines output frequency as per table above. Internal pull-up resistor.   |
| 13         | NC       | Input    | No Internal Connection.  |
| 14         | CLK      | Output   | Clock Output.  |
| 15         | SEL0     | Input    | Output Frequency Selection Pin 0. Determines output frequency as per table above. Internal pull-up resistor.   |
| 16         | ICLK2    | Input    | Input Clock Connection 2. Connect an input reference clock to this pin. If unused, connect to ground.  |
| 17         | ICLK1    | Input    | Input Clock Connection 1. Connect an input reference clock to this pin. If unused, connect to ground.  |
| 18         | ISEL     | Input    | Input Selection. Used to select which reference input clock is active. Low input level selects ICLK1, high input level selects ICLK2. Internal pull-up resistor. |
| 19         | GND      | Power    | Connect to ground.   |
| 20         | X2       | —        | Crystal Output. Connect this pin to the specified crystal.   |

## Functional Description

The MK2058-01 is a clock generator IC that generates an output clock directly from an internal VCXO circuit which works in conjunction with an external quartz crystal. The VCXO is controlled by an internal PLL (Phase-Locked Loop) circuit, enabling the device to perform clock regeneration from an input reference clock. The MK2058-01 is configured to provide an output clock that is the same frequency as the input clock. There are 12 selectable input / output frequency ranges, each of which is a submultiple of the supported quartz crystal frequency range. Please refer to the Output Clock Selection Table on Page 2.

Most typical PLL clock devices use an internal VCO (Voltage Controlled Oscillator) for output clock generation. By using a VCXO with an external crystal, the MK2058-01 is able to generate a low jitter, low phase-noise output clock within a low bandwidth PLL. This serves to provide input clock jitter attenuation and enables stable operation with a low-frequency reference clock.

The VCXO circuit requires an external pullable crystal for operation. External loop filter components enable a PLL configuration with low loop bandwidth.

## Application Information

### Input / Output Frequency Configuration

The MK2058-01 is configured to generate an output frequency that is equal to the input reference frequency. Clock frequencies that are supported are those which fall into the ranges listed in the Output Clock Selection Table on Page 2. Input bits SEL2:0 are set according to this table, as is the external crystal frequency. The nominal (center) frequency of the external crystal will be an integer multiple of the input / output clock as specified. Please refer to the Quartz Crystal section on this page regarding external crystal requirements.

### Input Mux

The Input Mux serves to select between two alternate input reference clocks. Upon reselection of the input clock, clock glitches on the output clock will not be generated due to the “fly-wheel” effect of the VCXO (the quartz crystal is a high-Q tuned circuit). When the input clocks are not phase aligned, the phase of the output clock will change to reflect the phase

of the newly selected input at a controlled phase slope (rate of phase change) as influenced by the PLL loop characteristics.

### Quartz Crystal

It is important that the correct type of quartz crystal is used with the MK2058-01. Failure to do so may result in reduced frequency pullability range, inability of the loop to lock, or excessive output phase jitter.

The MK2058-01 operates by phase-locking the VCXO circuit to the input signal of the selected ICLK input. The VCXO consists of the external crystal and the integrated VCXO oscillator circuit. To achieve the best performance and reliability, a crystal device with the recommended parameters (shown below) must be used, and the layout guidelines discussed in the PCB Layout Recommendations section must be followed.

The frequency of oscillation of a quartz crystal is determined by its cut and by the external load capacitance. The MK2058-01 incorporates variable load capacitors on-chip which “pull”, or change, the frequency of the crystal. The crystals specified for use with the MK2058-01 are designed to have zero frequency error when the total of on-chip + stray capacitance is 14 pF. To achieve this, the layout should use short traces between the MK2058-01 and the crystal.

A complete description of the recommended crystal parameters is in application note MAN05.

A list of approved crystals is located on the IDT web site.

### PLL Loop Filter Components

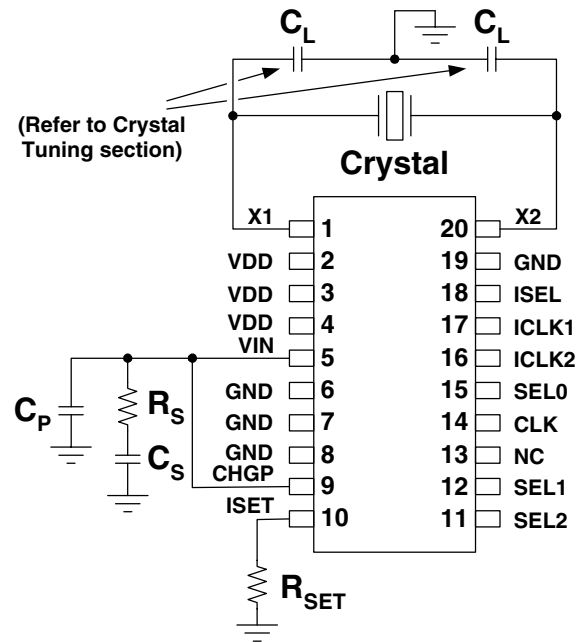
All analog PLL circuits use a loop filter to establish operating stability. The MK2058-01 uses external loop filter components for the following reasons:

- 1) Larger loop filter capacitor values can be used, allowing a lower loop bandwidth. This enables the use of lower input clock reference frequencies and also input clock jitter attenuation capabilities. Larger loop filter capacitors also allow higher loop damping factors when less passband peaking is desired.
- 2) The loop filter values can be user selected to optimize loop response characteristics for a given application.

Referencing the External Component Schematic on this

page, the external loop filter is made up of the components  $R_Z$ ,  $C_1$  and  $C_2$ .  $R_{SET}$  establishes PLL charge pump current and therefore influences loop filter characteristics.

### External Component Schematic



### Recommended Loop Filter Values Vs. Output Frequency Range Selection

| SEL2 | SEL1 | SEL0 | Crystal Multiplier (N) | $R_{SET}$      | $R_S$          | $C_S$       | $C_P$  | Loop Bandwidth (-3dB point) | Damping Factor |
|------|------|------|------------------------|----------------|----------------|-------------|--------|-----------------------------|----------------|
| 0    | 0    | 0    | 3072                   | 120 k $\Omega$ | 750 k $\Omega$ | 0.1 $\mu$ F | 4.7 nF | 14 Hz                       | 1              |
| 0    | 0    | 1    | 16                     | 1.4 M $\Omega$ | 160 k $\Omega$ | 0.1 $\mu$ F | 4.7 nF | 60 Hz                       | 1              |
| 0    | 1    | 0    | 10                     | 1.4 M $\Omega$ | 130 k $\Omega$ | 0.1 $\mu$ F | 4.7 nF | 75 Hz                       | 1              |
| 0    | 1    | 1    | 6                      | 1.4 M $\Omega$ | 100 k $\Omega$ | 0.1 $\mu$ F | 4.7 nF | 95 Hz                       | 1              |
| M    | 0    | 0    | 2048                   | 540 k $\Omega$ | 1.2 M $\Omega$ | 0.1 $\mu$ F | 4.7 nF | 8.5 Hz                      | 1              |
| M    | 0    | 1    | 1716                   | 540 k $\Omega$ | 1.1 M $\Omega$ | 0.1 $\mu$ F | 4.7 nF | 9 Hz                        | 1              |
| M    | 1    | 0    | 384                    | 1.4 M $\Omega$ | 820 k $\Omega$ | 0.1 $\mu$ F | 4.7 nF | 12 Hz                       | 1              |
| M    | 1    | 1    | 128                    | 1.4 M $\Omega$ | 470 k $\Omega$ | 0.1 $\mu$ F | 4.7 nF | 20 Hz                       | 1              |
| 1    | 0    | 0    | 4                      | 1.4 M $\Omega$ | 82 k $\Omega$  | 0.1 $\mu$ F | 4.7 nF | 120 Hz                      | 1              |
| 1    | 0    | 1    | 3                      | 1.4 M $\Omega$ | 68 k $\Omega$  | 0.1 $\mu$ F | 4.7 nF | 130 Hz                      | 1              |
| 1    | 1    | 0    | 2                      | 1.4 M $\Omega$ | 56 k $\Omega$  | 0.1 $\mu$ F | 4.7 nF | 160 Hz                      | 1              |
| 1    | 1    | 1    | 1                      | 1.4 M $\Omega$ | 39 k $\Omega$  | 0.1 $\mu$ F | 4.7 nF | 225 Hz                      | 1              |

Note: For SEL input pin programming: 0 = GND, 1 = VDD, M = Floating

A “normalized” PLL loop bandwidth may be calculated as follows:

$$NBW = \frac{R_S \times I_{CP} \times 575}{N}$$

The “normalized” bandwidth equation above does not take into account the effects of damping factor or the second pole. However, it does provide a useful approximation of filter performance.

The loop damping factor is calculated as follows:

$$\text{Damping Factor} = R_S \times \sqrt{\frac{625 \times I_{CP} \times C_S}{N}}$$

Where:

- $R_S$  = Value of resistor in loop filter (Ohms)
- $I_{CP}$  = Charge pump current (amps)  
(refer to Charge Pump Current Table, below)
- $N$  = Crystal multiplier shown in the above table
- $C_S$  = Value of capacitor  $C_1$  in loop filter (Farads)

As a general rule, the following relationship should be maintained between components  $C_1$  and  $C_2$  in the loop filter:

$$C_P = \frac{C_S}{20}$$

### Charge Pump Current Table

| $R_{SET}$      | Charge Pump Current ( $I_{CP}$ ) |
|----------------|----------------------------------|
| 1.4 M $\Omega$ | 10 $\mu$ A                       |
| 680 k $\Omega$ | 20 $\mu$ A                       |
| 540 k $\Omega$ | 25 $\mu$ A                       |
| 120 k $\Omega$ | 100 $\mu$ A                      |

Special considerations must be made in choosing loop components  $C_S$  and  $C_P$ . These recommendations can be found in the design aid tools section of [www.idt.com](http://www.idt.com)

### Series Termination Resistor

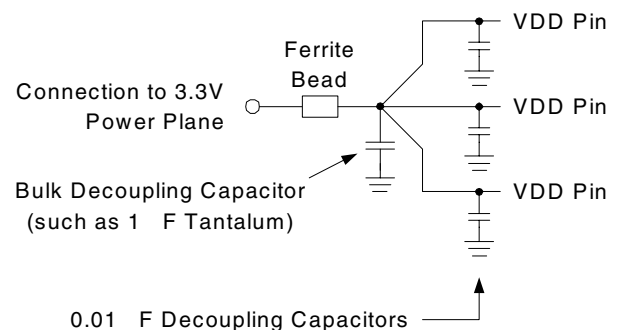
Clock output traces over one inch should use series termination. To series terminate a 50 $\Omega$  trace (a commonly used trace impedance), place a 33 $\Omega$  resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20 $\Omega$  (The optional series termination resistor is not shown in the External Component Schematic.)

### Decoupling Capacitors

As with any high-performance mixed-signal IC, the MK2058-01 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01 $\mu$ F must be connected between each VDD and the PCB ground plane. To further guard against interfering system supply noise, the MK2058-01 should use one common connection to the PCB power plane as shown in the diagram on the next page. The ferrite bead and bulk capacitor help reduce lower frequency noise in the supply that can lead to output clock phase modulation.

### Recommended Power Supply Connection for Optimal Device Performance



### Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground, shown as  $C_L$  in the External Component Schematic. These capacitors are used to adjust the stray capacitance of the

board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no via's) between the crystal and device.

In most cases the load capacitors will not be required. They should not be stuffed on the prototype evaluation board as the indiscriminate use of these trim capacitors will typically cause more crystal centering error than their absence. If the need for the load capacitors is later determined, the values will fall within the 1-4 pF range. The need for, and value of, these trim capacitors can only be determined at prototype evaluation. Please refer to MAN05 for the procedure to determine the component values.

### PCB Layout Recommendations

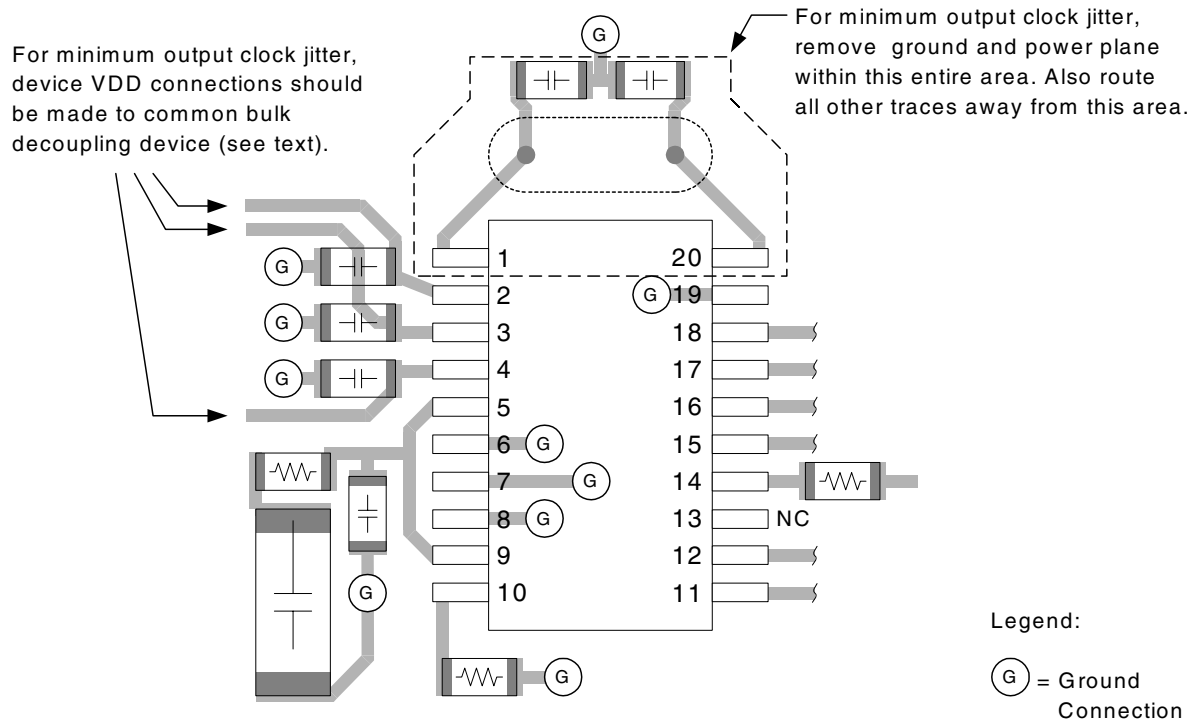
For optimum device performance and lowest output phase noise, the following guidelines should be observed. Please also refer to the Recommended PCB Layout drawing on page 7.

- 1) Each 0.01 $\mu$ F decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.
- 2) The loop filter components must also be placed close to the CHGP and VIN pins.  $C_P$  should be closest to the device. Coupling of noise from other system signal traces should be minimized by keeping traces short and away from active signal traces. Use of vias should be avoided.
- 3) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.
- 4) To minimize EMI, the 33 $\Omega$  series termination resistor (if needed) should be placed close to the clock output.
- 5) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the MK2058-01. This includes signal traces just underneath the device, or on layers adjacent to the ground

plane layer used by the device.

The IDT Applications Note MAN05 may also be referenced for additional suggestions on layout of the crystal section.

## Recommended PCB Layout



## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2058-01. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                          | Rating              |
|-------------------------------|---------------------|
| Supply Voltage, VDD           | 7 V                 |
| All Inputs and Outputs        | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | -40 to +85° C       |
| Storage Temperature           | -65 to +150° C      |
| Junction Temperature          | 125° C              |
| Soldering Temperature         | 260° C              |

## Recommended Operation Conditions

| Parameter   | Min.  | Typ. | Max.  | Units |
|---|-------|------|-------|-------|
| Ambient Operating Temperature                     | -40   |      | +85   | °C    |
| Power Supply Voltage (measured in respect to GND) | +3.15 | +3.3 | +3.45 | V     |

## DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85°C

| Parameter                        | Symbol           | Conditions                          | Min.    | Typ. | Max.    | Units |
|----------------------------------|------------------|-------------------------------------|---------|------|---------|-------|
| Operating Voltage                | VDD              |                                     | 3.15    | 3.3  | 3.45    | V     |
| Supply Current                   | IDD              | Clock outputs unloaded, VDD = 3.3 V |         | 10   | 15      | mA    |
| Input High Voltage, SEL2         | V <sub>IH</sub>  |                                     | VDD-0.5 |      |         | V     |
| Input Low Voltage, SEL2          | V <sub>IL</sub>  |                                     |         |      | 0.5     | V     |
| Input High Voltage, ISEL, SEL1:0 | V <sub>IH</sub>  |                                     | 2       |      |         | V     |
| Input Low Voltage, ISEL, SEL1:0  | V <sub>IL</sub>  |                                     |         |      | 0.8     | V     |
| Input High Voltage, ICLK1, 2     | V <sub>IH</sub>  |                                     | VDD/2+1 |      |         | V     |
| Input Low Voltage, ICLK1, 2      | V <sub>IL</sub>  |                                     |         |      | VDD/2-1 | V     |
| Input High Current               | I <sub>IH</sub>  | V <sub>IH</sub> = VDD               | -10     |      | +10     | μA    |
| Input Low Current                | I <sub>IL</sub>  | V <sub>IL</sub> = 0                 | -10     |      | +10     | μA    |
| Input Capacitance, except X1     | C <sub>IN</sub>  |                                     |         | 7    |         | pF    |
| Output High Voltage (CMOS Level) | V <sub>OH</sub>  | I <sub>OH</sub> = -4 mA             | VDD-0.4 |      |         | V     |
| Output High Voltage              | V <sub>OH</sub>  | I <sub>OH</sub> = -8 mA             | 2.4     |      |         | V     |
| Output Low Voltage               | V <sub>OL</sub>  | I <sub>OL</sub> = 8 mA              |         |      | 0.4     | V     |
| Short Circuit Current            | I <sub>OS</sub>  |                                     |         | ±50  |         | mA    |
| VIN, VCXO Control Voltage        | V <sub>XC</sub>  |                                     | 0       |      | VDD     | V     |
| Nominal Output Impedance         | Z <sub>OUT</sub> |                                     |         | 20   |         | Ω     |



## AC Electrical Characteristics

Unless stated otherwise,  $V_{DD} = 3.3\text{ V} \pm 5\%$ , Ambient Temperature  $-40$  to  $+85^\circ\text{C}$

| Parameter                                     | Symbol    | Conditions                                  | Min. | Typ. | Max. | Units  |
|---|-----------|---|------|------|------|--------|
| VCXO Crystal Pull Range                       | $f_{XP}$  | Using recommended crystal                   | -115 |      | +115 | ppm    |
| VCXO Crystal Nominal Frequency                | $f_X$     |   | 8.5  |      | 27   | MHz    |
| Input Jitter Tolerance                        | $t_{ji}$  |   |      |      | 0.4  | UI     |
| Input pulse width (1)                         | $t_{pi}$  |   | 10   |      |      | ns     |
| Output Frequency Error                        | $F_{OUT}$ | ICLK = 0 ppm error                          | 0    | 0    | 0    | ppm    |
| Output Duty Cycle (% high time)               | $t_{OD}$  | Measured at $V_{DD}/2$ , $C_L=15\text{ pF}$ | 40   |      | 60   | %      |
| Output Rise Time                              | $t_{OR}$  | 0.8 to 2.0V, $C_L=15\text{ pF}$             |      |      | 1.5  | ns     |
| Output Fall Time                              | $t_{OF}$  | 2.0 to 0.8 V, $C_L=15\text{ pF}$            |      |      | 1.5  | ns     |
| Skew, Input to Output Clock                   | $t_{IO}$  | Rising edges, $C_L=15\text{ pF}$            | -5   |      | +5   | ns     |
| Cycle Jitter (short term jitter)              | $t_{ja}$  |   |      | 150  |      | ps p-p |
| Timing Jitter, Filtered 500 Hz-1.3 MHz (OC-3) | $t_{jf}$  | Referenced to Mitel/Zarlink MT9045, Note 2  |      | 210  |      | ps p-p |
| Timing Jitter, Filtered 65 kHz-1.3 MHz (OC-3) | $t_{jf}$  | Referenced to Mitel/Zarlink MT9045, Note 2  |      | 150  |      | ps p-p |

Note 1: Minimum high or low time of input clock.

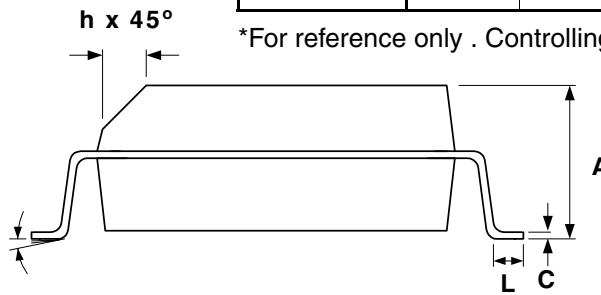
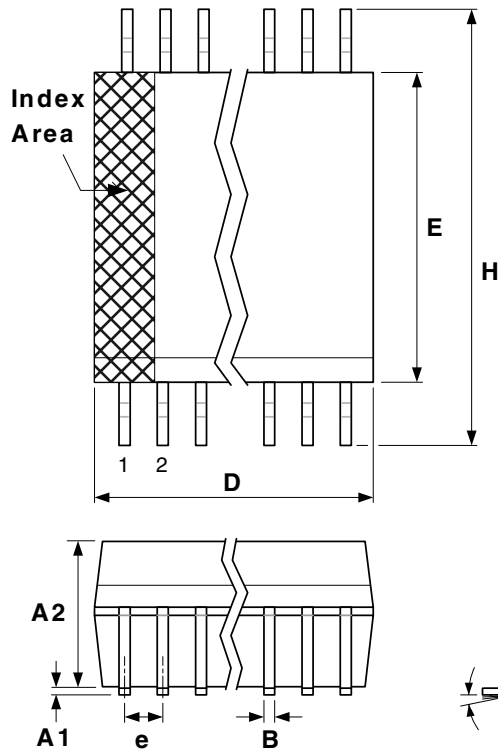
Note 2: Input reference is the 19.44 MHz output from a Mitel/Zarlink MT9045 device in freerun mode (SEL2:0 = 111, 19.44 MHz external crystal).

## Thermal Characteristics

| Parameter                              | Symbol        | Conditions     | Min. | Typ. | Max. | Units              |
|--|---------------|----------------|------|------|------|--------------------|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air      |      | 83   |      | $^\circ\text{C/W}$ |
|  | $\theta_{JA}$ | 1 m/s air flow |      | 71   |      | $^\circ\text{C/W}$ |
|  | $\theta_{JA}$ | 3 m/s air flow |      | 58   |      | $^\circ\text{C/W}$ |
| Thermal Resistance Junction to Case    | $\theta_{JC}$ |                |      | 46   |      | $^\circ\text{C/W}$ |

## Package Outline and Package Dimensions (20-pin SOIC, 300 Mil. Wide Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol   | Millimeters |       | Inches*     |       |
|----------|-------------|-------|-------------|-------|
|          | Min         | Max   | Min         | Max   |
| A        | --          | 2.65  | --          | 0.104 |
| A1       | 1.10        | --    | 0.0040      | --    |
| A2       | 2.05        | 2.55  | 0.081       | 0.100 |
| B        | 0.33        | 0.51  | 0.013       | 0.020 |
| C        | 0.18        | 0.32  | 0.007       | 0.013 |
| D        | 12.60       | 13.00 | 0.496       | 0.512 |
| E        | 7.40        | 7.60  | 0.291       | 0.299 |
| e        | 1.27 Basic  |       | 0.050 Basic |       |
| H        | 10.00       | 10.65 | 0.394       | 0.419 |
| h        | 0.25        | 0.75  | 0.010       | 0.029 |
| L        | 0.40        | 1.27  | 0.016       | 0.050 |
| $\alpha$ | 0°          | 8°    | 0°          | 8°    |

\*For reference only . Controlling dimensions in mm.

## Ordering Information

| Part / Order Number | Marking       | Shipping Packaging | Package     | Temperature   |
|---------------------|---------------|--------------------|-------------|---------------|
| MK2058-01SILF       | MK2058-01SILF | Tubes              | 20-pin SOIC | -40 to +85° C |
| MK2058-01SILFTR     | MK2058-01SILF | Tape and Reel      | 20-pin SOIC | -40 to +85° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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