

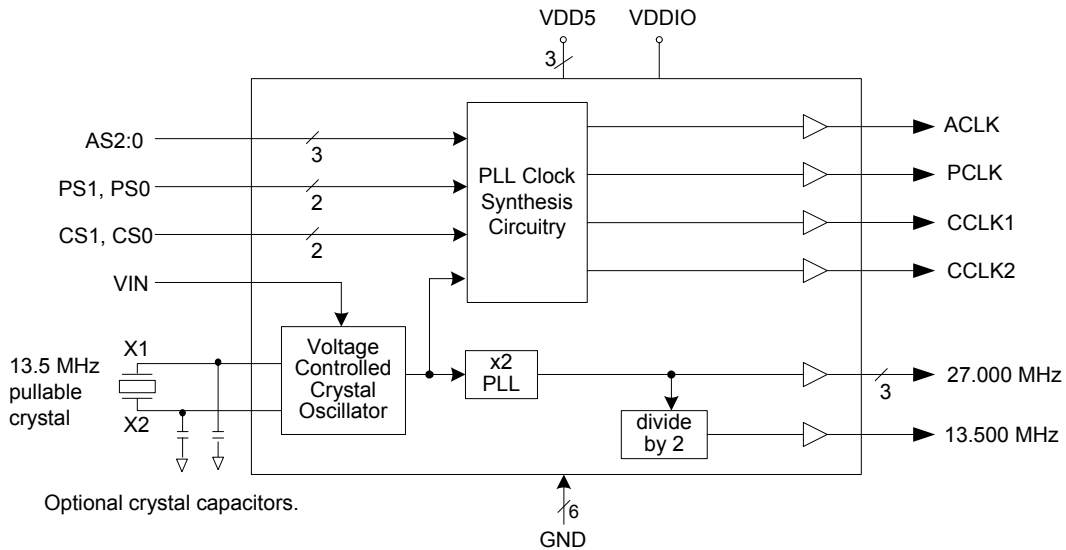
Description

The MK2771-16 is a low-cost, low-jitter, high-performance VCXO and clock synthesizer designed for set-top boxes. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3 V input voltage to cause the output clocks to vary by ± 100 ppm. Using IDT's patented VCXO and analog Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 13.5 MHz pullable crystal input to produce multiple output clocks including two selectable processor clocks, a selectable audio clock, two communications clocks, a 13.5 MHz clock, and three 27 MHz clocks. All clocks are frequency locked to the 27 MHz output (and to each other) with zero ppm error, so any output can be used as the VCXO output.

Features

- Packaged in 28-pin QSOP
- RoHS 5 (green) or RoHS 6 (green and lead free) compliant package
- On-chip patented VCXO with pull range of 200 ppm
- VCXO tuning voltage of 0 to 3 V
- Processor frequencies include 16.66, 20, 25, 32, 40, and 50 MHz
- Audio clocks support 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz sampling rates
- Zero ppm synthesis error in all clocks (all exactly track 27 MHz VCXO)
- Uses an inexpensive 13.5 MHz pullable crystal
- Full CMOS output swings with 25 mA output drive capability at TTL levels
- Advanced, low-power, sub-micron CMOS process
- 5 V operating voltage with 3.3 V capable I/O

Block Diagram



Pin Assignment

| | | | |
|-------|----|----|-------|
| PS0 | 1 | 28 | AS1 |
| X2 | 2 | 27 | AS0 |
| GND | 3 | 26 | CS0 |
| X1 | 4 | 25 | 27M |
| VDD5 | 5 | 24 | GND |
| VIN | 6 | 23 | 27M |
| VDDIO | 7 | 22 | VDD5 |
| VDD5 | 8 | 21 | AS2 |
| CS1 | 9 | 20 | GND |
| GND | 10 | 19 | GND |
| GND | 11 | 18 | 27M |
| PCLK | 12 | 17 | CCLK1 |
| CCLK2 | 13 | 16 | PS1 |
| ACLK | 14 | 15 | 13.5M |

28-pin QSOP

Processor Clock Select Table (MHz)

| PS1 | PS0 | PCLK |
|-----|-----|--------|
| 0 | 0 | 50 |
| 0 | 1 | 16.667 |
| M | 0 | 25 |
| M | 1 | 32 |
| 1 | 0 | 40 |
| 1 | 1 | 20 |

Audio Clock Table (MHz)

| AS2 | AS1 | AS0 | ACLK |
|-----|-----|-----|---------|
| 0 | 0 | 0 | 8.192 |
| 0 | 0 | 1 | 11.2896 |
| 0 | 1 | 0 | 12.288 |
| 0 | 1 | 1 | 5.6448 |
| 1 | 0 | 0 | 18.432 |
| 1 | 0 | 1 | 16.9344 |
| 1 | 1 | 0 | 49.152 |
| 1 | 1 | 1 | 21.576 |

Communications Clock Table (MHz)

| CS1 | CS0 | CCLK1 | CCLK2 |
|-----|-----|---------|--------|
| 0 | 0 | Low | 33.333 |
| 0 | 1 | Low | 24.576 |
| 1 | 0 | 11.0592 | 18.432 |
| 1 | 1 | 11.0592 | 3.6864 |

0 = connect directly to ground

1 = connect directly to VDDIO

M = leave floating or unconnected

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|-----------------|---|
| 1 | PS0 | Input | Processor clock select 0. Selects PCLK frequency. See table above. Internal pull-up resistor. |
| 2 | X2 | XO | Crystal connection. Connect to a 13.5 MHz fundamental mode pullable crystal. |
| 3, 10, 11 | GND | Power | Connect to ground. |
| 4 | X1 | XI | Crystal connection. Connect to a 13.5 MHz fundamental mode pullable crystal. |
| 5, 8, 22 | VDD5 | Power | Connect to +5 V. |
| 6 | VIN | Input | Voltage input to VCXO. Zero to 3 V signal which controls the frequency of the VCXO. |
| 7 | VDDIO | Power | Connect to +3.3 V or +5 V. Amplitude of inputs and outputs will match this. |
| 9 | CS1 | Input | Communications clock select pin 1. Selects CCLK 1 and 2 per table above. Internal pull-up. |
| 12 | PCLK | Output | Processor clock output. Determined by status of PS1, PS0. |
| 13 | CCLK2 | Output | Communications clock output 2 determined by status of CS1, CS0 per table above. |
| 14 | ACLK | Output | Audio clock output. Determined by status of AS2:0 per table above. |
| 15 | 13.5M | Output | 13.5 MHz VCXO clock output. |
| 16 | PS1 | Tri-level Input | Processor Clock Select 1. Selects PCLK frequency. See table above. Self-biased to M. |
| 17 | CCLK1 | Output | Communications clock output 1 determined by status of CS1, CS0 per table above. |
| 18, 23, 25 | 27M | Output | 27 MHz VCXO clock output. |
| 19, 20, 24 | GND | Power | Connect to ground. |
| 21 | AS2 | Input | Audio clock select 2. Selects ACLK on pin 14. See table above. Internal pull-up resistor. |
| 26 | CS0 | Input | Communications clock select pin 0. Selects CCLK 1 and 2 per table above. Internal pull-up. |
| 27 | AS0 | Input | Audio clock select 0. Selects ACLK on pin 14. See table above. Internal pull-up resistor. |
| 28 | AS1 | Input | Audio clock select 1. Selects ACLK on pin 14. See table above. Internal pull-up resistor. |

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK2771-16. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|---------------------|
| Supply Voltage, VDD (referenced to GND) | 7 V |
| Inputs and Clock Outputs (referenced to GND) | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature | 0 to +70° C |
| Storage Temperature | -65 to +150° C |
| Junction Temperature | 125° C |
| Soldering Temperature | 260° C |

DC Electrical Characteristics

Unless stated otherwise, VDD = 5 V ±5%, Ambient Temperature 0 to +70° C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------------|-----------------|--------------------------|---------|------|------|-------|
| Operating Voltage | VDD | | 4.75 | | 5.25 | V |
| Operating Voltage | VDDIO | All inputs/outputs | 3.00 | | 5.25 | V |
| Input High Voltage, X1 pin only | V _{IH} | | 3.5 | 2.5 | | V |
| Input Low Voltage, X1 pin only | V _{IL} | | | 2.5 | 1.5 | V |
| Input High Voltage (except PS1) | V _{IH} | | 2 | | | V |
| Input Low Voltage (except PS1) | V _{IL} | | | | 0.8 | V |
| Input High Voltage (PS1 only) | V _{IH} | | VDD-0.5 | | | V |
| Input Low Voltage (PS1 only) | V _{IL} | | | | 0.5 | V |
| Output High Voltage | V _{OH} | I _{OH} = -25 mA | 2.4 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 25 mA | – | – | 0.4 | V |
| Output High Voltage, CMOS Level | V _{OH} | I _{OH} = -8 mA | VDD-0.4 | | | V |
| Operating Supply Current | IDD5 | No load, Note 1 | | 42 | | mA |
| Operating Supply Current | IDDIO | No load, VDDIO = 3.3 V | | 19 | | mA |
| Short Circuit Current | I _{OS} | Each output | | ±100 | | mA |
| Input Capacitance, except X1 | C _{IN} | Except X1, X2 | | 7 | | pF |
| Frequency Synthesis Error | | All clocks | | | 0 | ppm |
| VIN, VCXO Control Voltage | | | 0 | | 3 | V |

AC Electrical Characteristics

Unless stated otherwise, $V_{DD} = 5\text{ V} \pm 5\%$, Ambient Temperature 0 to $+70^{\circ}\text{C}$

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-------------------------------------|----------|---|-----------|-----------|------|-------|
| Crystal Input Frequency | | | | 13.5 | | MHz |
| Output Clock Rise Time | t_{OR} | 0.8 to 2.0 V | | 1.5 | | ns |
| Output Clock Fall Time | t_{OF} | 2.0 to 0.8 V | | 1.5 | | ns |
| Output Clock Duty Cycle | t_{OD} | At 1.4 V | 40 | | 60 | % |
| Maximum Absolute Jitter, short term | t_{ja} | | | 300 | | ps |
| 27 MHz Output Pullability | | $0\text{V} \leq V_{IN} \leq 3\text{V}$, Note 3 | ± 100 | ± 140 | | ppm |

Note 1: With all clocks at highest frequencies.

Note 2: With a pullable crystal that conforms to IDT's specifications.

Pullable Crystal Specifications

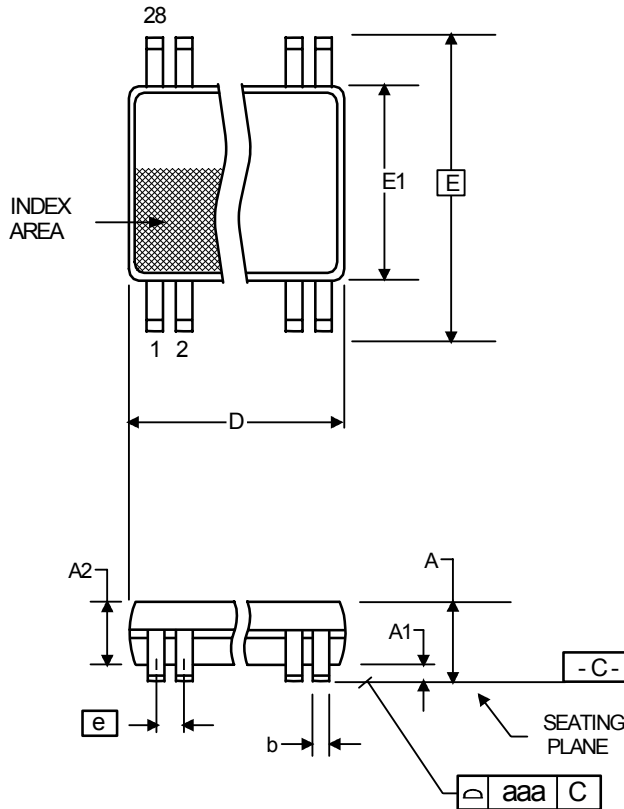
| | |
|----------------------------------|---------------------------|
| Frequency | 13.500000 MHz |
| Correlation (load) Capacitance | 14 pF |
| C0/C1 | 240 max. |
| ESR | 25 Ω max. |
| Operating Temperature | 0 to 70°C |
| Initial Accuracy | ± 20 ppm |
| Temperature plus Aging Stability | ± 50 ppm |

External Components

The MK2771-16 requires a minimum number of external components for proper operation. Use a low inductance ground plane, connect all GNDs to this. Connect $0.01\mu\text{F}$ decoupling caps on pins 5, 7, 8 and 22 directly to the ground plane, as close to the MK2771-16 as possible. A series termination resistor of 33Ω may be used for each clock output. The 13.500 MHz crystal must be connected as close to the chip as possible. The crystal should be a parallel mode, pullable, with load capacitance of 14 pF. Consult IDT full specifications. Please obey Application Note MAN05 for pullable crystal layout info except for the following: the MK2771-16 introduces a GND pin (pin #3) between the pullable crystal pins. This ground should be brought in straight from the right side underneath the device.

Package Outline and Package Dimensions (28-pin QSOP)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | | Inches* | |
|----------|-------------|-------|-------------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A2 | -- | 1.50 | -- | .059 |
| b | 0.20 | 0.30 | 0.008 | 0.012 |
| c | 0.18 | 0.25 | 0.007 | 0.010 |
| D | 9.80 | 10.00 | 0.386 | 0.394 |
| E | 5.80 | 6.20 | 0.228 | 0.244 |
| E1 | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 0.635 Basic | | 0.025 Basic | |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| α | 0° | 8° | 0° | 8° |

*For reference only. Controlling dimensions in mm.

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|--------------|--------------------|-------------|-------------|
| MK2771-16RLF | MK2771-16RLF | Tubes | 28-pin SSOP | 0 to +70° C |
| MK2771-16RLFTR | MK2771-16RLF | Tape and Reel | 28-pin SSOP | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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