

# NP45N06VUK, NP45N06PUK

60 V – 45 A – N-channel Power MOS FET

Application: Automotive

R07DS0953EJ0200

Rev.2.00

May 24, 2018

## Description

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

## Features

- Super low on-state resistance  
 $R_{DS(on)} = 9.6 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 23 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 1690 \text{ pF TYP. (} V_{DS} = 25 \text{ V)}$
- Designed for automotive application and AEC-Q101 qualified

## Ordering Information

Part No.	Lead Plating	Packing		Package
NP45N06VUK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252 (MP-3ZP)
NP45N06VUK-E2-AY *1			Taping (E2 type)	
NP45N06PUK-E1-AY *1		Tape 800 p/reel	Taping (E1 type)	TO-263 (MP-25ZP)
NP45N06PUK-E2-AY *1			Taping (E2 type)	

Note: \*1 Pb-free (This product does not contain Pb in the external electrode)

## Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit	
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	60	V	
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V	
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 45$	A	
Drain Current (pulse) *1, 3	$I_{D(pulse)}$	$\pm 135$	A	
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	75	W	
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	NP45N06VUK	$P_{T2}$	1.2	W
	NP45N06PUK		1.8	W
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$	
Storage Temperature	$T_{stg}$	-55 to +175	$^\circ\text{C}$	
Repetitive Avalanche Current *2, 3	$I_{AR}$	19	A	
Repetitive Avalanche Energy *2, 3	$E_{AR}$	36	mJ	

## Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-C)}$ *3		2.00 $^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$ *3	NP45N06VUK	125 $^\circ\text{C/W}$
		NP45N06PUK	83.3 $^\circ\text{C/W}$

Notes: \*1  $T_C = 25^\circ\text{C}$ ,  $P_w \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

\*2  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

\*3 Not subject of production test. Verified by design/characterization.

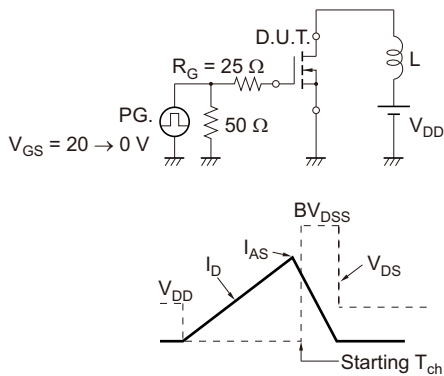
Electrical Characteristics (T<sub>A</sub> = 25°C)

Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	2.0	3.0	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA
Forward Transfer Admittance *1	y <sub>fs</sub>	17	34	—	S	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 23 A
Drain to Source On-state Resistance *1	R <sub>DS(on)</sub>	—	7.8	9.6	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 23 A
Input Capacitance *2	C <sub>iss</sub>	—	1690	2540	pF	V <sub>DS</sub> = 25 V V <sub>GS</sub> = 0 V f = 1 MHz
Output Capacitance *2	C <sub>oss</sub>	—	155	240	pF	
Reverse Transfer Capacitance *2	C <sub>rss</sub>	—	70	130	pF	
Turn-on Delay Time *2	t <sub>d(on)</sub>	—	15	40	ns	V <sub>DD</sub> = 30 V, I <sub>D</sub> = 23 A V <sub>GS</sub> = 10 V R <sub>G</sub> = 0 Ω
Rise Time *2	t <sub>r</sub>	—	5	20	ns	
Turn-off Delay Time *2	t <sub>d(off)</sub>	—	37	80	ns	
Fall Time *2	t <sub>f</sub>	—	3	10	ns	
Total Gate Charge *2	Q <sub>G</sub>	—	30	45	nC	V <sub>DD</sub> = 48 V V <sub>GS</sub> = 10 V I <sub>D</sub> = 45 A
Gate to Source Charge	Q <sub>GS</sub>	—	8	—	nC	
Gate to Drain Charge	Q <sub>GD</sub>	—	8	—	nC	
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>	—	0.9	1.5	V	I <sub>F</sub> = 45 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>	—	32	—	ns	I <sub>F</sub> = 45 A, V <sub>GS</sub> = 0 V
Reverse Recovery Charge	Q <sub>rr</sub>	—	35	—	nC	di/dt = 100 A/μs

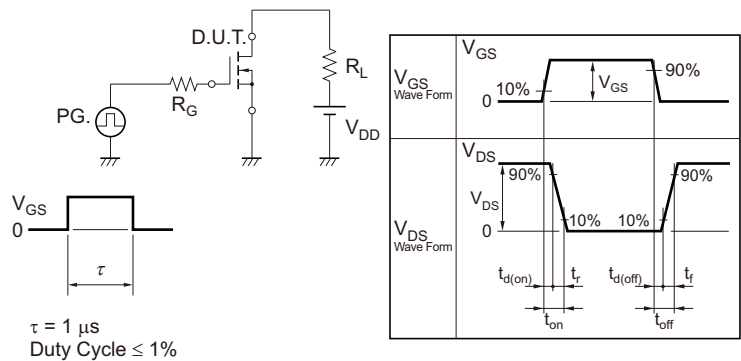
Note: \*1 Pulsed test

Note: \*2 Not subject of production test. Verified by design/characterization.

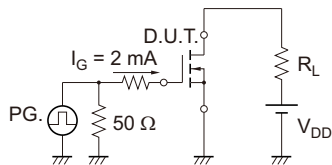
TEST CIRCUIT 1 AVALANCHE CAPABILITY



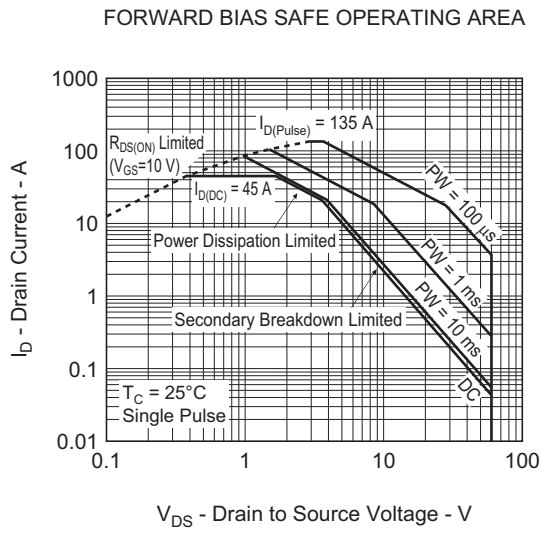
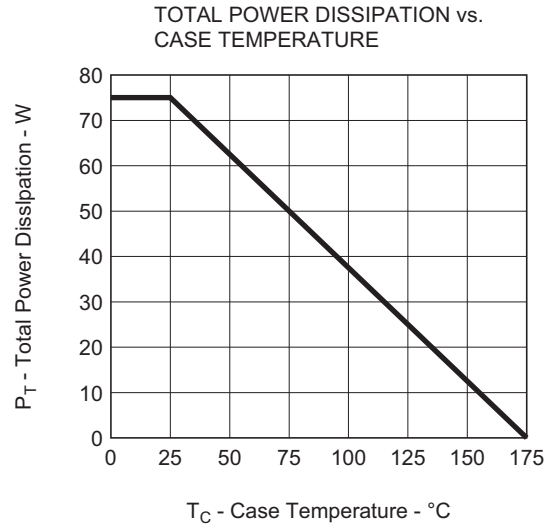
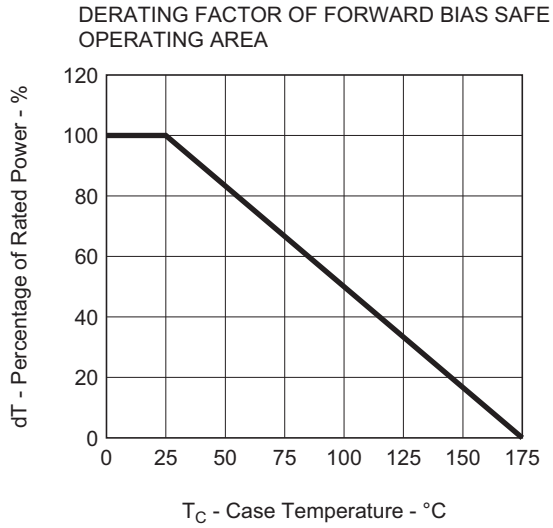
TEST CIRCUIT 2 SWITCHING TIME



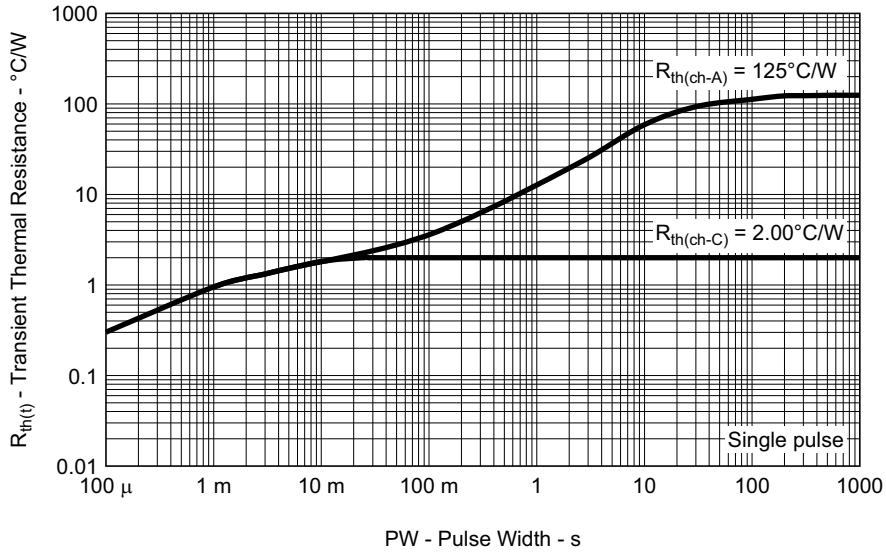
TEST CIRCUIT 3 GATE CHARGE



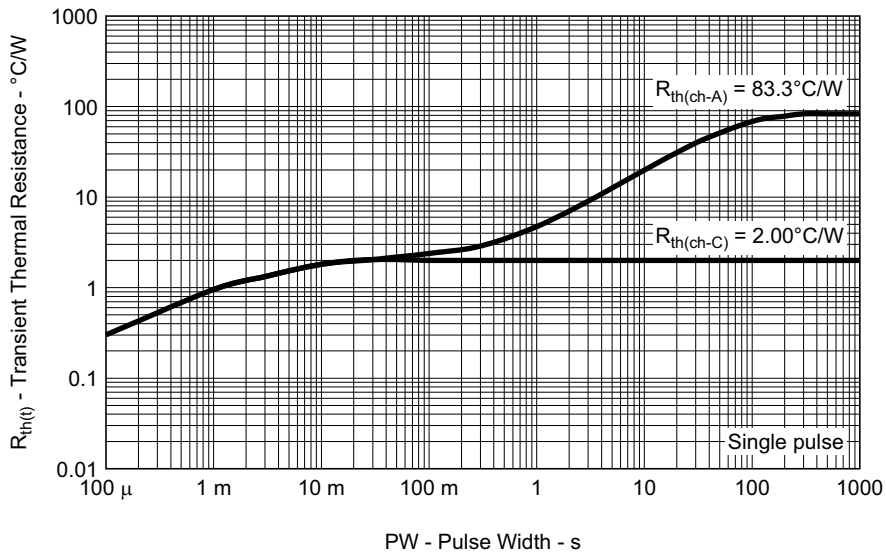
Typical Characteristics (T<sub>A</sub> = 25°C)



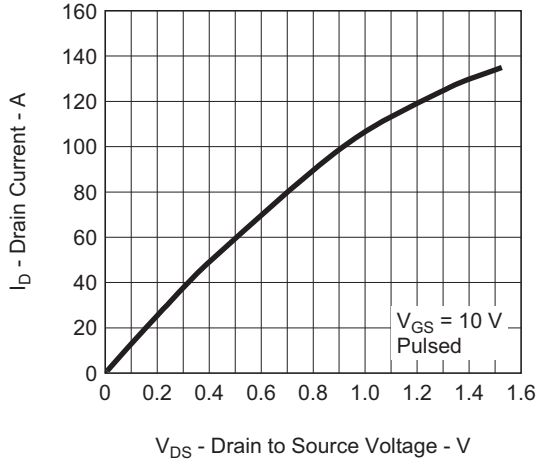
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP45N06VUK)



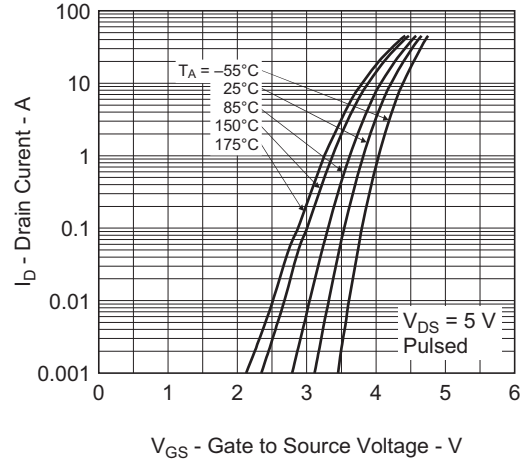
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP45N06PUK)



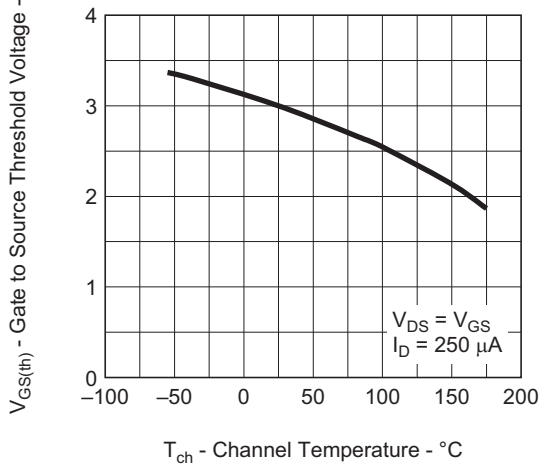
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



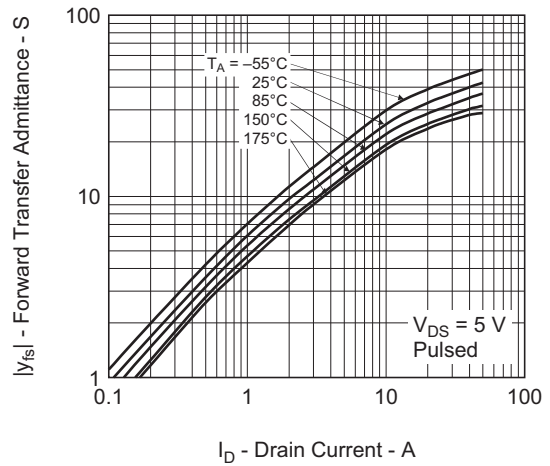
FORWARD TRANSFER CHARACTERISTICS



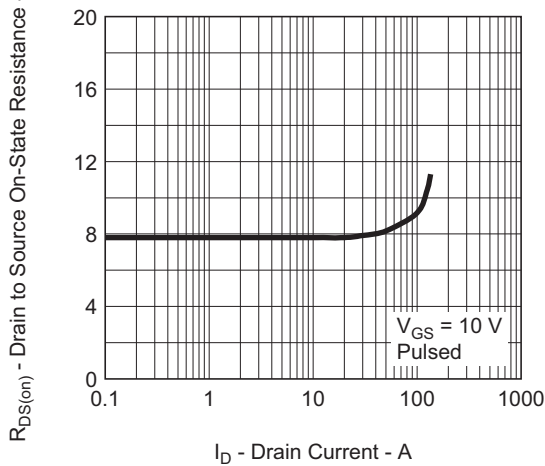
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



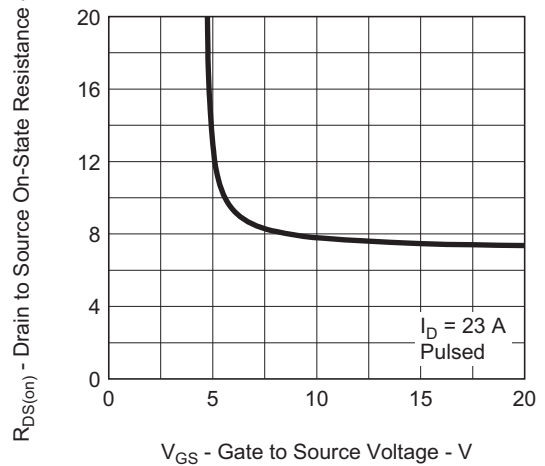
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



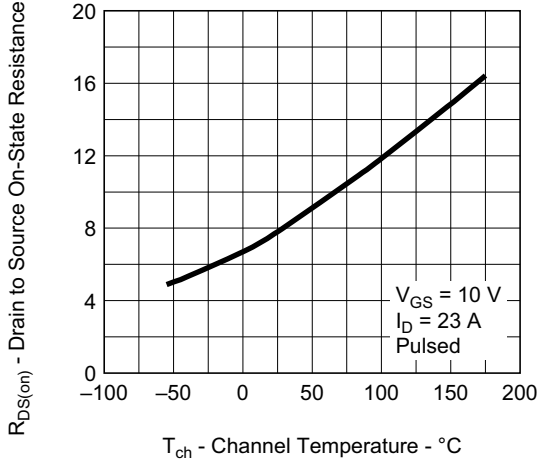
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



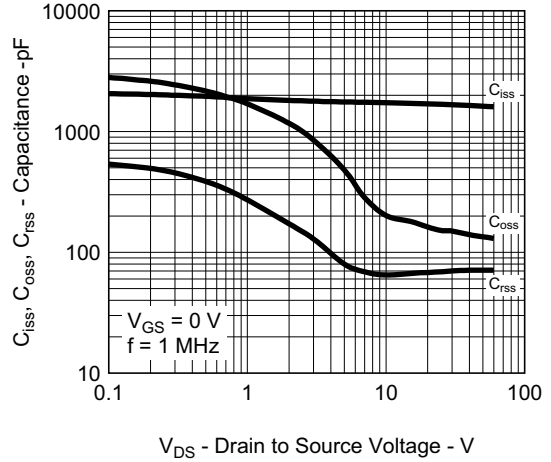
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



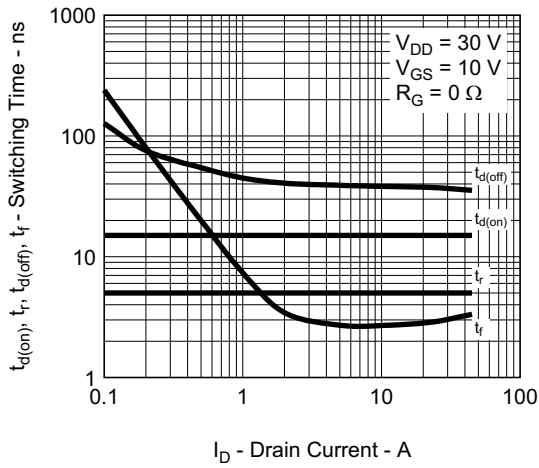
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



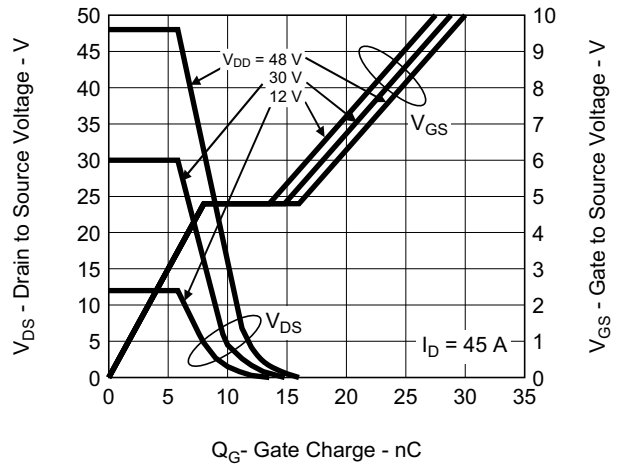
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



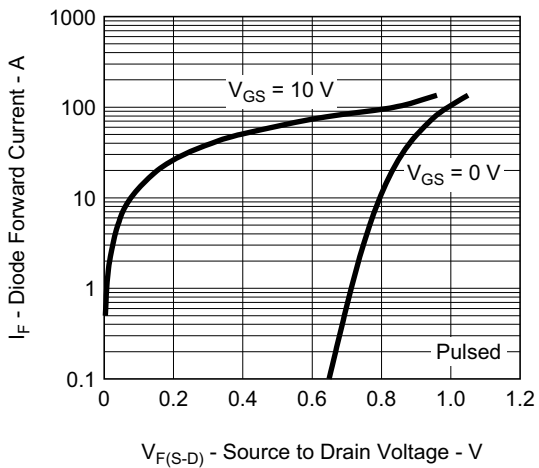
SWITCHING CHARACTERISTICS



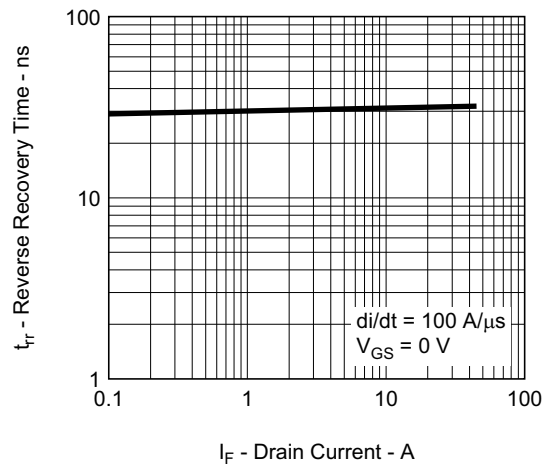
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

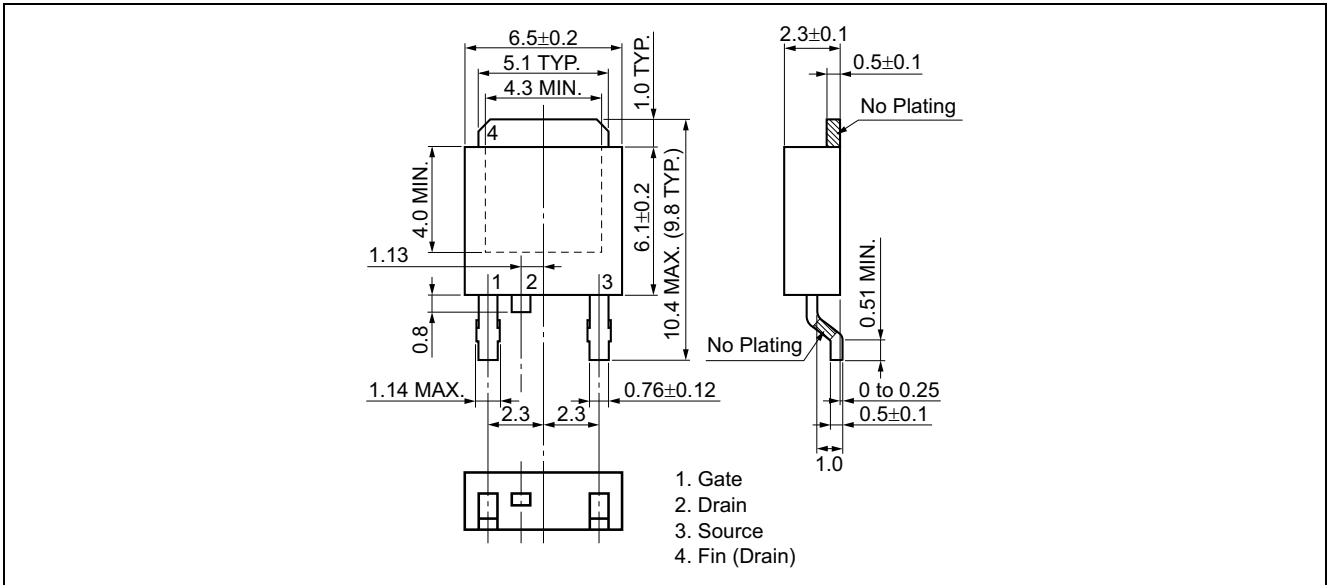


REVERSE RECOVERY TIME vs. DRAIN CURRENT

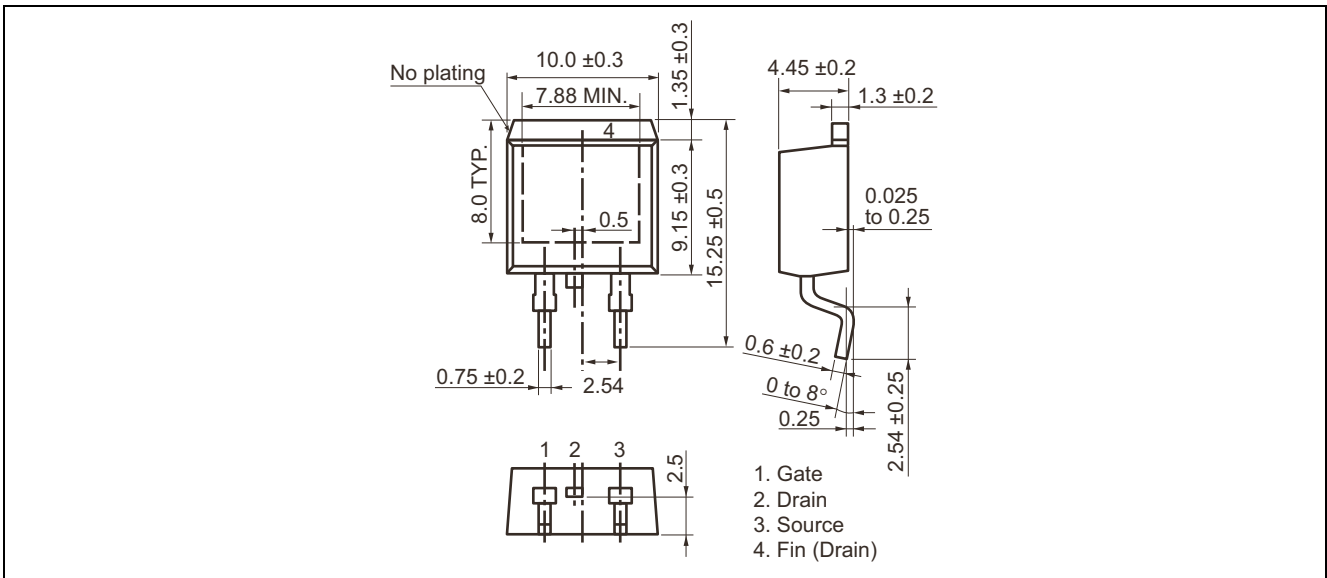


Package Drawing (Unit: mm)

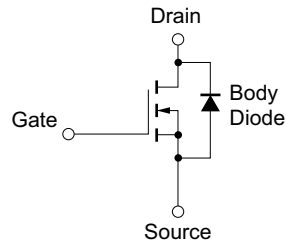
TO-252 (MP-3ZP) (Mass: 0.3 g TYP.)



TO-263 (MP-25ZP) (Mass: 1.48 g TYP.)



## Equivalent Circuit



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.



<b>Revision History</b>	<b>NP45N06VUK, NP45N06PUK Data Sheet</b>
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Rev.	Date	Description	
		Page	Summary
1.00	Nov 20, 2012	—	First Edition Issued
2.00	May 24 ,2018	1	Note 3 was added
		2	Note 2 was added

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1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.  
Tel: +1-408-432-8888, Fax: +1-408-434-5351

#### Renesas Electronics Canada Limited

9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3  
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#### Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-651-700, Fax: +44-1628-651-804

#### Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany  
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#### Renesas Electronics (China) Co., Ltd.

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Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

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#### Renesas Electronics Taiwan Co., Ltd.

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#### Renesas Electronics India Pvt. Ltd.

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