

# NP75N04VDK

40 V - 75 A - N-channel Power MOS FET Application: Automotive

R07DS1015EJ0200 Rev.2.00 May 24, 2018

### **Description**

The NP75N04VDK is N-channel MOS Field Effect Transistors designed for high current switching applications.

#### **Features**

- Super low on-state resistance
  - $R_{DS(on)} = 5.7 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 38 \text{ A})$
- Low  $C_{iss}$ :  $C_{iss} = 1630 \text{ pF TYP.} (V_{DS} = 25 \text{ V})$
- Logic level drive type
- Designed for automotive application and AEC-Q101 qualified

### **Ordering Information**

Part No.	Lead Plating	Pac	Package	
NP75N04VDK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252 (MP-3ZP)
NP75N04VDK-E2-AY *1			Taping (E2 type)	

Note: \*1 Pb-free (This product does not contain Pb in the external electrode)

### **Absolute Maximum Ratings** $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	40	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±75	Α
Drain Current (pulse) *1, 3	I <sub>D(pulse)</sub>	±225	Α
Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T1</sub>	75	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.2	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
Repetitive Avalanche Current *2, 3	I <sub>AR</sub>	22	Α
Repetitive Avalanche Energy *2, 3	Ear	48	mJ

### **Thermal Resistance**

Notes: \*1 T<sub>C</sub> = 25°C,  $P_W \le 10~\mu s$ , Duty Cycle  $\le 1\%$ 

\*2 R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20 V  $\rightarrow$  0 V

\*3. Not subject of production test. Verified by design/characterization.

### **Electrical Characteristics** (T<sub>A</sub> = 25°C)

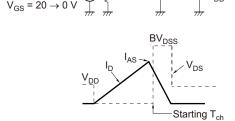
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_		1	μΑ	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>	_		±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.5	1.8	2.5	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
Forward Transfer Admittance *1	y <sub>fs</sub>	26	52	_	S	$V_{DS} = 5 \text{ V}, I_{D} = 38 \text{ A}$
Drain to Source On-state Resistance *1	R <sub>DS(on)1</sub>	_	4.7	5.7	mΩ	$V_{GS} = 10 \text{ V}, I_D = 38 \text{ A}$
	R <sub>DS(on)2</sub>	_	6.3	12.6	mΩ	$V_{GS} = 4.5 \text{ V}, I_D = 19 \text{ A}$
Input Capacitance *2	C <sub>iss</sub>	_	1630	2450	pF	V <sub>DS</sub> = 25 V
Output Capacitance *2	Coss	_	220	330	pF	$V_{GS} = 0 V$
Reverse Transfer Capacitance *2	C <sub>rss</sub>	_	100	180	pF	f = 1 MHz
Turn-on Delay Time *2	t <sub>d(on)</sub>	_	12	26	ns	$V_{DD} = 20 \text{ V}, I_D = 38 \text{ A}$
Rise Time *2	t <sub>r</sub>	_	5	13	ns	V <sub>GS</sub> = 10 V
Turn-off Delay Time *2	$t_{d(off)}$	_	40	80	ns	$R_G = 0 \Omega$
Fall Time *2	t <sub>f</sub>	_	5	13	ns	
Total Gate Charge *2	$Q_G$	_	27	41	nC	V <sub>DD</sub> = 32 V
Gate to Source Charge	Q <sub>G</sub> s	_	8	_	nC	V <sub>GS</sub> = 10 V
Gate to Drain Charge	Q <sub>GD</sub>	_	4	_	nC	I <sub>D</sub> = 75 A
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>	_	0.9	1.5	V	I <sub>F</sub> = 75 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>	_	32		ns	I <sub>F</sub> = 75 A, V <sub>GS</sub> = 0 V
Reverse Recovery Charge	Qrr	_	35		nC	di/dt = 100 A/μs

Note: \*1 Pulsed test

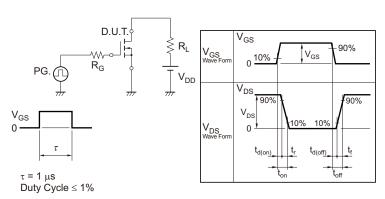
Note: \*2 Not subject of production test. Verified by design/characterization.

### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $R_{G} = 25 \Omega$ $PG. \square \leq 50 \Omega$ $T V_{DD}$



### **TEST CIRCUIT 2 SWITCHING TIME**

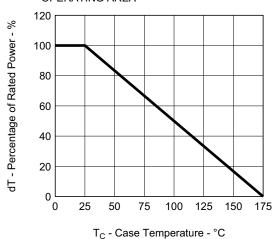


### **TEST CIRCUIT 3 GATE CHARGE**

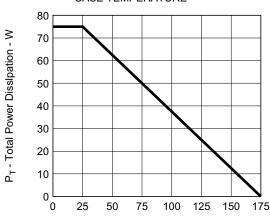
$$\begin{array}{c|c} D.U.T. \\ \hline I_G = 2 \text{ mA} \\ \hline WV \\ \hline \end{array} \begin{array}{c} R_L \\ \hline V_{DD} \end{array}$$

### **Typical Characteristics** (T<sub>A</sub> = 25°C)

# DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

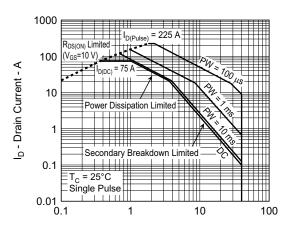


# TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



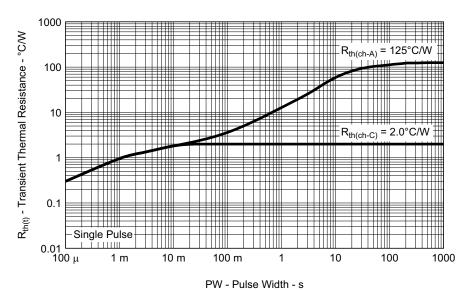
T<sub>C</sub> - Case Temperature - °C

### FORWARD BIAS SAFE OPERATING AREA

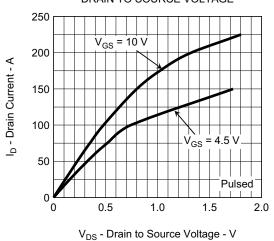


### $\mathrm{V}_{\mathrm{DS}}$ - Drain to Source Voltage - V

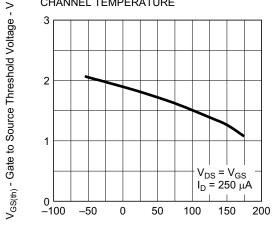
### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



# DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

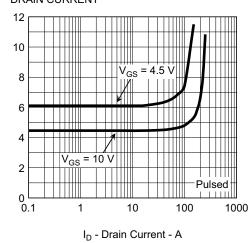


# GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

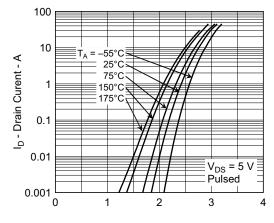


# DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

 $\rm T_{ch}$  - Channel Temperature -  $^{\circ}\rm C$ 

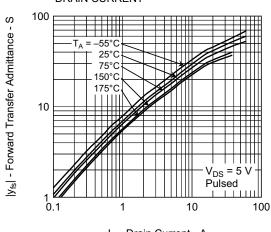


#### FORWARD TRANSFER CHARACTERISTICS



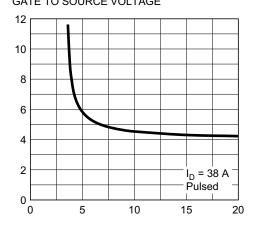
V<sub>GS</sub> - Gate to Source Voltage - V

# FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



I<sub>D</sub> - Drain Current - A

# DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



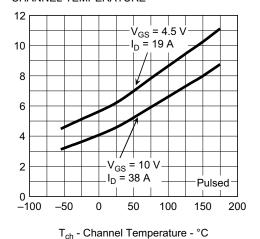
V<sub>GS</sub> - Gate to Source Voltage - V

 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 

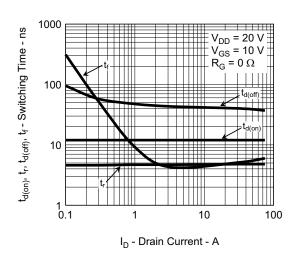
 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 

 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 

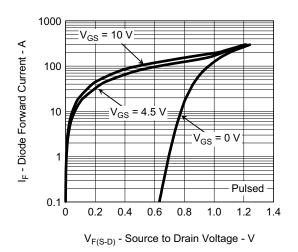
#### DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



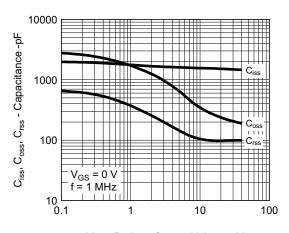
### SWITCHING CHARACTERISTICS



#### SOURCE TO DRAIN DIODE FORWARD VOLTAGE

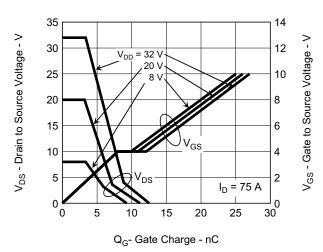


#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

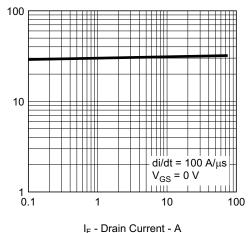


V<sub>DS</sub> - Drain to Source Voltage - V

#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS



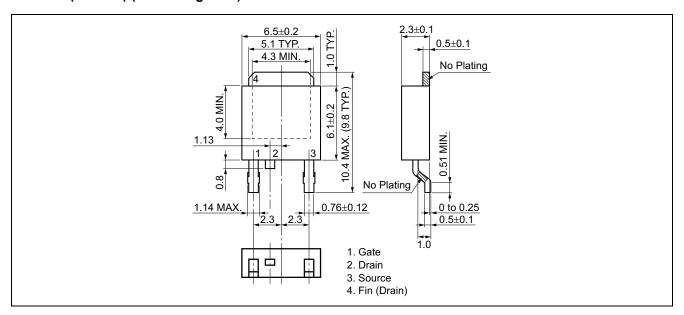
#### REVERSE RECOVERY TIME vs. DRAIN CURRENT



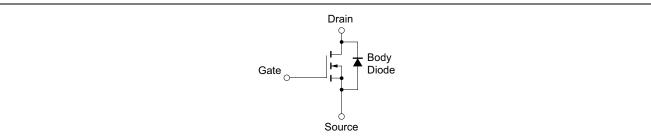
t<sub>rr</sub> - Reverse Recovery Time - ns

### Package Drawing (Unit: mm)

### TO-252 (MP-3ZP) (Mass: 0.3g TYP.)



### **Equivalent Circuit**



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

**Revision History** 

### NP75N04VDK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Feb 21, 2013	_	First Edition Issued	
2.00	May 24 ,2018	1	Note 3 was added	
		2	Note 2 was added	

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