To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

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RENESAS

R1EX24008ASA00A
R1EX24008ATA00A

Two-wire serial interface
8k EEPROM (1-kword × 8-bit)

REJ03C0351-0100
Rev.1.00
Oct. 26, 2009

Description

R1EX24xxx series are two-wire serial interface EEPROM (Electrically Erasable and Programmable ROM). They realize high speed, low power consumption and a high level of reliability by employing advanced MONOS memory technology and CMOS process and low voltage circuitry technology. They also have a 16-byte page programming function to make their write operation faster.

Note: Renesas Technology's serial EEPROM are authorized for using consumer applications such as cellular phone, camcorders, audio equipment. Therefore, please contact Renesas Technology's sales office before using industrial applications such as automotive systems, embedded controllers, and meters.

Features

- Single supply: 1.8 V to 5.5 V
- Two-wire serial interface (I^2C serial bus)
- Clock frequency: 400 kHz
- Power dissipation:
  - — Standby: 2 µA (max)
  - — Active (Read): 1 mA (max)
  - — Active (Write): 3.0 mA (max)
- Automatic page write: 16-byte/page
- Write cycle time: 5 ms
- Endurance: 1,000k Cycles @25°C
- Data retention: 100 Years @25°C

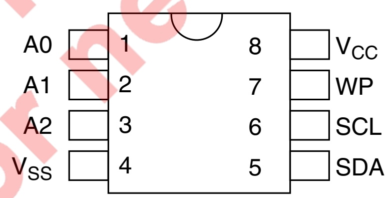
- Small size packages: SOP-8pin, TSSOP-8pin
- Shipping tape and reel
  - — TSSOP 8-pin: 3,000 IC/reel
  - — SOP 8-pin: 2,500 IC/reel
- Temperature range: −40 to +85°C
- Lead free products.

Ordering Information

Type No.	Internal organization	Operating voltage	Frequency	Package
R1EX24008ASA00A	8k bit (1024× 8-bit)	1.8 V to 5.5 V	400 kHz	150 mil 8-pin plastic SOP PRSP0008DF-B (FP-8DBV) Lead free
R1EX24008ATA00A	8k bit (1024× 8-bit)	1.8 V to 5.5 V	400 kHz	8-pin plastic TSSOP PTSP0008JC-B (TTP-8DAV) Lead free

Pin Arrangement

8-pin SOP/8-pin TSSOP

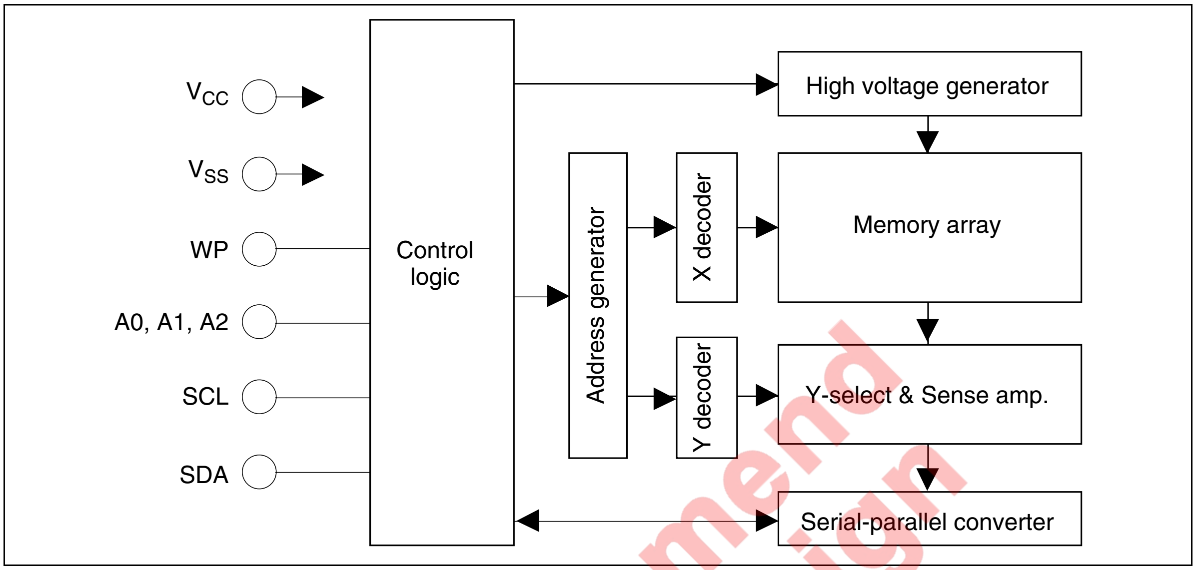


(Top view)

Pin Description

Pin name	Function
A0 to A2	Device address
SCL	Serial clock input
SDA	Serial data input/output
WP	Write protect
V_{cc}	Power supply
V_{ss}	Ground

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V_{SS}	V_{CC}	–0.6 to +7.0	V
Input voltage relative to V_{SS}	Vin	–0.5*[2] to +7.0*[3]	V
Operating temperature range*[1]	Topr	–40 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. Including electrical characteristics and data retention.
2. Vin (min): –3.0 V for pulse width ≤ 50 ns.
3. Should not exceed V_{CC} + 1.0 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	1.8	—	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	V_{CC} × 0.7	—	V_{CC} + 0.5	V
Input low voltage	V_{IL}	–0.3*[1]	—	V_{CC} × 0.3	V
Operating temperature	Topr	–40	—	+85	°C

Notes: 1. V_{IL} (min): –1.0 V for pulse width ≤ 50 ns.

DC Characteristics (Ta = –40 to +85°C, V_{CC} = 1.8 V to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2.0	µA	V_{CC} = 5.5 V, Vin = 0 to 5.5 V
Output leakage current	I_{LO}	—	—	2.0	µA	V_{CC} = 5.5 V, Vout = 0 to 5.5 V
Standby V_{CC} current	I_{SB}	—	1.0	2.0	µA	Vin = V_{SS} or V_{CC}
Read V_{CC} current	I_{CC1}	—	—	1.0	mA	V_{CC} = 5.5 V, Read at 400 kHz
Write V_{CC} current	I_{CC2}	—	—	3.0	mA	V_{CC} = 5.5 V, Write at 400 kHz
Output low voltage	V_{OL2}	—	—	0.4	V	V_{CC} = 2.7 to 5.5 V, I_{OL} = 3.0 mA
	V_{OL1}	—	—	0.2	V	V_{CC} = 1.8 to 2.7 V, I_{OL} = 1.5 mA

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance (A0 to A2, SCL, WP)	Cin*[1]	—	—	6.0	pF	Vin = 0 V
Output capacitance (SDA)	$C_{I/O}$*[1]	—	—	6.0	pF	Vout = 0 V

Note: 1. Not 100% tested.

Memory cell characteristics (V_{CC} = 1.8 V to 5.5 V)

	Ta=25°C	Ta=85°C	Notes
Endurance	1,000k Cycles min.	100k Cycles min	1
Data retention	100 Years min.	10 Years min.	1

Notes: 1. Not 100% tested.

AC Characteristics (Ta = –40 to +85°C, V_{CC} = 1.8 to 5.5 V)

Test Conditions

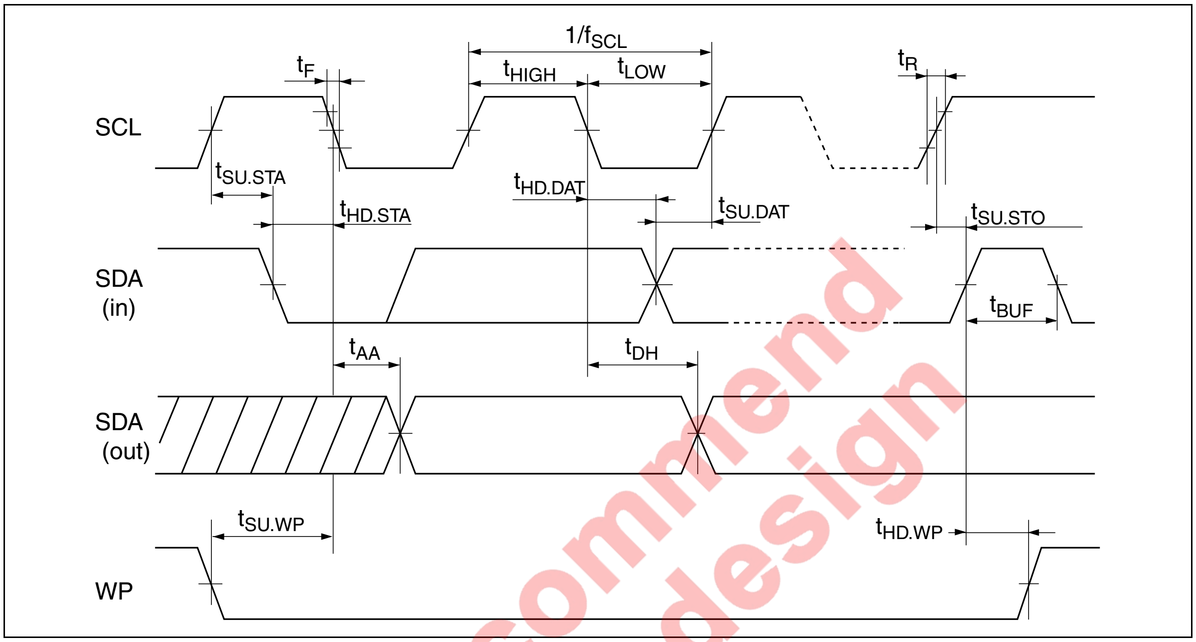
- Input pules levels:
  — $V_{IL} = 0.2 \times V_{CC}$
  — $V_{IH} = 0.8 \times V_{CC}$
- Input rise and fall time: ≤ 20 ns
- Input and output timing reference levels: $0.5 \times V_{CC}$
- Output load: TTL Gate + 100 pF

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Clock frequency	f_{SCL}	—	—	400	kHz	
Clock pulse width low	t_{LOW}	1200	—	—	ns	
Clock pulse width high	t_{HIGH}	600	—	—	ns	
Noise suppression time	t_{I}	—	—	50	ns	1
Access time	t_{AA}	100	—	900	ns	
Bus free time for next mode	t_{BUF}	1200	—	—	ns	
Start hold time	$t_{HD.STA}$	600	—	—	ns	
Start setup time	$t_{SU.STA}$	600	—	—	ns	
Data in hold time	$t_{HD.DAT}$	0	—	—	ns	
Data in setup time	$t_{SU.DAT}$	100	—	—	ns	
Input rise time	t_{R}	—	—	300	ns	1
Input fall time	t_{F}	—	—	300	ns	1
Stop setup time	$t_{SU.STO}$	600	—	—	ns	
Data out hold time	t_{DH}	50	—	—	ns	
Write protect hold time	$t_{HD.WP}$	1200	—	—	ns	
Write protect setup time	$t_{SU.WP}$	0	—	—	ns	
Write cycle time	t_{WC}	—	—	5	ms	2

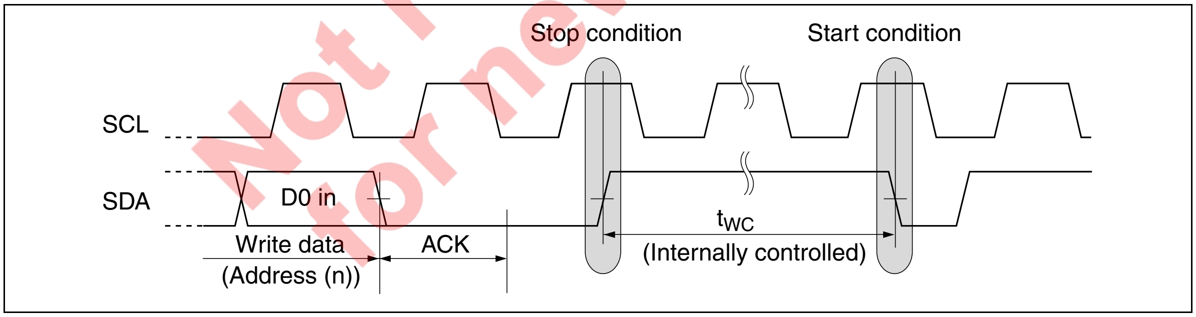
Notes: 1. Not 100% tested.
2. t_{WC} is the time from a stop condition to the end of internally controlled write cycle.

Timing Waveforms

Bus Timing



Write Cycle Timing



Pin Function

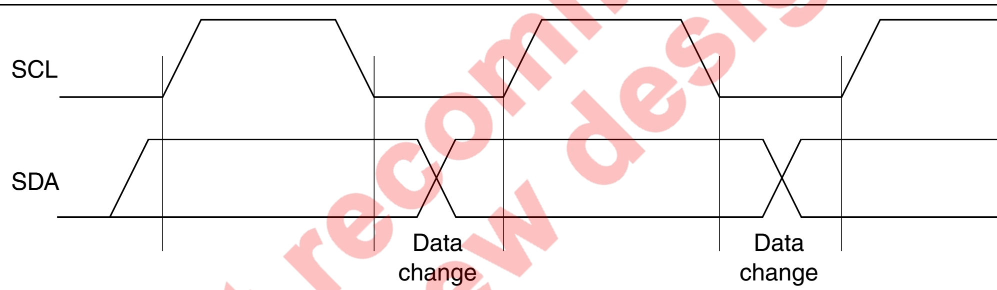
Serial Clock (SCL)

The SCL pin is used to control serial input/output data timing. The SCL input is used to positive edge clock data into EEPROM device and negative edge clock data out of each device. Maximum clock rate is 400 kHz.

Serial Input/Output Data (SDA)

The SDA pin is bidirectional for serial data transfer. The SDA pin needs to be pulled up by resistor as that pin is open-drain driven structure. Use proper resistor value for your system by considering V_{OL}, I_{OL} and the SDA pin capacitance. Except for a start condition and a stop condition which will be discussed later, the SDA transition needs to be completed during the SCL low period.

Data Validity (SDA data change timing waveform)



Note: High-to-low and low-to-high change of SDA should be done during the SCL low period.

Device Address (A0, A1, A2)

Two devices can be wired for one common data bus line as maximum. Device address pins are used to distinguish each device and device address pins should be connected to V_{cc} or V_{ss}. When device address code provided from SDA pin matches corresponding hard-wired device address pins A0 to A2, that one device can be activated.
A2 pin is internally pulled-down to V_{ss}. The device reads these pins as Low if unconnected.

Pin Connections for A0 to A2

Memory size	Max connect number	Pin connection A2	A1	A0	Note
8k bit	2	V_{CC}/V_{SS}	×*2	×*2	Use A0,A1 for memory address a8and a9

Note: 1. During floating, "V_{CC}/V_{SS}" are fixed to V_{SS}.
2. Floating state can be possible.

Write Protect (WP)

When the Write Protect pin (WP) is high, the write protection feature is enabled and operates as shown in the following table. When the WP is low, write operation for all memory arrays are allowed. The read operation is always activated irrespective of the WP pin status.
The WP pin is internally pulled-down to V_{ss}. Write operations for all memory array are allowed if unconnected.

Write Protect Area

WP pin status	Write protect area 8k bit
V_{IH}	Upper 1/2 (4k bit)
V_{IL}	Normal read/write operation

Functional Description

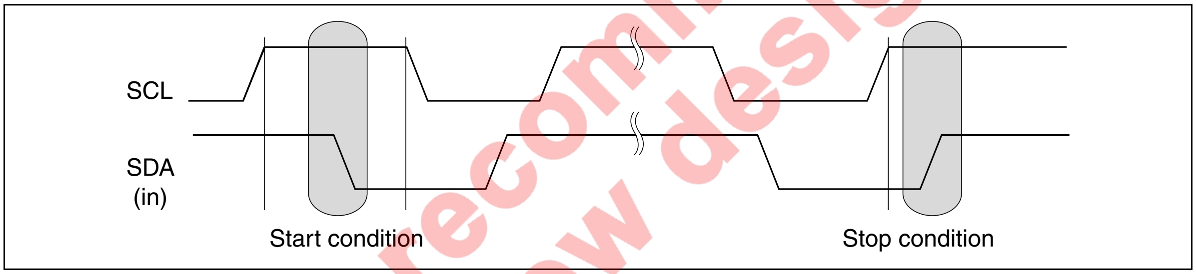
Start Condition

A high-to-low transition of the SDA with the SCL high is needed in order to start read, write operation (See start condition and stop condition).

Stop Condition

A low-to-high transition of the SDA with the SCL high is a stop condition. The stand-by operation starts after a read sequence by a stop condition. In the case of write operation, a stop condition terminates the write data inputs and place the device in a internally-timed write cycle to the memories. After the internally-timed write cycle which is specified as t_{WC}, the device enters a standby mode (See write cycle timing).

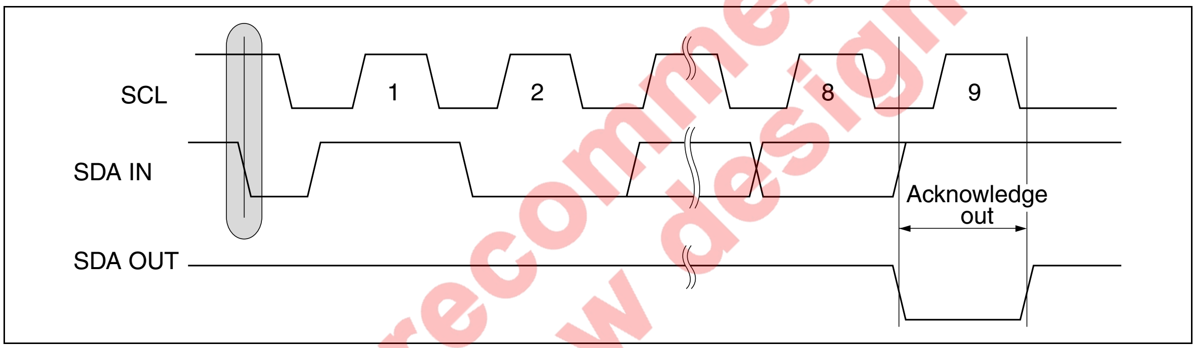
Start Condition and Stop Condition



Acknowledge

All addresses and data words are serially transmitted to and from in 8-bit words. The receiver sends a zero to acknowledge that it has received each word. This happens during ninth clock cycle. The transmitter keeps bus open to receive acknowledgment from the receiver at the ninth clock. In the write operation, EEPROM sends a zero to acknowledge after receiving every 8-bit words. In the read operation, EEPROM sends a zero to acknowledge after receiving the device address word. After sending read data, the EEPROM waits acknowledgment by keeping bus open. If the EEPROM receives zero as an acknowledge, it sends read data of next address. If the EEPROM receives acknowledgment "1" (no acknowledgment) and a following stop condition, it stops the read operation and enters a stand-by mode. If the EEPROM receives neither acknowledgment "0" nor a stop condition, the EEPROM keeps bus open without sending read data.

Acknowledge Timing Waveform



Device Addressing

The EEPROM device requires an 8-bit device address word following a start condition to enable the chip for a read or a write operation. The device address word consists of 4-bit device code, 3-bit device address code and 1-bit read/write(R/W) code. The most significant 4-bit of the device address word are used to distinguish device type and this EEPROM uses "1010" fixed code. The device address word is followed by the 1-bit device address code A2, memory adderess a9, a8. The device address code selects one device out of two devices which are connected to the bus. This means that the device is selected if the inputted 1-bit device address code is equal to the corresponding hard-wired A2 pin status.
The eighth bit of the device address word is the read/write(R/W) bit. A write operation is initiated if this bit is "0" and a read operation is initiated if this bit is "1". The EEPROM turns to a stand-by state if the device code is not "1010" or device address code doesn't coincide with status of the correspond hard-wired device address pins A0 to A2.

Device Address Word

	Device address word (8-bit)							
	Device code (fixed)				Device address code			R/W code*[1]
8k	1	0	1	0	A2	a9	a8	R/W

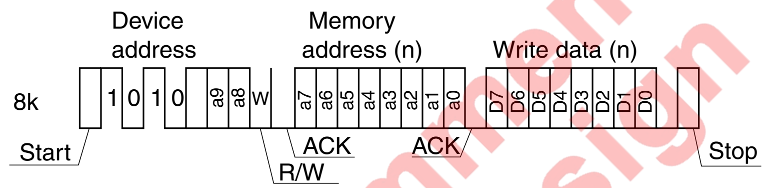
Note: 1. R/W="1" is read and R/W = "0" is write.

Write Operations

Byte Write:

A write operation requires an 8-bit device address word with R/W = “0”. Then the EEPROM sends acknowledgment "0" at the ninth clock cycle. After these, the 8kbit EEPROM receives 2 sequence 8-bit memory address words. Upon receipt of this memory address, the EEPROM outputs acknowledgment "0" and receives a following 8-bit write data. After receipt of write data, the EEPROM outputs acknowledgment "0". If the EEPROM receives a stop condition, the EEPROM enters an internally-timed write cycle and terminates receipt of SCL, SDA inputs until completion of the write cycle. The EEPROM returns to a standby mode after completion of the write cycle.

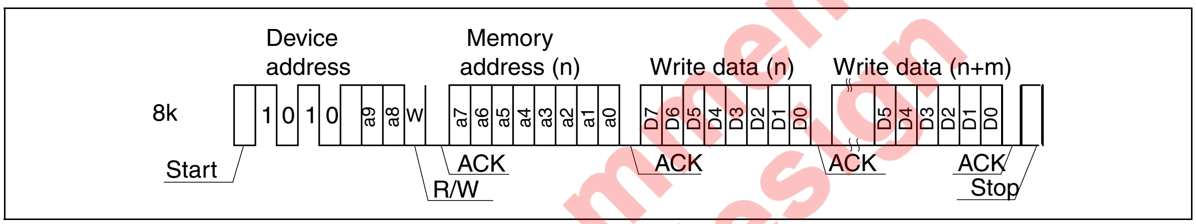
Byte Write Operation



Page Write:

The EEPROM is capable of the page write operation which allows any number of bytes up to 32 bytes to be written in a single write cycle. The page write is the same sequence as the byte write except for inputting the more write data. The page write is initiated by a start condition, device address word, memory address(n) and write data (Dn) with every ninth bit acknowledgment. The EEPROM enters the page write operation if the EEPROM receives more write data (Dn+1) instead of receiving a stop condition. The a0 to a4 address bits are automatically incremented upon receiving write data (Dn+1). The EEPROM can continue to receive write data up to 32 bytes. If the a0 to a4 address bits reaches the last address of the page, the a0 to a4 address bits will roll over to the first address of the same page and previous write data will be overwritten. Upon receiving a stop condition, the EEPROM stops receiving write data and enters internally-timed write cycle.

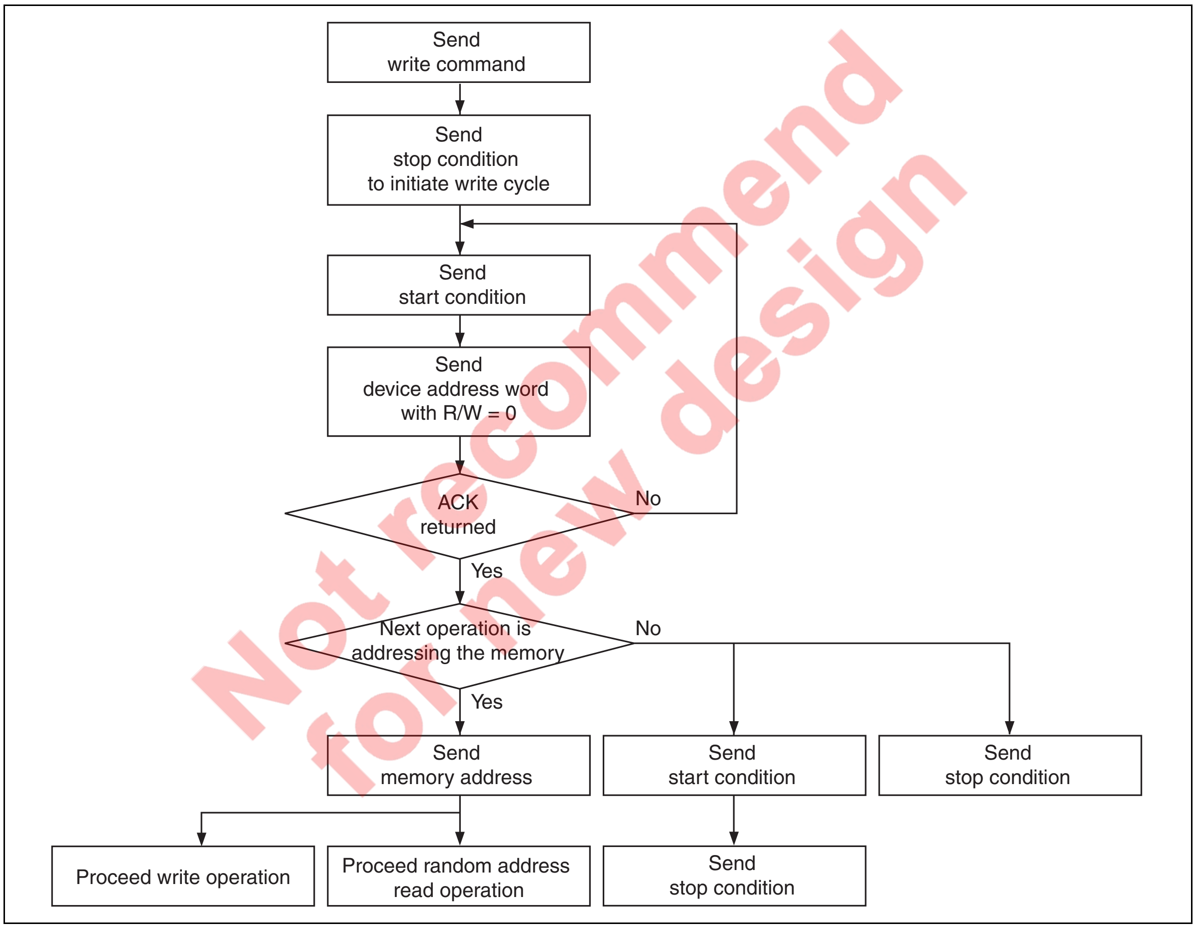
Page Write Operation



Acknowledge Polling:

Acknowledge polling feature is used to show if the EEPROM is in a internally-timed write cycle or not. This feature is initiated by the stop condition after inputting write data. This requires the 8-bit device address word following the start condition during a internally-timed write cycle. Acknowledge polling will operate when the R/W code = "0". Acknowledgment "1" (no acknowledgment) shows the EEPROM is in a internally-timed write cycle and acknowledgment "0" shows that the internally-timed write cycle has completed. See Write Cycle Polling using ACK.

Write Cycle Polling Using ACK



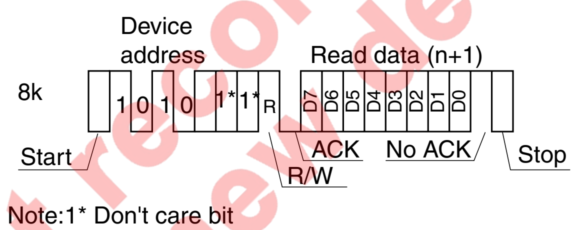
Read Operation

There are three read operations: current address read, random read, and sequential read. Read operations are initiated the same way as write operations with the exception of R/W = "1".

Current Address Read:

The internal address counter maintains the last address accessed during the last read or write operation, with incremented by one. Current address read accesses the address kept by the internal address counter. After receiving a start condition and the device address word (R/W is "1"), the EEPROM outputs the 8-bit current address data from the most significant bit following acknowledgment "0". If the EEPROM receives acknowledgment "1" (no acknowledgment) and a following stop condition, the EEPROM stops the read operation and is turned to a standby state. In case the EEPROM has accessed the last address of the last page at previous read operation, the current address will roll over and returns to zero address. In case the EEPROM has accessed the last address of the page at previous write operation, the current address will roll over within page addressing and returns to the first address in the same page. The current address is valid while power is on. The current address after power on will be indefinite. The random read operation described below is necessary to define the memory address.

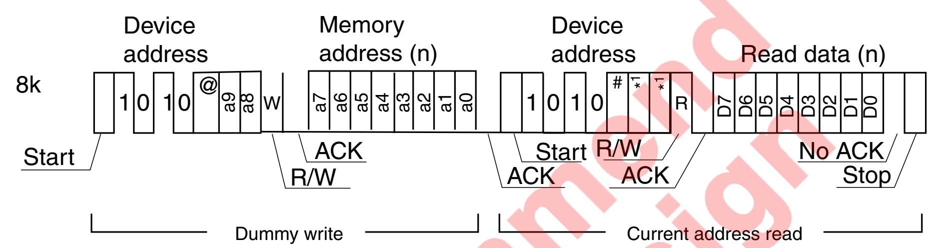
Current Address Read Operation



Random Read:

This is a read operation with defined read address. A random read requires a dummy write to set read address. The EEPROM receives a start condition, device address word (R/W=0) and memory address 2 × 8-bit sequentially. The EEPROM outputs acknowledgment "0" after receiving memory address then enters a current address read with receiving a start condition. The EEPROM outputs the read data of the address which was defined in the dummy write operation. After receiving acknowledgment "1"(no acknowledgment) and a following stop condition, the EEPROM stops the random read operation and returns to a standby state.

Random Read Operation

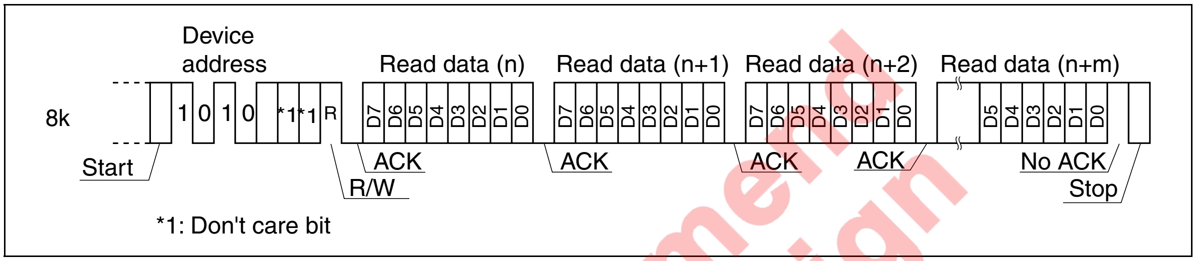


Notes: 1. Don't care bit
2. 2nd device address code(#)should be same as 1st(@).

Sequential Read:

Sequential reads are initiated by either a current address read or a random read. If the EEPROM receives acknowledgment "0" after 8-bit read data, the read address is incremented and the next 8-bit read data are coming out. This operation can be continued as long as the EEPROM receives acknowledgment "0". The address will roll over and returns address zero if it reaches the last address of the last page. The sequential read can be continued after roll over. The sequential read is terminated if the EEPROM receives acknowledgment "1" (no acknowledgment) and a following stop condition.

Sequential Read Operation



Notes

Data Protection at V_{CC} On/Off

When V_{CC} is turned on or off, noise on the SCL and SDA inputs generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to unintentional program mode. To prevent this unintentional programming, this EEPROM has a power on reset function. Be careful of the notices described below in order for the power on reset function to operate correctly.

- SCL and SDA should be fixed to V_{CC} or V_{SS} during V_{CC} on/off. Low to high or high to low transition during V_{CC} on/off may cause the trigger for the unintentional programming.
- V_{CC} should be turned off after the EEPROM is placed in a standby state.
- V_{CC} should be turned on from the ground level(V_{SS}) in order for the EEPROM not to enter the unintentional programming mode.
- V_{CC} turn on rate should be longer than 2 µs/V.

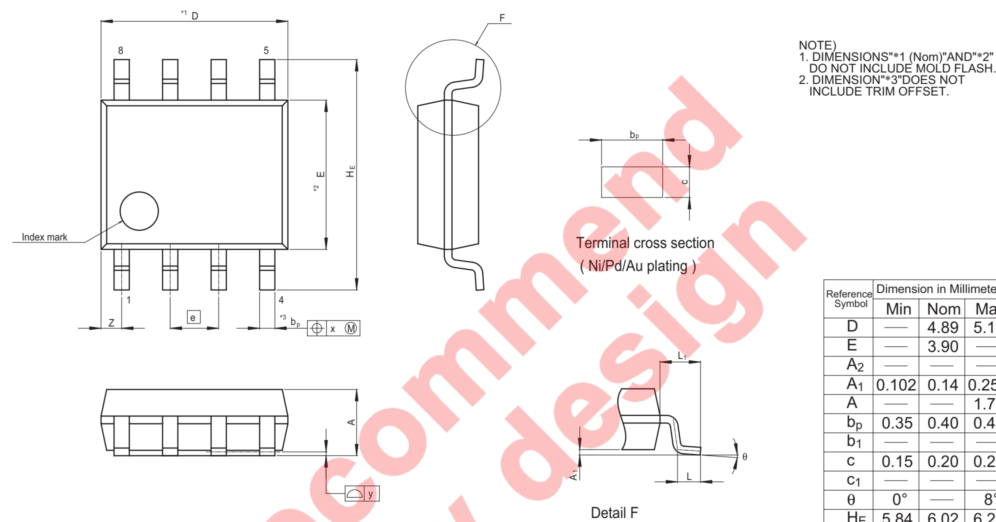
Noise Suppression Time

This EEPROM have a noise suppression function at SCL and SDA inputs, that cut noise of width less than 50 ns. Be careful not to allow noise of width more than 50 ns.

Package Dimensions

R1EX24008ASA00A (PRSP0008DF-B / Previous Code: FP-8DBV)

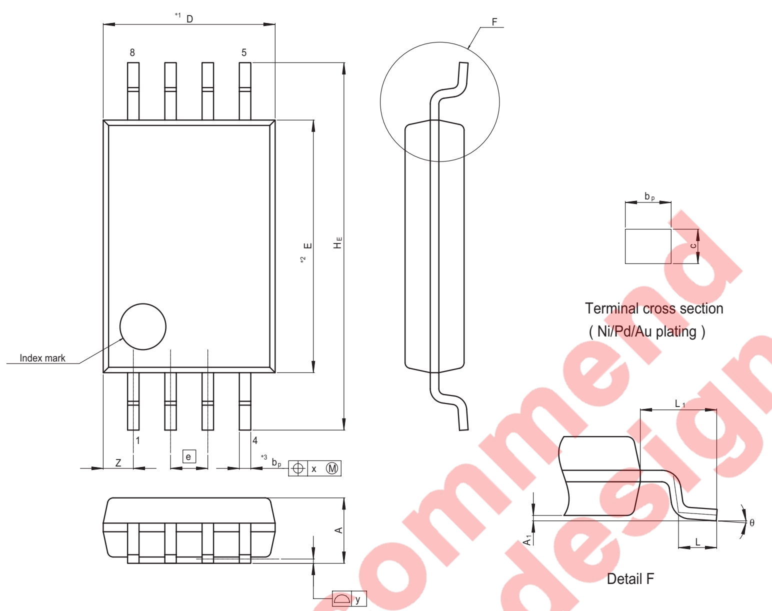
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-3.9x4.89-1.27	PRSP0008DF-B	FP-8DBV	0.08g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.89	5.15
E	—	3.90	—
A_2	—	—	—
A_1	0.102	0.14	0.254
A	—	—	1.73
b_p	0.35	0.40	0.45
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.84	6.02	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.10
Z	—	—	0.69
L	0.406	0.60	0.889
L_1	—	1.06	—

R1EX24008ATA00A (PTSP0008JC-B / Previous Code: TTP-8DAV)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP8-4.4x3-0.65	PTSP0008JC-B	TTP-8DAV	0.034g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	3.00	3.30
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.805
L	0.40	0.50	0.60
L_1	—	1.00	—

Revision History	R1EX24008Axx00A Data Sheet

Rev.	Date	Contents of Modification	
		Page	Description
1.00	Oct. 26, 2009	—	Initial issue

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Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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Colophon .7.2