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April 1st, 2010
Renesas Electronics Corporation

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R8A66153FP

PROGRAMMABLE BUFFERED I/O EXPANDER

REJ03F0260-0100
Rev. 1.00
Jan. 10. 2008

DESCRIPTION

The R8A66153FP is a programmable I/O expander using a high-voltage CMOS process.
And has three sets of 8-bit I/O ports, two sets of 8-bit high voltage output ports, and one 4-bit input port.

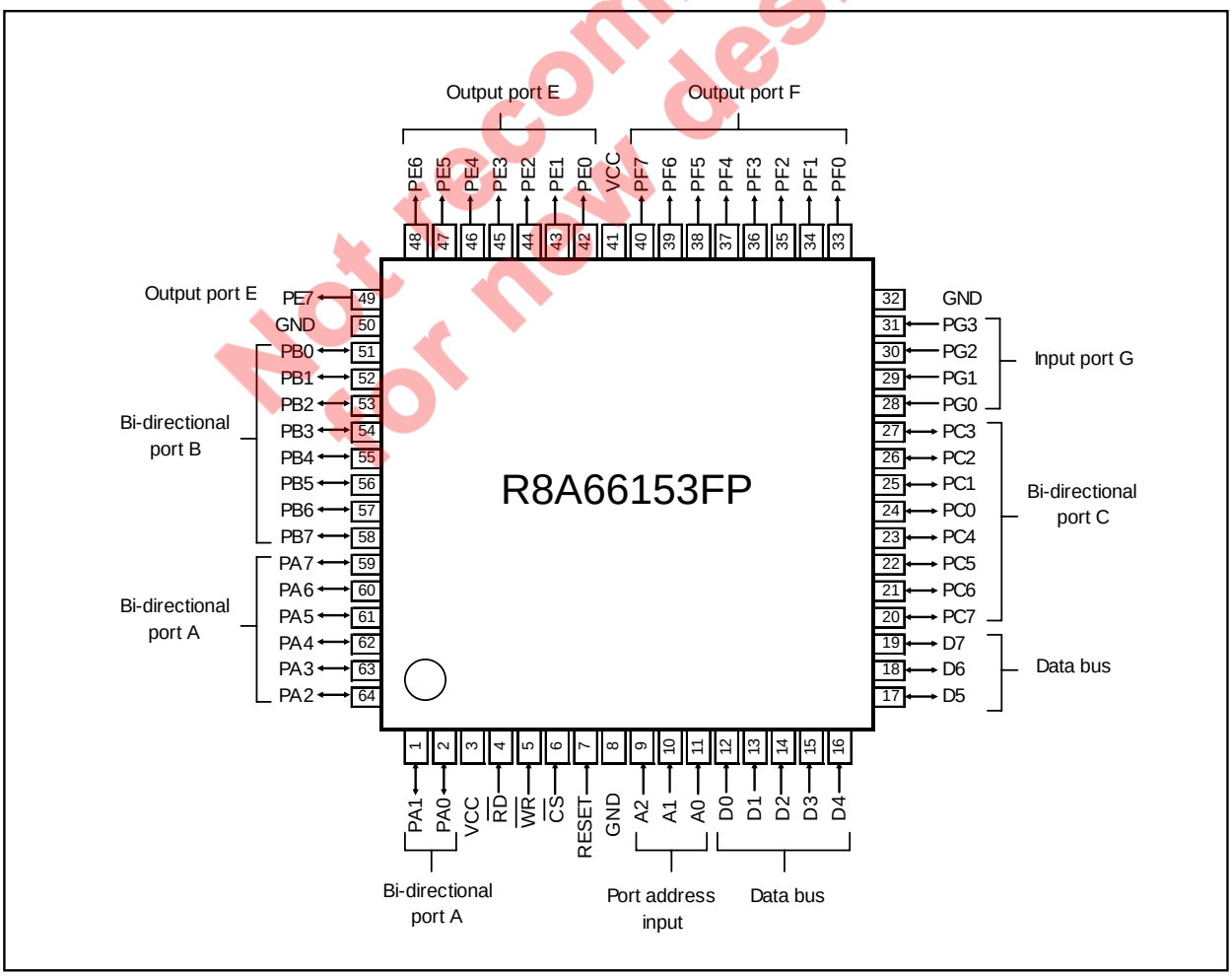
FEATURES

- Output pattern can be written in input mode
- 8-bit X 2 high voltage output ports with IOL=24mA
- CMOS level schmitt trigger input
- Vcc=4.5~5.5V, Ta=-40~85°C

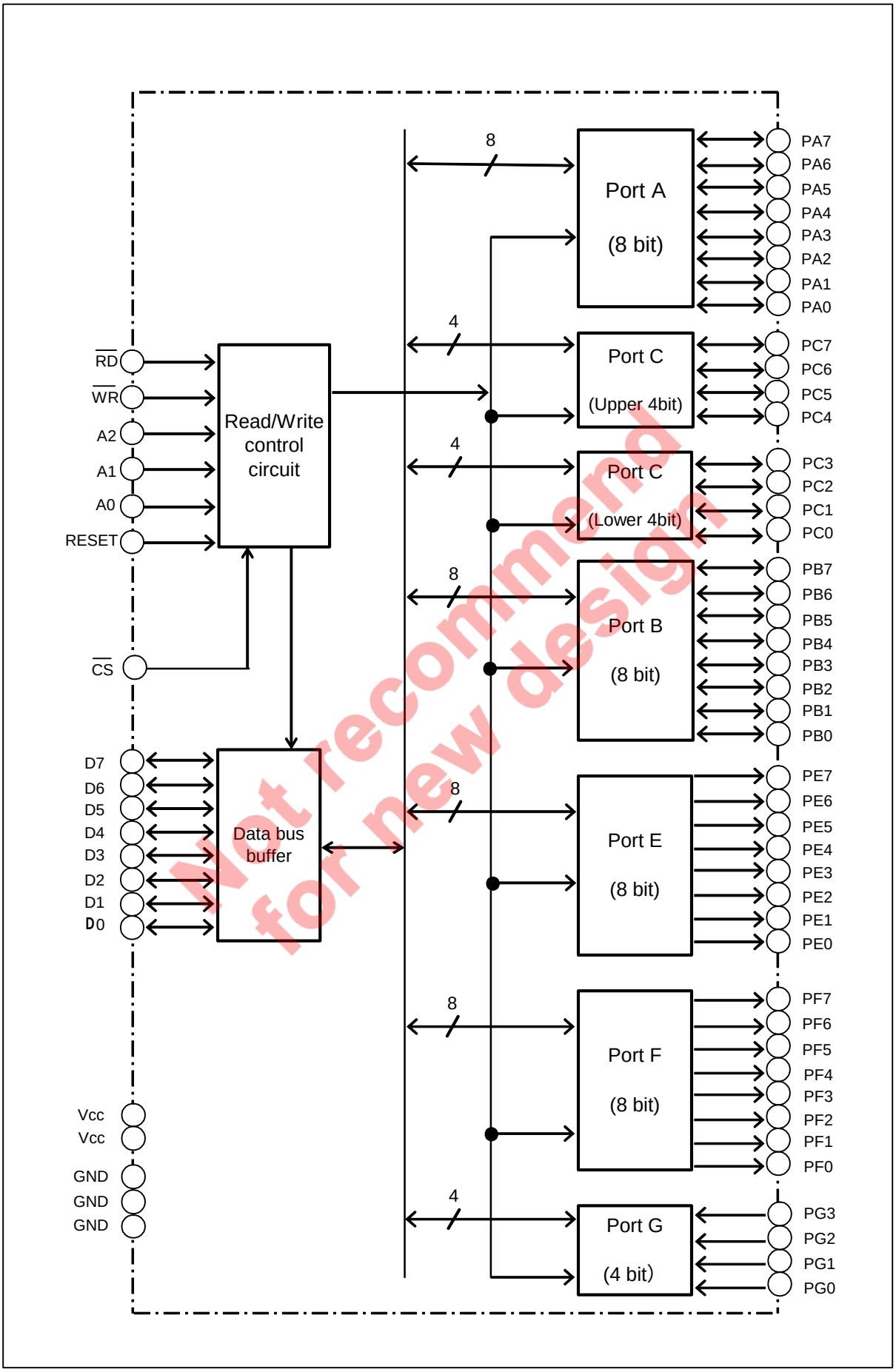
APPLICATION

- I/O port expansion for MCU.

PIN CONFIGRATION (TOP VIEW)



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The R8A66153FP is a general purpose programmable I/O expander with three 8-bit I/O ports (portA,B,C) and two 8-bit high voltage output ports (portE,F) and one 4-bit input port (portG).
I/O ports can be set INPUT for OUTPUT by a command.
The portC can be divided into two 4-bit ports, and if it is set to output, bit set/reset operation is available.
The portE and port F is the high voltage N-channel open drain output. (Vo=24V, IOL=24mA)
The port G is a 4-bit input port with CMOS level schimitt trigger input.
When RESET="H", output port E and F turn to disable state and other I/O ports turn to input mode.

FUNCTION

$\overline{RD}$ (read input)

If the input is "L", the port input data or port latch data appear at the data bus.

$\overline{WR}$ (write input)

By the positive edge of $\overline{WR}$ input, data bus data is written into the control register or into the port latch.

A2, A1, A0 (Port selection input)

Select the port or the control register. (see table 1)

RESET (reset input)

If the input is "H", all I/O and output port turn to high impedance state.
(Port A,B,C : input mode, Port E,F : "Z")

$\overline{CS}$ (chip select input)

"L" enables to communicate with MCU. When "H", data bus keeps high impedance state and ignored the command from MCU. The port condition and the data of the port latch are not changed even if $\overline{CS}$="H".

Read/Write control circuit

According to the data from the MCU, set the port condition and transmit the data between port and data bus.

Data bus buffer

This is the bi-directional bus buffer. When $\overline{WR}$="L" data bas data is written into the register of R8A66153, and when $\overline{RD}$="L" port data or port latch data is appears.

Port A and Port B

Port A and Port B are 8-bit bi-directional port with output latch. By the command from MCU, set these port as an input or an output.

The output circuit of these ports are CMOS 3-state output and input buffer is CMOS schmitt trigger input.

When port is set to output, data bus data is written into the port latch by the positive edge of /WR and is output to the terminal.

When $\overline{RD}$="L" in the state of output mode, port terminal data(=output data) is appears to the data bus.

When $\overline{RD}$="L" in the state of input mode, port terminal data(=input data) is appears to the data bus.

In the state of input mode, data bus data is written into the port latch by the positive edge of $\overline{WR}$.

Port latch data is not determined when power ON.

Port C

Basic function of port C is the same as the port A and port B. The difference between port A/B and port C is that port C can be used as the two 4-bit ports. And when is set to output, bit set/reset function is available by a bit.

Port E and Port F

Port E and Port F are 8-bit high voltage output ports with Vo=24V/IOL=24mA. Output transistor is N-ch open drain transistor.

When this port is selected, data bus data is written into the port latch by the positive edge of $\overline{WR}$.

And if is set to output enable, port latch

Port G

Port G is a input port with CMOS schmitt trigger. When this port is selected and $\overline{RD}$="L", input data is appears to the data bus.

Table 1. Function Table

A2	A1	A0	$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	0	0	0	1	Data bus ⟵ Port A
0	0	1	0	0	1	Data bus ⟵ Port B
0	1	0	0	0	1	Data bus ⟵ Port C
0	1	1	0	0	1	Data bus ⟵ Port G
1	0	0	0	0	1	Data bus ⟵ Port E latch data
1	0	1	0	0	1	Data bus ⟵ Port F latch data
0	0	0	0	1	↑	Port A ⟵ Data bus
0	0	1	0	1	↑	Port B ⟵ Data bus
0	1	0	0	1	↑	Port C ⟵ Data bus
1	0	0	0	1	↑	Port E ⟵ Data bus
1	0	1	0	1	↑	Port F ⟵ Data bus
1	1	1	0	1	↑	Control register ⟵ Data bus
×	×	×	1	×	×	Data bus is in high impedance state

note: "0" means "L" level and "1" means "H" level.

CONTROL WORD

When (A0, A1, A2)=(1,1,1), data bus data is recognized as the control word.
This control word is to set the port condition and the bit set/reset function of port C. (see Fig.1 and Fig.2)

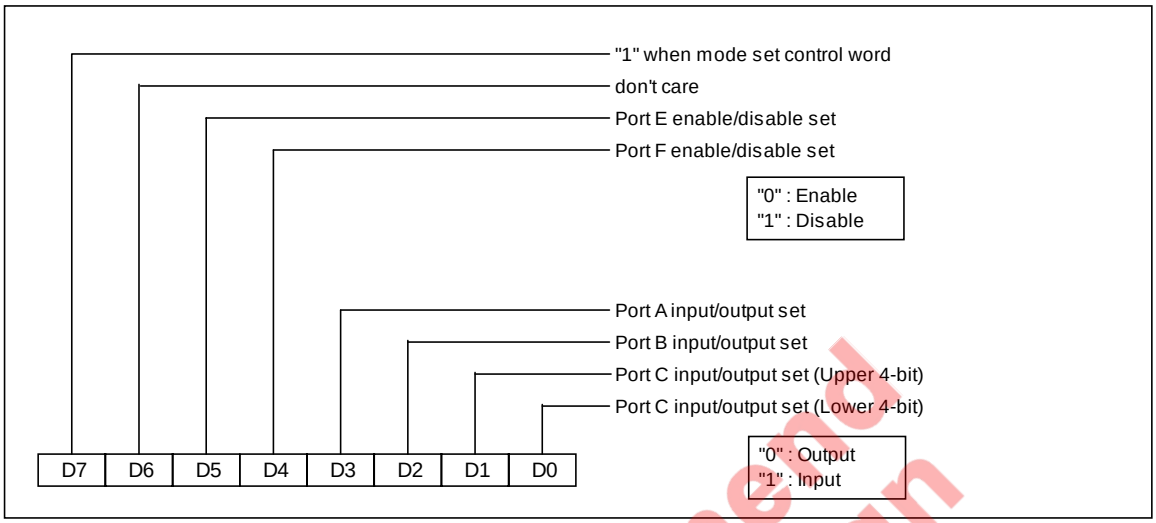
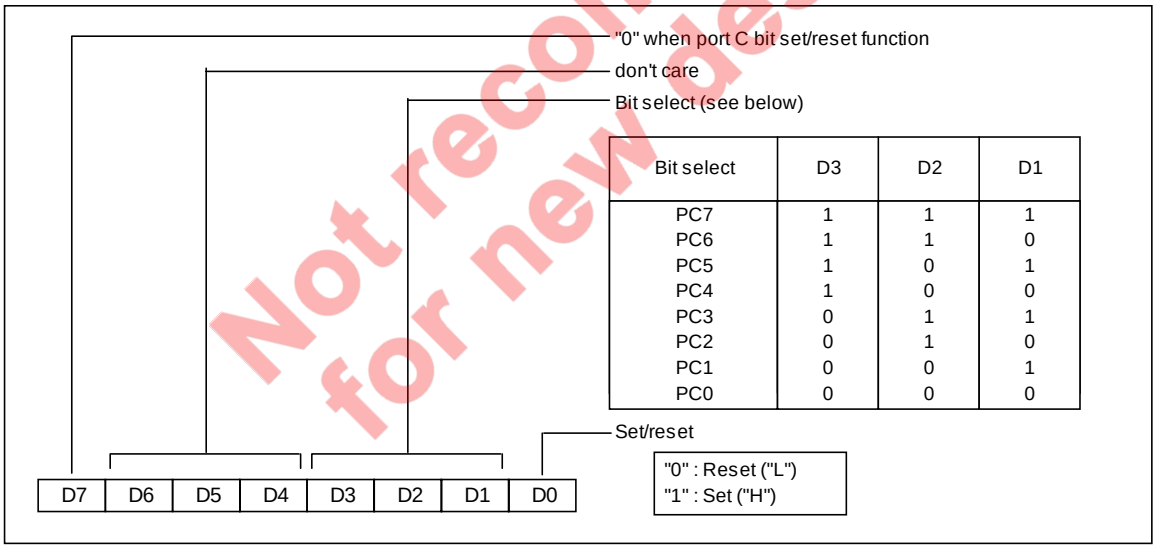


Fig.1 Control word to set port conditions



Bit select	D3	D2	D1
PC7	1	1	1
PC6	1	1	0
PC5	1	0	1
PC4	1	0	0
PC3	0	1	1
PC2	0	1	0
PC1	0	0	1
PC0	0	0	0

Fig.2 Control word for bit set/reset function of port C

ABSOLUTE MAXIMUM RATINGS (Ta=-40~+85°C, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
Vcc	Supply voltage			-0.3 to +7	V
VI	Input voltage			-0.3 to Vcc+0.3	V
VO	Output voltage	except port E, F		-0.3 to Vcc+0.3	V
		Port E,F		-0.3 to +28	V
Pd	Power dissipation		Ta=85°C	500	mW
Tstg	Storage temperature			-65 to 150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=-40~+85°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits			Unit
				Min.	Typ.	Max.	
Vcc	Supply voltage			4.5	5	5.5	V
VO	"H" output voltage	Port E,F	IOH < 250uA	0		24	V
IOL	"L" output current		VOL < 0.6V	0		24	mA
Topr	Operating temperature			-40		85	°C

ELECTRICAL CHARACTERISTICS (Vcc=4.5~5.5V, Ta=-40~+85°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits		Unit
				Min.	Max.	
VIH	"H" input voltage	Control pin (note),		0.7Vcc		V
VIL	"L" input voltage	Data bus			0.3Vcc	V
VT+	Positive going threshold voltage	Port A,B,C,G		0.35Vcc	0.78Vcc	V
VT-	Negative going threshold voltage	Port A,B,C,G		0.2Vcc	0.55Vcc	V
VOH	"H" output voltage	Data bus,	IOH=-2.5mA	Vcc-2		V
VOL	"L" output voltage	Port A,B,C	IO=2.5mA		0.45	V
VOL	"L" output voltage	Port E,F	IOL=24mA		0.6	V
IOH	"H" output leak current	Port E,F	VO=24V		250	uA
I_I	Input leak current		VO=0 to Vcc		±10	uA
IOZ	OFF-state output current		VO=0 to Vcc		±10	uA
ICCS	Static supply current with no output load.		All ports "H" output		2	mA
C_I	Input pin capacitance		f=1MHz		10	pF
$C_{I/O}$	I/O pin capacitance		Other pins 0V		20	pF

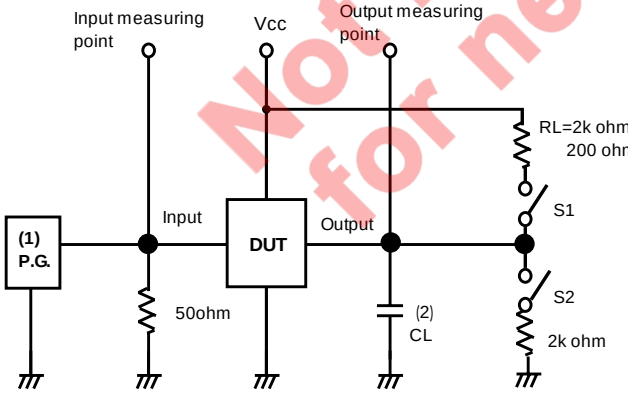
note : Control pins are $\overline{RD}$, $\overline{WR}$, RESET, $\overline{CS}$, A2, A1 and A0 pin.

TIMING REQUIREMENTS (Vcc=4.5~5.5V, Ta=-40~+85°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits		Unit
				Min.	Max.	
tw(R)	Read pulse width	tsu(A-R)=0ns		160		ns
		tsu(A-R)>40ns		120		
tsu(PE-R)	Peripheral setup time before read			0		ns
th(R-PE)	Peripheral hold time after read			0		ns
tsu(A-R)	Address setup time before read			0		ns
th(R-A)	Address hold time after read			0		ns
tw(W)	Write pulse width			120		ns
tsu(DQ-W)	Data setup time before write			40		ns
th(W-DQ)	Data hold time after write			0		ns
tsu(A-W)	Address setup time before write			0		ns
th(W-A)	Address hold time after write			0		ns

SWITCHING CHARACTERISTICS (Vcc=4.5~5.5V, Ta=-40~+85°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits		Unit
				Min.	Max.	
tpZH(R-DQ)	Read access time	tsu(A-R)=0ns	CL=150pF (note)		120	ns
tpZL(R-DQ)		tsu(A-R)>40ns			85	
tpHZ(R-DQ) tpLZ(R-DQ)	Read to data floating time		CL=150pF (note)	3	85	ns
tpHL(W-PE)	Write to output	Port A,B,C	CL=150pF (note)		200	ns
tpLH(W-PE)	delay time	Port E,F	CL=150pF, RL=200ohm (note)		250	



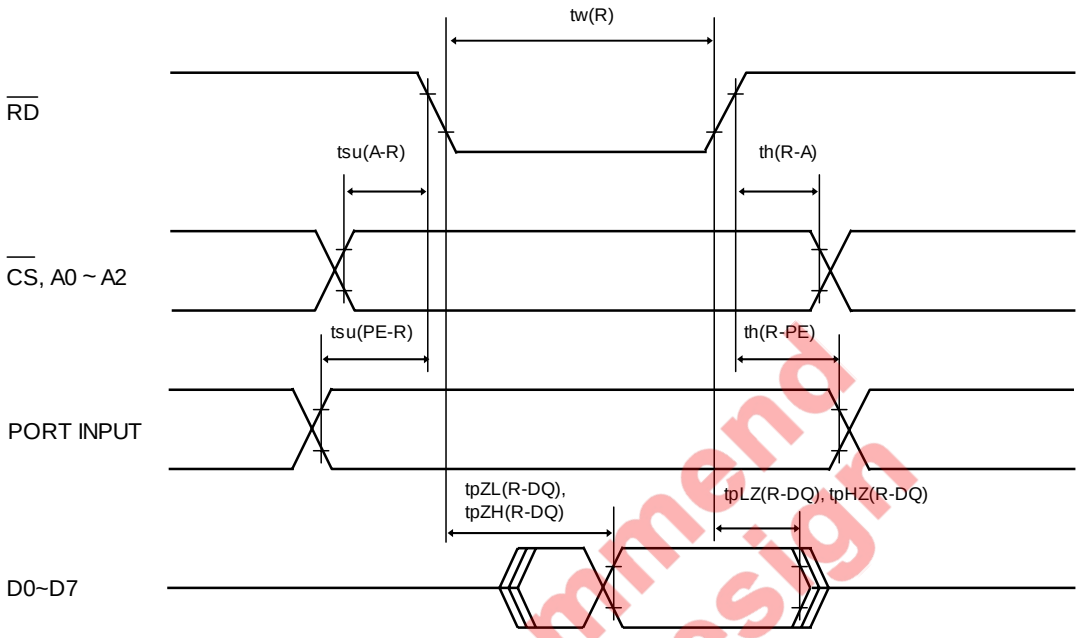
Symbol	Output pin	S1	S2
tpHL(W-PE)	Port A,B,C	Open	Open
tpLH(W-PE)	Port E,F	Closed	Open
tpZH(R-DQ) tpHZ(R-DQ)	Data bus	Open	Closed
tpZL(R-DQ) tpLZ(R-DQ)	Data bus	Closed	Open

(1) Pulse Generator (P.G.)
tr=6ns, tf=6ns, Zo=50ohm

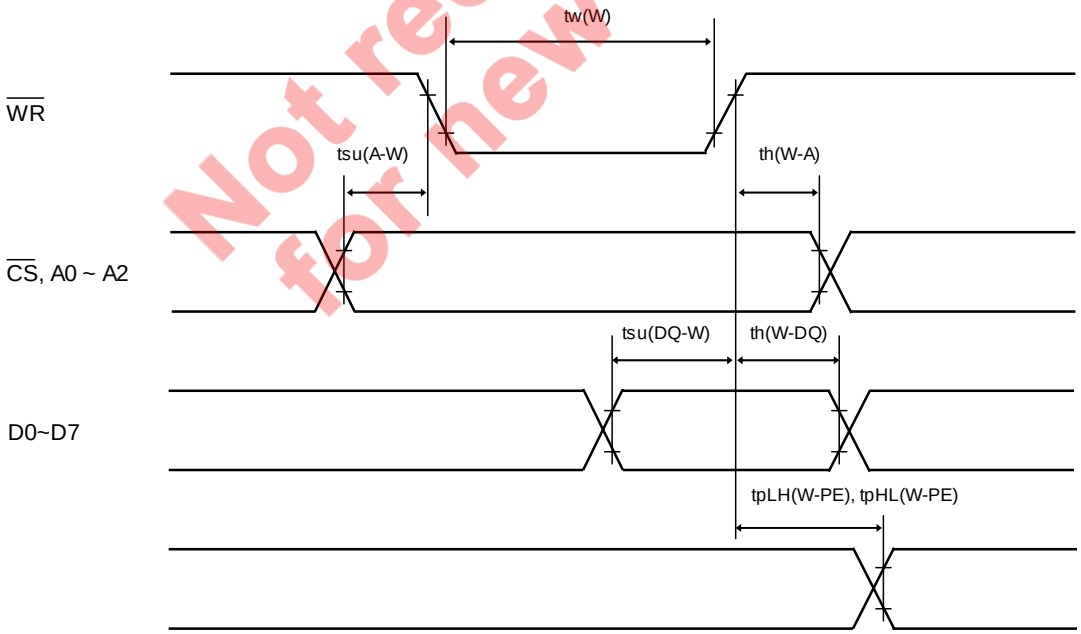
(2) CL includes stray capacitance and probe capacitance.

TIMING DIAGRAM

Read operation

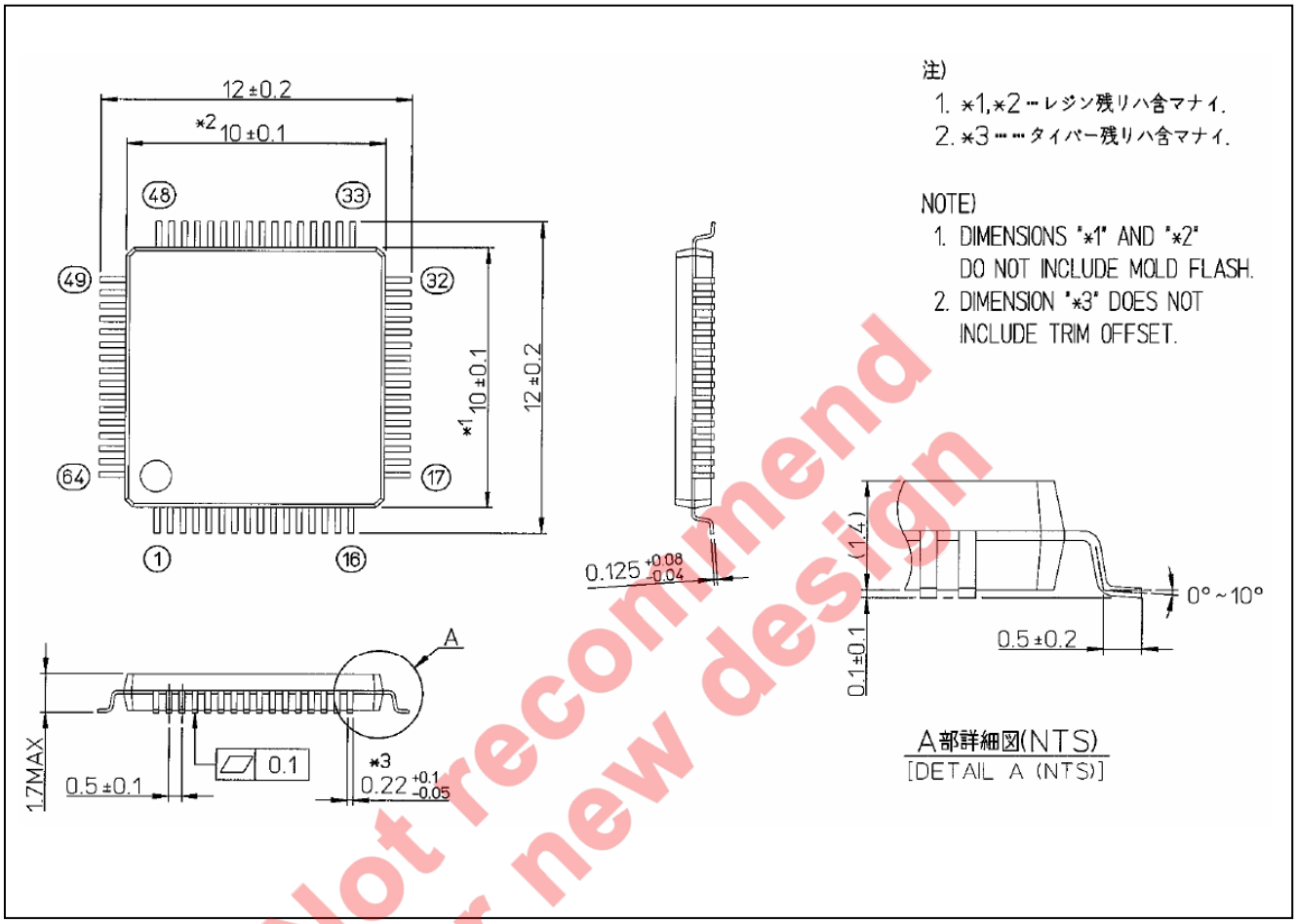


Write operation



PACKAGE OUTLINE

Package	RENESAS Code	Previous Code
64pin LQFP	PLQP0064KD-A	64P6X-B



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