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April 1st, 2010
Renesas Electronics Corporation

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REJ03F0272-0100
Rev. 1.00
Apr.01.2008

## DESCRIPTION

R8A66170 is a programmable 4-channel PWM generator produced using the silicon gate CMOS process.
R8A66170 can connect directly to the MPU data bus, and consists of a 16-bit prescaler and a PWM counter.
The pulse output includes three kinds of modes, allowing the independent control of each channel.
R8A66170 provides a software servo system in combination with the A-D function and the timer function of a one-chip microcomputer. R8A66170 is a succession product of M66240.

## FEATURES

- 4-channel individually controllable
- Built-in three kind of pulse output modes
- PWM repetitive frequency: 50 kHz (max.) (Mode 0, 8-bit resolution, fxin/255 at prescaler setting = 0)
- Output polarity selection possible
- External triggering possible
- The output after reset is in the high impedance state.
- Change of mode setting becomes effective after the current cycle.
- High output current : Io = ±24 mA ($V_{CC}$ = 5.0V)
- Wide operating power voltage range ($V_{CC}$ = 5.0V or 3.3V single power supply)
- Wide operating temperature range (Ta = -40~85 ºC)

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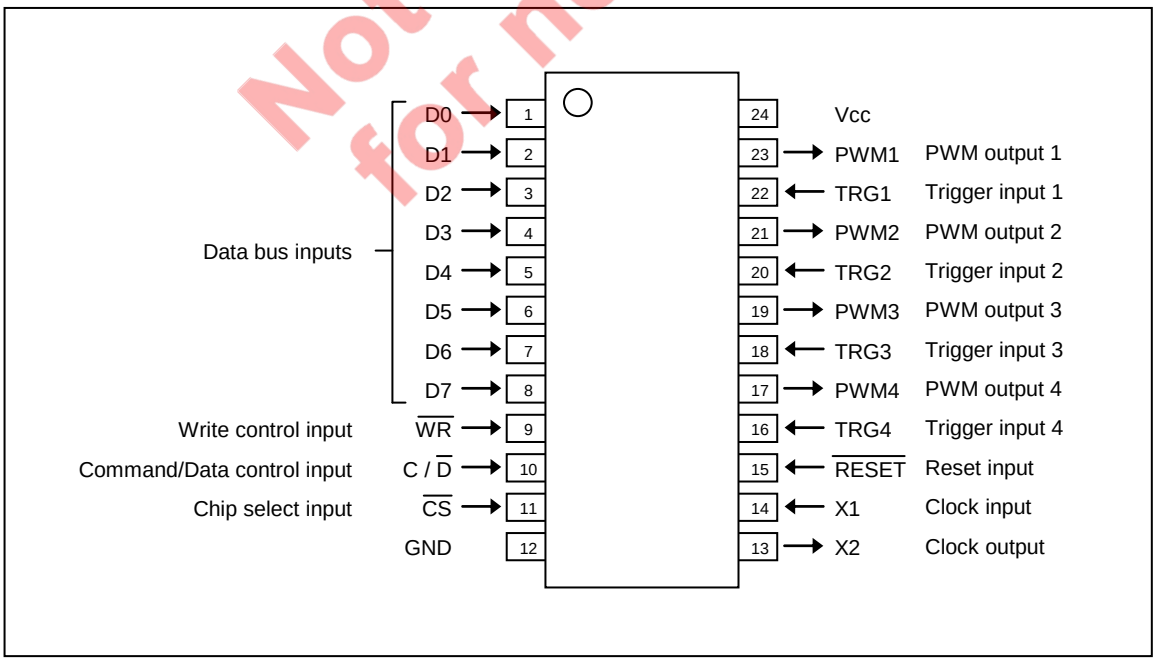
## APPLICATION

- Control of DC motors and stepping motors
- Control of Heater phase controllers
- Software servos for office automation equipment , and industrial equipment

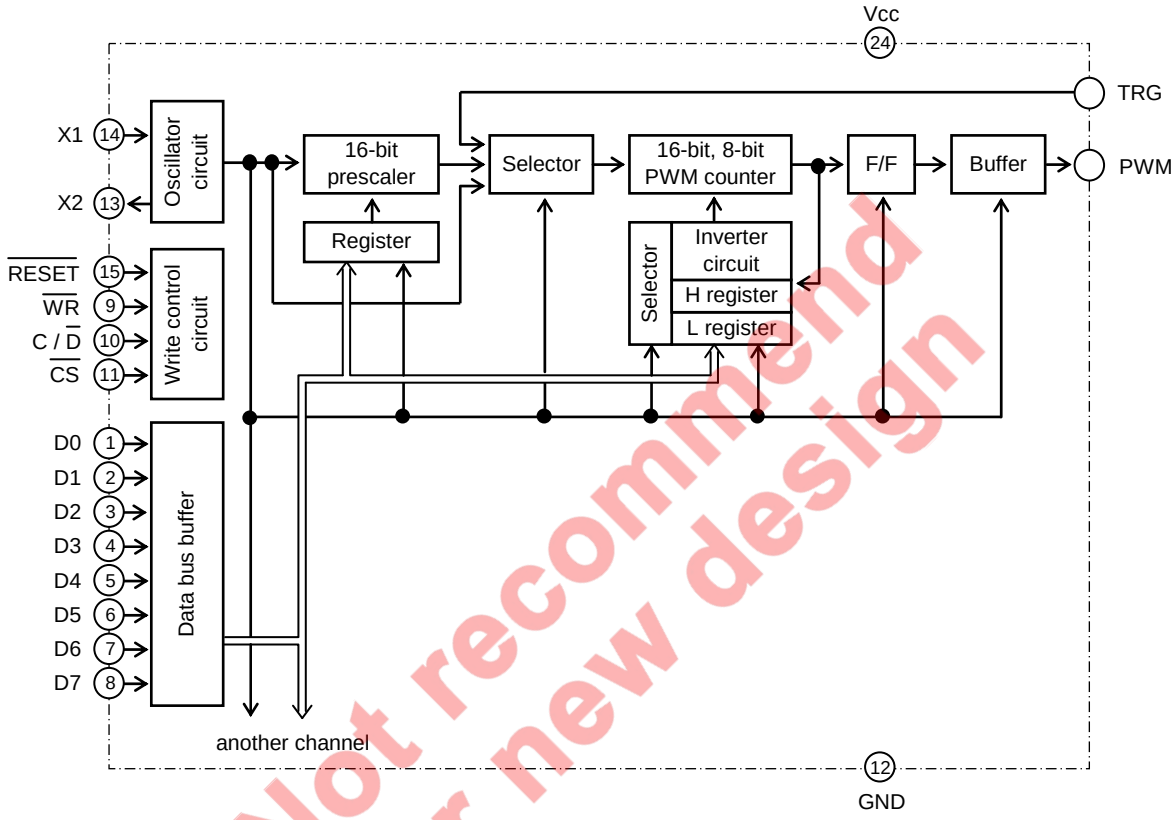
## PIN CONFIGURATION (TOP VIEW)



## FUNCTION

Four separate 16-bit prescalers and 16-bit PWM counters can be separately programmed by the control instruction from the MPU.
The output is made in one of three modes (Mode 0, Mode 1, and Mode 2).
In Mode0, setting only the value of H width repeatedly outputs the set pulse width.
In Mode1, setting only the value of H width outputs one shot of the pulse width set by trigger input.
In Mode2, setting both H width and L width repeatedly outputs the set pulse width.

## BLOCK DIAGRAM

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## PIN DESCRIPTIONS

| Pin name | Description | I/O | Function |
|---|---|---|---|
| $\overline{RESET}$ | Reset input | Input | Clears the command register and the flip-flop at “L”. |
| D0~D7 | Data bus input | Input | Inputs the data from MPU over the 8-bit data bus. |
| $\overline{WR}$ | Write control input | Input | Writes the data on data bus to the control register or data register when its state changes from “L” to “H” of rising edge. |
| C/$\overline{D}$ | Command/Data control input | Input | The Data on data bus is regarded as a command at “H” level, and as data at “L” level. |
| $\overline{CS}$ | Chip select input | Input | Communication with MPU is enabled at “L” level. Any control from MPU is ignored at “H” level. |
| $X_1$ | Clock input | Input | Input and output to the built-in clock generator circuit. By providing a crystal resonator between $X_1$ and $X_2$, sets the frequency.<br>To make external clock input, connect the clock source to $X_1$ pin and leave $X_2$ pin open. |
| $X_2$ | Clock output | Output | |
| TRG1~ TRG4 | Trigger input | Input | These are used when external trigger is selected in mode setting. These should be set to “L” level when not in use. |
| PWM1~ PWM4 | PWM output | Output | PWM output pins. Outputs become the high-impedance state after reset is inputted or after disable is specified by command 3.<br>D0 of command 1 allows the selection of output polarity. |

## OPERATION

### Commands

The information on data bus inputs D0 through D7 is treated as command when command / data control input C/$\overline{D}$ = 1, and is treated as data when C/$\overline{D}$ = 0.

There are three kinds of commands. (See Figure 1.)

- Command 1 selects the output mode and external trigger input of each channel and sets the output polarity of H width.
- Command 2 specifies, on a byte basis, to which 16-bit register of the prescaler and PWM counter of each channel data is to be written. The second and subsequent bytes of command 2 write prescaler value and PWM value. Depending on the location specified by command 2, the data of the second and subsequent bytes must be written in the order shown in Figure2.
- Command 3 is used to start or stop the prescalers and PWM counters operation.

### Data input

At initialization, all 16-bit of prescaler values must be written.

In mode 0 or 1, the PWM values must be written to all 16-bits of H register (*1), In mode 2, the value must be written to all 16-bits of H and L registers.

(*1): In mode0, at 8-bit resolution, only the lower byte of the H register is used.

In case of changing the value of prescaler and PWM during for operation, the procedure is as follows.

- To change the values of all 16-bits in the prescaler or the PWM counter during operation, values should be written to the upper byte first and then to the lower byte.
- To change the values of the lower byte only, the values of only the lower byte should be written.
- To change the values of the upper byte only, the values of all 16-bits should be written.
- To change the values of H register in Mode 2, the H register values should be written followed by the L register value.

When values are written to the lower byte (lower byte of L register in Mode 2), the write cycle of data registers is completed.

(Note)

- If the data registers values is changed during a PWM signal is outputted (exactly, finish to write those values), the PWM output is updated at the start of next cycle.
- To change the mode (i.e., to execute command 1), disable the output first (i.e., execute command 3).

Figure 3 shows the flow chart of the basic operation.

The order of the prescaler's and PWM counter's data setting is not fixed.

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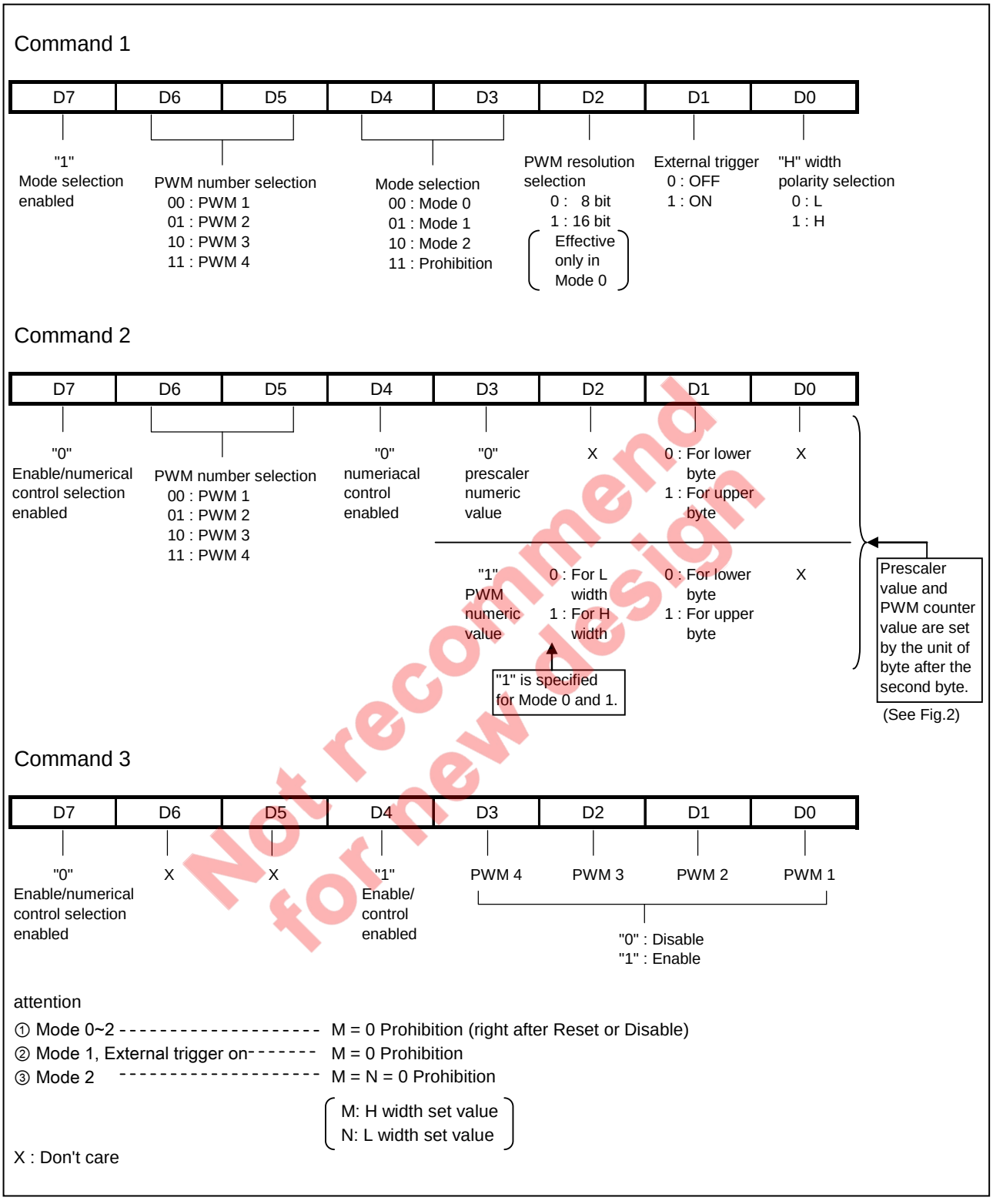


Fig.1 Commands

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| First byte (Command 2) | | | The second byte | The third byte | The fourth byte | The fifth byte | Remark |
|---|---|---|---|---|---|---|---|
| D3 | D2 | D1 | | | | | |
| 1 | 1 | 1 | Upper byte of PWM H register | Lower byte of PWM H register | - | - | In Mode 0 or 1 |
| 1 | 1 | 0 | Lower byte of PWM H register | - | - | - | |
| 1 | 1 | 1 | Upper byte of PWM H register | Lower byte of PWM H register | Upper byte of PWM L register | Lower byte of PWM L register | In Mode 2 |
| 1 | 1 | 0 | Lower byte of PWM H register | Upper byte of PWM L register | Lower byte of PWM L register | - | |
| 1 | 0 | 1 | Upper byte of PWM L register | Lower byte of PWM L register | - | - | |
| 1 | 0 | 0 | Lower byte of PWM L register | - | - | - | |
| 0 | X | 1 | Upper byte of prescaler register | Lower byte of prescaler register | - | - | |
| 0 | X | 0 | Lower byte of prescaler register | - | - | - | |

Fig.2 Data-setting sequence for registers

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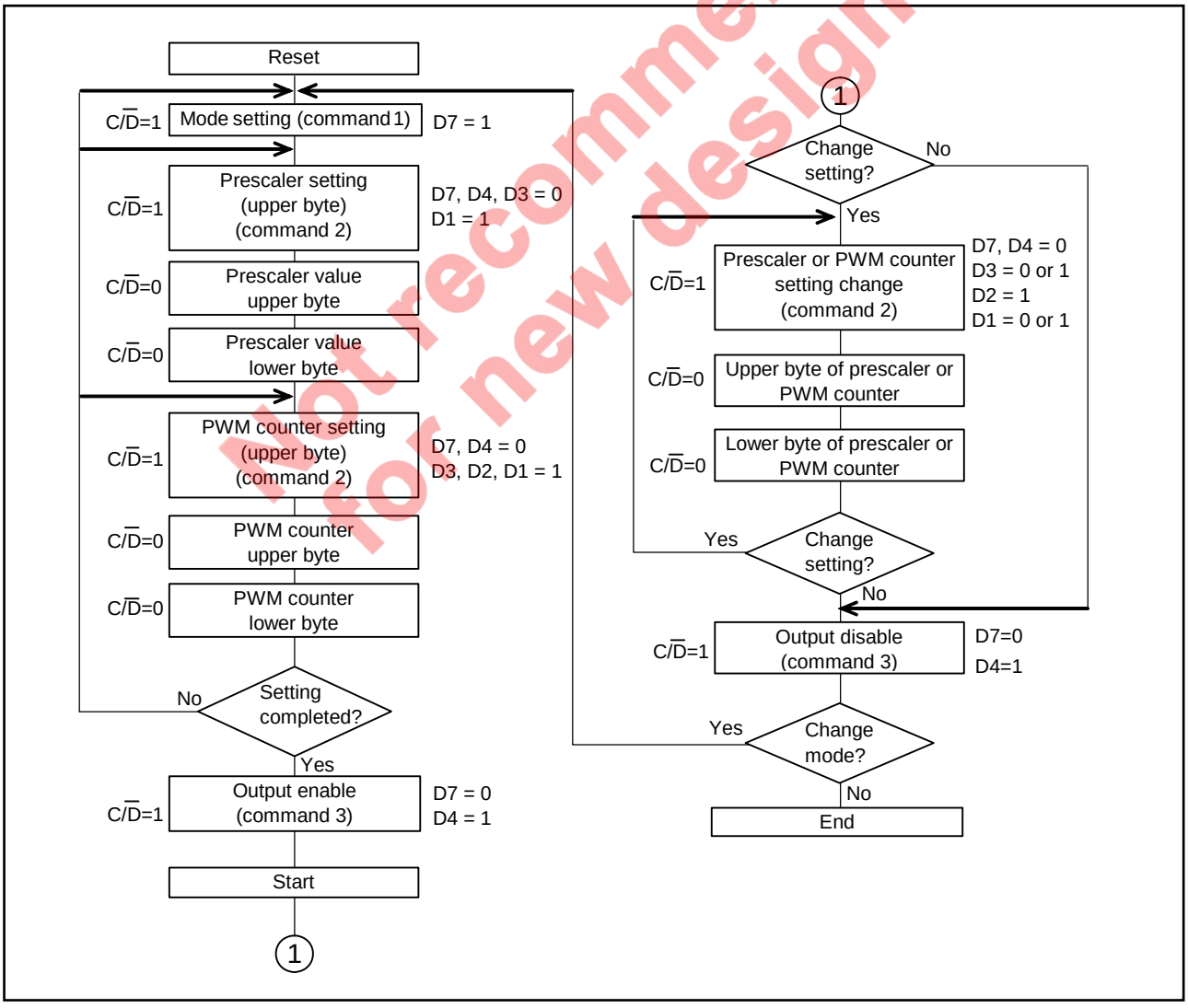


Fig.3 Flow chart in Mode 0 or 1 (for one channel)

## PWM WAVEFORM OUTPUT

R8A66170 has a built-in 16-bit prescaler and a PWM counter. The duty cycle of output pulse can be freely specified by changing the values of the prescaler and the PWM counter. The output is made in one of three modes (Mode 0, Mode 1, and Mode 2). The description of these modes is given below.

(1) Mode 0

This mode is selected by writing “0” to D4 and D3 in command 1. Figure 9 shows the block diagram in this mode (for one channel). The 16-bit PWM counter can be used as an 8-bit PWM counter only in this mode (command 1: D2 = 0). The setting with PWM resolution = 8-bits must be written to the lower 8 bytes of H register.
In this mode, the H output pulse width is determined by the prescaler register value L and PWM register value M.
The PWM output cycle time is determined by the prescaler register value L, irrespective of the PWM register value M. (See Fig.4)

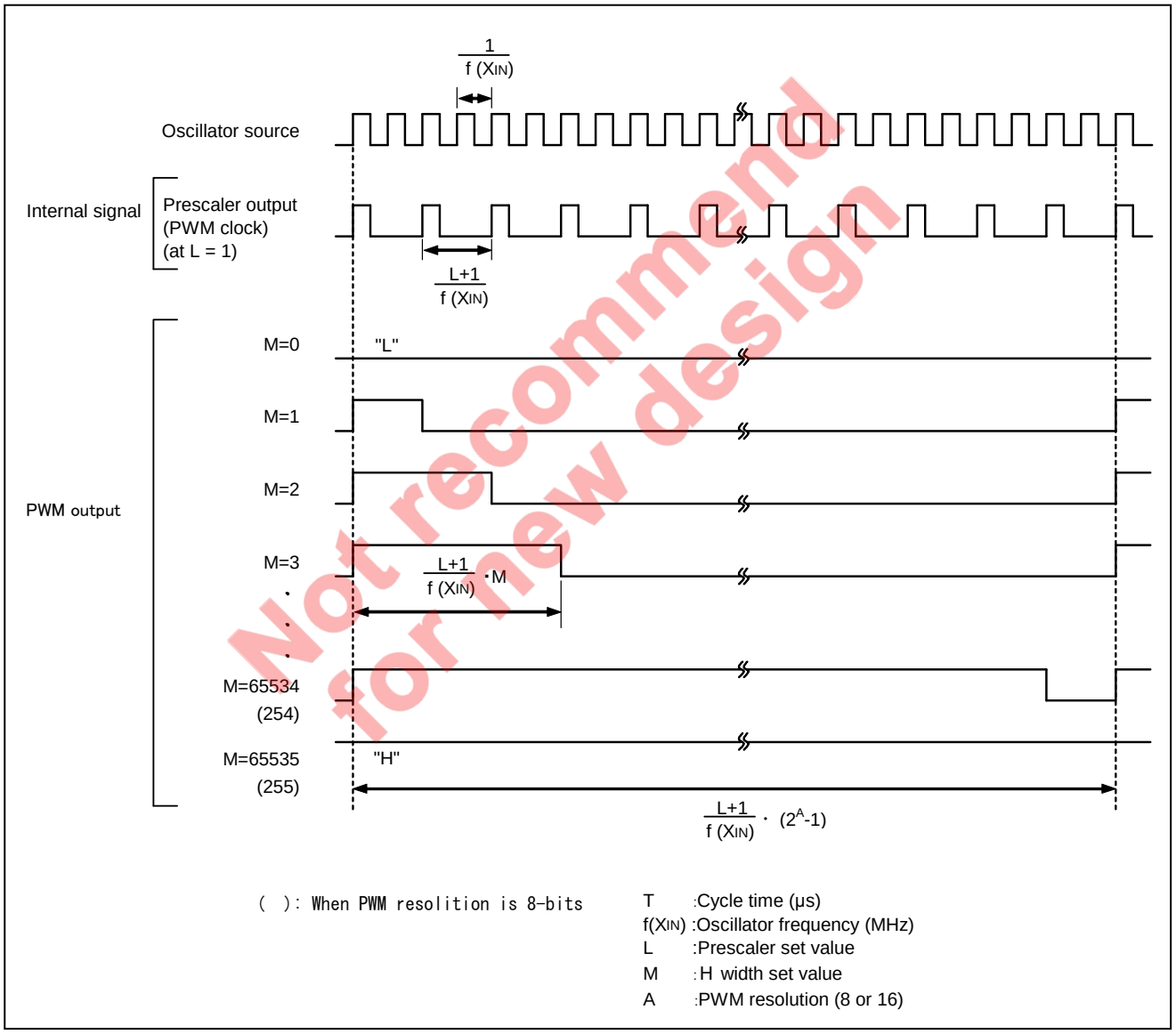


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Fig.4 (When H width polarity is “H”)

(2) Mode1

This mode is selected by setting D4 = 0 and D3 = 1 in command 1. Figure 10 shows the block diagram in this mode (for one channel).

This mode outputs the pulse which is determined by value M of PWM register as one shot by trigger signal.

The type of this output operation is determined by whether the external trigger signal or the internal trigger signal is used. Operation varies according to the choice of external and internal trigger signals.

(a) External trigger selected (D1 = 1 in command 1)

This mode outputs, when a trigger pulse is applied to trigger input TRG, one shot of output pulse. Therefore, cycle time T becomes cycle time $f_{IN}$ of the trigger pulse to be applied to trigger input TRG.

The output pulse width is determined by the prescaler register value L and PWM register value M. (See Fig.5)

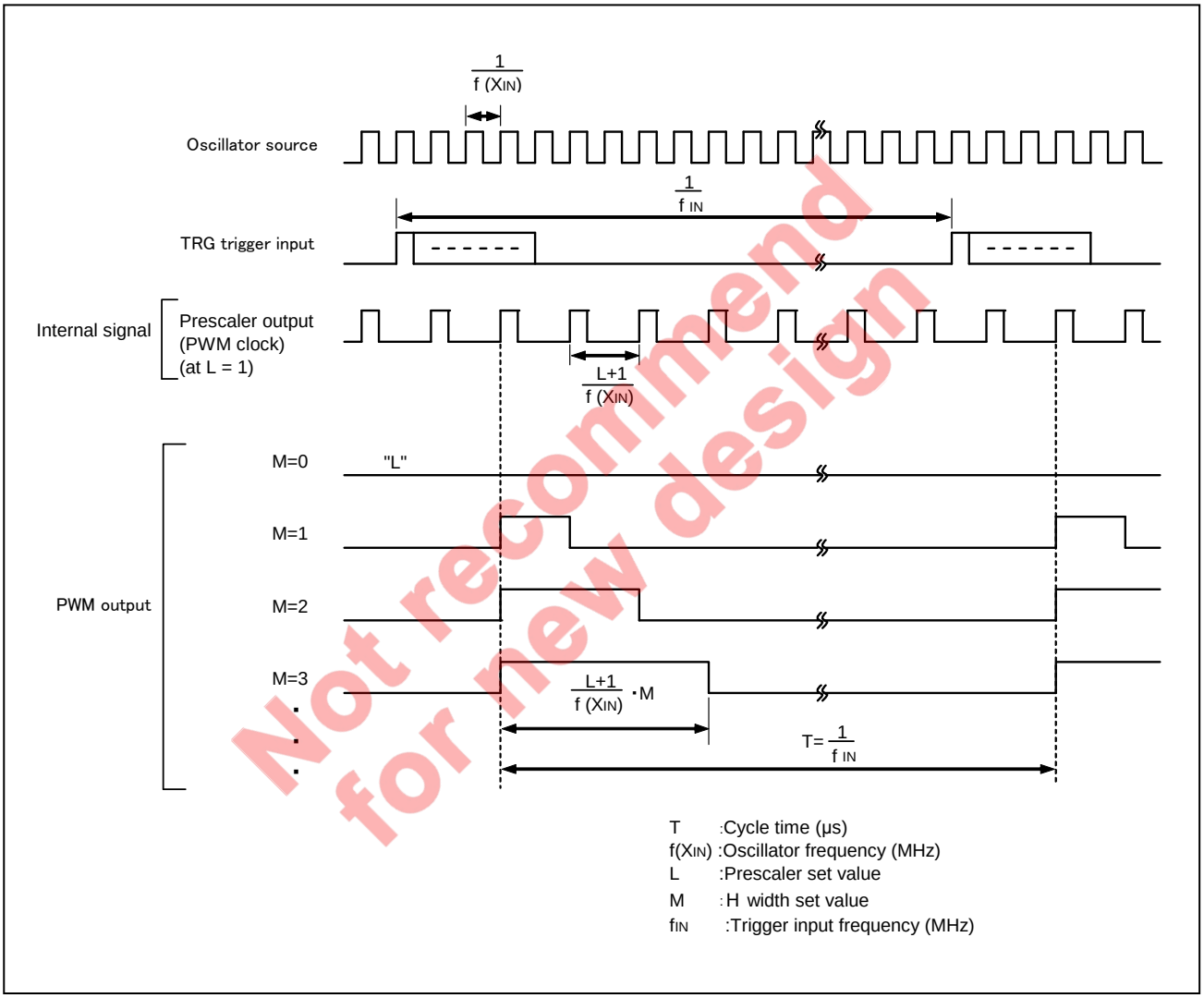


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Fig.5 (When H width polarity is “H”)

(b) Internal trigger selected (D1 = 0 in command 1)

In this mode, the trigger signal is generated by the prescaler. Therefore, the cycle time T of output pulse is determined by the prescaler register value L.

In this case, the oscillator source becomes the PWM counter clock and the output pulse width is determined by the PWM register value M. (See Fig.6)

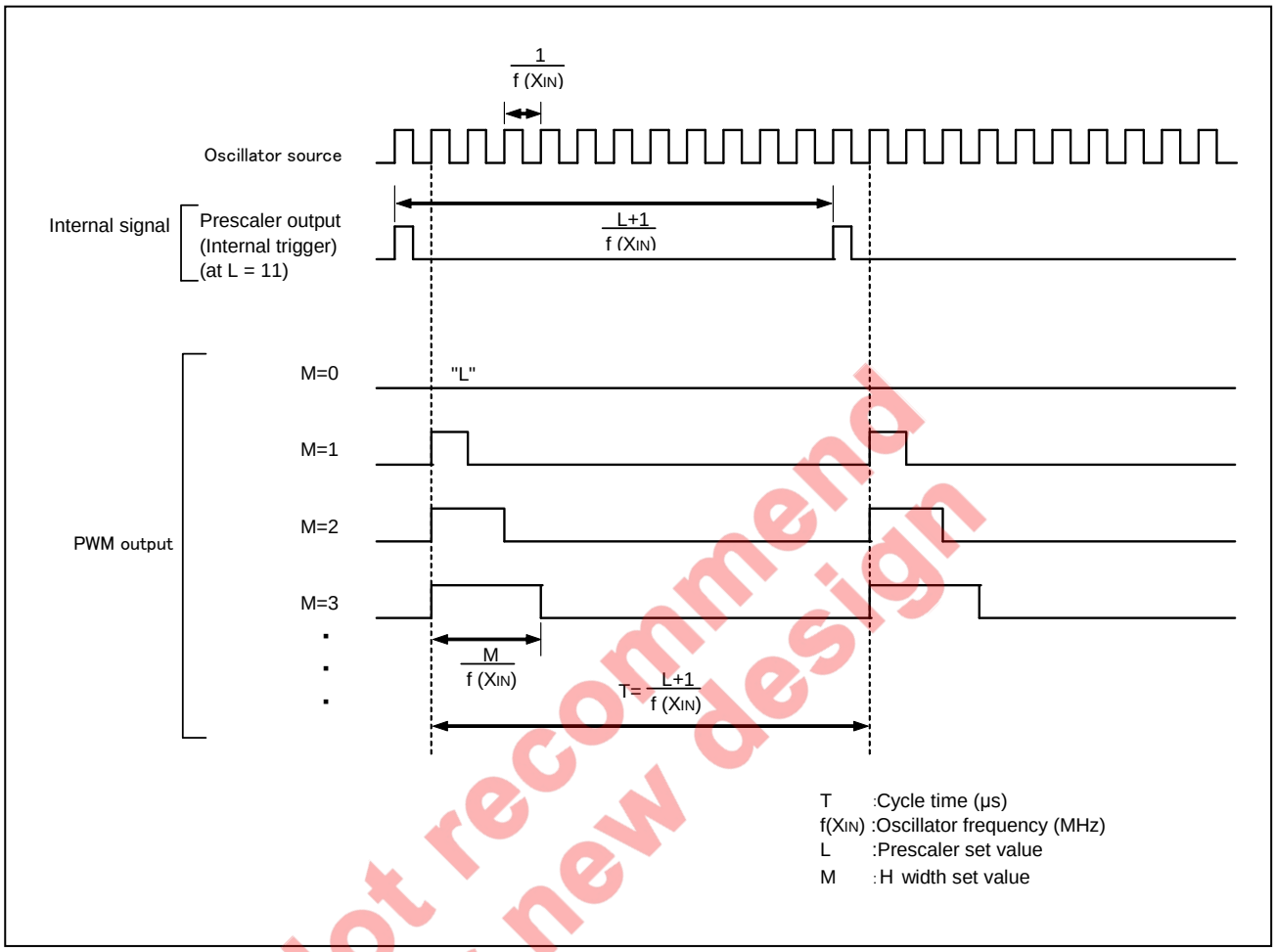


Fig.6 (When H width polarity is “H”)

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In Mode 1, the retrigger state is caused when the cycle time of trigger pulse gets smaller than the value M of PWM register.

(3) Mode 2

This mode is selected by writing D4 = 1 and D3 = 0 in command 1. Fig.11 shows the block diagram of this mode (for one channel).

The high-level pulse value M is set to the H register of PWM in Mode 0 and 1, but in this mode, the high-level pulse value M is set to the H register of PWM and the low-level pulse value N is set to the L register of PWM. Therefore, the pulse width and cycle time T of PWM output are determined by value L of the prescaler register and values M and N of H and L registers of PWM. (See Fig.7)

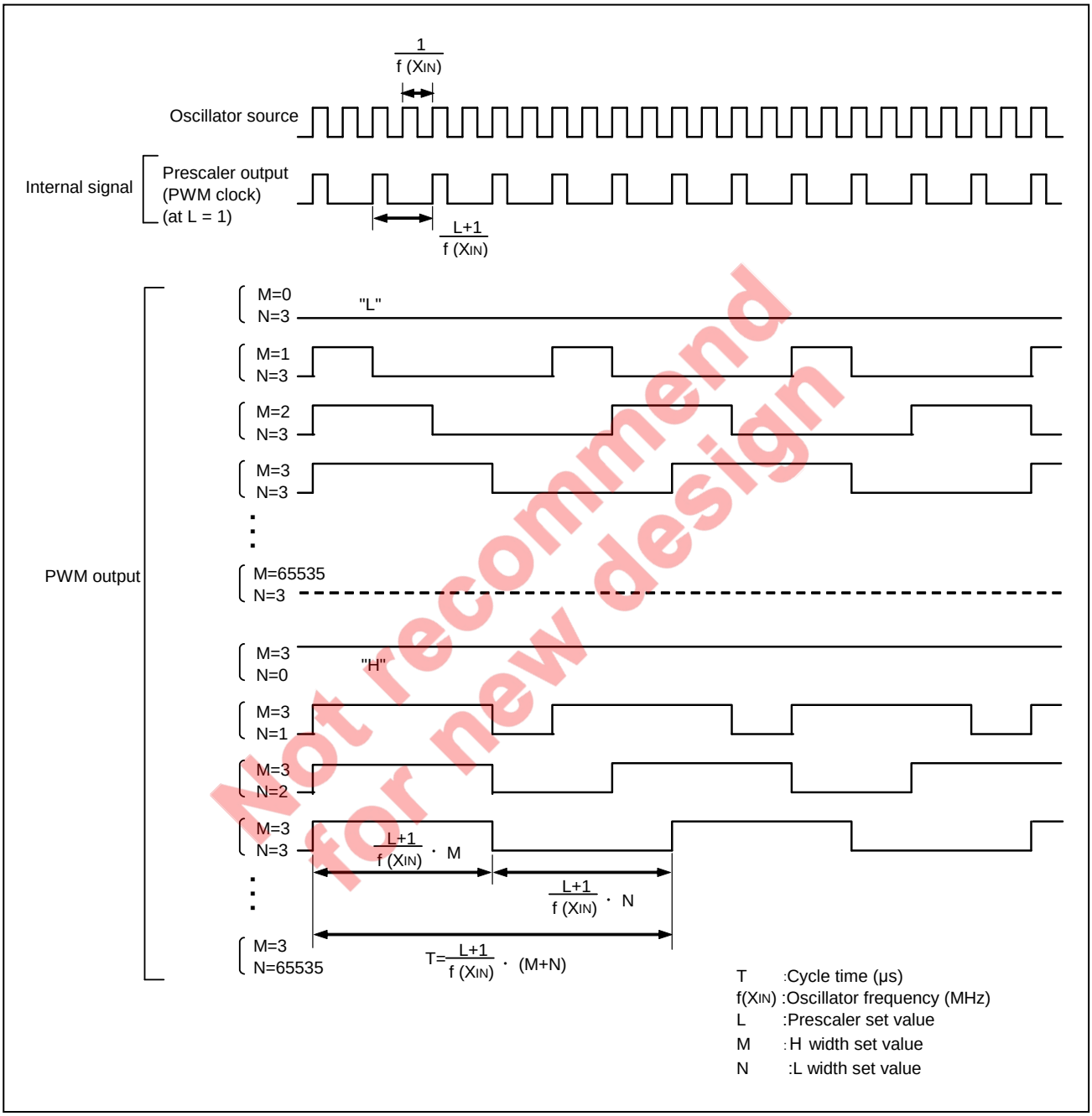


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Fig.7 (When H width polarity is “H”)

## Initial state

In the case of command 1, if the D1 is set as “external trigger ON” it does not output a pulse to PWM output and its status is held in the high impedance even if the operation of internal circuit is started by specifying enable condition with command 3.

In this case the pulse can be output to PWM output by entering H level into TRG input in Mode 0,Mode 2 or entering H pulse into TRG input in Mode1. (See Fig.8)

In Mode 0 or Mode 2, putting TRG input to L level during PWM is outputting pulse makes PWM output keeps its state. When TRG input is put back to H level, the operation are resumed from that point.

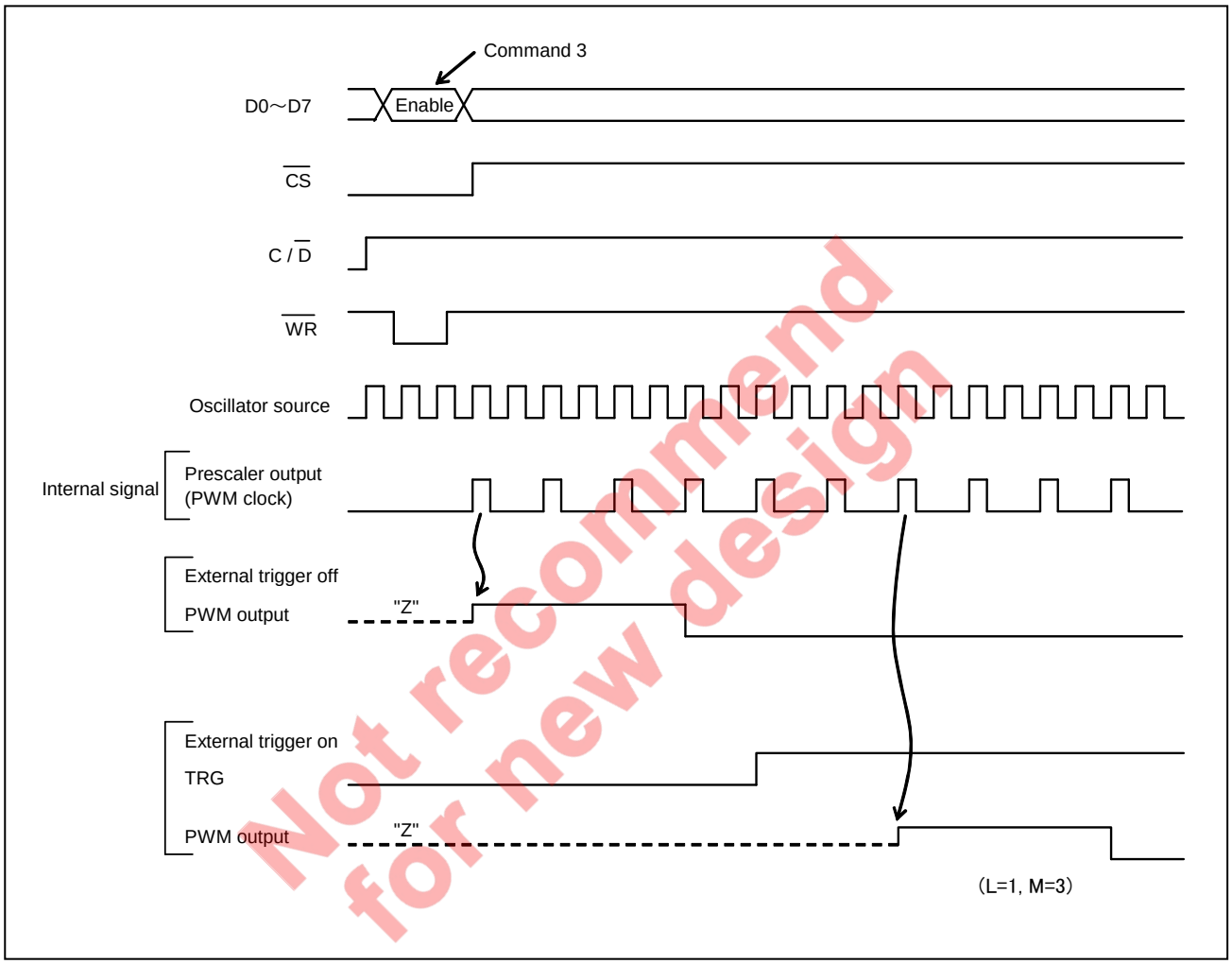


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Fig.8 (When H width polarity is “H”)

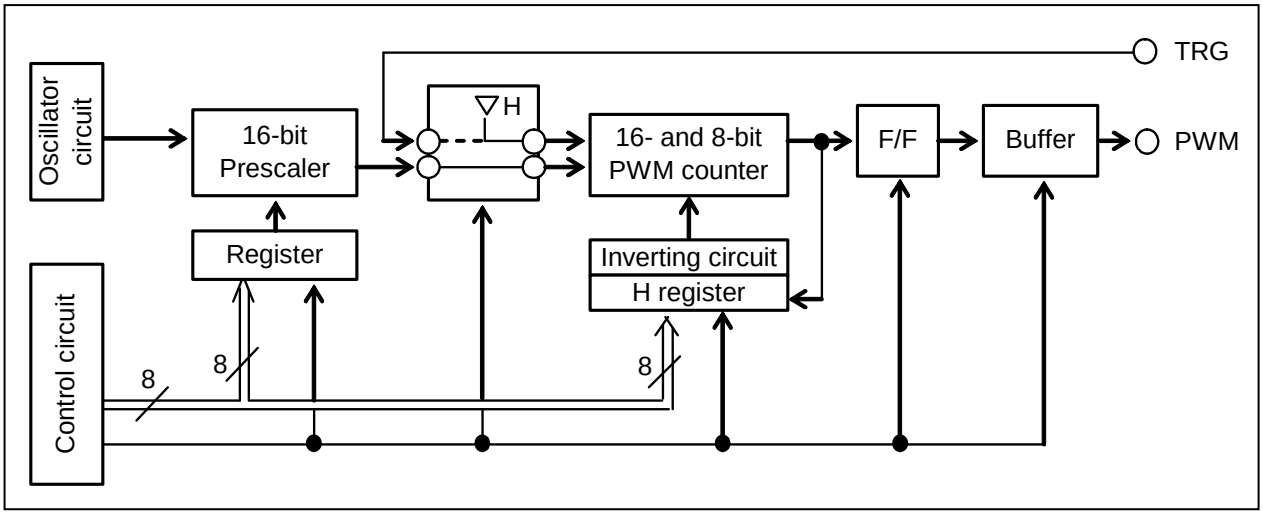


Fig.9 Block diagram in Mode 0 (for one channel)

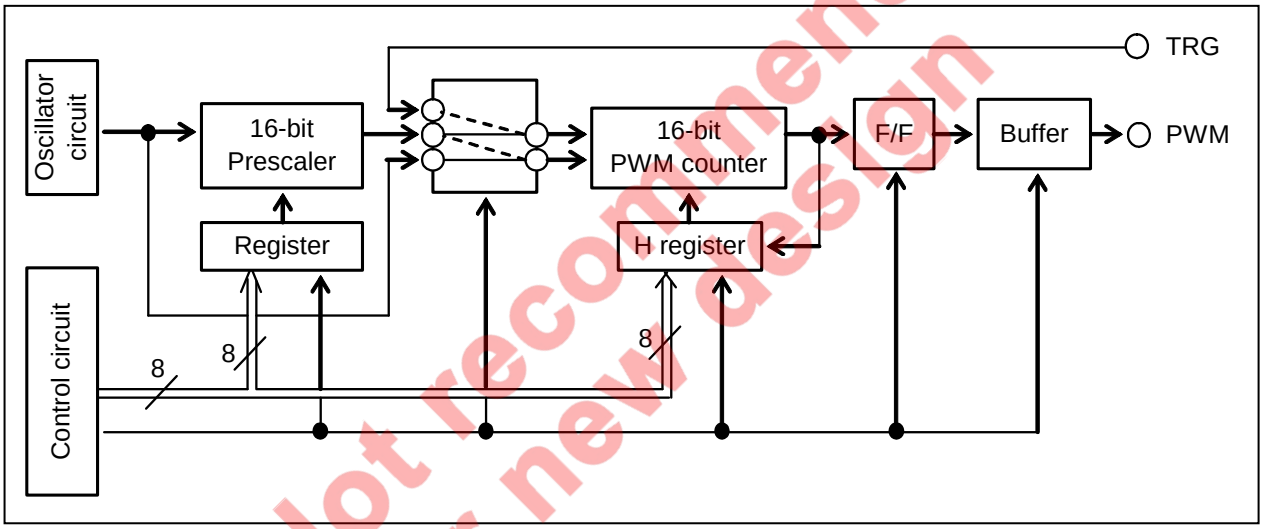


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Fig.10 Block diagram in Mode 1 (for one channel)

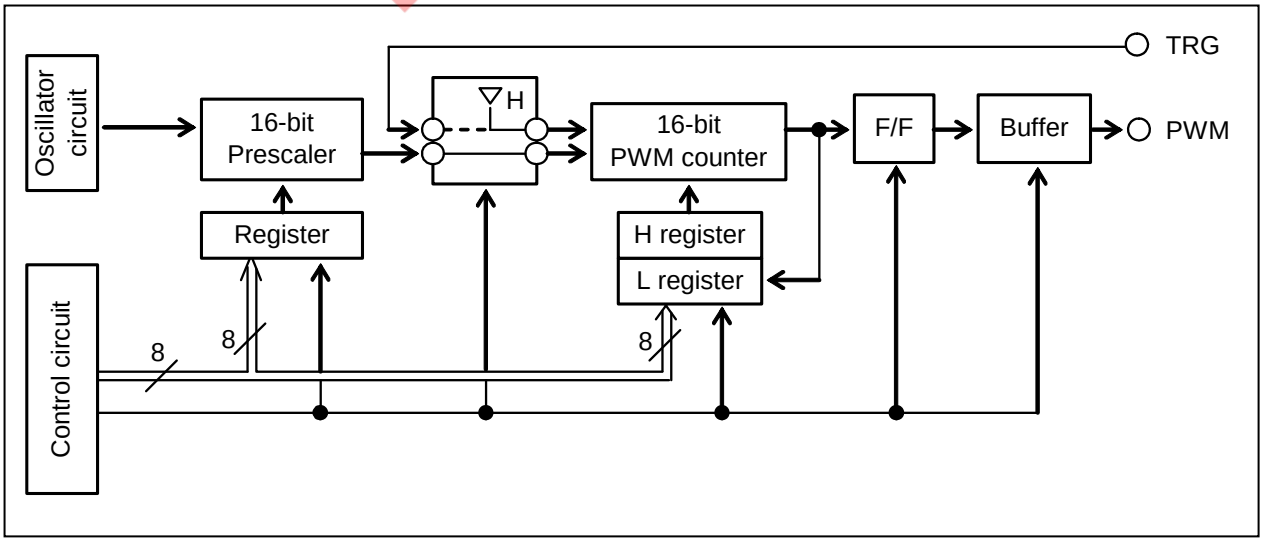


Fig.11 Block diagram in Mode 2 (for one channel)

## ABSOLUTE MAXIMUM RATINGS ( Ta=-40~85°C, unless otherwise noted )

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Vcc | Power voltage | | -0.5~+7.0 | V |
| $V_I$ | Input voltage | | -0.5~Vcc+0.5 | V |
| $V_O$ | Output voltage | | -0.5~Vcc+0.5 | V |
| Pd | Power dissipation | | 500 | mW |
| Tstg | Storage temperature | | -65~150 | °C |

## RECOMMENDED OPERATING CONDITIONS ( Ta=-40~85°C, unless otherwise noted )

| Symbol | Parameter | | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Vcc | Power voltage | 5.0V support | 4.5 | 5.0 | 5.5 | V |
| | | 3.3V support | 3.0 | 3.3 | 3.6 | V |
| GND | Power voltage | | | 0 | | V |
| $V_I$ | Input voltage | | 0 | | Vcc | V |
| $V_O$ | Output voltage | | 0 | | Vcc | V |
| Topr | Ambient operating temperature | | -40 | | 85 | °C |

## ELECTRICAL CHARACTERISTICS

### 5.0V version support specifications ( Ta=-40~85°C, Vcc=4.5~5.5V, unless otherwise noted )

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{T+}$ | Positive going threshold voltage | $\overline{RESET}$, TRG1~4 | $I_O$=20uA | 0.35×Vcc | | 0.8×Vcc | V |
| $V_{T-}$ | Negative going threshold voltage | | | 0.2×Vcc | | 0.65×Vcc | V |
| $V_H$ | Hysteresis width | | | 0.4 | | | V |
| $V_{IH}$ | "H" input voltage | D0~D7, $\overline{CS}$,$\overline{WR}$,C/$\overline{D}$ | $I_O$=20uA | 0.75×Vcc | | | V |
| $V_{IL}$ | "L" input voltage | | | | | 0.25×Vcc | V |
| $V_{IH}$ | "H" input voltage | X1 | $I_O$=20uA | 0.8×Vcc | | | V |
| $V_{IL}$ | "L" input voltage | | | | | 0.2×Vcc | V |
| $V_{OH}$ | "H" output voltage | PWM1~ PWM4 | $I_{OH}$=-24mA | Vcc - 0.8 | | | V |
| $V_{OL}$ | "L" output voltage | | $I_{OL}$=24mA | | | 0.55 | V |
| $I_{IH}$ | "H" input current | | $V_I$=Vcc | | | 1.0 | uA |
| $I_{IL}$ | "L" input current | | $V_I$=GND | | | -1.0 | uA |
| $I_{OZH}$ | Off-state "H" output current | | $V_O$=Vcc | | | 5.0 | uA |
| $I_{OZL}$ | Off-state "L" output current | | $V_O$=GND | | | -5.0 | uA |
| Icc | Quiescent current consumption | | $V_I$=Vcc, GND, Outputs are open. | | | 100 | uA |

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## ELECTRICAL CHARACTERISTICS

3.3V version support specifications ( Ta=-40~85°C, Vcc=3.0~3.6V, unless otherwise noted )

| Symbol | Parameter | | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{T+}$ | Positive going threshold voltage | $\overline{RESET}$, TRG1~4 | $I_O$=20uA | 0.35×Vcc | | 0.8×Vcc | V |
| $V_{T-}$ | Negative going threshold voltage | | | 0.2×Vcc | | 0.65×Vcc | V |
| $V_H$ | Hysteresis width | | | 0.4 | | | V |
| $V_{IH}$ | "H" input voltage | D0~D7, $\overline{CS}$,$\overline{WR}$,C/$\overline{D}$ | $I_O$=20uA | 0.75×Vcc | | | V |
| $V_{IL}$ | "L" input voltage | | | | | 0.25×Vcc | V |
| $V_{IH}$ | "H" input voltage | X1 | $I_O$=20uA | 0.8×Vcc | | | V |
| $V_{IL}$ | "L" input voltage | | | | | 0.2×Vcc | V |
| $V_{OH}$ | "H" output voltage | PWM1~ PWM4 | $I_{OH}$=-12mA | Vcc - 0.6 | | | V |
| $V_{OL}$ | "L" output voltage | | $I_{OL}$=12mA | | | 0.4 | V |
| $I_{IH}$ | "H" input current | | $V_I$=Vcc | | | 1.0 | uA |
| $I_{IL}$ | "L" input current | | $V_I$=GND | | | -1.0 | uA |
| $I_{OZH}$ | Off-state "H" output current | | $V_O$=Vcc | | | 5.0 | uA |
| $I_{OZL}$ | Off-state "L" output current | | $V_O$=GND | | | -5.0 | uA |
| Icc | Quiescent current consumption | | $V_I$=Vcc, GND, Outputs are open. | | | 100 | uA |

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## SWITCHING CHARACTERISTICS ( Ta=-40~85°C, Vcc=4.5~5.5V or Vcc=3.0~3.6V, unless otherwise noted)

| Symbol | Parameter | Test conditions | 5.0V specification | | | 3.3V specification | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| tpZL($\overline{W}$-PWM) | Output enable time after write (Mode0, 2, external trigger OFF) | CL=50pF | | | $\frac{2}{f}$ +110 | | | $\frac{2}{f}$ +130 | ns |
| tpZH($\overline{W}$-PWM) | | | | | $\frac{2}{f}$ +110 | | | $\frac{2}{f}$ +130 | ns |
| tpZL($\overline{W}$-PWM) | Output enable time after write (Mode1, external trigger OFF) | | | | $\frac{3}{f}$ +110 | | | $\frac{3}{f}$ +130 | ns |
| tpZH($\overline{W}$-PWM) | | | | | $\frac{3}{f}$ +110 | | | $\frac{3}{f}$ +130 | ns |
| tpZL(T-PWM) | Output enable time after trigger (Mode0, 2, external trigger ON) | | | | $\frac{2}{f}$ +110 | | | $\frac{2}{f}$ +130 | ns |
| tpZH(T-PWM) | | | | | $\frac{2}{f}$ +110 | | | $\frac{2}{f}$ +130 | ns |
| tpZL(T-PWM) | Output enable time after trigger (Mode1, external trigger ON) | | | | $\frac{L+2}{f}$ +110 | | | $\frac{L+2}{f}$ +130 | ns |
| tpZH(T-PWM) | | | | | $\frac{L+2}{f}$ +110 | | | $\frac{L+2}{f}$ +130 | ns |
| tpLH(X1-PWM) | Output propagation time after clock (all modes) | | | | 110 | | | 130 | ns |
| tpHL(X1-PWM) | | | | | 110 | | | 130 | ns |
| tpLH(T-PWM) | Output propagation time after trigger (Mode1, external trigger ON) | | | | $\frac{L+2}{f}$ +110 | | | $\frac{L+2}{f}$ +130 | ns |
| tpHL(T-PWM) | | | | | $\frac{L+2}{f}$ +110 | | | $\frac{L+2}{f}$ +130 | ns |
| tpLZ($\overline{R}$-PWM) | Output disable time after reset | | | | 150 | | | 160 | ns |
| tpHZ($\overline{R}$-PWM) | | | | | 150 | | | 160 | ns |
| tpLZ($\overline{W}$-PWM) | Output disable time after write | | | | 150 | | | 160 | ns |
| tpHZ($\overline{W}$-PWM) | | | | | 150 | | | 160 | ns |

f : Clock input frequency (MHz)
L: Prescaler set value

Not recommend for new design

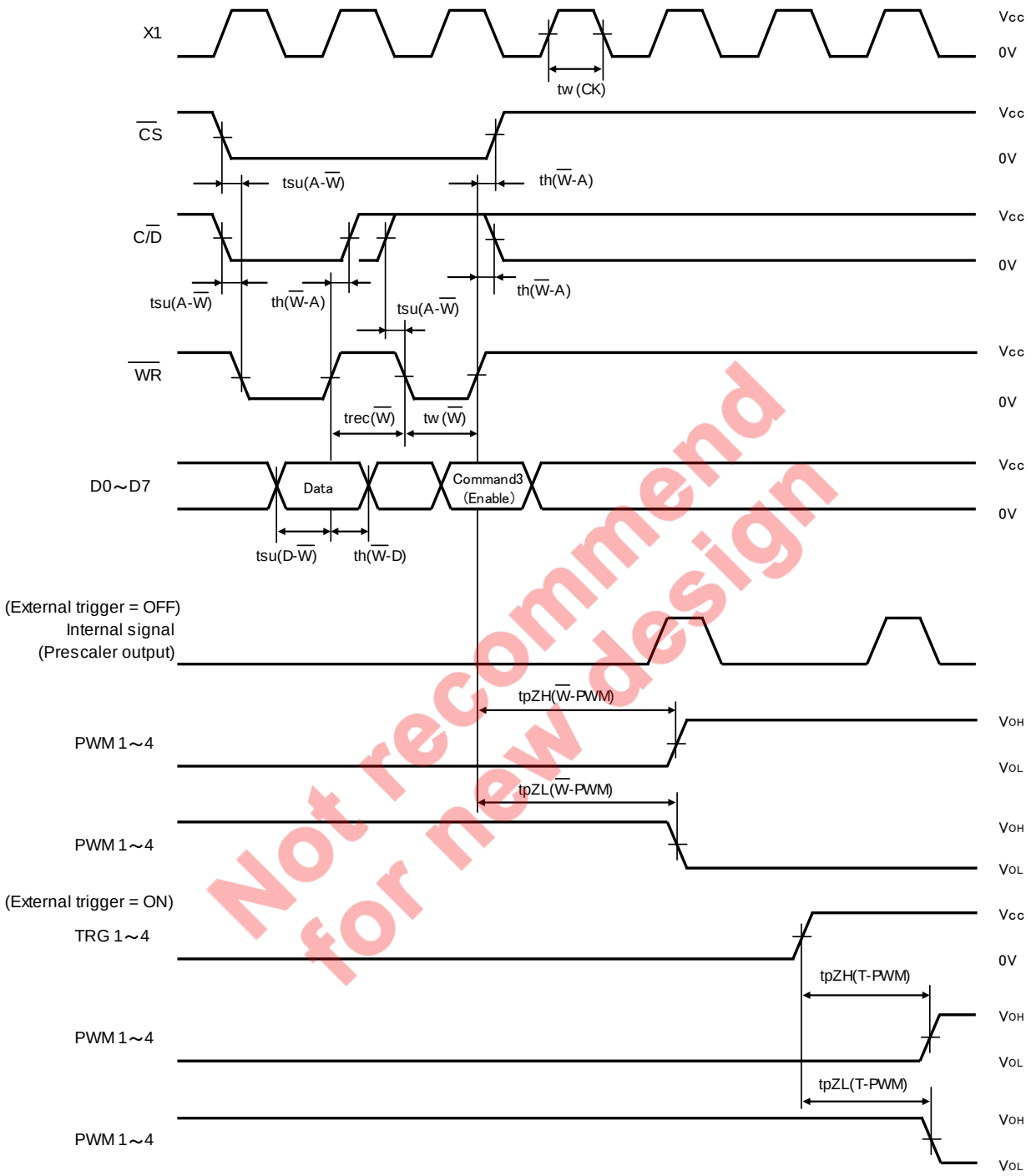
## TIMING REQUIREMENTS ( Ta=-40~85°C, Vcc=4.5~5.5V or Vcc=3.0~3.6V, unless otherwise noted)

| Symbol | Parameter | Test conditions | 5.0V specification | | | 3.3V specification | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| tc(X1) | Clock cycle | | 78.5 | | | 78.5 | | | ns |
| tWH(X1) | Clock "H" pulse width | | 35 | | | 35 | | | ns |
| tWL(X1) | Clock "L" pulse width | | 35 | | | 35 | | | ns |
| tr(X1) | Clock rise time | | | | 20 | | | 20 | ns |
| tf(X1) | Clock fall time | | | | 20 | | | 20 | ns |
| tsu(A-$\overline{W}$) | Address setup time before write ($\overline{CS}$, C/$\overline{D}$) | | 0 | | | 0 | | | ns |
| th($\overline{W}$-A) | Address hold time after write ($\overline{CS}$, C/$\overline{D}$) | | 0 | | | 0 | | | ns |
| tsu(D-$\overline{W}$) | Data setup time before write | | 100 | | | 100 | | | ns |
| th($\overline{W}$-D) | Data hold time after write | | 0 | | | 0 | | | ns |
| tw($\overline{W}$) | Write pulse width | | 100 | | | 100 | | | ns |
| trec($\overline{W}$) | Write recovery time | | 100 | | | 100 | | | ns |
| tw(T) | Trigger pulse width | | 100 | | | 100 | | | ns |
| tw($\overline{R}$) | Reset pulse width | | 100 | | | 100 | | | ns |
| trec($\overline{R}$-$\overline{W}$) | Recovery time before write | | 100 | | | 100 | | | ns |

Not recommend for new design

# TIMING DIAGRAM

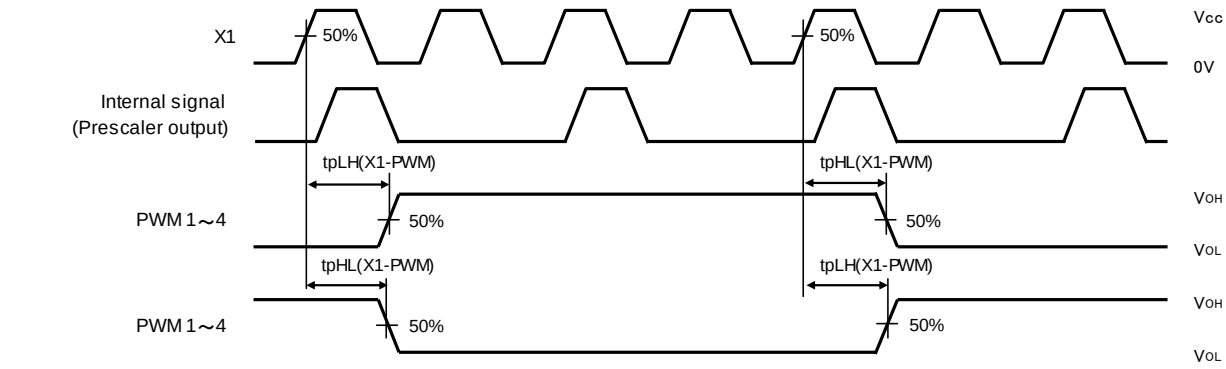
## (1) MCU interface



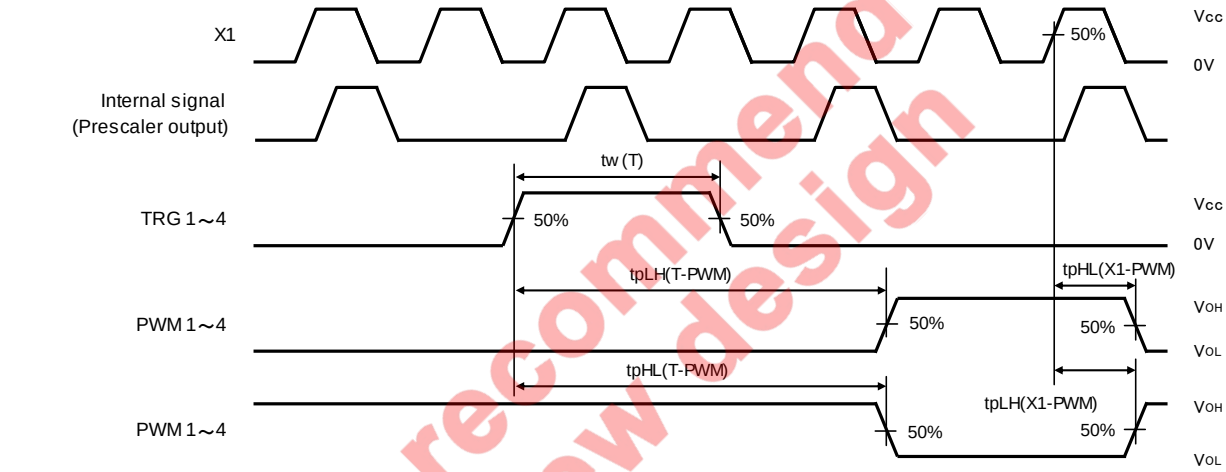

Not recommend for new design

(2) In operation

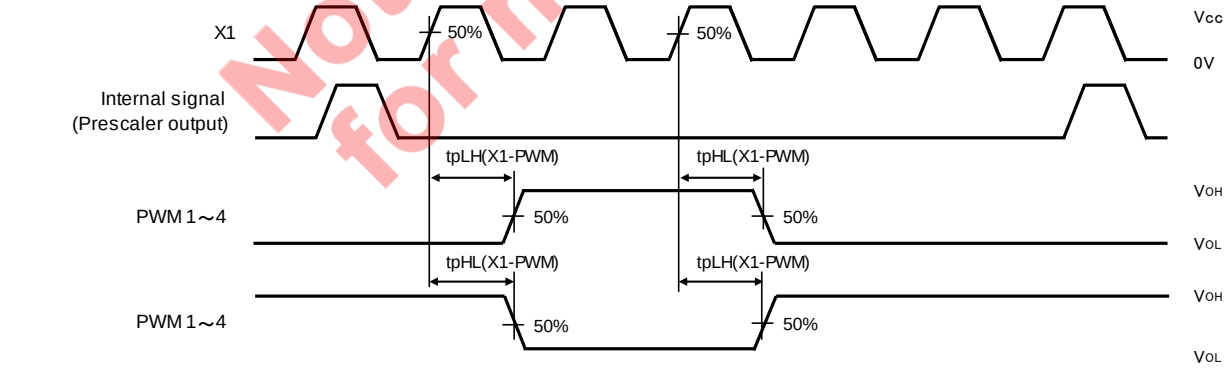
Mode 0,2 (external trigger ON, OFF)




Mode 1 (external trigger ON)

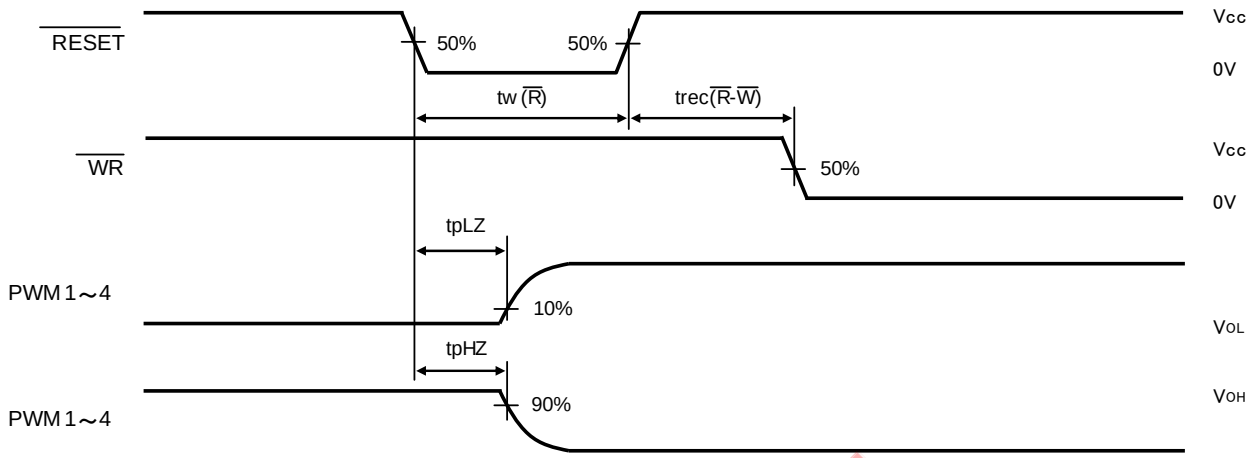



Mode 1 (external trigger OFF)

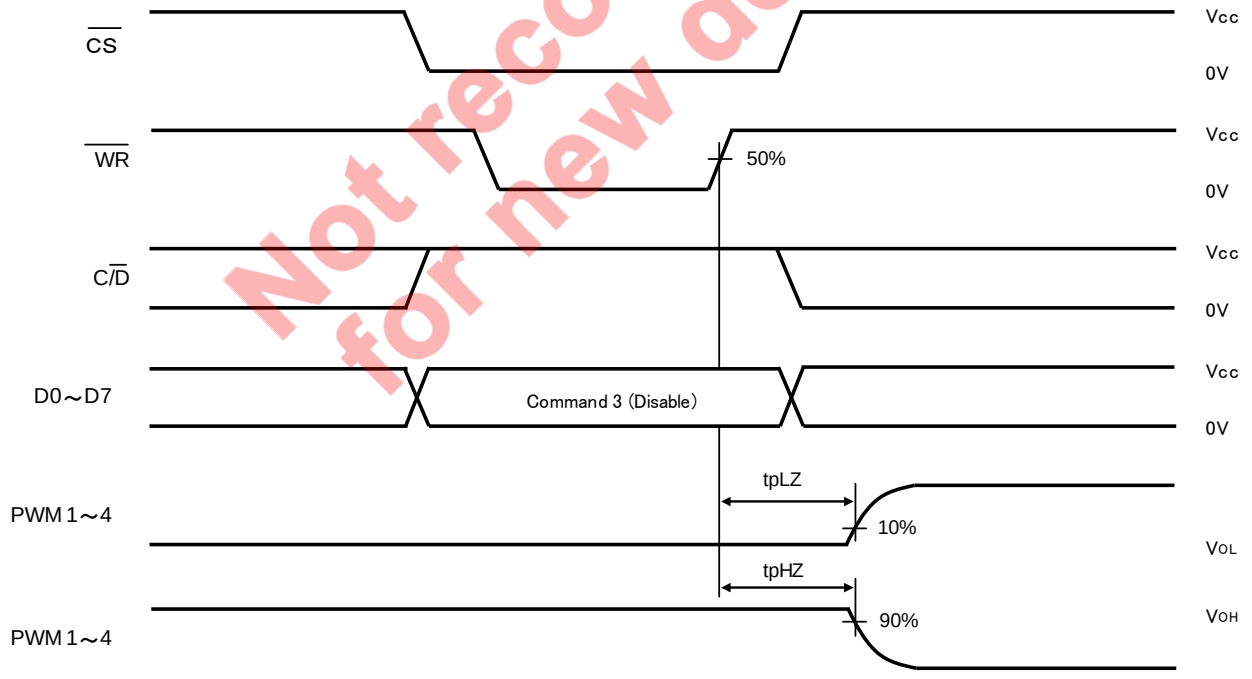



Not recommend for new design

(3) At reset

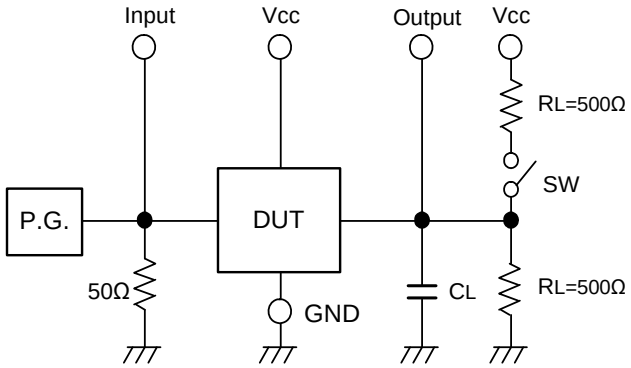



(4) At disable




Not recommend for new design

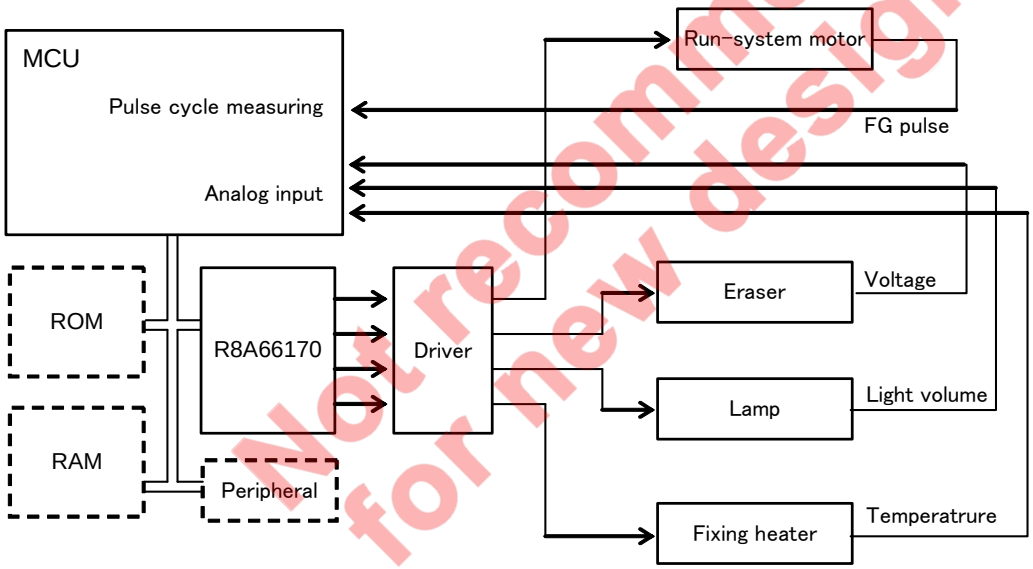
## TEST CIRCUIT




| Parameter | SW |
|---|---|
| tTLH, tTHL | Open |
| tpLH, tpHL | |
| tpLZ | Close |
| tpHZ | Open |
| tpZL | Close |
| tpZH | Open |

(1) Characteristics of pulse generater(P.G.) (10%～90%)
tr=3ns, tf=3ns
(2) $C_L$ includes stray probe and wiring capacitance.

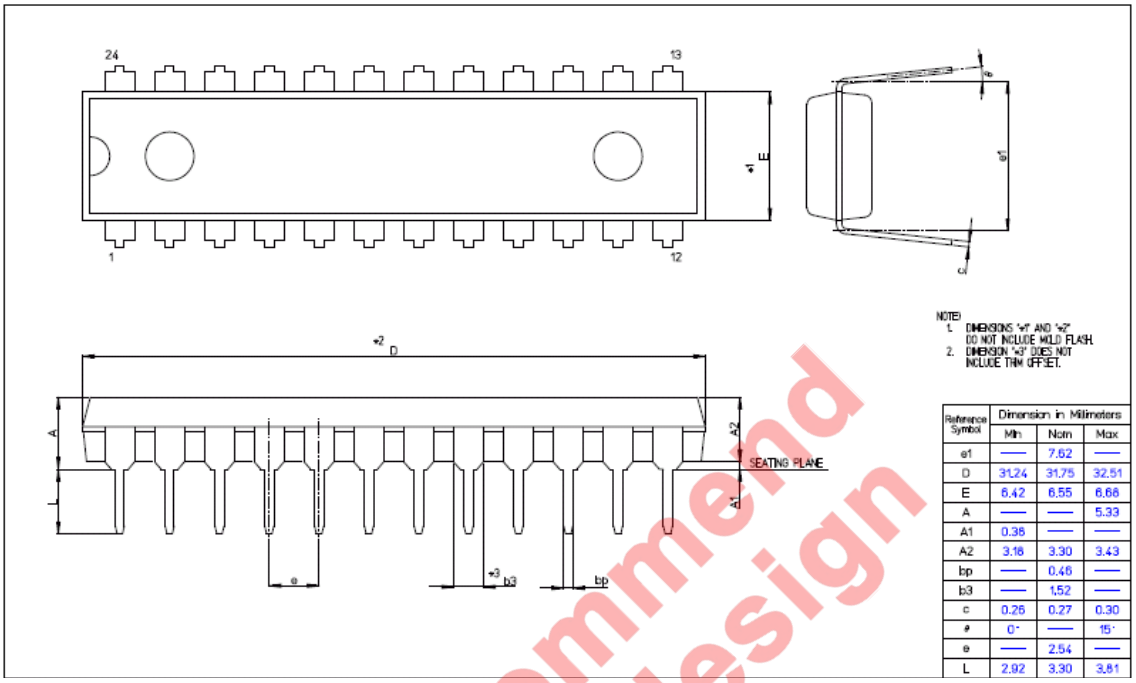
## APPLICATION EXAMPLE




Not recommend for new design

## PACKAGE OUTLINE

| Product Name | Package | RENESAS Code | Previous Code |
|---|---|---|---|
| R8A66170DD | 24pin DIP | PRDP0024AF-A | 24P4X-A |
| R8A66170SP | 24pin SOP | PRSP0024DF-A | 24P2X-B |




| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| e1 | — | 7.62 | — |
| D | 31.24 | 31.75 | 32.51 |
| E | 6.42 | 6.55 | 6.68 |
| A | — | — | 5.33 |
| A1 | 0.38 | — | — |
| A2 | 3.16 | 3.30 | 3.43 |
| bp | — | 0.46 | — |
| b3 | — | 1.52 | — |
| c | 0.26 | 0.27 | 0.30 |
| θ | 0° | — | 15° |
| e | — | 2.54 | — |
| L | 2.92 | 3.30 | 3.81 |

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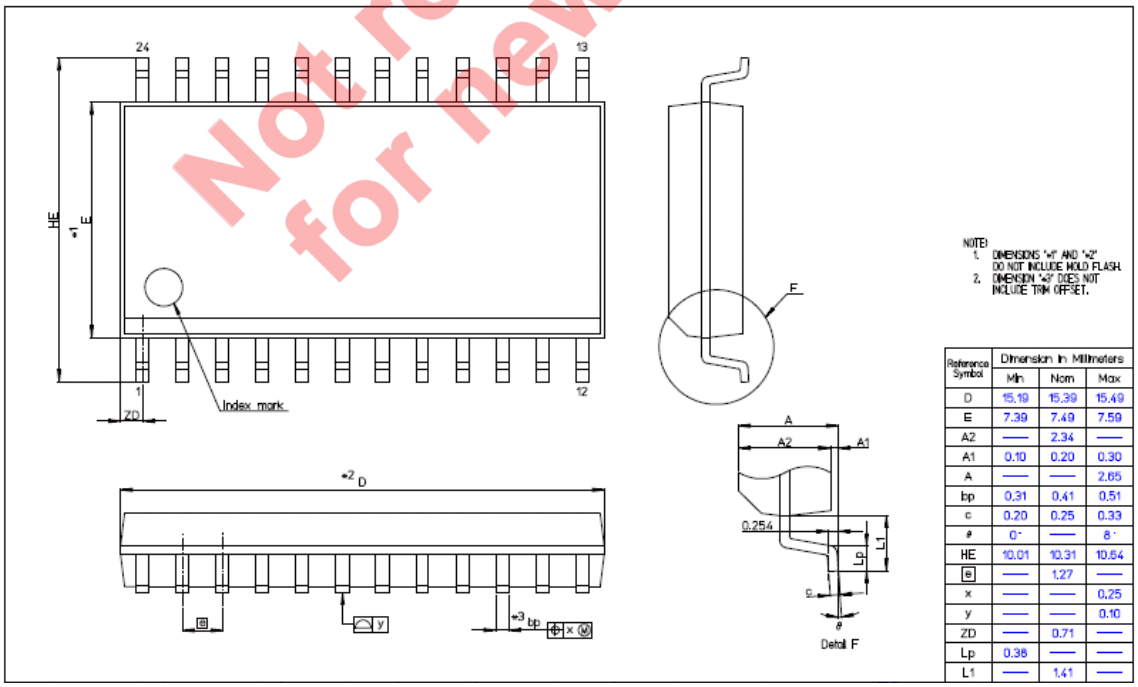


| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 15.19 | 15.39 | 15.49 |
| E | 7.39 | 7.49 | 7.59 |
| A2 | — | 2.34 | — |
| A1 | 0.10 | 0.20 | 0.30 |
| A | — | — | 2.65 |
| bp | 0.31 | 0.41 | 0.51 |
| c | 0.20 | 0.25 | 0.33 |
| θ | 0° | — | 8° |
| HE | 10.01 | 10.31 | 10.64 |
| e | — | 1.27 | — |
| x | — | — | 0.25 |
| y | — | — | 0.10 |
| ZD | — | 0.71 | — |
| Lp | 0.38 | — | — |
| L1 | — | 1.41 | — |

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