

RAA210833

Pin-Configurable 33A DC/DC Power Module with PMBus Interface

FN9348  
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The [RAA210833](#) is a pin-strap-configurable 33A step-down PMBus-compliant DC/DC power supply module that integrates a digital PWM controller, synchronous MOSFETs, power inductor, and passive components. Only input and output capacitors are needed to finish the design. Because of its thermally enhanced HDA packaging technology, the module can deliver up to 33A of continuous output current without the need for airflow or additional heat sinking. The RAA210833 simplifies configuration and control of Renesas [digital power technology](#) while offering an upgrade path to full PMBus configuration through the pin-compatible ISL8278M.

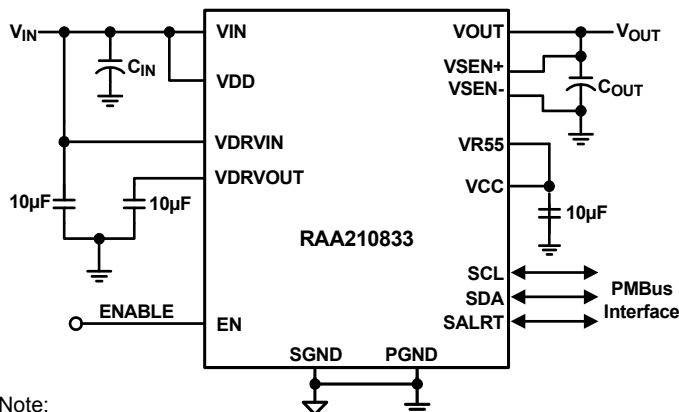
The RAA210833 uses ChargeMode™ control architecture, which responds to a transient load within a single switching cycle. The RAA210833 comes with a preprogrammed configuration for operating in a pin-strap mode. Output voltage, switching frequency, input UVLO, soft-start/stop delay and ramp times, and the device SMBus address can be programmed with external pin-strap resistors. A standard PMBus interface addresses fault management, as well as real-time full telemetry and point-of-load monitoring.

The RAA210833 is available in a 41 Ld compact 17mmx19mm HDA module with a very low profile height of 3.6mm, suitable for automated assembly by standard surface mount equipment. The RAA210833 is RoHS compliant by exemption.

**Related Literature**

For a full list of related documents, visit our website

- [RAA210833](#) product page



Note:  
1. Only bulk input and output capacitors are required to finish the design.

Figure 1. A Complete Digital Switch-Mode Power Supply

**Features**

- 33A single channel output current
- Wide  $V_{IN}$  range: 4.5V to 14V
- Programmable output voltage
  - 0.6V to 5V output voltage settings
  - $\pm 1.2\%$  accuracy over line/load/temperature
- PMBus Interface and/or Pin-strap mode
  - Pin-strap mode for standard settings
  - $V_{OUT}$  switching frequency, input UVLO, soft-start/stop, and external sync
  - Real time telemetry for  $V_{IN}$ ,  $V_{OUT}$ ,  $I_{OUT}$ , temperature, duty cycle, and switching frequency.
- ChargeMode control loop architecture
  - 296kHz to 1.06MHz fixed switching frequency operations
  - No compensation required
  - Fast single clock cycle transient response
- Complete input and output over/undervoltage, output current, and temperature protections with fault logging
- [PowerNavigator](#) supported
- Thermally enhanced HDA package

**Applications**

- Server, telecom, storage, and datacom
- Industrial/ATE and networking equipment
- General purpose power for ASIC, FPGA, DSP, and memory

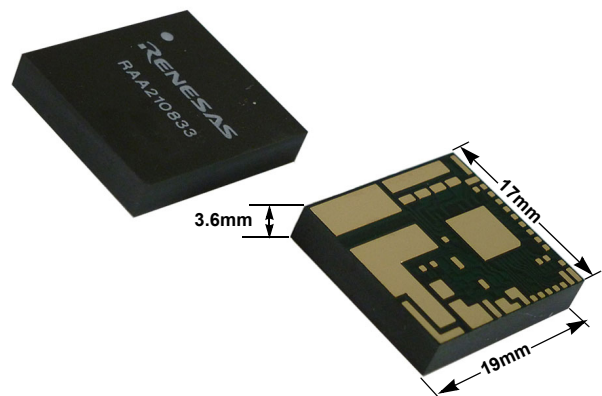


Figure 2. A Small Package for High Power Density

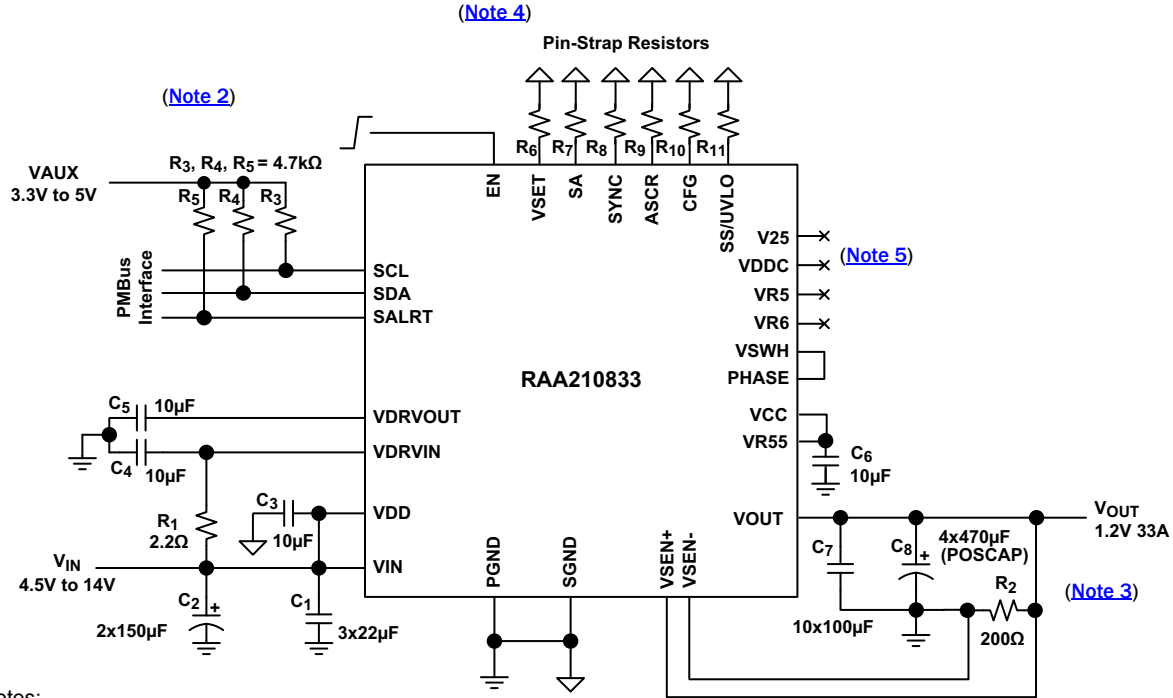
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# 1. Overview

## 1.1 Typical Application Circuit



Notes:

- $R_3$  and  $R_4$  are not required if the PMBus host already has I<sup>2</sup>C pull-up resistors.
- $R_2$  is optional but is recommended to sink possible ~100µA back-flow current from the VSEN+ pin. Back-flow current is present only when the module is in a disabled state with power still available at the VDD pin.
- $R_6$  through  $R_{11}$  can be selected according to the tables for the pin-strap resistor setting in this document.
- Internal reference supply pins (V25, VDDC, VR5, VR6) do not need external capacitors and can be no connect. Refer to "[PCB Layout Guidelines](#)" on page 30 for more information.

Figure 3. Typical Single-Phase Application Circuit for 1.2V/33A Output

Table 1. RAA210833 Design Guide Matrix and Output Voltage Response

| V <sub>IN</sub> (V) | V <sub>OUT</sub> (V) | Input Capacitors             | Output Capacitors              | ASCR Gain<br>(Note 7) | ASCR Residual<br>(Note 7) | Frequency<br>(kHz)<br>(Note 9) | V <sub>OUT</sub> Dev<br>Peak-to-Peak<br>(mV)<br>(Note 8) |
|---------------------|----------------------|------------------------------|--------------------------------|-----------------------|---------------------------|--------------------------------|----------------------------------------------------------|
| 5                   | 0.7                  | 3x22µF Ceramic + 2x150µF POS | 12x100µF Ceramic + 6x470µF POS | 350                   | 100                       | 296                            | 75                                                       |
| 5                   | 0.7                  | 3x22µF Ceramic + 2x150µF POS | 4x100µF Ceramic + 6x470µF POS  | 400                   | 90                        | 615                            | 73                                                       |
| 12                  | 0.7                  | 3x22µF Ceramic + 2x150µF POS | 12x100µF Ceramic + 6x470µF POS | 350                   | 100                       | 296                            | 78                                                       |
| 12                  | 0.7                  | 3x22µF Ceramic + 2x150µF POS | 4x100µF Ceramic + 6x470µF POS  | 500                   | 90                        | 615                            | 72                                                       |
| 5                   | 0.8                  | 3x22µF Ceramic + 2x150µF POS | 12x100µF Ceramic + 6x470µF POS | 350                   | 100                       | 296                            | 74                                                       |
| 5                   | 0.8                  | 3x22µF Ceramic + 2x150µF POS | 4x100µF Ceramic + 6x470µF POS  | 400                   | 80                        | 615                            | 73                                                       |
| 12                  | 0.8                  | 3x22µF Ceramic + 2x150µF POS | 12x100µF Ceramic + 6x470µF POS | 350                   | 100                       | 296                            | 75                                                       |

Table 1. RAA210833 Design Guide Matrix and Output Voltage Response (Continued)

| $V_{IN}$ (V) | $V_{OUT}$ (V) | Input Capacitors                         | Output Capacitors                          | ASCR Gain<br>(Note 7) | ASCR Residual<br>(Note 7) | Frequency<br>(kHz)<br>(Note 9) | $V_{OUT}$ Dev<br>Peak-to-Peak<br>(mV)<br>(Note 8) |
|--------------|---------------|------------------------------------------|--------------------------------------------|-----------------------|---------------------------|--------------------------------|---------------------------------------------------|
| 12           | 0.8           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 6x470 $\mu$ F POS  | 400                   | 80                        | 615                            | 73                                                |
| 5            | 0.9           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 12x100 $\mu$ F Ceramic + 5x470 $\mu$ F POS | 350                   | 90                        | 364                            | 75                                                |
| 5            | 0.9           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 5x470 $\mu$ F POS  | 300                   | 70                        | 615                            | 84                                                |
| 12           | 0.9           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 12x100 $\mu$ F Ceramic + 5x470 $\mu$ F POS | 350                   | 80                        | 364                            | 85                                                |
| 12           | 0.9           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 5x470 $\mu$ F POS  | 400                   | 80                        | 615                            | 84                                                |
| 5            | 1             | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 12x100 $\mu$ F Ceramic + 4x470 $\mu$ F POS | 350                   | 90                        | 364                            | 81                                                |
| 5            | 1             | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 4x470 $\mu$ F POS  | 350                   | 80                        | 615                            | 89                                                |
| 12           | 1             | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 12x100 $\mu$ F Ceramic + 4x470 $\mu$ F POS | 350                   | 90                        | 364                            | 85                                                |
| 12           | 1             | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 4x470 $\mu$ F POS  | 350                   | 80                        | 615                            | 90                                                |
| 5            | 1.2           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 10x100 $\mu$ F Ceramic + 4x470 $\mu$ F POS | 250                   | 90                        | 364                            | 100                                               |
| 5            | 1.2           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 3x470 $\mu$ F POS  | 300                   | 80                        | 727                            | 103                                               |
| 12           | 1.2           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 10x100 $\mu$ F Ceramic + 4x470 $\mu$ F POS | 250                   | 90                        | 364                            | 110                                               |
| 12           | 1.2           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 3x470 $\mu$ F POS  | 300                   | 80                        | 727                            | 110                                               |
| 5            | 1.5           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 7x100 $\mu$ F Ceramic + 2x470 $\mu$ F POS  | 250                   | 90                        | 471                            | 130                                               |
| 5            | 1.5           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 2x470 $\mu$ F POS  | 350                   | 90                        | 727                            | 125                                               |
| 12           | 1.5           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 7x100 $\mu$ F Ceramic + 2x470 $\mu$ F POS  | 250                   | 90                        | 471                            | 147                                               |
| 12           | 1.5           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 2x470 $\mu$ F POS  | 350                   | 90                        | 727                            | 130                                               |
| 5            | 1.8           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 6x100 $\mu$ F Ceramic + 2x470 $\mu$ F POS  | 200                   | 90                        | 471                            | 155                                               |
| 5            | 1.8           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 2x470 $\mu$ F POS  | 210                   | 80                        | 727                            | 155                                               |
| 12           | 1.8           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 6x100 $\mu$ F Ceramic + 2x470 $\mu$ F POS  | 200                   | 90                        | 471                            | 160                                               |
| 12           | 1.8           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 2x470 $\mu$ F POS  | 210                   | 80                        | 727                            | 160                                               |
| 5            | 2.5           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 1x470 $\mu$ F POS  | 190                   | 100                       | 615                            | 215                                               |
| 12           | 2.5           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 1x470 $\mu$ F POS  | 190                   | 100                       | 615                            | 226                                               |

**Table 1. RAA210833 Design Guide Matrix and Output Voltage Response (Continued)**

| $V_{IN}$ (V) | $V_{OUT}$ (V) | Input Capacitors                         | Output Capacitors                         | ASCR Gain<br>( <a href="#">Note 7</a> ) | ASCR Residual<br>( <a href="#">Note 7</a> ) | Frequency<br>(kHz)<br>( <a href="#">Note 9</a> ) | $V_{OUT}$ Dev<br>Peak-to-Peak<br>(mV) ( <a href="#">Note 8</a> ) |
|--------------|---------------|------------------------------------------|-------------------------------------------|-----------------------------------------|---------------------------------------------|--------------------------------------------------|------------------------------------------------------------------|
| 12           | 3.3           | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 1x470 $\mu$ F POS | 190                                     | 100                                         | 615                                              | 236                                                              |
| 12           | 5             | 3x22 $\mu$ F Ceramic + 2x150 $\mu$ F POS | 4x100 $\mu$ F Ceramic + 1x470 $\mu$ F POS | 160                                     | 100                                         | 727                                              | 278                                                              |

Notes:

6.  $C_{IN}$  bulk capacitor is optional only for energy buffer from the long input power supply cable.
7. ASCR gain and residual are selected to ensure that the phase margin is higher than 60° at ambient room temperature (+25°C).
8. Peak-to-peak voltage deviation is measured under 0% - 50% load transient and slew rate = 15A/ $\mu$ s.
9. Frequency is selected to achieve best efficiency at full load. Higher frequency can be selected because less output capacitance is required to meet the transient response specification.

**Table 2. Recommended I/O Capacitor in [Table 1](#)**

| Vendors                    | Value                   | Part Number        |
|----------------------------|-------------------------|--------------------|
| Murata, Input Ceramic      | 22 $\mu$ F, 25V, 1210   | GRM32ER71E226KE15L |
| Taiyo Yuden, Input Ceramic | 22 $\mu$ F, 25V, 1210   | TMK325BJ226MM-T    |
| Murata, Output Ceramic     | 100 $\mu$ F, 6.3V, 1210 | GRM32EC80J107ME20L |
| TDK, Output Ceramic        | 100 $\mu$ F, 6.3V, 1210 | C3225X5R0J107M     |
| Sanyo POSCAP, Input Bulk   | 150 $\mu$ F, 16V        | 16TQC150MYF        |
| Sanyo POSCAP, Output Bulk  | 470 $\mu$ F, 6.3V       | 6TPE470MI          |

## 1.2 RAA210833 Internal Block Diagram

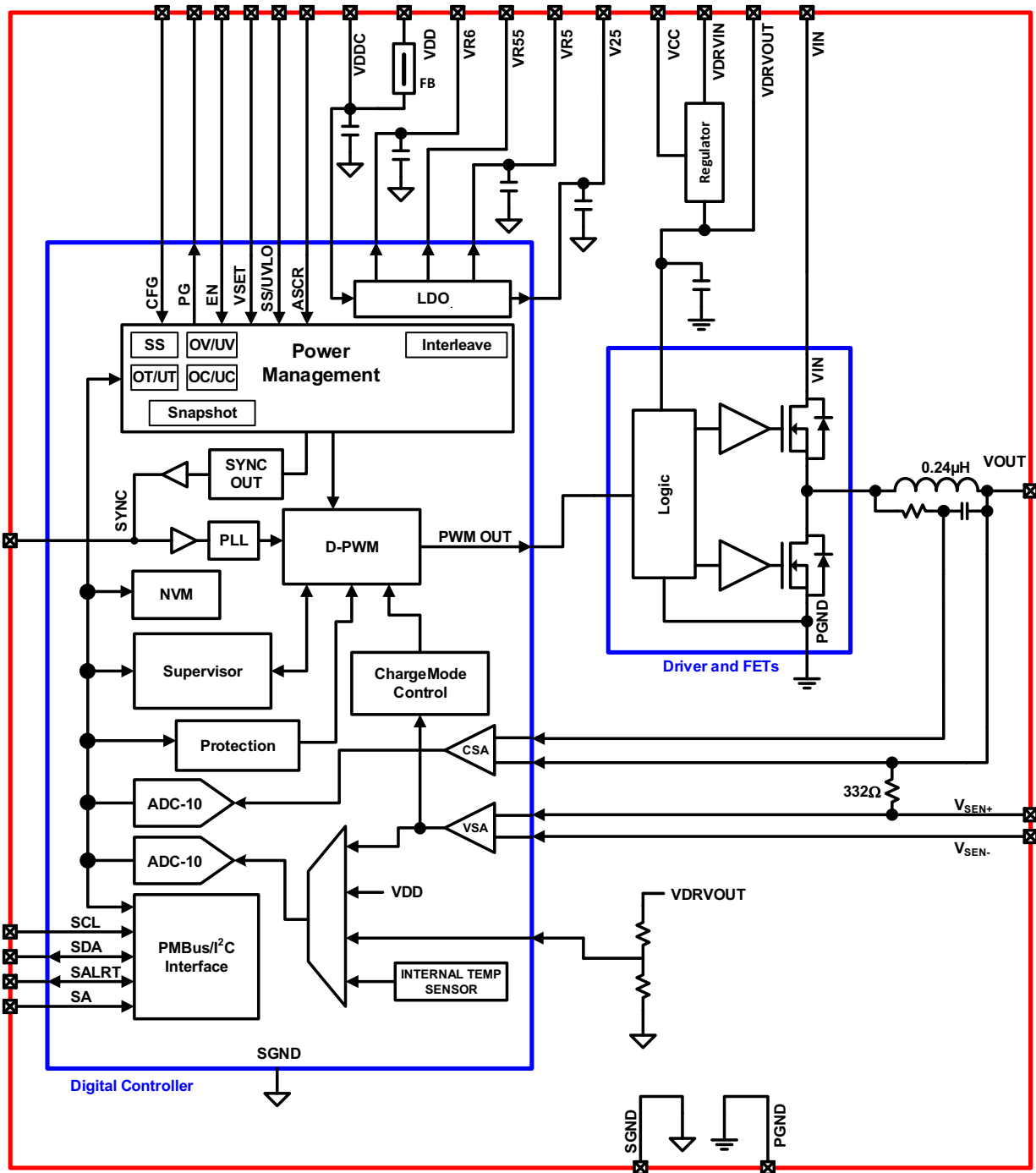


Figure 4. Internal Block Diagram

### 1.3 Ordering Information

| Part Number<br>(Notes 10, 11, 12) | Part Marking     | Temp Range (°C) | Tape and Reel (Units) (Note 1) | Package (RoHS Compliant) | Pkg. Dwg. # |
|-----------------------------------|------------------|-----------------|--------------------------------|--------------------------|-------------|
| RAA2108332GLG#AG0                 | RAA2108332       | -40 to +85      | -                              | 41 Ld 17x19 HDA          | Y41.17x19   |
| RAA2108332GLG#HG0                 | RAA2108332       | -40 to +85      | 500                            | 41 Ld 17x19 HDA          | Y41.17x19   |
| RAA2108332GLG#MG0                 | RAA2108332       | -40 to +85      | 100                            | 41 Ld 17x19 HDA          | Y41.17x19   |
| RTKA2108332H00000BU               | Evaluation Board |                 |                                |                          |             |

Notes:

10. Refer to [TB347](#) for details about reel specifications.
11. These Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I and 7A. They employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
12. For Moisture Sensitivity Level (MSL), see the [RAA210833](#) device page. For more information about MSL, see [TB363](#).

**Table 3. Key Differences between Family of Parts**

| Part Number | Description                             | V <sub>IN</sub> Range (V) | V <sub>OUT</sub> Range (V) | I <sub>OUT</sub> (A) |
|-------------|-----------------------------------------|---------------------------|----------------------------|----------------------|
| RAA210833   | 33A DC/DC single channel Power Module   | 4.5 - 14                  | 0.6 - 5                    | 33                   |
| RAA210825   | 25A DC/DC single channel Power Module   | 4.5 - 14                  | 0.6 - 5                    | 25                   |
| RAA210850   | 50A DC/DC single channel Power Module   | 4.5 - 14                  | 0.6 - 5                    | 50                   |
| RAA210870   | 70A DC/DC single channel Power Module   | 4.5 - 14                  | 0.6 - 2.5                  | 70                   |
| RAA210925   | 25A/25A DC/DC dual channel Power Module | 4.5 - 14                  | 0.6 - 5                    | 25/25                |

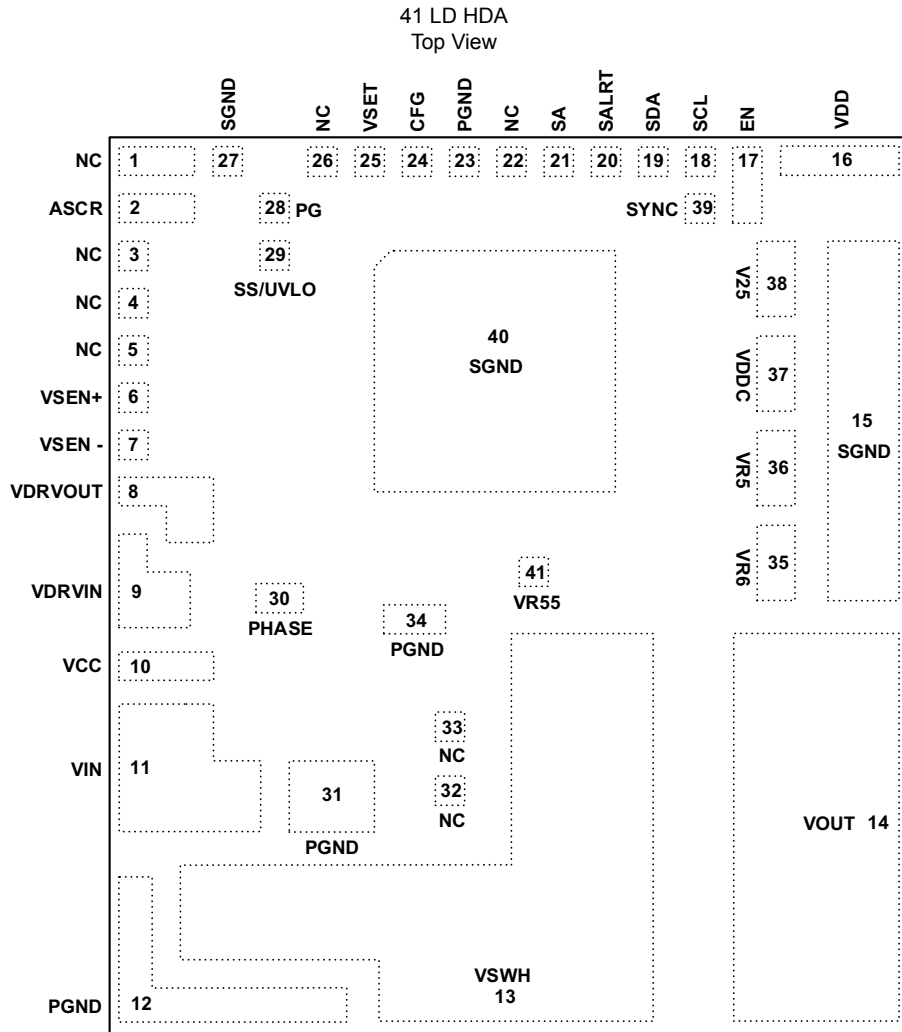
**Table 4. Comparison of Simple Digital and Full Digital Parts**

|                                                                   | ISL8278M                                                     | RAA210833                                                                                                                                                                                                                |
|-------------------------------------------------------------------|--------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>IN</sub> (V)                                               | 4.5 - 14                                                     | 4.5 - 14                                                                                                                                                                                                                 |
| V <sub>OUT</sub> (V)                                              | 0.6 - 5                                                      | 0.6 - 5                                                                                                                                                                                                                  |
| I <sub>OUT</sub> (Max) (A)                                        | 33                                                           | 33                                                                                                                                                                                                                       |
| f <sub>sw</sub> (kHz)                                             | 296 - 1067                                                   | 296 - 1067                                                                                                                                                                                                               |
| <b>Digital PMBus Programmability for Configuration of Modules</b> | All PMBus commands, NVM access to store module configuration | Configuration of modules supported by pin-strap resistors. Digital programmability supports configuration changes during run-time operation with a subset of PMBus commands. No NVM access to store module configuration |
| <b>Power Navigator Support</b>                                    | Yes                                                          | Yes                                                                                                                                                                                                                      |
| <b>SYNC Capability</b>                                            | Yes                                                          | Yes                                                                                                                                                                                                                      |
| <b>Current Sharing Multi-Modules</b>                              | No                                                           | No                                                                                                                                                                                                                       |
| <b>DDC Pin (Inter-Device Communication)</b>                       | Yes                                                          | No                                                                                                                                                                                                                       |

Note: For a full comparison of all the RAA210XXX and ISL827XM product offerings, visit the [simple-digital module family](#) page.



## 1.4 Pin Configuration



## 1.5 Pin Descriptions

| Pin Number | Label   | Type | Description                                                                                                                                                                                                                                                                                                                                 |
|------------|---------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2          | ASCR    | I    | ChargeMode control ASCR parameters selection pin. Used to set ASCR gain and residual values.                                                                                                                                                                                                                                                |
| 6          | VSEN+   | I    | Differential output voltage sense feedback. Connect to the positive output regulation point.                                                                                                                                                                                                                                                |
| 7          | VSEN-   | I    | Differential output voltage sense feedback. Connect to the negative output regulation point.                                                                                                                                                                                                                                                |
| 8          | VDRVOUT | PWR  | Output of internal regulator for powering internal MOSFET driver. Connect a 10µF bypass capacitor to this pin. The regulator output is dedicated to powering internal MOSFET drivers. Do not use this regulator for any other purpose. For applications with $V_{IN}$ less than 5.2V, use an external 5V supply or connect this pad to VIN. |
| 9          | VDRVIN  | PWR  | Input supply to internal regulator for powering internal MOSFET drivers. Connect this pad to VIN.                                                                                                                                                                                                                                           |
| 10         | VCC     | PWR  | Bias pin for internal regulator. Connect the VCC pad to the VR55 pin directly with a short loop trace. Not recommended to power external circuit.                                                                                                                                                                                           |
| 11         | VIN     | PWR  | Main input supply. Refer to <a href="#">"PCB Layout Guidelines" on page 30</a> for the decoupling capacitor's placement from VIN to PGND.                                                                                                                                                                                                   |

| Pin Number                 | Label   | Type | Description                                                                                                                                                                                                                                                                                                                 |
|----------------------------|---------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12, 23, 31, 34             | PGND    | PWR  | Power ground. Refer to <a href="#">"PCB Layout Guidelines" on page 30</a> for the PGND pad connections and decoupling capacitor's placement.                                                                                                                                                                                |
| 13                         | VSWH    | PWR  | Switch node. Refer to <a href="#">"PCB Layout Guidelines" on page 30</a> for connecting VSWH pads to electrically isolate the PCB copper island to dissipate internal heat.                                                                                                                                                 |
| 14                         | VOUT    | PWR  | Power supply output. Range: 0.6V to 5V. Refer to <a href="#">"Derating Curves" on page 17</a> for maximum recommended output current at various output voltages.                                                                                                                                                            |
| 15, 27, 40                 | SGND    | PWR  | Controller signal ground. Refer to <a href="#">"PCB Layout Guidelines" on page 30</a> for the SGND pad connections.                                                                                                                                                                                                         |
| 16                         | VDD     | PWR  | Input supply to digital controller. Connect the VDD pad to the VIN supply.                                                                                                                                                                                                                                                  |
| 17                         | EN      | I    | External enable input. Logic high enables the module.                                                                                                                                                                                                                                                                       |
| 18                         | SCL     | I/O  | Serial clock input. A pull-up resistor is required for this application.                                                                                                                                                                                                                                                    |
| 19                         | SDA     | I/O  | Serial data. A pull-up resistor is required for this application.                                                                                                                                                                                                                                                           |
| 20                         | SALRT   | O    | Serial alert. A pull-up resistor is required for this application.                                                                                                                                                                                                                                                          |
| 21                         | SA      | I    | Serial bus address select pin. Refer to <a href="#">Table 11 on page 25</a> for list of resistor values to set various serial bus address.                                                                                                                                                                                  |
| 24                         | CFG     | I    | Clock source configuration. If the clock source is internal, set the internal FREQUENCY_SWITCH according to the SYNC pin resistor setting. If the clock source is external, the internal FREQUENCY_SWITCH is set according to CFG pin resistor. Refer to <a href="#">Table 8 on page 23</a> for more details.               |
| 25                         | VSET    | I    | Output voltage selection pin. Refer to <a href="#">Table 5 on page 19</a> for list of resistor values to set various output voltages.                                                                                                                                                                                       |
| 28                         | PG      | O    | Power-good output. The power-good is configured as an open-drain output.                                                                                                                                                                                                                                                    |
| 29                         | SS/UVLO | I    | Soft-start/stop and undervoltage lockout selection pin. Used to set turn on/off delay and ramp time as well as input UVLO threshold levels. Refer to <a href="#">Table 6 on page 21</a> and <a href="#">Table 10 on page 24</a> for a list of resistors.                                                                    |
| 30                         | PHASE   | PWR  | Switch node pad for DCR sensing. Electrically shorted inside to VSWH, but for higher current sensing accuracy connect the PHASE pad to the VSWH pad externally. Refer to <a href="#">"PCB Layout Guidelines" on page 30</a> .                                                                                               |
| 35                         | VR6     | PWR  | 6V internal reference supply voltage.                                                                                                                                                                                                                                                                                       |
| 36                         | VR5     | PWR  | 5V internal reference supply voltage.                                                                                                                                                                                                                                                                                       |
| 37                         | VDDC    | PWR  | VDD clean. Noise at the VDD pin is filtered by an internal ferrite bead and capacitor. For VDD > 6V, leave this pin as no connect. For $5.5 \leq VDD \leq 6V$ , connect the VDDC pin to the VR6 pin. For $4.5 \leq VDD < 5.5V$ , connect the VDDC pin to VR6 and the VR5 pin.                                               |
| 38                         | V25     | PWR  | 2.5V internal reference supply voltage.                                                                                                                                                                                                                                                                                     |
| 39                         | SYNC    | I/O  | Clock synchronization input. Sets the frequency of the internal switch clock, or synchronizes to an external clock. If using external synchronization, the external clock must be active before enable. Refer to <a href="#">Table 7 on page 22</a> for a list of resistor values to program various switching frequencies. |
| 41                         | VR55    | PWR  | Internal 5.5V bias for internal regulator use only. Connect the VR55 pin directly to the VCC pin. Not recommended to power external circuit.                                                                                                                                                                                |
| 1, 3, 4, 5, 22, 26, 32, 33 | NC      |      | These are test pins and are not electrically isolated. Leave these pins as no connect.                                                                                                                                                                                                                                      |

## 2. Specifications

### 2.1 Absolute Maximum Ratings

| Parameter                                                                              | Minimum      | Maximum | Unit        |
|----------------------------------------------------------------------------------------|--------------|---------|-------------|
| Input Supply Voltage, VIN Pin                                                          | -0.3         | +17     | V           |
| Input Supply Voltage for Controller, VDD, VDDC Pin                                     | -0.3         | +17     | V           |
| Input Gate Driver Supply Voltage, VDRVIN Pin                                           | -0.3         | +17     | V           |
| Output Gate Driver Supply Voltage, VDRVOUT Pin                                         | -0.3         | +6      | V           |
| Output Voltage, VOUT Pin                                                               | -0.3         | +6      | V           |
| Switch Node Referenced to PGND Pin, VSWH Pin                                           | -0.3         | +25     | V           |
| Switch Node for DCR Sensing Referenced to SGND Pin, PHASE Pin                          | -0.3         | +25     | V           |
| Input Bias Voltage for Internal Regulator, VCC Pin                                     | -0.3         | +6.5    | V           |
| 6V Internal Reference Supply Voltage, VR6 Pin                                          | -0.3         | +6.6    | V           |
| Internal Reference Supply Voltage, VR5, VR55 Pin                                       | -0.3         | +6.5    | V           |
| 2.5V Internal Reference Supply Voltage, V25 Pin                                        | -0.3         | +3      | V           |
| Logic I/O Voltage for DDC, EN, CFG, PG, ASCR, SA, SCL, SDA, SALRT, SYNC, SS/UVLO, VSET | -0.3         | +6      | V           |
| Analog Input Voltages for                                                              |              |         |             |
| V <sub>SEN+</sub> , X <sub>TEMP+</sub>                                                 | -0.3         | 6       | V           |
| V <sub>SEN-</sub> , X <sub>TEMP-</sub>                                                 | -0.3         | 0.3     | V           |
| <b>ESD Rating</b>                                                                      | <b>Value</b> |         | <b>Unit</b> |
| Human Body Model (Tested per JS-001-2017)                                              | 2            |         | kV          |
| Machine Model (Tested per JESD22-A115C)                                                | 200          |         | V           |
| Charged Device Model (Tested per JS-002-2014)                                          | 750          |         | V           |
| Latch-Up (Tested per JESD78E; Class 2, Level A)                                        | 100          |         | mA          |

### 2.2 Thermal Information

| Thermal Resistance (Typical)                       | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|----------------------------------------------------|----------------------|----------------------|
| 41 Ld HDA Package ( <a href="#">Notes 13, 14</a> ) | 7.5                  | 2.2                  |

Notes:

13.  $\theta_{JA}$  is measured in free air with the module mounted on an 8-layer evaluation board 4.7x4.8inch in size with 2oz Cu on all layers and multiple via interconnects as specified in the [RTKA2108332H00000BU evaluation board user guide](#).
14. For  $\theta_{JC}$ , the “case temp” location is the center of the package underside.

| Parameter                                      | Minimum                                       | Maximum | Unit |
|------------------------------------------------|-----------------------------------------------|---------|------|
| Maximum Junction Temperature (Plastic Package) |                                               | +125    | °C   |
| Storage Temperature Range                      | -55                                           | +150    | °C   |
| Pb-Free Reflow Profile                         | Refer to <a href="#">Figure 29 on page 32</a> |         |      |

## 2.3 Recommended Operating Conditions

| Parameter                                           | Minimum | Maximum | Unit |
|-----------------------------------------------------|---------|---------|------|
| Input Supply Voltage Range, $V_{IN}$                | 4.5     | 14      | V    |
| Input Supply Voltage Range for Controller, $V_{DD}$ | 4.5     | 14      | V    |
| Output Voltage Range, $V_{OUT}$                     | 0.6     | 5       | V    |
| Output Current Range, $I_{OUT(DC)}$ (Note 17)       | 0       | 33      | A    |
| Operating Junction Temperature Range, $T_J$         | -40     | +125    | °C   |

## 2.4 Electrical Specifications

$V_{IN} = V_{DD} = 12V$ ,  $f_{SW} = 533kHz$ ,  $C_{OUT} = 1340\mu F$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .  
**Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ .**

| Parameter                                                           | Symbol               | Test Conditions                                                                  | Min<br>(Note 15) | Typ         | Max<br>(Note 15) | Unit |
|---------------------------------------------------------------------|----------------------|----------------------------------------------------------------------------------|------------------|-------------|------------------|------|
| <b>Input and Supply Characteristics</b>                             |                      |                                                                                  |                  |             |                  |      |
| Input Supply Current for Controller                                 | $I_{DD}$             | $V_{IN} = V_{DD} = 12V$ , $V_{OUT} = 0V$ ,<br>module not enabled                 |                  | 40          | <b>50</b>        | mA   |
| 6V Internal Reference Supply Voltage                                | $V_{R6}$             |                                                                                  | <b>5.5</b>       | 6.1         | <b>6.6</b>       | V    |
| Internal Regulator Output Voltage                                   | $V_{DRVOUT}$         | $V_{CC}$ connected to $V_{R55}$                                                  |                  | 5.2         |                  | V    |
| 5V Internal Reference Supply Voltage                                | $V_{R5}$             | $I_{VR5} < 5mA$                                                                  | <b>4.5</b>       | 5.2         | <b>5.5</b>       | V    |
| 2.5V Internal Reference Supply Voltage                              | $V_{25}$             |                                                                                  | <b>2.25</b>      | 2.50        | <b>2.75</b>      | V    |
| 5.5V Internal Reference Supply Voltage                              | $V_{R55}$            | $V_{DD} > 6V$ ; 0A to 80mA                                                       |                  | 5.7         |                  | V    |
| Input Supply Voltage for Controller Read Back Resolution            | $V_{DD\_READ\_RES}$  |                                                                                  |                  | $\pm 20$    |                  | mV   |
| Input Supply Voltage for Controller Read Back Total Error (Note 18) | $V_{DD\_READ\_ERR}$  | PMBus read                                                                       |                  | $\pm 2$     |                  | %FS  |
| <b>Output Characteristics</b>                                       |                      |                                                                                  |                  |             |                  |      |
| Output Voltage Adjustment Range                                     | $V_{OUT\_RANGE}$     | $V_{IN} > V_{OUT} + 1.8V$                                                        | <b>0.54</b>      |             | <b>5.5</b>       | V    |
| Output Voltage Set-Point Range                                      | $V_{OUT\_RES}$       | Configured using PMBus                                                           |                  | $\pm 0.025$ |                  | %    |
| Output Voltage Set-Point Accuracy (Notes 16, 18)                    | $V_{OUT\_ACCY}$      | Includes line, load, and temperature ( $-20^\circ C \leq T_A \leq +85^\circ C$ ) | <b>-1.2</b>      |             | <b>+1.2</b>      | %FS  |
| Output Voltage Readback Resolution                                  | $V_{OUT\_READ\_RES}$ |                                                                                  |                  | $\pm 20$    |                  | mV   |
| Output Voltage Readback Total Error (Note 18)                       | $V_{OUT\_READ\_ERR}$ | PMBus read                                                                       | <b>-2</b>        |             | <b>+2</b>        | %FS  |
| Output Current Readback Resolution                                  | $I_{OUT\_READ\_RES}$ |                                                                                  |                  | 10          |                  | Bits |
| Output Current Range (Note 17)                                      | $I_{OUT\_RANGE}$     |                                                                                  |                  |             | <b>33</b>        | A    |
| Output Current Readback Total Error                                 | $I_{OUT\_READ\_ERR}$ | PMBus read at max load at ambient room temperature                               |                  | $\pm 3$     |                  | A    |
| <b>Soft-Start and Sequencing</b>                                    |                      |                                                                                  |                  |             |                  |      |
| Delay Time From Enable to $V_{OUT}$ Rise                            | $t_{ON\_DELAY}$      | Configured using pin-strap resistor or PMBus                                     | <b>2</b>         |             | <b>300</b>       | ms   |

$V_{IN} = V_{DD} = 12V$ ,  $f_{SW} = 533kHz$ ,  $C_{OUT} = 1340\mu F$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ . **Boldface limits apply across the operating temperature range,  $-40^{\circ}C$  to  $+85^{\circ}C$ . (Continued)**

| Parameter                                                               | Symbol                  | Test Conditions                              | Min<br>( <a href="#">Note 15</a> ) | Typ                   | Max<br>( <a href="#">Note 15</a> ) | Unit        |
|-------------------------------------------------------------------------|-------------------------|----------------------------------------------|------------------------------------|-----------------------|------------------------------------|-------------|
| $t_{ON\_DELAY}$ Accuracy                                                | $t_{ON\_DELAY\_ACCY}$   |                                              |                                    | $\pm 2$               |                                    | ms          |
| Output Voltage Ramp-Up Time                                             | $t_{ON\_RISE}$          | Configured using pin-strap resistor or PMBus | <b>0.5</b>                         |                       | <b>120</b>                         | ms          |
| Output Voltage Ramp-Up Time Accuracy                                    | $t_{ON\_RISE\_ACCY}$    |                                              |                                    | $\pm 250$             |                                    | $\mu s$     |
| Delay Time From Disable to $V_{OUT}$ Fall                               | $t_{OFF\_DELAY}$        | Configured using pin-strap resistor or PMBus | <b>2</b>                           |                       | <b>300</b>                         | ms          |
| $t_{OFF\_DELAY}$ Accuracy                                               | $t_{OFF\_DELAY\_ACCY}$  |                                              |                                    | $\pm 2$               |                                    | ms          |
| Output Voltage Fall Time                                                | $t_{OFF\_FALL}$         | Configured using pin-strap resistor or PMBus | <b>0.5</b>                         |                       | <b>120</b>                         | ms          |
| Output Voltage Fall Time Accuracy                                       | $t_{ON\_FALL\_ACCY}$    |                                              |                                    | $\pm 250$             |                                    | $\mu s$     |
| <b>Power-Good</b>                                                       |                         |                                              |                                    |                       |                                    |             |
| Power-Good Delay                                                        | $V_{PG\_DELAY}$         |                                              |                                    | 4                     |                                    | ms          |
| <b>Temperature Sense</b>                                                |                         |                                              |                                    |                       |                                    |             |
| Temperature Sense Range                                                 | $T_{SENSE\_RANGE}$      | Configured using PMBus                       | <b>-50</b>                         |                       | <b>150</b>                         | $^{\circ}C$ |
| Internal Temperature Sensor Accuracy                                    | $INT\_TEMP\_ACCY$       | Tested at $+100^{\circ}C$                    | <b>-5</b>                          |                       | <b>+5</b>                          | $^{\circ}C$ |
| <b>Fault Protection</b>                                                 |                         |                                              |                                    |                       |                                    |             |
| $V_{DD}$ Undervoltage Threshold Range                                   | $V_{DD\_UVLO\_RANGE}$   | Measured internally                          | <b>4.18</b>                        |                       | <b>16</b>                          | V           |
| $V_{DD}$ Undervoltage Threshold Accuracy ( <a href="#">Note 18</a> )    | $V_{DD\_UVLO\_ACCY}$    |                                              |                                    | $\pm 2$               |                                    | %FS         |
| $V_{DD}$ Undervoltage Response Time                                     | $V_{DD\_UVLO\_DELAY}$   |                                              |                                    | 10                    |                                    | $\mu s$     |
| $V_{OUT}$ Overvoltage Threshold Range                                   | $V_{OUT\_OV\_RANGE}$    | Factory default                              |                                    | $1.15 \times V_{OUT}$ |                                    | %           |
|                                                                         |                         | Configured using pin-strap resistor or PMBus | <b><math>1.05V_{OUT}</math></b>    |                       | <b><math>V_{OUT\_MAX}</math></b>   | %           |
| $V_{OUT}$ Undervoltage Threshold Range                                  | $V_{OUT\_UV\_RANGE}$    | Factory default                              |                                    | $0.85 \times V_{OUT}$ |                                    | %           |
|                                                                         |                         | Configured using pin-strap resistor or PMBus | <b>0</b>                           |                       | <b><math>0.95V_{OUT}</math></b>    | %           |
| $V_{OUT}$ OV/UV Threshold Accuracy ( <a href="#">Note 16</a> )          | $V_{OUT\_OV/UV\_ACCY}$  |                                              | <b>-2</b>                          |                       | <b>+2</b>                          | %           |
| $V_{OUT}$ OV/UV Response Time                                           | $V_{OUT\_OV/UV\_DELAY}$ |                                              |                                    | 10                    |                                    | $\mu s$     |
| Output Current Limit Set-Point Accuracy ( <a href="#">Note 18</a> )     | $I_{LIMIT\_ACCY}$       | Tested at $I_{OUT\_OC\_FAULT\_LIMIT} = 40A$  |                                    | $\pm 10$              |                                    | %FS         |
| Output Current Fault Response Time ( <a href="#">Note 19</a> )          | $I_{LIMIT\_DELAY}$      | Factory default                              |                                    | 3                     |                                    | $t_{SW}$    |
| Over-Temperature Protection Threshold (Controller Junction Temperature) | $T_{JUNCTION}$          | Factory default                              |                                    | 115                   |                                    | $^{\circ}C$ |
|                                                                         |                         | Configured using PMBus                       | <b>-40</b>                         |                       | <b>125</b>                         | $^{\circ}C$ |
| Thermal Protection Hysteresis                                           | $T_{JUNCTION\_HYS}$     |                                              |                                    | 15                    |                                    | $^{\circ}C$ |
| <b>Oscillator and Switching Characteristics</b>                         |                         |                                              |                                    |                       |                                    |             |
| Switching Frequency Range                                               | $f_{SW\_RANGE}$         | Configured using pin-strap resistor or PMBus | <b>296</b>                         |                       | <b>1067</b>                        | kHz         |
| Switching Frequency Set-Point Accuracy                                  | $f_{SW\_ACCY}$          |                                              | <b>-5</b>                          |                       | <b>+5</b>                          | %           |

$V_{IN} = V_{DD} = 12V$ ,  $f_{SW} = 533kHz$ ,  $C_{OUT} = 1340\mu F$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .  
**Boldface limits apply across the operating temperature range,  $-40^\circ C$  to  $+85^\circ C$ . (Continued)**

| Parameter                                             | Symbol                      | Test Conditions                                                | Min<br>(Note 15) | Typ | Max<br>(Note 15) | Unit |
|-------------------------------------------------------|-----------------------------|----------------------------------------------------------------|------------------|-----|------------------|------|
| Minimum Pulse Width Required from External SYNC Clock | EXT_SYNC <sub>PW</sub>      | Measured at 50% amplitude                                      | <b>150</b>       |     |                  | ns   |
| Drift Tolerance for External SYNC Clock               | EXT_SYNC <sub>DRIFT</sub>   | External SYNC clock equal to 500kHz is not supported           | <b>-10</b>       |     | <b>+10</b>       | %    |
| <b>Logic Input/Output Characteristics</b>             |                             |                                                                |                  |     |                  |      |
| Bias Current at the Logic Input Pins                  | I <sub>LOGIC_BIAS</sub>     | EN, CFG, PG, SA, SCL, SDA, SALRT, SYNC, UVLO, V <sub>SET</sub> | <b>-100</b>      |     | <b>+100</b>      | nA   |
| Logic Input Low Threshold Voltage                     | V <sub>LOGIC_IN_LOW</sub>   |                                                                |                  |     | <b>0.8</b>       | V    |
| Logic Input High Threshold Voltage                    | V <sub>LOGIC_IN_HIGH</sub>  |                                                                | <b>2.0</b>       |     |                  | V    |
| Logic Output Low Threshold Voltage                    | V <sub>LOGIC_OUT_LOW</sub>  | 2mA sinking                                                    |                  |     | <b>0.5</b>       | V    |
| Logic Output High Threshold Voltage                   | V <sub>LOGIC_OUT_HIGH</sub> | 2mA sourcing                                                   | <b>2.25</b>      |     |                  | V    |
| <b>PMBus Interface Timing Characteristic</b>          |                             |                                                                |                  |     |                  |      |
| PMBus Operating Frequency                             | f <sub>SMB</sub>            |                                                                | <b>100</b>       |     | <b>400</b>       | kHz  |

Notes:

- 15. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
- 16. V<sub>OUT</sub> measured at the termination of the V<sub>SEN+</sub> and V<sub>SEN-</sub> sense points.
- 17. The MAX load current is determined by the thermal ["Derating Curves" on page 17](#).
- 18. "FS" stands for Full Scale of recommended maximum operation range.
- 19. "t<sub>SW</sub>" stands for time period of operation switching frequency.

### 3. Typical Performance Curves

#### 3.1 Efficiency Performance

Operating condition:  $T_A = +25^\circ\text{C}$ , No air flow.  $C_{OUT} = 1340\mu\text{F}$ . Typical values are used unless otherwise noted.

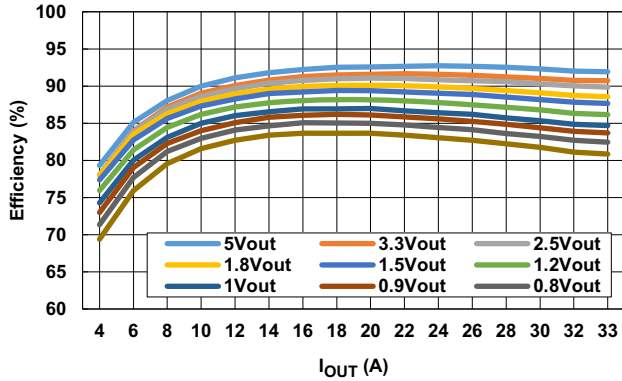


Figure 5. Efficiency vs Output Current at  $V_{IN} = 12\text{V}$  and  $f_{SW} = 364\text{kHz}$  for Various Output Voltages

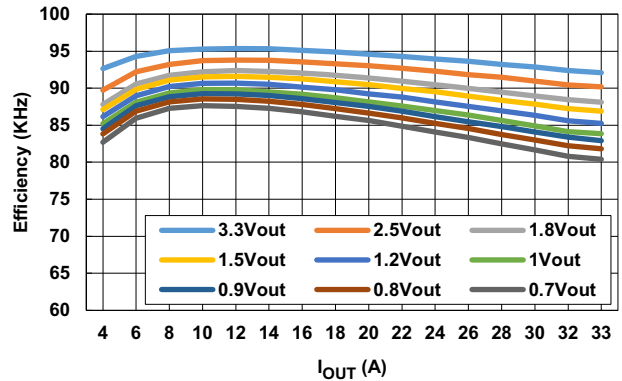


Figure 6. Efficiency vs Output Current at  $V_{IN} = 5\text{V}$  and  $f_{SW} = 364\text{kHz}$  for Various Output Voltages

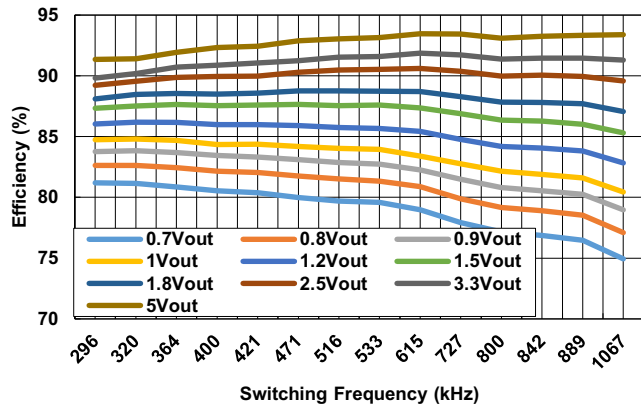


Figure 7. Efficiency vs Switching Frequency at  $V_{IN} = 12\text{V}$  and  $I_{OUT} = 33\text{A}$  for Various Output Voltages

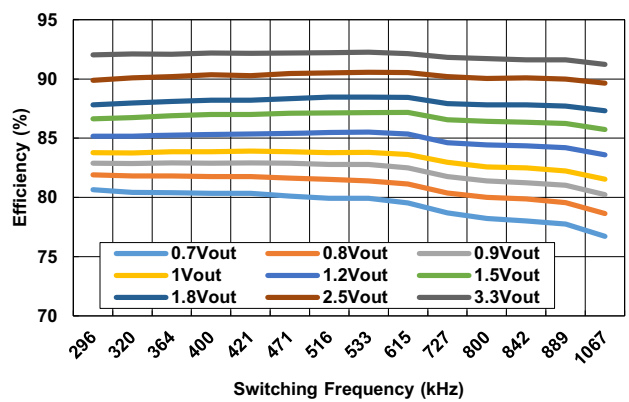


Figure 8. Efficiency vs Switching Frequency at  $V_{IN} = 5\text{V}$  and  $I_{OUT} = 33\text{A}$  for Various Output Voltages

### 3.2 Transient Response Performance

Operating conditions: Step load = 0 to 16.5A,  $I_{OUT}$  slew rate = 15A/ $\mu$ s,  $T_A$  = +25°C, OLFM airflow. Typical values are used unless otherwise noted.

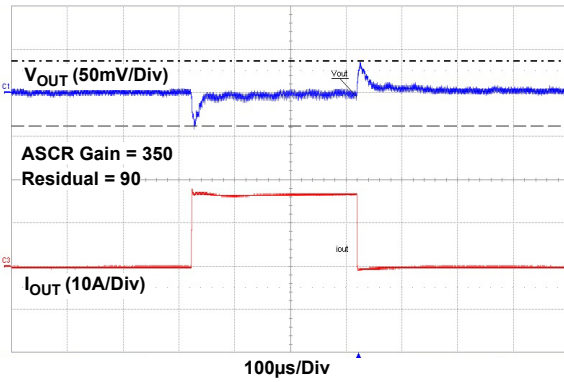


Figure 9.  $5V_{IN}$  to  $0.9V_{OUT}$ ,  $f_{SW}$  = 364kHz,  $C_{OUT}$  = 12x100 $\mu$ F Ceramic + 5x470 $\mu$ F POSCAP

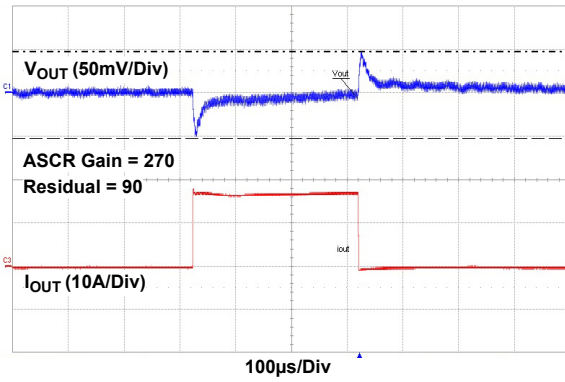


Figure 10.  $5V_{IN}$  to  $1.2V_{OUT}$ ,  $f_{SW}$  = 364kHz,  $C_{OUT}$  = 10x100 $\mu$ F Ceramic + 4x470 $\mu$ F POSCAP

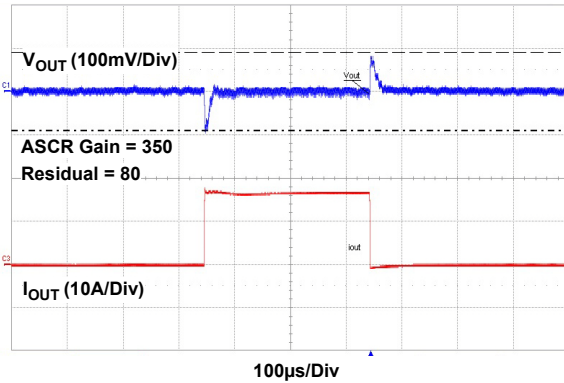


Figure 11.  $12V_{IN}$  to  $1V_{OUT}$ ,  $f_{SW}$  = 615kHz,  $C_{OUT}$  = 4x100 $\mu$ F Ceramic + 4x470 $\mu$ F POSCAP

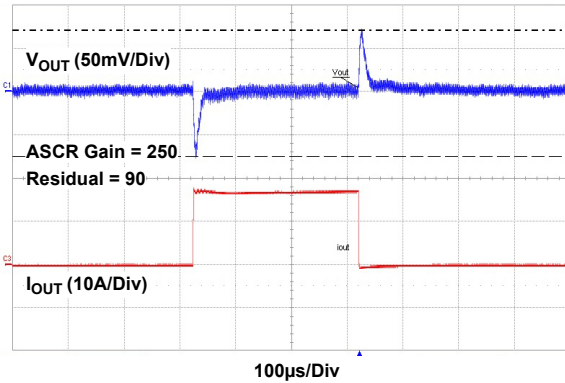


Figure 12.  $12V_{IN}$  to  $1.5V_{OUT}$ ,  $f_{SW}$  = 471kHz,  $C_{OUT}$  = 7x100 $\mu$ F Ceramic + 2x470 $\mu$ F POSCAP

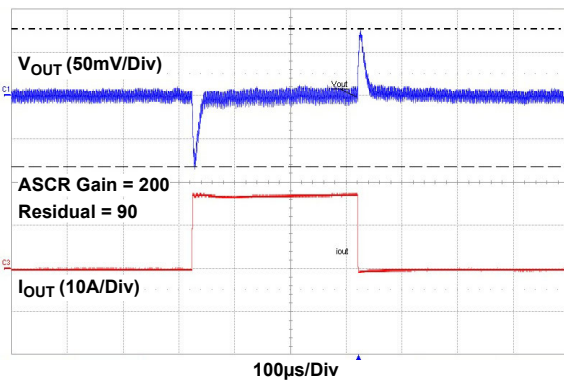


Figure 13.  $12V_{IN}$  to  $1.8V_{OUT}$ ,  $f_{SW}$  = 471kHz,  $C_{OUT}$  = 6x100 $\mu$ F Ceramic + 2x470 $\mu$ F POSCAP

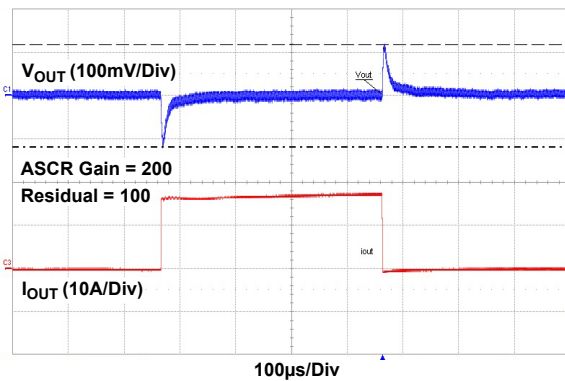


Figure 14.  $12V_{IN}$  to  $3.3V_{OUT}$ ,  $f_{SW}$  = 615kHz,  $C_{OUT}$  = 4x100 $\mu$ F Ceramic + 1x470 $\mu$ F POSCAP



### 3.3 Derating Curves

All of the following curves were plotted at  $T_J = +120^\circ\text{C}$

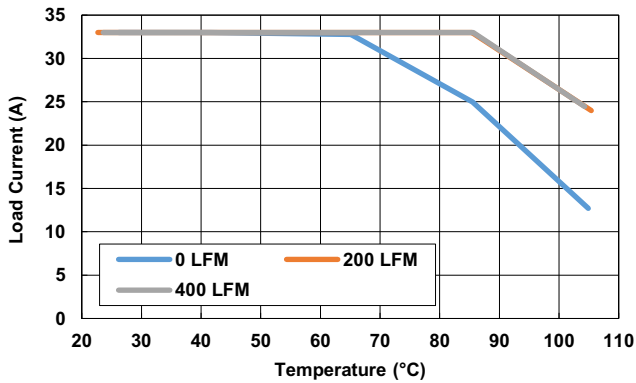


Figure 15. 5V<sub>IN</sub> to 1V<sub>OUT</sub>, 364kHz

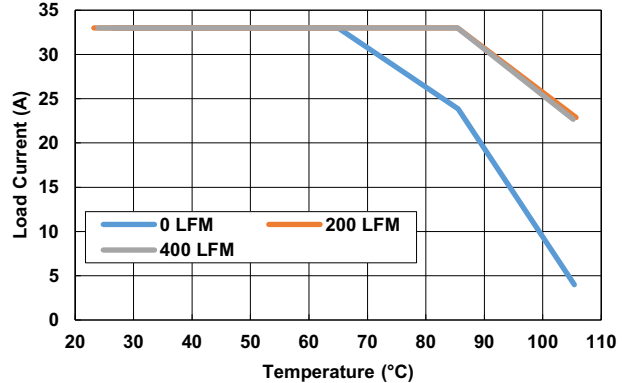


Figure 16. 12V<sub>IN</sub> to 1V<sub>OUT</sub>, 364kHz

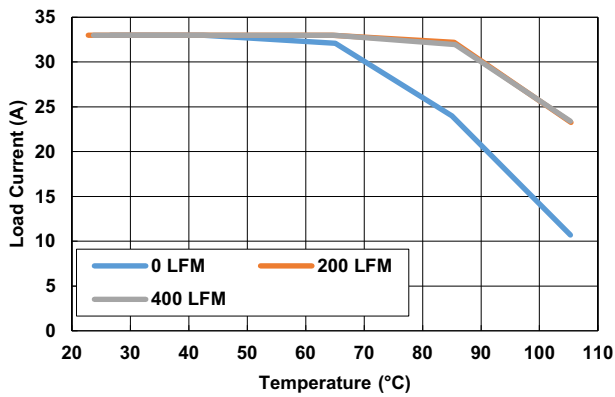


Figure 17. 5V<sub>IN</sub> to 1.2V<sub>OUT</sub>, 364kHz

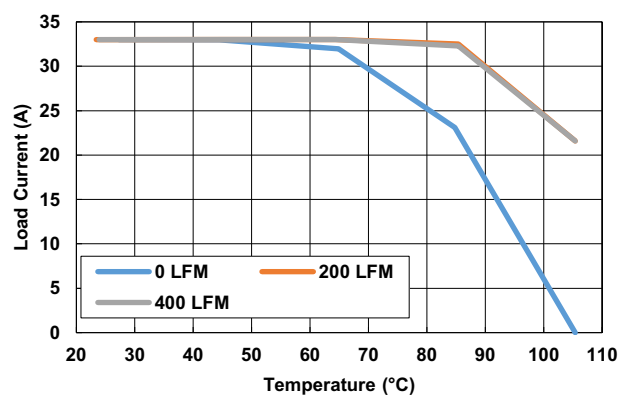


Figure 18. 12V<sub>IN</sub> to 1.2V<sub>OUT</sub>, 364kHz

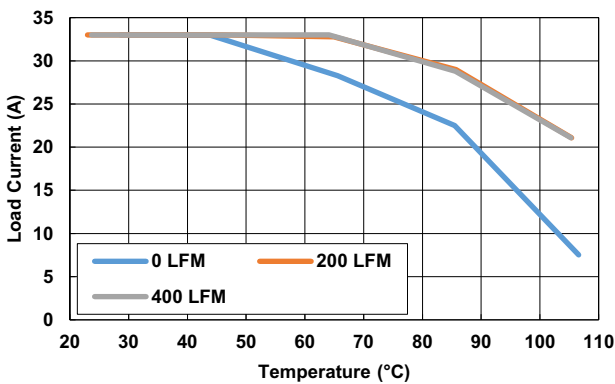


Figure 19. 5V<sub>IN</sub> to 1.8V<sub>OUT</sub>, 471kHz

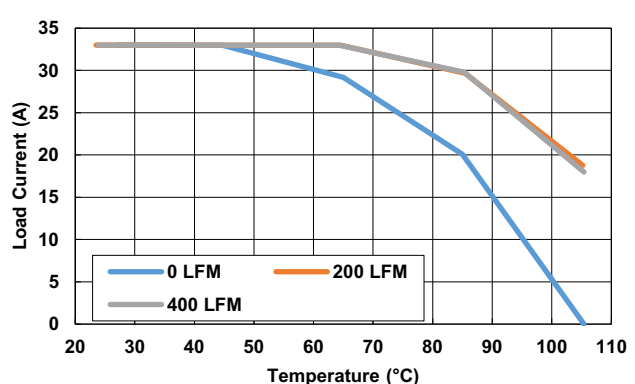


Figure 20. 12V<sub>IN</sub> to 1.8V<sub>OUT</sub>, 471kHz

All of the following curves were plotted at  $T_J = +120^\circ\text{C}$  (Continued)

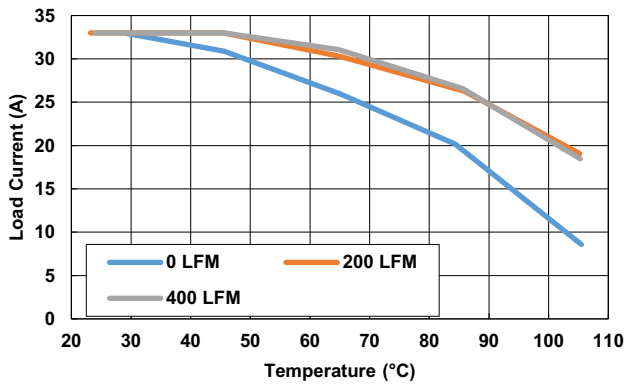


Figure 21.  $5V_{IN}$  to  $2.5V_{OUT}$ , 615kHz

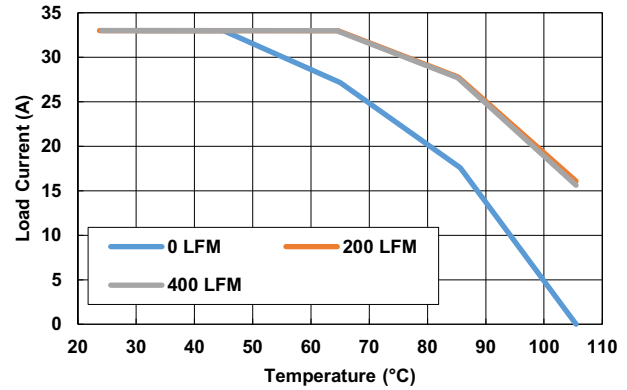


Figure 22.  $12V_{IN}$  to  $2.5V_{OUT}$ , 615kHz

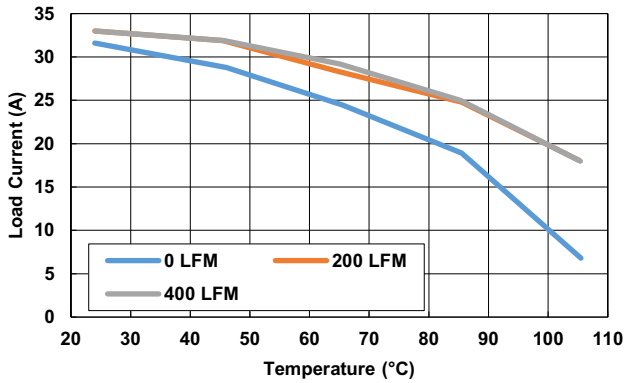


Figure 23.  $5V_{IN}$  to  $3.3V_{OUT}$ , 615kHz

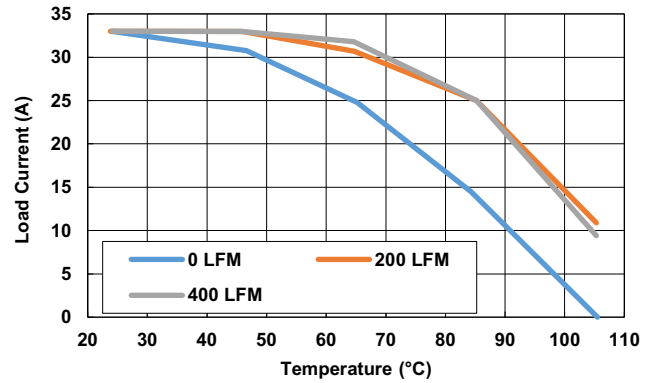


Figure 24.  $12V_{IN}$  to  $3.3V_{OUT}$ , 615kHz

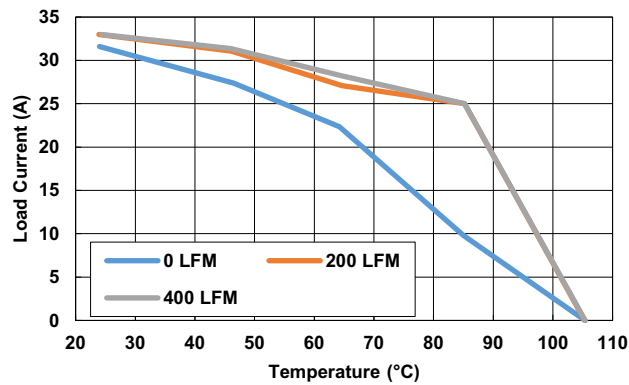


Figure 25.  $12V_{IN}$  to  $5V_{OUT}$ , 727kHz

## 4. Functional Description

### 4.1 SMBus Communications

The RAA210833 provides an SMBus digital interface that enables you to configure the module operation and monitor the input and output parameters. You can use the RAA210833 with any SMBus host device. In addition, the module is compatible with PMBus Power System Management Protocol Specification Parts I and II version 1.2. The RAA210833 accepts most standard PMBus commands. When controlling the device with PMBus commands, it is recommended that the enable pin be tied to SGND.

The SMBus device address is the only parameter that must be set by external pins.

### 4.2 Output Voltage Selection

The output voltage can be set to a voltage between 0.6V and 5V if the input voltage is higher than the output voltage by an amount sufficient to maintain regulation.

The VSET pin sets the output voltage to any values between 0.6V and 5V as shown in [Table 5](#). The R<sub>SET</sub> resistor is placed between the VSET pin and SGND. A standard 1% resistor is recommended.

**Table 5. Output Voltage Resistor Settings**

| V <sub>OUT</sub> (V) | VSET_GROUP (Set by SA Pin) | R <sub>SET</sub> (kΩ) |
|----------------------|----------------------------|-----------------------|
| 0.600                | Group 0                    | 10                    |
| 0.650                | Group 0                    | 11                    |
| 0.675                | Group 0                    | 12.1                  |
| 0.690                | Group 0                    | 13.3                  |
| 0.700                | Group 0                    | 14.7                  |
| 0.710                | Group 0                    | 16.2                  |
| 0.720                | Group 0                    | 17.8                  |
| 0.730                | Group 0                    | 19.6                  |
| 0.740                | Group 0                    | 21.5                  |
| 0.750                | Group 0                    | 23.7                  |
| 0.760                | Group 0                    | 26.1                  |
| 0.770                | Group 0                    | 28.7                  |
| 0.780                | Group 0                    | 31.6                  |
| 0.790                | Group 0                    | 34.8                  |
| 0.800                | Group 0                    | 38.3                  |
| 0.810                | Group 0                    | 42.2                  |
| 0.820                | Group 0                    | 46.4                  |
| 0.830                | Group 0                    | 51.1                  |
| 0.840                | Group 0                    | 56.2                  |
| 0.850                | Group 0                    | 61.9                  |
| 0.860                | Group 0                    | 68.1                  |
| 0.870                | Group 0                    | 75                    |
| 0.880                | Group 0                    | 82.5                  |
| 0.890                | Group 0                    | 90.9                  |
| 0.900                | Group 0                    | 100                   |
| 0.910                | Group 0                    | 110                   |

Table 5. Output Voltage Resistor Settings (Continued)

| V <sub>OUT</sub> (V) | VSET_GROUP (Set by SA Pin) | R <sub>SET</sub> (kΩ) |
|----------------------|----------------------------|-----------------------|
| 0.920                | Group 0                    | 121                   |
| 0.930                | Group 0                    | 133                   |
| 0.940                | Group 0                    | 147                   |
| 0.950                | Group 0                    | 162                   |
| 0.960                | Group 0                    | 178                   |
| 0.970                | Group 0                    | Connect to SGND       |
| 0.980                | Group 0                    | OPEN                  |
| 0.990                | Group 0                    | Connect to V25        |
| 1.000                | Group 1                    | Connect to SGND       |
| 1.030                | Group 1                    | 10                    |
| 1.050                | Group 1                    | 11                    |
| 1.100                | Group 1                    | 12.1                  |
| 1.120                | Group 1                    | 13.3                  |
| 1.150                | Group 1                    | 14.7                  |
| 1.200                | Group 1                    | OPEN                  |
| 1.250                | Group 1                    | 16.2                  |
| 1.300                | Group 1                    | 17.8                  |
| 1.350                | Group 1                    | 19.6                  |
| 1.400                | Group 1                    | 21.5                  |
| 1.500                | Group 1                    | 23.7                  |
| 1.600                | Group 1                    | 26.1                  |
| 1.650                | Group 1                    | 28.7                  |
| 1.700                | Group 1                    | 31.6                  |
| 1.800                | Group 1                    | 34.8                  |
| 1.850                | Group 1                    | 38.3                  |
| 1.900                | Group 1                    | 42.2                  |
| 2.000                | Group 1                    | 46.4                  |
| 2.100                | Group 1                    | 51.1                  |
| 2.200                | Group 1                    | 56.2                  |
| 2.300                | Group 1                    | 61.9                  |
| 2.400                | Group 1                    | 68.1                  |
| 2.500                | Group 1                    | Connect to V25        |
| 2.600                | Group 1                    | 75                    |
| 2.700                | Group 1                    | 82.5                  |
| 2.800                | Group 1                    | 90.9                  |
| 2.900                | Group 1                    | 100                   |
| 3.000                | Group 1                    | 110                   |
| 3.200                | Group 1                    | 121                   |
| 3.300                | Group 1                    | 133                   |
| 3.400                | Group 1                    | 147                   |
| 3.600                | Group 1                    | 162                   |

**Table 5. Output Voltage Resistor Settings (Continued)**

| V <sub>OUT</sub> (V) | VSET_GROUP (Set by SA Pin) | R <sub>SET</sub> (kΩ) |
|----------------------|----------------------------|-----------------------|
| 5.000                | Group 1                    | 178                   |

By default, V<sub>OUT\_MAX</sub> is set 110% higher than V<sub>OUT</sub> by the pin-strap resistor, which can be changed to any value up to 5.5V with the PMBus Command VOUT\_MAX.

### 4.3 Soft-Start Delay and Ramp Times

The RAA210833 follows an internal start-up procedure after power is applied to the VDD pin. The module requires approximately 60ms to 70ms to check for specific values stored in its internal memory and programmed by pin-strap resistors. After this process is complete, the device is ready to accept commands through the PMBus interface and the module is ready to be enabled. If the module is to be synchronized to an external clock source, the clock frequency must be stable before asserting the EN pin.

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, you may want to precisely set the time required for V<sub>OUT</sub> to ramp to its target value after the delay period has expired. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The RAA210833 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay (TON\_DELAY) and ramp-up time (TON\_RISE) can be set to custom values with pin-strap resistors or PMBUS. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. It is generally recommended to set the soft-start ramp to a value greater than 500μs to prevent inadvertent fault conditions due to excessive inrush current.

Similar to the soft-start delay and ramp-up time, the delay (TOFF\_DELAY) and ramp-down time (TOFF\_FALL) for soft-stop/off can be set to custom values with pin-strap resistors or PMBUS. In addition, the module can be configured as “immediate off” with the command ON\_OFF\_CONFIG, so that the internal MOSFETs are turned off immediately after the delay time expires.

Use the SS/UVLO pin to set the soft-start/stop delay time and ramp time to some typical values as shown in [Table 6](#). A standard 1% resistor is required.

**Table 6. Soft-Start/Stop and Input UVLO Resistor Settings**

| Resistor (kΩ)   | UVLO (V) | Delay Time (ms) | Ramp Time (ms) |
|-----------------|----------|-----------------|----------------|
| Open            | 4.2      | 5               | 5              |
| Connect to V25  | 4.5      | 10              | 10             |
| Connect to SGND | 4.5      | 5               | 2              |
| 12.1            | 4.5      | 5               | 2              |
| 13.3            | 4.5      | 5               | 5              |
| 14.7            | 4.5      | 5               | 10             |
| 16.2            | 4.5      | 10              | 2              |
| 17.8            | 4.5      | 10              | 5              |
| 19.6            | 4.5      | 10              | 10             |
| 21.5            | 4.5      | 20              | 5              |
| 23.7            | 4.5      | 20              | 10             |
| 26.1            | 4.2      | 5               | 2              |
| 28.7            | 4.59     | 5               | 5              |
| 31.6            | 5.06     | 5               | 10             |

**Table 6. Soft-Start/Stop and Input UVLO Resistor Settings (Continued)**

| Resistor (kΩ) | UVLO (V) | Delay Time (ms) | Ramp Time (ms) |
|---------------|----------|-----------------|----------------|
| 34.8          | 5.57     | 10              | 2              |
| 38.3          | 6.13     | 10              | 5              |
| 42.2          | 6.75     | 10              | 10             |
| 46.4          | 7.42     | 20              | 5              |
| 51.1          | 8.18     | 20              | 10             |
| 56.2          | 10.8     | 5               | 2              |
| 61.9          | 10.8     | 5               | 5              |
| 68.1          | 10.8     | 5               | 10             |
| 75            | 10.8     | 10              | 2              |
| 82.5          | 10.8     | 10              | 5              |
| 90.9          | 10.8     | 10              | 10             |
| 100           | 10.8     | 20              | 5              |
| 110           | 10.8     | 20              | 10             |

#### 4.4 Power-Good

The RAA210833 provides a Power-Good (PG) signal that indicates that the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. These limits and the polarity of the pin can be changed with PMBus command POWER\_GOOD\_ON.

A PG delay period is defined as the time from when all conditions within the RAA210833 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. A fixed PG delay of 4ms is programmed for the RAA210833.

#### 4.5 Switching Frequency and PLL

Set the device’s switching frequency from 296kHz to 1067kHz using the pin-strap method as shown in [Table 7](#), or by using the PMBus command FREQUENCY\_SWITCH.

**Table 7. Switching Frequency Resistor Settings**

| f <sub>sw</sub> (kHz) | R <sub>SET</sub> (kΩ)    |
|-----------------------|--------------------------|
| 296                   | 14.7, or connect to SGND |
| 320                   | 16.2                     |
| 348                   | 17.8                     |
| 364                   | 19.6                     |
| 400                   | 21.5                     |
| 421                   | 23.7                     |
| 471                   | 26.1                     |
| 516                   | 28.7                     |
| 533                   | 31.6, or OPEN            |
| 615                   | 34.8                     |
| 640                   | 38.3                     |
| 696                   | 42.2                     |
| 727                   | 46.4                     |
| 800                   | 51.1                     |

**Table 7. Switching Frequency Resistor Settings (Continued)**

| $f_{sw}(kHz)$ | $R_{SET} (k\Omega)$     |
|---------------|-------------------------|
| 842           | 56.2                    |
| 889           | 61.9                    |
| 1067          | 68.1, or connect to V25 |

The RAA210833 incorporates an internal Phase-Locked Loop (PLL) to clock the internal circuitry. The PLL can also be driven by an external clock source connected to the SYNC pin. Connect a resistor to the CFG pin to set this configuration. If the clock source is set to internal, the internal frequency is set according to the SYNC pin resistor settings. If the clock source is set to external, the internal frequency is set according to the resistor connected to the CFG pin as shown in [Table 8](#). The external clock frequency should be within  $\pm 10\%$  of the listed options.

**Table 8. External Frequency SYNC Settings**

| Clock Source | Internal Frequency Switch (kHz) | $R_{SET} (k\Omega)$      |
|--------------|---------------------------------|--------------------------|
| Internal     | Determined by SYNC resistor     | 10, or OPEN              |
| External     | 296                             | 11                       |
| External     | 340                             | 12.1                     |
| External     | 390                             | 13.3                     |
| External     | 444                             | 14.7                     |
| External     | 516                             | 16.2, or connect to SGND |
| External     | 593                             | 17.8                     |
| External     | 696                             | 19.6                     |
| External     | 800                             | 21.5                     |
| External     | 941                             | 23.7                     |
| External     | 1067                            | 26.1, or Connect to V25  |

The external clock signal must not vary more than 10% from its initial value, should be stable, and should have a minimum pulse-width of 150ns. Note: if the pin-strap method is used, a standard 1% resistor is required.

## 4.6 Loop Compensation

The module loop response is programmable using the pin-strap method or the PMBus command ASCR\_CONFIG according to [Table 9](#). A standard 1% resistor is required. The RAA210833 uses the ChargeMode control algorithm that responds to output current changes within a single PWM switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers.

**Table 9. ASCR Resistor Settings**

| ASCR Gain | ASCR Residual | $R_{SET} (k\Omega)$ |
|-----------|---------------|---------------------|
| 190       | 60            | 10                  |
| 200       | 60            | 11                  |
| 90        | 65            | 12.1                |
| 80        | 70            | 13.3                |
| 120       | 70            | Connect to SGND     |
| 160       | 70            | 14.7                |
| 200       | 70            | OPEN                |
| 250       | 70            | 16.2                |
| 300       | 70            | 17.8                |

**Table 9. ASCR Resistor Settings (Continued)**

| ASCR Gain | ASCR Residual | R <sub>SET</sub> (kΩ) |
|-----------|---------------|-----------------------|
| 120       | 80            | 19.6                  |
| 190       | 80            | 21.5                  |
| 210       | 80            | 23.7                  |
| 250       | 80            | 26.1                  |
| 300       | 80            | 28.7                  |
| 350       | 80            | 31.6                  |
| 400       | 80            | 34.8                  |
| 110       | 90            | 38.3                  |
| 160       | 90            | 42.2                  |
| 200       | 90            | 46.4                  |
| 250       | 90            | 51.1                  |
| 350       | 90            | 56.2                  |
| 400       | 90            | 61.9                  |
| 500       | 90            | 68.1                  |
| 600       | 90            | 75                    |
| 300       | 95            | 82.5                  |
| 120       | 100           | 90.9                  |
| 160       | 100           | 100                   |
| 190       | 100           | 110                   |
| 220       | 100           | 121                   |
| 250       | 100           | Connect to V25        |
| 350       | 100           | 133                   |
| 400       | 100           | 147                   |
| 500       | 100           | 162                   |
| 600       | 100           | 178                   |

#### 4.7 Input Undervoltage Lockout (UVLO)

The Input Undervoltage Lockout (UVLO) prevents the RAA210833 from operating when the input falls below a preset threshold, indicating that the input supply is out of its specified range. The UVLO threshold ( $V_{UVLO}$ ) can be set between 4.18V and 16V or by using the pin-strap method as shown in [Table 10](#), or by using the PMBus command VIN\_UV\_FAULT\_LIMIT. A standard 1% resistor is required.

The module shuts down immediately when the UVLO threshold is reached. The fault needs to be cleared for the module to restart.

**Table 10. UVLO Resistor Settings**

| UVLO (V) | Resistor (kΩ)   |
|----------|-----------------|
| 4.2      | Open            |
| 4.5      | Connect to V25  |
| 4.5      | Connect to SGND |
| 4.5      | 12.1            |
| 4.5      | 13.3            |
| 4.5      | 14.7            |



**Table 10. UVLO Resistor Settings (Continued)**

| UVLO (V) | Resistor (kΩ) |
|----------|---------------|
| 4.5      | 16.2          |
| 4.5      | 17.8          |
| 4.5      | 19.6          |
| 4.5      | 21.5          |
| 4.5      | 23.7          |
| 4.2      | 26.1          |
| 4.59     | 28.7          |
| 5.06     | 31.6          |
| 5.57     | 34.8          |
| 6.13     | 38.3          |
| 6.75     | 42.2          |
| 7.42     | 46.4          |
| 8.18     | 51.1          |
| 10.8     | 56.2          |
| 10.8     | 61.9          |
| 10.8     | 68.1          |
| 10.8     | 75            |
| 10.8     | 82.5          |
| 10.8     | 90.9          |
| 10.8     | 100           |
| 10.8     | 110           |

#### 4.8 SMBus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between the SA pin and SGND. This pin can also be used to make VSET\_Group selection as shown in [Table 11](#). A standard 1% resistor is required.

**Table 11. SMBus Address Resistor Selection**

| R <sub>SET</sub> (kΩ) | SMBus Address | VSET_GROUP |
|-----------------------|---------------|------------|
| 10                    | 19h           | Group 0    |
| 11                    | 1Ah           | Group 0    |
| 12.1                  | 1Bh           | Group 0    |
| 13.3                  | 1Ch           | Group 0    |
| 14.7                  | 1Dh           | Group 0    |
| 16.2                  | 1Eh           | Group 0    |
| 17.8                  | 1Fh           | Group 0    |
| 19.6                  | 20h           | Group 0    |
| 21.5                  | 21h           | Group 0    |
| 23.7                  | 22h           | Group 0    |
| 26.1                  | 23h           | Group 0    |
| 28.7                  | 24h           | Group 0    |
| 31.6                  | 25h           | Group 0    |

Table 11. SMBus Address Resistor Selection (Continued)

| R <sub>SET</sub> (k $\Omega$ ) | SMBus Address | VSET_GROUP |
|--------------------------------|---------------|------------|
| 34.8                           | 26h           | Group 0    |
| 38.3                           | 27h           | Group 0    |
| 42.2                           | 28h           | Group 0    |
| 46.4                           | 29h           | Group 0    |
| 51.1                           | 19h           | Group 1    |
| 56.2                           | 1Ah           | Group 1    |
| 61.9                           | 1Bh           | Group 1    |
| 68.1                           | 1Ch           | Group 1    |
| 75                             | 1Dh           | Group 1    |
| 82.5                           | 1Eh           | Group 1    |
| 90.9                           | 1Fh           | Group 1    |
| 100                            | 20h           | Group 1    |
| 110                            | 21h           | Group 1    |
| 121                            | 22h           | Group 1    |
| 133                            | 23h           | Group 1    |
| 147                            | 24h           | Group 1    |
| 162                            | 25h           | Group 1    |
| Connect to SGND                | 26h           | Group 1    |
| 178                            | 27h           | Group 1    |
| OPEN                           | 28h           | Group 1    |

## 4.9 Output Overvoltage Protection

The RAA210833 offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the VSEN+ and VSEN- pins) to a threshold set to 15% higher than the target output voltage (the default setting). Fault threshold can be programmed to a desired level with PMBus command VOUT\_OV\_FAULT\_LIMIT. If the V<sub>SEN+</sub> voltage exceeds this threshold, the module initiates an immediate shutdown without retry.

Internal to the module, a 332 $\Omega$  resistor is populated from VOUT to VSEN+ to protect from overvoltage conditions in case of open at VSENSE pin and differential remote sense traces due to assembly error. As long as the differential remote sense traces have low resistance, V<sub>OUT</sub> regulation accuracy is not sacrificed.

## 4.10 Output Prebias Protection

An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The RAA210833 provides prebias protection by sampling the output voltage before initiating an output ramp.

If a prebias voltage lower than the target voltage exists after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage, and both drivers are enabled. The output voltage is then ramped to the final regulation value at the preconfigured ramp rate.

The actual time the output takes to ramp from the prebias voltage to the target voltage varies depending on the prebias voltage. However, the total time elapsed from when the delay period expires and when the output reaches its target value matches the preconfigured ramp time (see [Figure 26 on page 27](#)).

If the prebias voltage is higher than the target voltage after the preconfigured delay period expires, the target voltage is set to match the existing prebias voltage, and both drivers are enabled with a PWM duty cycle that would ideally creates the prebias voltage.

After the preconfigured soft-start ramp period expires, the PG pin is asserted (assuming the prebias voltage is not higher than the overvoltage limit). The PWM then adjusts its duty cycle to match the original target voltage and the output ramps down to the preconfigured output voltage.

If a prebias voltage is higher than the overvoltage limit, the device does not initiate a turn-on sequence and declares an overvoltage fault condition.

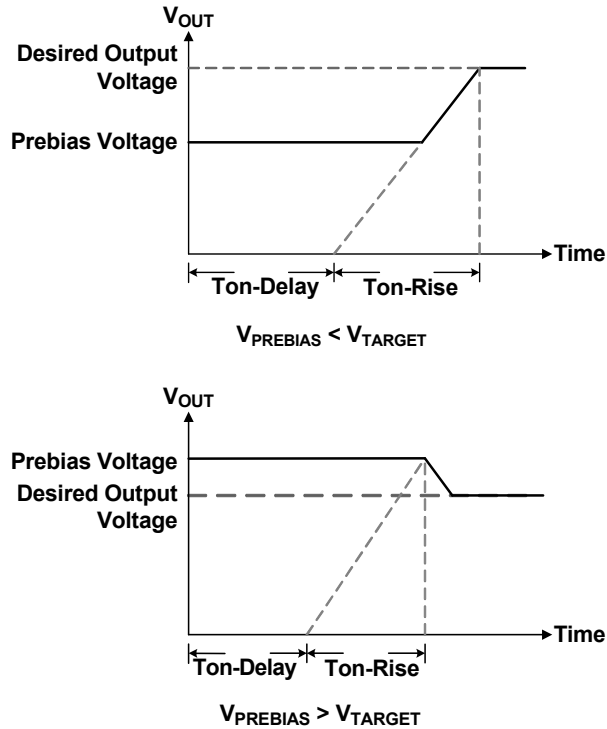


Figure 26. Output Responses to Prebias Voltages

#### 4.11 Output Overcurrent Protection

The RAA210833 can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. The average output overcurrent fault threshold can be programmed with the PMBus command `IOUT_OC_FAULT_LIMIT`. The module automatically programs the peak inductor current fault threshold by reading the real-time input voltage, switching frequency, and `VOUT_COMMAND` to calculate inductor ripple current.

The default response from an overcurrent fault is an immediate shutdown with a continuous retry of 70ms delay.

### 4.12 Thermal Overload Protection

The RAA210833 includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The default temperature limit is set to +115°C in the factory, but can be changed with PMBus command OT\_FAULT\_LIMIT.

The response from an over-temperature fault is an immediate shutdown without retry.

### 4.13 Phase Spreading

When multiple point-of-load converters share a common DC input supply, adjust the clock phase offset of each device, so that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to the  $I_{RMS}^2$  are reduced dramatically.

To enable phase spreading, all converters must be synchronized to the same switching clock. The phase offset between devices is determined from the lower four bits of the SMBus address of each interleaved device. The phase offset of each device can be set to any value between 0° and 360° in 22.5° increments by setting the device address appropriately as shown in [Table 12](#). This functionality can also be accessed using the PMBus command INTERLEAVE.

**Table 12. INTERLEAVE Settings from SA**

| INTERLEAVE vs SA |              |            |            |                 |
|------------------|--------------|------------|------------|-----------------|
| SA               | SA in Binary | Low 4-Bits | INTERLEAVE | Phase Shift (°) |
| 19h              | 00011001     | 1001       | 9          | 202.5           |
| 1Ah              | 00011010     | 1010       | 10         | 225             |
| 1Bh              | 00011011     | 1011       | 11         | 247.5           |
| 1Ch              | 00011100     | 1100       | 12         | 270             |
| 1Dh              | 00011101     | 1101       | 13         | 292.5           |
| 1Eh              | 00011110     | 1110       | 14         | 315             |
| 1Fh              | 00011111     | 1111       | 15         | 337.5           |
| 20h              | 00100000     | 0000       | 0          | 0               |
| 21h              | 00100001     | 0001       | 1          | 22.5            |
| 22h              | 00100010     | 0010       | 2          | 45              |
| 23h              | 00100011     | 0011       | 3          | 67.5            |
| 24h              | 00100100     | 0100       | 4          | 90              |
| 25h              | 00100101     | 0101       | 5          | 112.5           |
| 26h              | 00100110     | 0110       | 6          | 135             |
| 27h              | 00100111     | 0111       | 7          | 157.5           |
| 28h              | 00101000     | 1000       | 8          | 180             |
| 29h              | 00101001     | 1001       | 9          | 202.5           |

### 4.14 Monitoring Through SMBus

A system controller can monitor a wide variety of different RAA210833 system parameters with PMBus commands:

- READ\_VIN
- READ\_VOUT
- READ\_IOUT

- READ\_INTERNAL\_TEMP
- READ\_DUTY\_CYCLE
- READ\_FREQUENCY
- MFR\_READ\_VMON

#### **4.15 Snapshot Parameter Capture**

The RAA210833 offers a special feature to capture parametric data and some fault status following a fault. A detailed description is provided in [“PMBus Commands Description” on page 36](#) under PMBus command SNAPSHOT and SNAPSHOT\_CONTROL.

## 5. PCB Layout Guidelines

To achieve stable operation, low losses, and good thermal performance, some layout considerations are necessary.

- For  $V_{DD} > 6V$ , the recommended PCB layout is shown in [Figure 27](#). Leave V25, VDDC, VR5, and VR6 as “No Connect”.
- For  $5.5V \leq V_{DD} \leq 6V$ , connect VDDC pin to VR6 pin. For  $4.5 \leq V_{DD} < 5.5V$ , connect VDDC pin to VR6 and VR5 pin. An RC filter is required at the input of  $V_{DRVIN}$  pin if input supply is shared with VIN pin.
- Establish a separate SGND plane and PGND plane, then connect SGND to the PGND plane as shown in [Figure 28](#) in the middle layer. For making connections between SGND/PGND on the top layer and other layers, use multiple vias for each pin to connect to the inner SGND/PGND layer. Do not connect SGND directly to PGND on a top layer. Connecting SGND directly to PGND without establishing an SGND plane bypasses the decoupling capacitor at internal reference supplies, making the controller susceptible to noise.
- Place enough ceramic capacitors between VIN and PGND, and VOUT and PGND. Place bypass capacitors between VDD and the ground plane, as close to the module as possible to minimize high frequency noise.
- Use large copper areas for the power path (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Use multiple vias to connect the power planes in different layers. Extra ceramic capacitors at VIN and VOUT can be placed on the bottom layer under the VIN and VOUT pads when multiple vias are used for connecting copper pads on top and bottom layers.
- Connect differential remote-sensing traces to the regulation point to achieve a tight output voltage regulation. Route a trace from  $V_{SEN-}$  and  $V_{SEN+}$  to the point-of-load where the tight output voltage is desired. Avoid routing any sensitive signal traces such as the VSENSE signal near VSWH pads.
- For noise sensitive applications, it is recommended that the user connect the VSWH pads only on the top layer only (however, thermal performance gets sacrificed). External airflow might be required to keep module heat at desired level. For applications where switching noise is less critical, an excellent thermal performance can be achieved in the RAA210833 module by increasing copper mass attached to VSWH pad. To increase copper mass on the VSWH node, create copper islands in the middle and bottom layers under the VSWH pad, and connect them to the top layer with multiple vias. Make sure to shield the copper islands with a PGND layer to avoid any interference from noise sensitive signals.

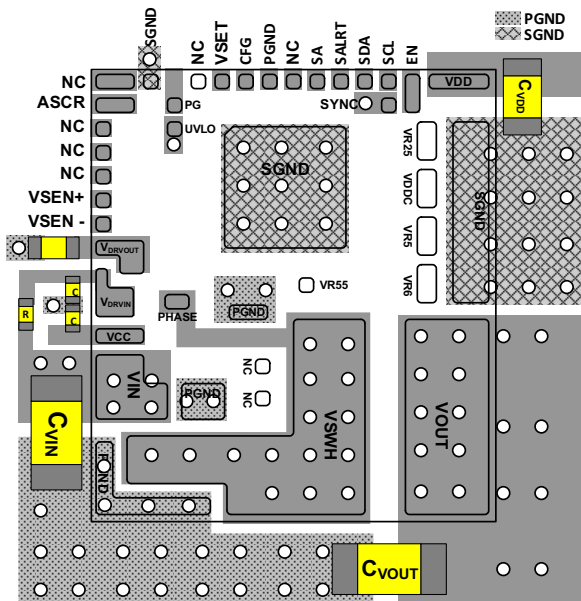


Figure 27. Recommended Layout - Top PCB Layer

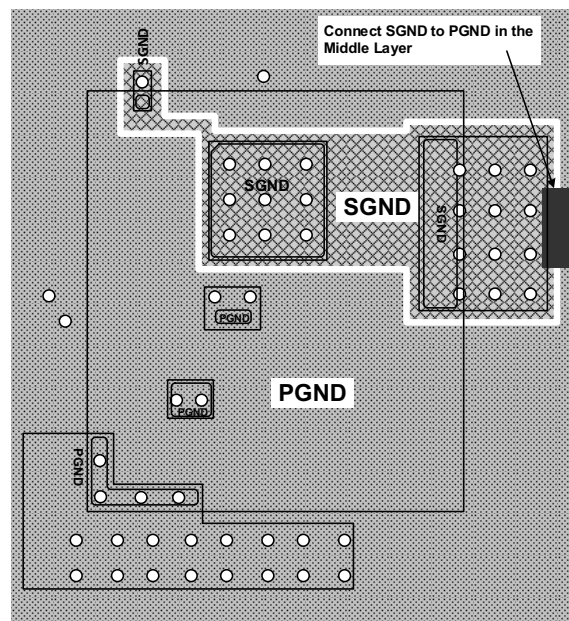


Figure 28. Recommended Layout - Connect SGND to PGND in the Middle PCB Layer after Establishing Separate SGND and PGND

## 5.1 Thermal Considerations

Experimental power loss curves, along with  $\theta_{JA}$  from thermal modeling analysis, can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In actual applications, other heat sources and design margins should be considered.

## 5.2 Package Description

The structure of the RAA210833 belongs to the High Density Array (HDA) no-lead package. This package has advantages, such as good thermal and electrical conductivity, low weight, and small size. The HDA package is applicable for surface mounting technology and is being more readily used in the industry. The RAA210833 contains several types of devices, including resistors, capacitors, inductors, and control ICs. The RAA210833 is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper leadframe and multi-component assembly is overmolded with polymer mold compound to protect these devices.

The package outline, a typical PCB land pattern design, and a typical stencil opening edge position are shown in the Package Outline Drawing section starting on [page 50](#). The module has a small size of 17mm x 19mm x 3.6mm. [Figure 29](#) shows typical reflow profile parameters. These guidelines are general design rules. You can modify parameters according to your application.

## 5.3 PCB Layout Pattern Design

The bottom of the RAA210833 is a lead-frame footprint, that is attached to the PCB by a surface mounting process. The PCB land pattern is shown in the [“Package Outline Drawing”](#) section starting on [page 50](#).

The PCB layout pattern is an array of solder mask defined PCB lands that align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pad perimeters. The exposed solder mask defined PCB land area should be 50-80% of the available module I/O area.

## 5.4 Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) improves the thermal performance, diminishing returns are seen as more and more vias are added. Use as many vias as practical for the thermal land size and that your board design rules allow.

## 5.5 Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50 $\mu$ m to 75 $\mu$ m (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints.

The stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width can be reduced slightly to help prevent solder bridging between adjacent I/O lands. A typical solder stencil pattern is shown in the [“Package Outline Drawing”](#) section starting on [page 50](#).

Consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing “smooths” the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a “brick like” paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) HDA.

## 5.6 Reflow Parameters

Due to the low mount height of the HDA, a “No Clean” Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile given in [Figure 29](#) is provided as a guideline to be customized for varying manufacturing practices and applications.

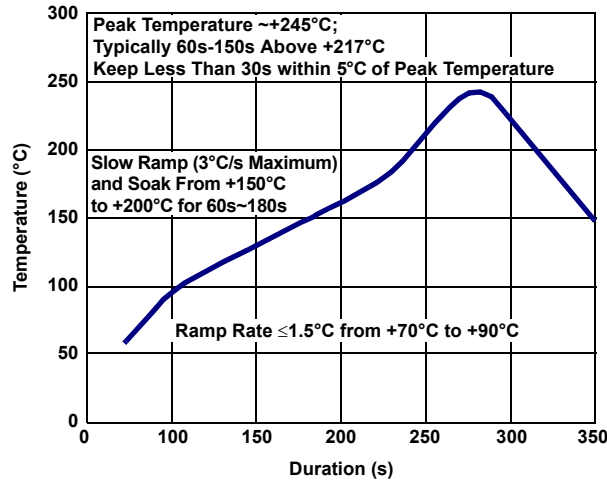


Figure 29. Typical Reflow Profile



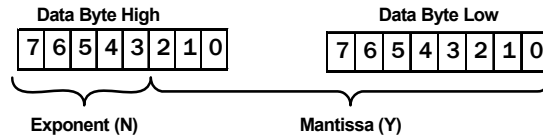
## 6. PMBus Command Summary

| Command Code | Command Name        | Description                                                                  | Type      | Data Format | Default Value | Default Setting            | Page               |
|--------------|---------------------|------------------------------------------------------------------------------|-----------|-------------|---------------|----------------------------|--------------------|
| 01h          | OPERATION           | Sets Enable and Disable modes.                                               | R/W Byte  | BIT         |               |                            | <a href="#">36</a> |
| 02h          | ON_OFF_CONFIG       | Configures the EN pin and PMBus commands to turn the unit ON and OFF.        | R/W Byte  | BIT         | 16h           | Hardware Enable, soft-off  | <a href="#">36</a> |
| 03h          | CLEAR_FAULTS        | Clears fault indications.                                                    | SEND Byte |             |               |                            | <a href="#">36</a> |
| 21h          | VOUT_COMMAND        | Sets the nominal value of the output voltage.                                | R/W Word  | L16u        |               | Pin-strap                  | <a href="#">37</a> |
| 24h          | VOUT_MAX            | Sets the maximum possible value of $V_{OUT}$ . 110% of pin-strap $V_{OUT}$ . | R/W Word  | L16u        |               | 1.1 x $V_{OUT}$ Pin-strap  | <a href="#">37</a> |
| 33h          | FREQUENCY_SWITCH    | Sets the switching frequency.                                                | R/W Word  | L11         |               | Pin-strap                  | <a href="#">37</a> |
| 37h          | INTERLEAVE          | Configures a phase offset between devices sharing a SYNC clock.              | R/W Word  | BIT         |               | Set based on PMBus Address | <a href="#">38</a> |
| 40h          | VOUT_OV_FAULT_LIMIT | Sets the $V_{OUT}$ overvoltage fault threshold.                              | R/W Word  | L16u        |               | 1.15 x $V_{OUT}$ Pin-strap | <a href="#">38</a> |
| 44h          | VOUT_UV_FAULT_LIMIT | Sets the $V_{OUT}$ undervoltage fault threshold.                             | R/W Word  | L16u        |               | 0.85 x $V_{OUT}$ Pin-strap | <a href="#">38</a> |
| 46h          | IOUT_OC_FAULT_LIMIT | Sets the $I_{OUT}$ average overcurrent fault threshold.                      | R/W Word  | L11         | E280h         | 40A                        | <a href="#">38</a> |
| 4Bh          | IOUT_UC_FAULT_LIMIT | Sets the $I_{OUT}$ average undercurrent fault threshold.                     | R/W Word  | L11         | E57Fh         | -40A                       | <a href="#">39</a> |
| 4Fh          | OT_FAULT_LIMIT      | Sets the over-temperature fault threshold.                                   | R/W Word  | L11         | EB98h         | +115°C                     | <a href="#">39</a> |
| 53h          | UT_FAULT_LIMIT      | Sets the under-temperature fault threshold.                                  | R/W Word  | L11         | E530h         | -45°C                      | <a href="#">39</a> |
| 55h          | VIN_OV_FAULT_LIMIT  | Sets the $V_{IN}$ overvoltage fault threshold.                               | R/W Word  | L11         | D3A0h         | 14.5V                      | <a href="#">39</a> |
| 59h          | VIN_UV_FAULT_LIMIT  | Sets the $V_{IN}$ undervoltage fault threshold.                              | R/W Word  | L11         |               | Pin-strap                  | <a href="#">40</a> |
| 5Eh          | POWER_GOOD_ON       | Sets the voltage threshold for Power-Good indication.                        | R/W Word  | L16u        |               | 0.9 x $V_{OUT}$ Pin-strap  | <a href="#">40</a> |
| 60h          | TON_DELAY           | Sets the delay time from ENABLE to start of $V_{OUT}$ rise.                  | R/W Word  | L11         |               | Pin-strap                  | <a href="#">40</a> |
| 61h          | TON_RISE            | Sets the rise time of $V_{OUT}$ after ENABLE and TON_DELAY.                  | R/W Word  | L11         |               | Pin-strap                  | <a href="#">40</a> |
| 64h          | TOFF_DELAY          | Sets the delay time from DISABLE to start of $V_{OUT}$ fall.                 | R/W Word  | L11         |               | Pin-strap                  | <a href="#">41</a> |
| 65h          | TOFF_FALL           | Sets the fall time for $V_{OUT}$ after DISABLE and TOFF_DELAY.               | R/W Word  | L11         |               | Pin-strap                  | <a href="#">41</a> |
| 78h          | STATUS_BYTE         | Returns an abbreviated status for fast reads.                                | Read Byte | BIT         | 00h           | No Faults                  | <a href="#">41</a> |
| 79h          | STATUS_WORD         | Returns information with a summary of the units's fault condition.           | Read Word | BIT         | 0000h         | No Faults                  | <a href="#">42</a> |

| Command Code | Command Name               | Description                                                                                                                  | Type       | Data Format | Default Value | Default Setting                   | Page               |
|--------------|----------------------------|------------------------------------------------------------------------------------------------------------------------------|------------|-------------|---------------|-----------------------------------|--------------------|
| 7Ah          | STATUS_VOUT                | Returns the V <sub>OUT</sub> specific status.                                                                                | Read Byte  | BIT         | 00h           | No Faults                         | <a href="#">42</a> |
| 7Bh          | STATUS_IOUT                | Returns the I <sub>OUT</sub> specific status.                                                                                | Read Byte  | BIT         | 00h           | No Faults                         | <a href="#">43</a> |
| 7Ch          | STATUS_INPUT               | Returns status specific to the input.                                                                                        | Read Byte  | BIT         | 00h           | No Faults                         | <a href="#">43</a> |
| 7Dh          | STATUS_TEMPERATURE         | Returns the temperature specific status.                                                                                     | Read Byte  | BIT         | 00h           | No Faults                         | <a href="#">43</a> |
| 7Eh          | STATUS_CML                 | Returns the Communication, Logic, and Memory specific status.                                                                | Read Byte  | BIT         | 00h           | No Faults                         | <a href="#">44</a> |
| 80h          | STATUS_MFR_SPECIFIC        | Returns the VMON and External Sync clock specific status.                                                                    | Read Byte  | BIT         | 00h           | No Faults                         | <a href="#">44</a> |
| 88h          | READ_VIN                   | Returns the input voltage reading.                                                                                           | Read Word  | L11         |               |                                   | <a href="#">44</a> |
| 8Bh          | READ_VOUT                  | Returns the output voltage reading.                                                                                          | Read Word  | L16u        |               |                                   | <a href="#">45</a> |
| 8Ch          | READ_IOUT                  | Returns the output current reading.                                                                                          | Read Word  | L11         |               |                                   | <a href="#">45</a> |
| 8Dh          | READ_INTERNAL_TEMP         | Returns the temperature reading internal to the device.                                                                      | Read Word  | L11         |               |                                   | <a href="#">45</a> |
| 94h          | READ_DUTY_CYCLE            | Returns the duty cycle reading during the ENABLE state.                                                                      | Read Word  | L11         |               |                                   | <a href="#">45</a> |
| 95h          | READ_FREQUENCY             | Returns the measured operating switch frequency.                                                                             | Read Word  | L11         |               |                                   | <a href="#">45</a> |
| DFh          | ASCR_CONFIG                | Configures the ASCR control loop.                                                                                            | R/W Block  | CUS         |               | Pin-strap                         | <a href="#">46</a> |
| E4h          | DEVICE_ID                  | Returns the 16-byte (character) device identifier string.                                                                    | Read Block | ASCII       |               | Reads Device Version              | <a href="#">46</a> |
| E5h          | MFR_IOUT_OC_FAULT_RESPONSE | Configures the I <sub>OUT</sub> overcurrent fault response.                                                                  | R/W Byte   | BIT         | B9h           | Disable and Retry with 70ms delay | <a href="#">46</a> |
| E6h          | MFR_IOUT_UC_FAULT_RESPONSE | Configures the I <sub>OUT</sub> undercurrent fault response.                                                                 | R/W Byte   | BIT         | B9h           | Disable and Retry with 70ms delay | <a href="#">47</a> |
| EAh          | SNAPSHOT                   | Returns 32-byte read-back of parametric and status values.                                                                   | Read Block | BIT         |               |                                   | <a href="#">47</a> |
| F3h          | SNAPSHOT_CONTROL           | Snapshot feature control command.                                                                                            | R/W Byte   | BIT         |               |                                   | <a href="#">48</a> |
| F5h          | MFR_VMON_OV_FAULT_LIMIT    | Returns the VMON overvoltage threshold.                                                                                      | Read Word  | L11         | CB00h         | 6V                                | <a href="#">48</a> |
| F6h          | MFR_VMON_UV_FAULT_LIMIT    | Returns the VMON undervoltage threshold.                                                                                     | Read Word  | L11         | CA00h         | 4V                                | <a href="#">48</a> |
| F7h          | MFR_READ_VMON              | Returns the VMON voltage reading. VMON is used to monitor VDRVOUT (Pin 8) voltage through an internal 16:1 resistor divider. | Read Word  | L11         |               |                                   | <a href="#">48</a> |

## 6.1 PMBus Data Formats

- **Linear-11 (L11)** - The L11 data format uses a 5-bit two’s complement exponent (N) and 11-bit two’s complement mantissa (Y) to represent a real world decimal value (X). The relation between the real world decimal value (X), N, and Y is:  $X = Y \cdot 2^N$



- **Linear-16 Unsigned (L16u)** - The L16u data format uses a fixed exponent (hard-coded to  $N = -13$ ) and a 16-bit unsigned integer mantissa (Y) to represent the real world decimal value (X). The relation between the real world decimal value (X), N and Y is:  $X = Y \cdot 2^{-13}$
- **Linear-16 Signed (L16s)** - The L16s data format uses a fixed exponent (hardcoded to  $N = -13$ ) and a 16-bit two’s complement mantissa (Y) to represent the real world decimal value (X). The relation between the real world decimal value (X), N, and Y is:  $X = Y \cdot 2^{-13}$
- **Bit Field (BIT)** - An explanation of the Bit Field format is provided in PMBus on [“PMBus Commands Description” on page 36](#).
- **Custom (CUS)** - An explanation of the custom data format is provided in PMBus [“PMBus Commands Description” on page 36](#). A combination of Bit Field and integer are common type of Custom data format.
- **ASCII (ASC)** - A variable length string of text characters that uses the ASCII data format.

## 6.2 PMBus Use Guidelines

The PMBus is a powerful tool that allows you to optimize circuit performance by configuring devices for your application. When configuring a device in a circuit, the device should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON\_OFF\_CONFIG, CLEAR\_FAULTS, VOUT\_COMMAND, and ASCR\_CONFIG. While the device is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

Commands not listed in the PMBus command summary are not allowed for customer use, and are reserved for factory use only. Issuing reserved commands may result in unexpected operation.

## 7. PMBus Commands Description

### OPERATION (01h)

**Definition:** Sets Enable and Disable settings.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** 40h

**Units:** N/A

| Settings | Actions       |
|----------|---------------|
| 00h      | Immediate off |
| 40h      | Soft off      |
| 80h      | On.           |

### ON\_OFF\_CONFIG (02h)

**Definition:** Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN).

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** 16h (Device starts from ENABLE pin with soft off)

**Units:** N/A

| Settings | Actions                                                 |
|----------|---------------------------------------------------------|
| 16h      | Device starts from ENABLE pin with soft off             |
| 17h      | Device starts from ENABLE pin with immediate off        |
| 1Ah      | Device starts from OPERATION command with soft off      |
| 1Bh      | Device starts from OPERATION command with immediate off |

### CLEAR\_FAULTS (03h)

**Definition:** Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit reasserts immediately. This command does not restart a device if it has shut down, it only clears the faults.

**Data Length in Bytes:** 0 Byte

**Data Format:** N/A

**Type:** Send only

**Default Value:** N/A

**Units:** N/A

**Reference:** N/A

**VOUT\_COMMAND (21h)**

**Definition:** Sets or reports the target output voltage. This command cannot set a value higher than either VOUT\_MAX or 110% of the pin-strap V<sub>OUT</sub> setting.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default Value:** Pin-strap setting

**Units:** Volts

**Range:** 0V to VOUT\_MAX

**VOUT\_MAX (24h)**

**Definition:** Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. This command provides a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. The default value can be changed through PMBus.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default Value:** 1.10 x V<sub>OUT</sub> pin-strap setting

**Units:** Volts

**Range:** 0V to 5.5V

**FREQUENCY\_SWITCH (33h)**

**Definition:** Sets the switching frequency of the device. The initial default value is defined by a pin-strap and this value can be overridden by writing this command through PMBus. If an external SYNC is used, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** Pin-strap setting

**Units:** kHz

**Range:** 296kHz to 1067kHz

**INTERLEAVE (37h)**

**Definition:** Configures the phase offset of a device that is sharing a common SYNC clock with other devices. The phase offset of each device can be set to any value between 0° and 360° in 22.5° increments.

**Data Length in Bytes:** 2

**Data Format:** BIT

**Type:** R/W

**Default Value:** Pin-strap setting of SA

**Units:** kHz

| Bits | Purpose           | Value   | Description                                                               |
|------|-------------------|---------|---------------------------------------------------------------------------|
| 15:8 | Reserved          | 0       | Reserved                                                                  |
| 7:4  | Group Number      | 0 to 15 | Sets the number of rails in the group. A value of 0 is interpreted as 16. |
| 3:0  | Position in Group | 0 to 15 | Sets position of the device's rail within the group.                      |

**VOUT\_OV\_FAULT\_LIMIT (40h)**

**Definition:** Sets the  $V_{OUT}$  overvoltage fault threshold.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default Value:** 1.15 x  $V_{OUT}$  pin-strap setting

**Units:** V

**Range:** 0V to  $V_{OUT\_MAX}$

**VOUT\_UV\_FAULT\_LIMIT (44h)**

**Definition:** Sets the  $V_{OUT}$  undervoltage fault threshold. This fault is masked during ramp or when disabled.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default Value:** 0.85 x  $V_{OUT}$  pin-strap setting

**Units:** V

**Range:** 0V to  $V_{OUT\_MAX}$

**IOUT\_OC\_FAULT\_LIMIT (46h)**

**Definition:** Sets the  $I_{OUT}$  average overcurrent fault threshold. The device automatically calculates the peak inductor overcurrent fault limit.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** E280h (40A)

**Units:** A

**Range:** -100A to 100A

**IOUT\_UC\_FAULT\_LIMIT (4Bh)**

**Definition:** Sets the  $I_{OUT}$  average undercurrent fault threshold. The device automatically calculates the valley inductor undercurrent fault limit.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** E57Fh (-40A)

**Units:** A

**Range:** -100A to 100A

**OT\_FAULT\_LIMIT (4Fh)**

**Definition:** Sets the temperature at which the device should indicate an over-temperature fault. Note that the temperature must drop below OT\_FAULT\_LIMIT to clear this fault.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** EB98h (+115°C)

**Units:** Celsius

**Range:** 0°C to +150°C

**UT\_FAULT\_LIMIT (53h)**

**Definition:** Sets the temperature, in degrees Celsius, of the unit where it should indicate an under-temperature fault. Note that the temperature must rise above UT\_FAULT\_LIMIT to clear this fault.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** E530h (-45°C)

**Units:** Celsius

**Range:** -55°C to +25°C

**VIN\_OV\_FAULT\_LIMIT (55h)**

**Definition:** Sets the  $V_{IN}$  overvoltage fault threshold.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** D3A0h (14.5V)

**Units:** V

**Range:** 0V to 16V

**VIN\_UV\_FAULT\_LIMIT (59h)**

**Definition:** Sets the  $V_{IN}$  undervoltage fault threshold.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** Pin-strap setting

**Units:** V

**Range:** 0V to 12V

**POWER\_GOOD\_ON (5Eh)**

**Definition:** Sets the voltage threshold for Power-good indication. Power-good asserts after the output voltage exceeds POWER\_GOOD\_ON and deasserts when the output voltage is less than the VOUT\_UV\_FAULT\_LIMIT. Renesas recommends setting POWER\_GOOD\_ON higher than the VOUT\_UV\_FAULT\_LIMIT.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** R/W

**Default Value:** 0.9 x VOUT pin-strap setting

**Units:** V

**TON\_DELAY (60h)**

**Definition:** Sets the delay time from when the device is enabled to the start of  $V_{OUT}$  rise.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** Pin-strap setting

**Units:** ms

**Range:** 2ms to 300ms

**TON\_RISE (61h)**

**Definition:** Sets the rise time of  $V_{OUT}$  after ENABLE and TON\_DELAY.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** Pin-strap setting

**Units:** ms

**Range:** 1ms to 120ms



**TOFF\_DELAY (64h)**

**Definition:** Sets the delay time from DISABLE to the start of V<sub>OUT</sub> fall.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** Pin-strap setting

**Units:** ms

**Range:** 2ms to 300ms

**TOFF\_FALL (65h)**

**Definition:** Sets the fall time for V<sub>OUT</sub> after DISABLE and TOFF\_DELAY.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** R/W

**Default Value:** Pin-strap setting

**Units:** ms

**Range:** 0ms to 120ms

**STATUS\_BYTE (78h)**

**Definition:** Returns one byte of information with a summary of the most critical faults.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read only

**Default Value:** 00h

**Units:** N/A

| Bit Number | Status Bit Name   | Meaning                                                                                                                              |
|------------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 7          | BUSY              | A fault was declared because the device was busy and unable to respond.                                                              |
| 6          | OFF               | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| 5          | VOUT_OV_FAULT     | An output overvoltage fault occurred.                                                                                                |
| 4          | IOUT_OC_FAULT     | An output overcurrent fault occurred.                                                                                                |
| 3          | VIN_UV_FAULT      | An input undervoltage fault occurred.                                                                                                |
| 2          | TEMPERATURE       | A temperature fault occurred.                                                                                                        |
| 1          | CML               | A communications, memory, or logic fault occurred.                                                                                   |
| 0          | NONE OF THE ABOVE | A fault not listed in Bits 7:1 occurred.                                                                                             |

**STATUS\_WORD (79h)**

**Definition:** Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS\_WORD is the same register as the STATUS\_BYTE (78h) command.

**Data Length in Bytes:** 2

**Data Format:** BIT

**Type:** Read only

**Default Value:** 0000h

**Units:** N/A

| Bit Number | Status Bit Name   | Meaning                                                                                                                              |
|------------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 15         | VOUT              | An output voltage fault has occurred.                                                                                                |
| 14         | IOUT/POUT         | An output current or output power fault occurred.                                                                                    |
| 13         | INPUT             | An input voltage, input current, or input power fault occurred.                                                                      |
| 12         | MFG_SPECIFIC      | A manufacturer specific fault occurred.                                                                                              |
| 11         | POWER_GOOD#       | The POWER_GOOD signal, if present, is negated.                                                                                       |
| 10         | Reserved          | Reserved                                                                                                                             |
| 9          | OTHER             | A bit in STATUS_OTHER is set.                                                                                                        |
| 8          | UNKNOWN           | A fault type not given in Bits 15:1 of the STATUS_WORD detected.                                                                     |
| 7          | BUSY              | A fault was declared because the device was busy and unable to respond.                                                              |
| 6          | OFF               | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| 5          | VOUT_OV_FAULT     | An output overvoltage fault occurred.                                                                                                |
| 4          | IOUT_OC_FAULT     | An output overcurrent fault occurred.                                                                                                |
| 3          | VIN_UV_FAULT      | An input undervoltage fault occurred.                                                                                                |
| 2          | TEMPERATURE       | A temperature fault occurred.                                                                                                        |
| 1          | CML               | A communications, memory, or logic fault occurred.                                                                                   |
| 0          | NONE OF THE ABOVE | A fault not listed in Bits 7:1 occurred.                                                                                             |

**STATUS\_VOUT (7Ah)**

**Definition:** Returns one data byte with the status of the output voltage.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read only

**Default Value:** 00h

**Units:** N/A

| BIT NUMBER | STATUS BIT NAME | MEANING                                 |
|------------|-----------------|-----------------------------------------|
| 7          | VOUT_OV_FAULT   | Indicates an output overvoltage fault.  |
| 6:5        | Reserved        | Reserved                                |
| 4          | VOUT_UV_FAULT   | Indicates an output undervoltage fault. |
| 3:0        | N/A             | These bits are not used.                |

**STATUS\_IOUT (7Bh)**

**Definition:** Returns one data byte with the status of the output current.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read only

**Default Value:** 00h

**Units:** N/A

| Bit Number | Status Bit Name | Meaning                                    |
|------------|-----------------|--------------------------------------------|
| 7          | IOUT_OC_FAULT   | An output overcurrent fault has occurred.  |
| 6:5        | Reserved        | Reserved                                   |
| 4          | IOUT_UC_FAULT   | An output undercurrent fault has occurred. |
| 3:0        | N/A             | Not used.                                  |

**STATUS\_INPUT (7Ch)**

**Definition:** Returns input voltage and input current status information.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read only

**Default Value:** 00h

**Units:** N/A

| Bit Number | Status Bit Name | Meaning                                   |
|------------|-----------------|-------------------------------------------|
| 7          | VIN_OV_FAULT    | An input overvoltage fault has occurred.  |
| 6:5        | Reserved        | Reserved                                  |
| 4          | VIN_UV_FAULT    | An input undervoltage fault has occurred. |
| 3:0        | N/A             | Not used.                                 |

**STATUS\_TEMPERATURE (7Dh)**

**Definition:** Returns one byte of information with a summary of any temperature related faults.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read only

**Default Value:** 00h

**Units:** N/A

| Bit Number | Status Bit Name | Meaning                                  |
|------------|-----------------|------------------------------------------|
| 7          | OT_FAULT        | An over-temperature fault has occurred.  |
| 6:5        | Reserved        | Reserved                                 |
| 4          | UT_FAULT        | An under-temperature fault has occurred. |
| 3:0        | N/A             | These bits are not used.                 |

**STATUS\_CML (7Eh)**

**Definition:** Returns one byte of information with a summary of any Communications, Logic, and/or Memory errors.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read only

**Default Value:** 00h

**Units:** N/A

| Bit Number | Meaning                                                                                                                                             |
|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 7          | Invalid or unsupported PMBus command was received.                                                                                                  |
| 6          | The PMBus command was sent with invalid or unsupported data.                                                                                        |
| 5          | Packet error was detected in the PMBus command.                                                                                                     |
| 4          | Memory/logic fault has occurred.                                                                                                                    |
| 3:2        | Reserved                                                                                                                                            |
| 1          | A PMBus command tried to write to a read only or protected command, or a communication fault other than the ones listed in this table has occurred. |
| 0          | Not used                                                                                                                                            |

**STATUS\_MFR\_SPECIFIC (80h)**

**Definition:** Returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** Read only

**Default Value:** 00h

**Units:** N/A

| Bit Number | Field Name                      | Meaning                                                                   |
|------------|---------------------------------|---------------------------------------------------------------------------|
| 7:4        | Reserved                        | Reserved                                                                  |
| 3          | External Switching Period Fault | Loss of external clock synchronization occurred.                          |
| 2          | Reserved                        | Reserved                                                                  |
| 1          | VMON UV Fault                   | The voltage on the VMON pin dropped below the level set by VMON_UV_FAULT. |
| 0          | VMON OV Fault                   | The voltage on the VMON pin rose above the level set by VMON_OV_FAULT.    |

**READ\_VIN (88h)**

**Definition:** Returns the input voltage reading.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Units:** V

**READ\_VOUT (8Bh)**

**Definition:** Returns the output voltage reading.

**Data Length in Bytes:** 2

**Data Format:** L16u

**Type:** Read only

**Units:** V

**READ\_IOUT (8Ch)**

**Definition:** Returns the output current reading.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Default Value:** N/A

**Units:** A

**READ\_INTERNAL\_TEMP (8Dh)**

**Definition:** Returns the controller junction temperature reading from the internal temperature sensor.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Units:** °C

**READ\_DUTY\_CYCLE (94h)**

**Definition:** Reports the actual duty cycle of the converter during the enable state.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Units:** %

**READ\_FREQUENCY (95h)**

**Definition:** Reports the actual switching frequency of the converter during the enable state.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Units:** kHz

**ASCR\_CONFIG (DFh)**

**Definition:** Allows you to configure the ASCR settings. ASCR gain is analogous to bandwidth and ASCR residual is analogous to damping. To improve load transient response performance, increase ASCR gain. To decrease transient response overshoot, increase ASCR residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR residual to improve transient response damping can result in slower recovery times, but does not affect the peak output voltage deviation.

**Data Length in Bytes:** 4

**Data Format:** CUS

**Type:** R/W

**Default Value:** Pin-strap setting

| Bit   | Purpose               | Data Format | Value    | Description |
|-------|-----------------------|-------------|----------|-------------|
| 31:25 | Not Used              |             | 0000000h | Not used    |
| 24    | Reserved              |             |          | Reserved    |
| 23:16 | ASCR Residual Setting | Integer     |          |             |
| 15:0  | ASCR Gain Setting     | Integer     |          |             |

**DEVICE\_ID (E4h)**

**Definition:** Returns the 16-byte (character) device identifier string.

**Data Length in Bytes:** 16

**Data Format:** ASCII

**Type:** Block Read

**Default Value:** Part number/Die revision/Firmware revision

**MFR\_IOUT\_OC\_FAULT\_RESPONSE (E5h)**

**Definition:** Configures the I<sub>OUT</sub> overcurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS\_IOUT.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** B9h (Disable and continuous retry with 70ms delay)

**Units:** N/A

| Settings | Actions                                       |
|----------|-----------------------------------------------|
| 80h      | Disable with no retry.                        |
| B9h      | Disable and continuous retry with 70ms delay. |

**MFR\_IOUT\_UC\_FAULT\_RESPONSE (E6h)**

**Definition:** Configures the I<sub>OUT</sub> undercurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS\_IOUT.

**Data Length in Bytes:** 1

**Data Format:** BIT

**Type:** R/W

**Default Value:** B9h (Disable and continuous retry with 70ms delay)

**Units:** N/A

| Settings | Actions                                       |
|----------|-----------------------------------------------|
| 80h      | Disable with no retry.                        |
| B9h      | Disable and continuous retry with 70ms delay. |

**SNAPSHOT (EAh)**

**Definition:** A 32-byte readback of parametric and status values. It allows monitoring and status data to be stored to flash following a fault condition. In case of a fault, the most recently updated values are stored to the flash memory. When SNAPSHOT STATUS Byte 22 is set stored, the device will no longer automatically captures parametric and status values following a fault until stored data are erased. Use the SNAPSHOT\_CONTROL command to erase stored data and clear the status bit before the next ramp up. Data erased are not allowed when the module is enabled.

**Data Length in Bytes:** 32

**Data Format:** Bit field

**Type:** Block Read

| Byte Number | Value                                                      | Pmbus Command             | Format |
|-------------|------------------------------------------------------------|---------------------------|--------|
| 31:23       | Reserved                                                   | Reserved                  | 00h    |
| 22          | Flash Memory Status Byte<br>FF - Not Stored<br>00 - Stored | NVM Status Byte           | Bit    |
| 21          | Manufacturer Specific Status Byte                          | STATUS_MFR_SPECIFIC (80h) | Byte   |
| 20          | CML Status Byte                                            | STATUS_CML (7Eh)          | Byte   |
| 19          | Temperature Status Byte                                    | STATUS_TEMPERATURE (7Dh)  | Byte   |
| 18          | Input Status Byte                                          | STATUS_INPUT (7Ch)        | Byte   |
| 17          | I <sub>OUT</sub> Status Byte                               | STATUS_IOUT (7Bh)         | Byte   |
| 16          | V <sub>OUT</sub> Status Byte                               | STATUS_VOUT (7Ah)         | Byte   |
| 15:14       | Switching Frequency                                        | READ_FREQUENCY (95h)      | L11    |
| 13:12       | Reserved                                                   | Reserved                  |        |
| 11:10       | Internal Temperature                                       | READ_INTERNAL_TEMP (8Dh)  | L11    |
| 9:8         | Duty Cycle                                                 | READ_DUTY_CYCLE (94h)     | L11    |
| 7:6         | Reserved                                                   | Reserved                  | L11    |
| 5:4         | Output Current                                             | READ_IOUT (8Ch)           | L11    |
| 3:2         | Output Voltage                                             | READ_VOUT (8Bh)           | L16u   |
| 1:0         | Input Voltage                                              | READ_VIN (88h)            | L11    |

**SNAPSHOT\_CONTROL (F3h)**

**Definition:** Writing a 01h causes the device to copy the current Snapshot values from NVRAM to the 32-byte Snapshot command parameter. Writing a 02h causes the device to write the current Snapshot values to NVRAM. Writing a 03h erases all Snapshot values from NVRAM. Write (02h) and Erase (03h) can only be used when the device is disabled. All other values are ignored.

**Data Length in Bytes:** 1

**Data Format:** Bit field

**Type:** R/W byte

| Value | Description                            |
|-------|----------------------------------------|
| 01h   | Read Snapshot values from NVRAM.       |
| 02h   | Write Snapshot values to NVRAM.        |
| 03h   | Erase Snapshot values stored in NVRAM. |

**MFR\_VMON\_OV\_FAULT\_LIMIT (F5h)**

**Definition:** Reads the VMON OV fault threshold.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Default Value:** CB00h (6V)

**Units:** V

**Range:** 4V to 6V

**MFR\_VMON\_UV\_FAULT\_LIMIT (F6h)**

**Definition:** Reads the VMON UV fault threshold.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Default Value:** CA00h (4V)

**Units:** V

**Range:** 4V to 6V

**MFR\_READ\_VMON (F7h)**

**Definition:** Reads the VMON voltage.

**Data Length in Bytes:** 2

**Data Format:** L11

**Type:** Read only

**Default Value:** N/A

**Units:** V

**Range:** 4V to 6V



## 8. Revision History

### 8.1 Firmware

| Firmware Revision Code | Change Description | Note |
|------------------------|--------------------|------|
| RAA210833--G0100       | Initial release    |      |

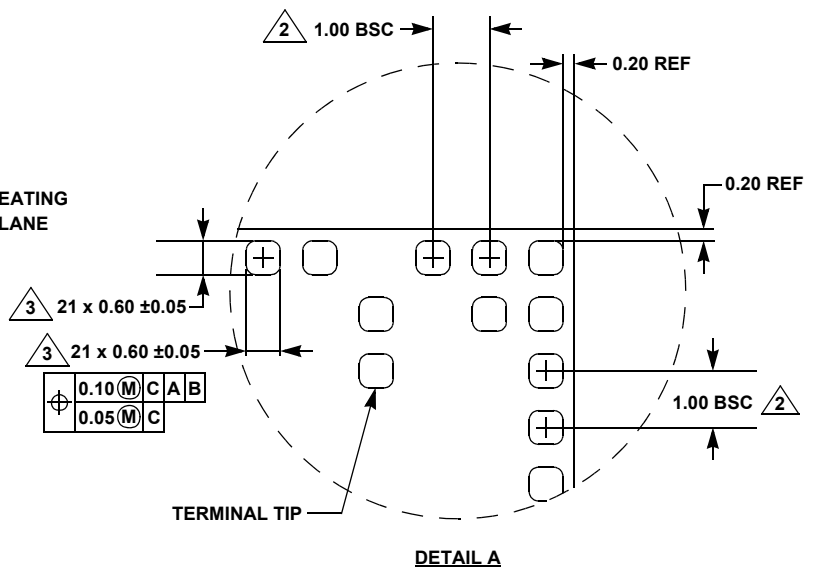
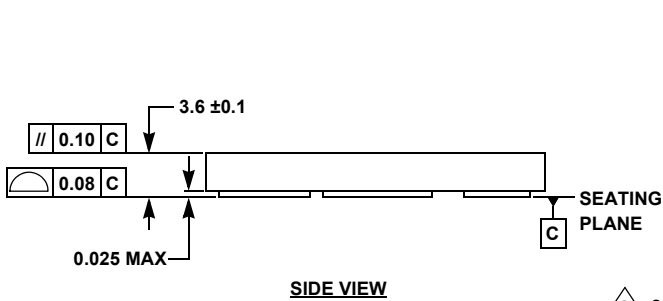
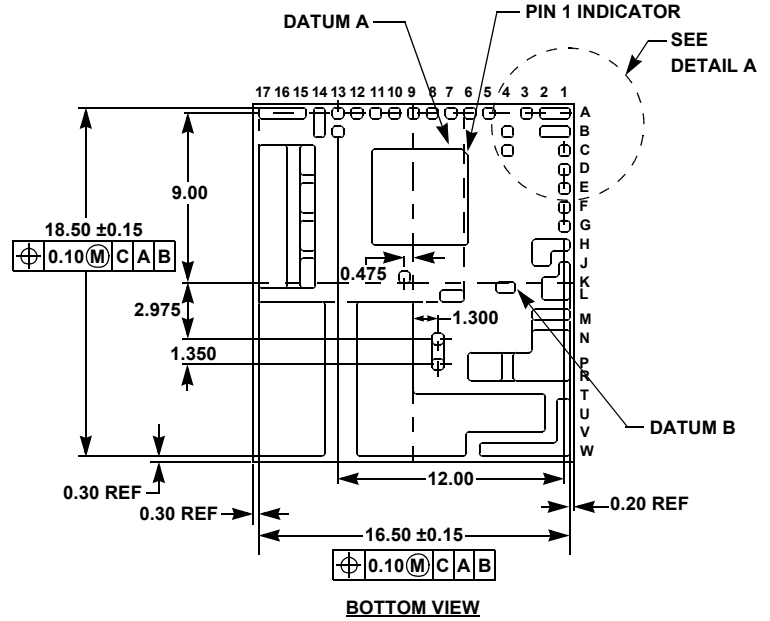
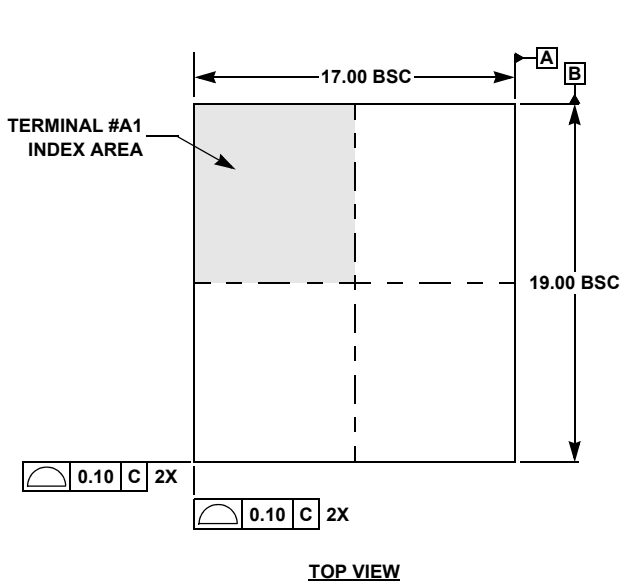
### 8.2 Datasheet

| Rev. | Date         | Description                                                                                                       |
|------|--------------|-------------------------------------------------------------------------------------------------------------------|
| 1.00 | Feb 8, 2019  | Updated the description for PG pin 28 on page 10.<br>Updated 80h action under OPERATION (01h) command on page 36. |
| 0.00 | Aug 31, 2018 | Initial release                                                                                                   |

## 9. Package Outline Drawing

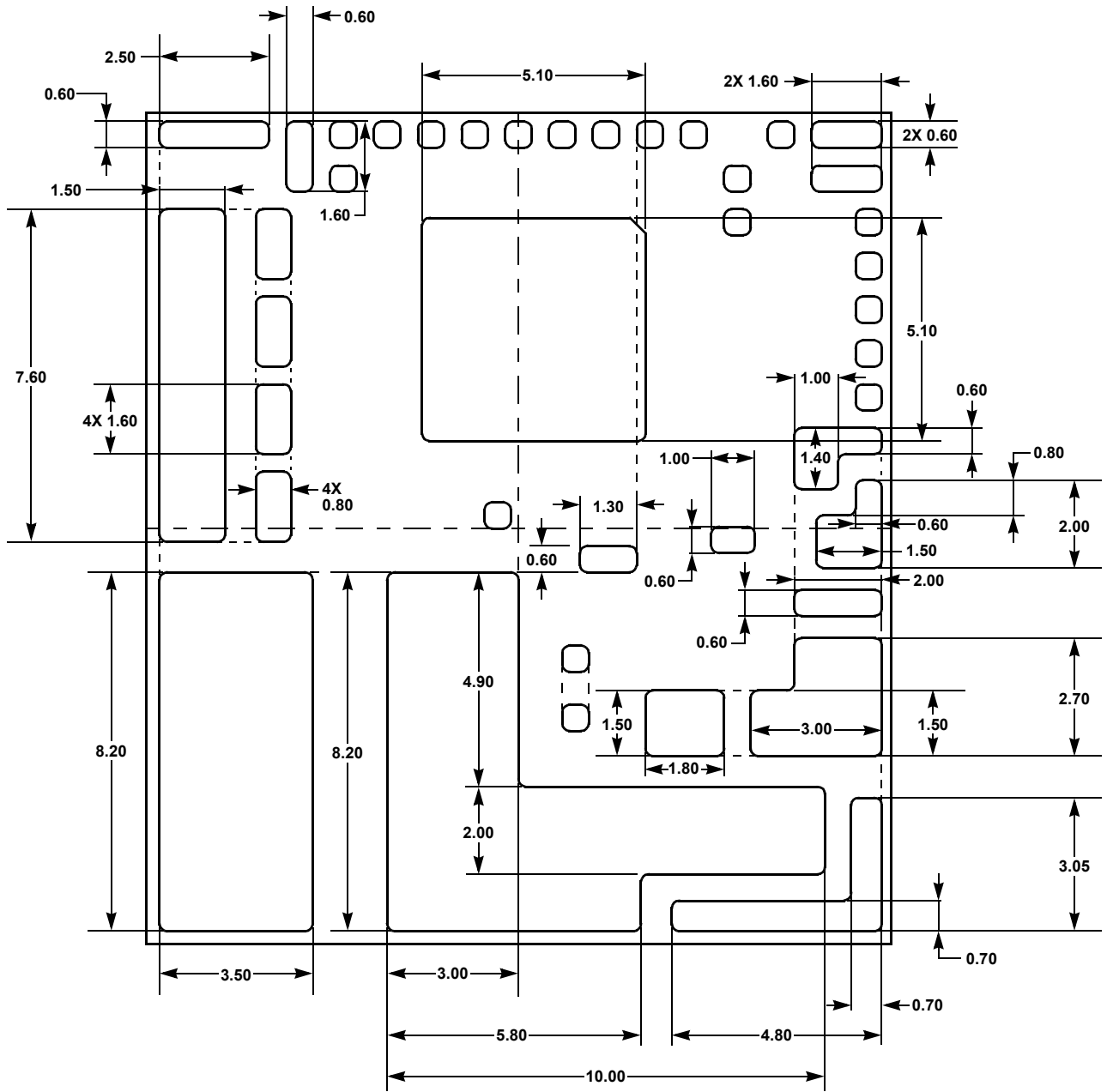
For the most recent package outline drawing, see [Y41.17x19](#).

Y41.17x19  
 41 I/O 17.0mm x 19.0mmx3.6mm HDA Module  
 Rev 1, 5/16

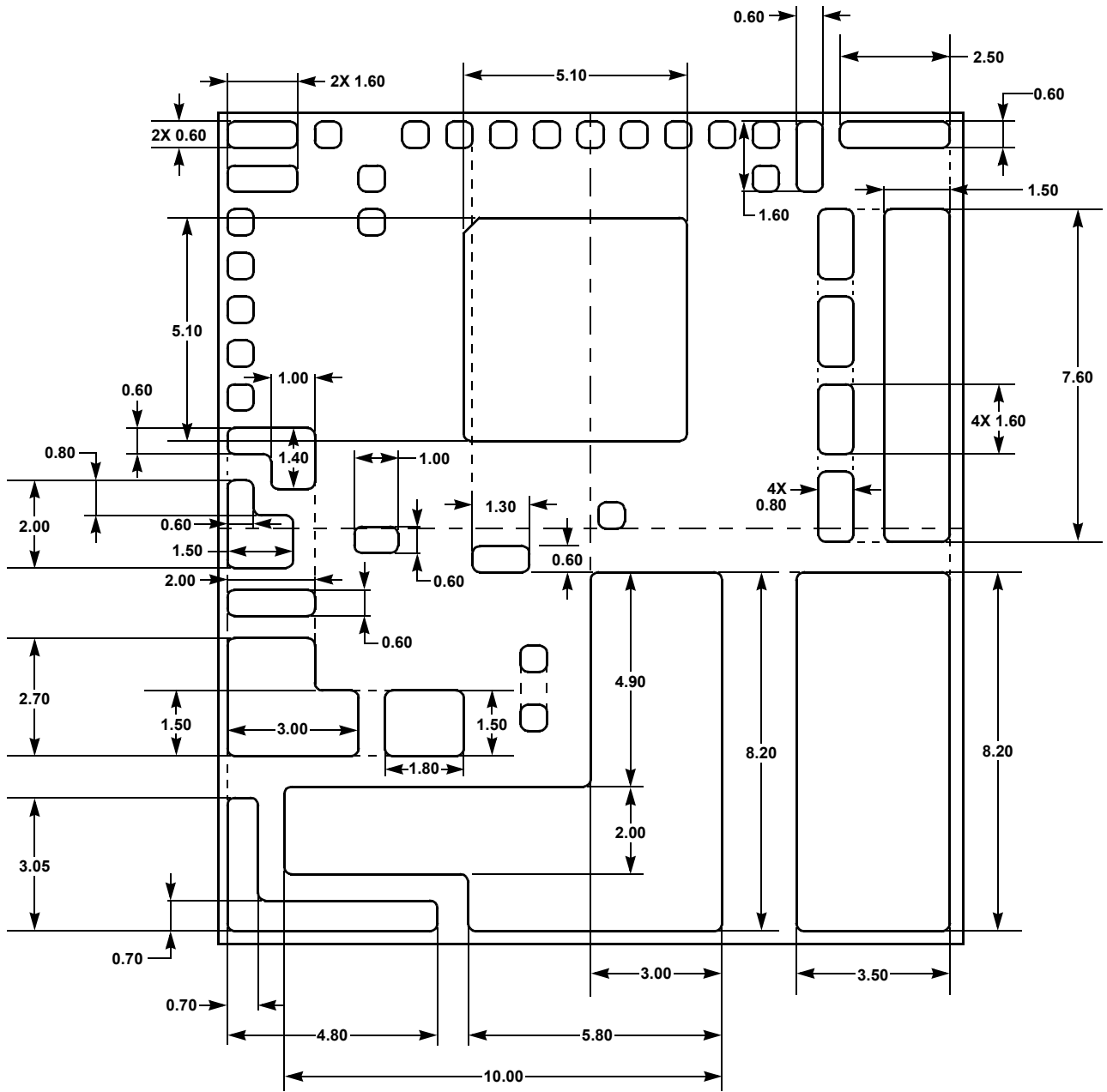


**NOTES:**

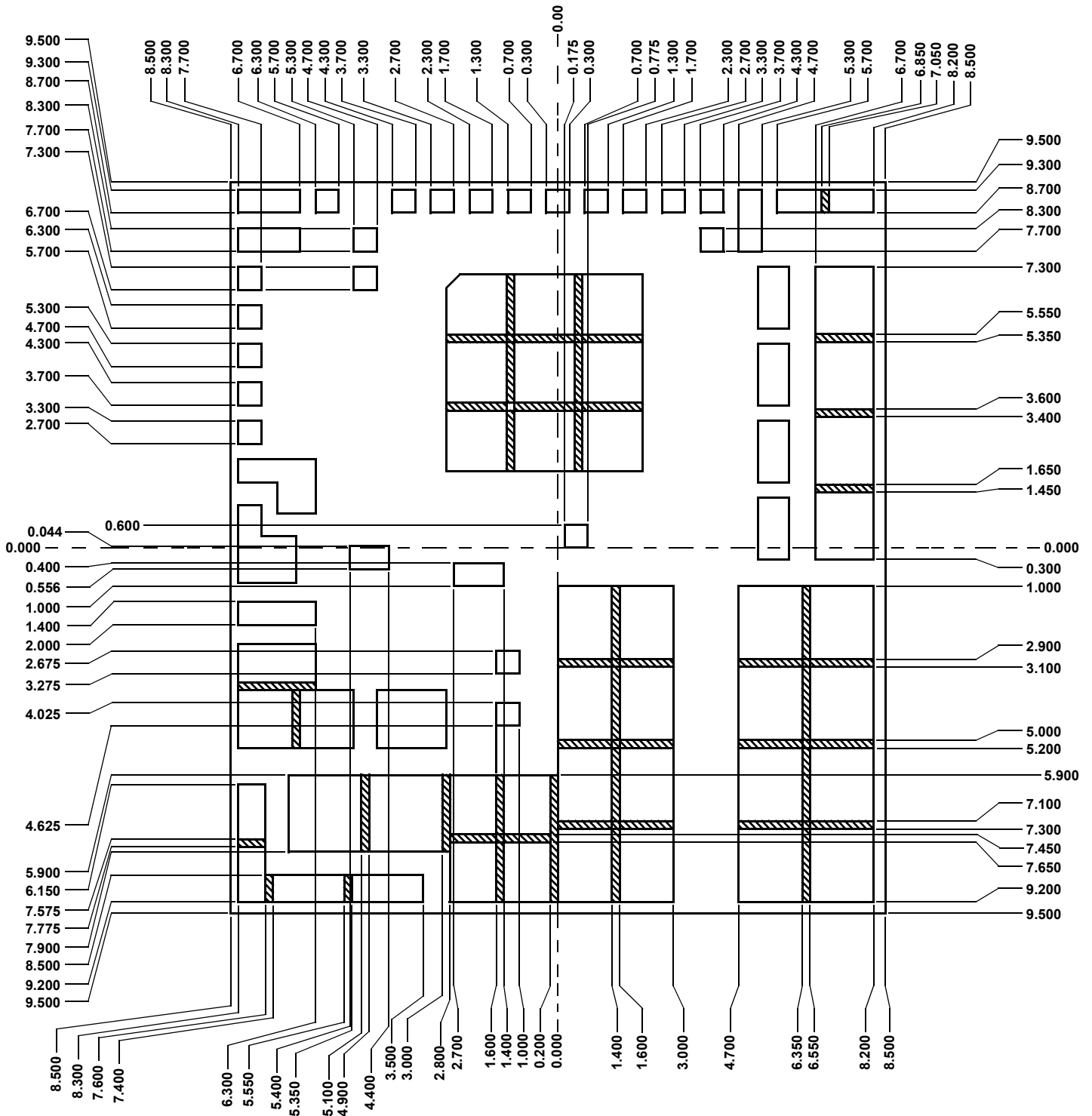
1. All dimensions are in millimeters.
- ② Represents the basic land grid pitch.
- ③ The total number of I/O (excluding dummy pads).
4. Unless otherwise specified, tolerance: decimal ±0.10.
5. Dimensioning and tolerancing per ASME Y14.M-2009.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.



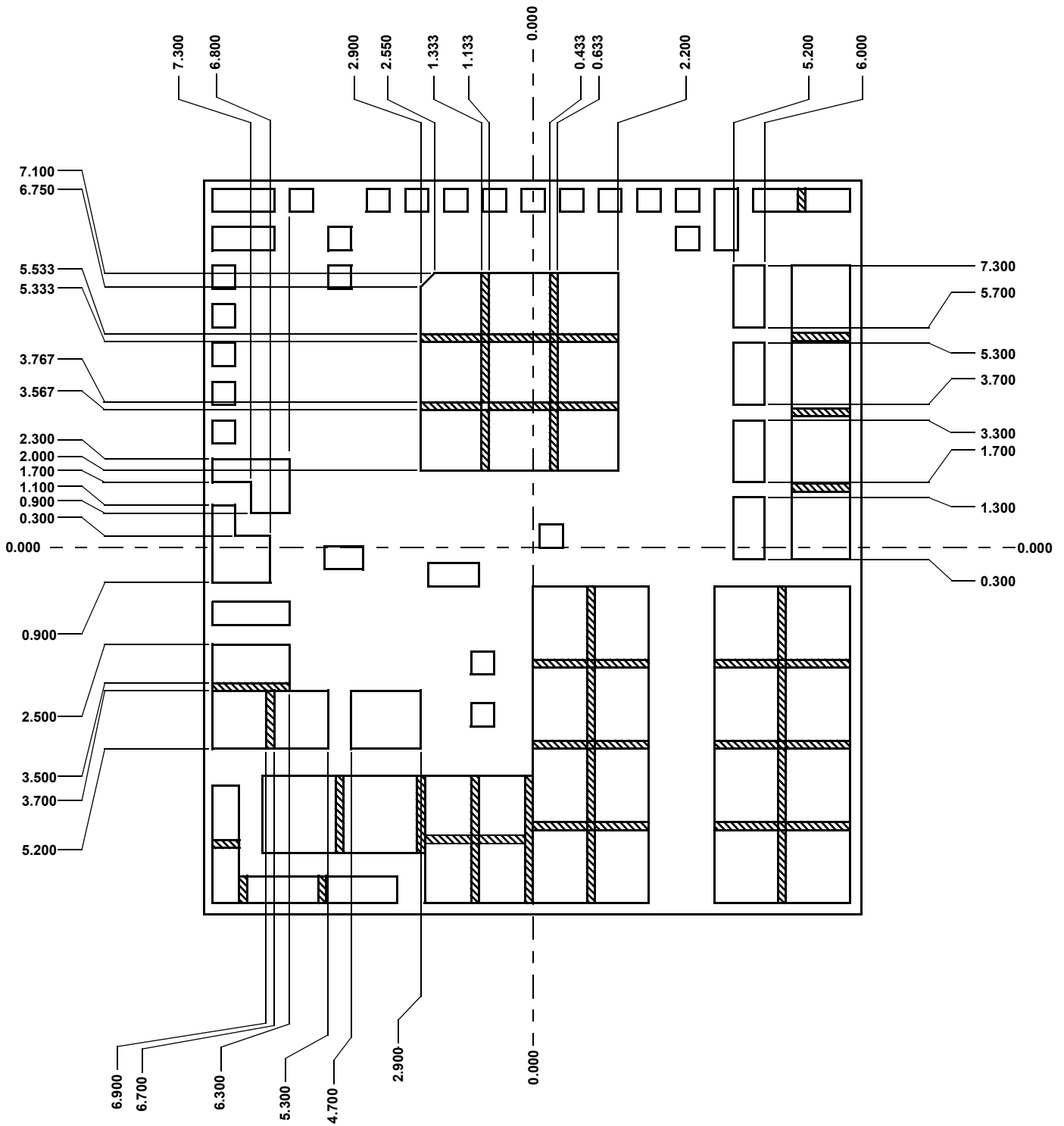
**SIZE DETAILS FOR THE 16 EXPOSED DAPS  
BOTTOM VIEW**



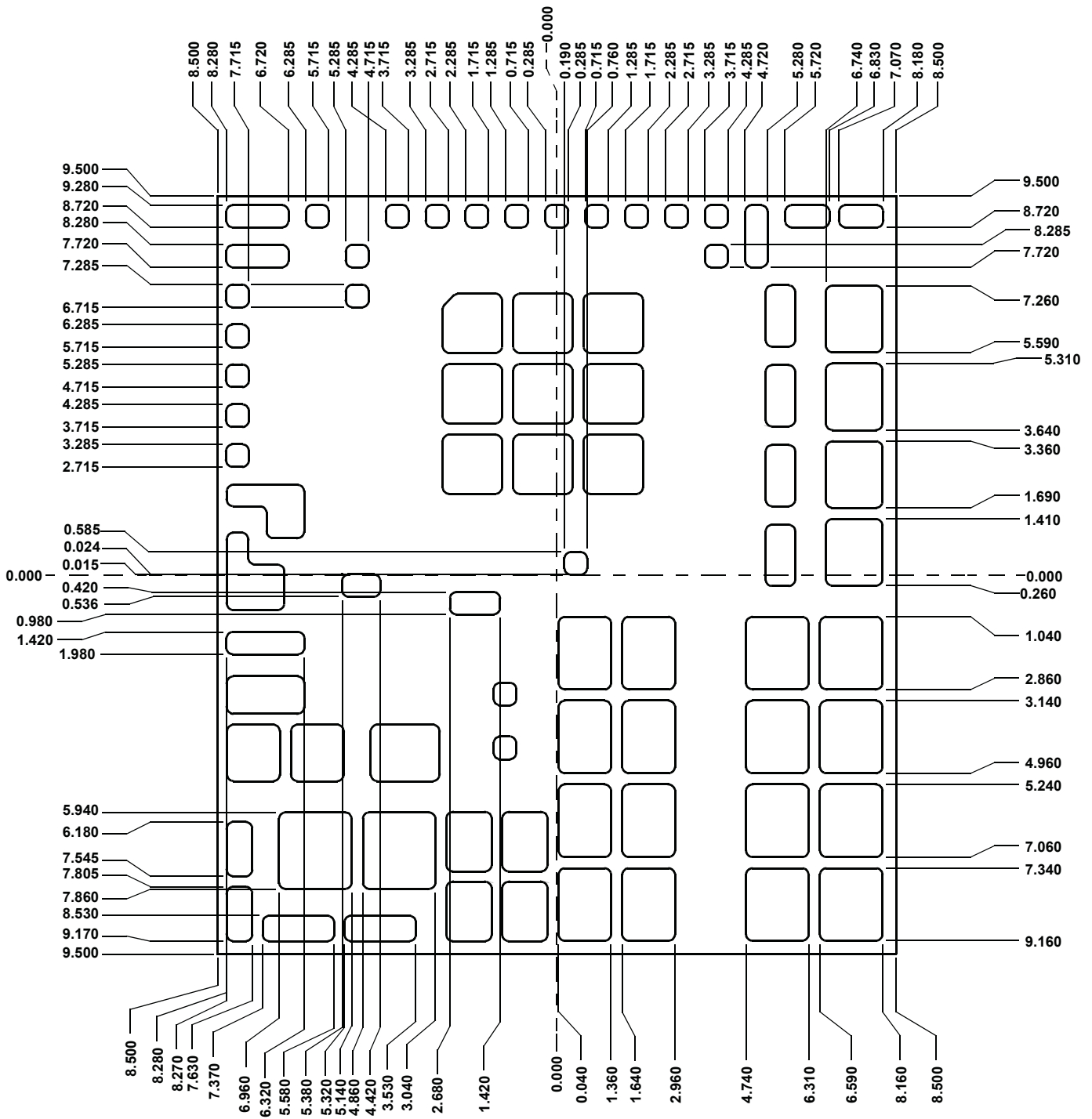
**SIZE DETAILS FOR THE 16 EXPOSED DAPS**  
**TOP VIEW**



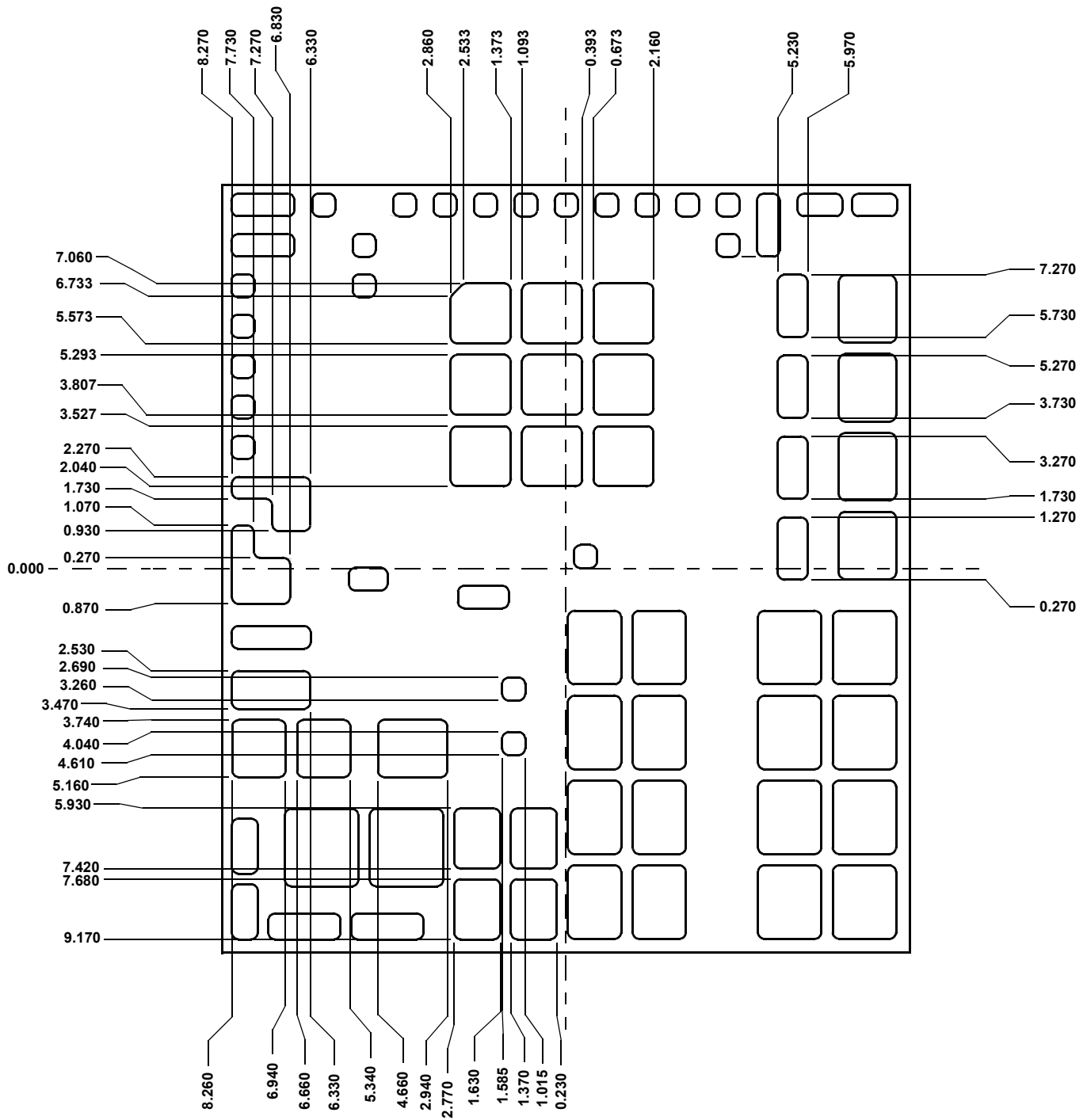
RECOMMENDED SOLDER MASK DEFINED PCB LAND PATTERN (1)  
TOP VIEW



**RECOMMENDED SOLDER MASK DEFINED PCB LAND PATTERN (2)**  
**TOP VIEW**



**RECOMMENDED STENCIL PATTERN (90% PASTE TO PAD) (1)**  
**TOP VIEW**



**RECOMMENDED STENCIL PATTERN (90% PASTE TO PAD) (2)**  
**TOP VIEW**



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