RAA730301

Monolithic Programmable Analog IC

R02DS0012EJ0110
Rev.1.10
May. 31, 2014

Overview

The RAA730301 is a monolithic programmable analog IC that supports low voltages and features a range of on-chip circuits such as an instrumentation amplifier, a D/A converter, and a temperature sensor, allowing the RAA730301 to be used as an analog front-end device for processing minute sensor signals. The RAA730301 uses a Serial Peripheral Interface (SPI) to allow external devices to control each on-chip circuit, enabling a more compact package and a reduction in the number of control pins. The compact package used by the RAA730301—a 48-pin LQFP—in turns enables a more compact set design.

Features

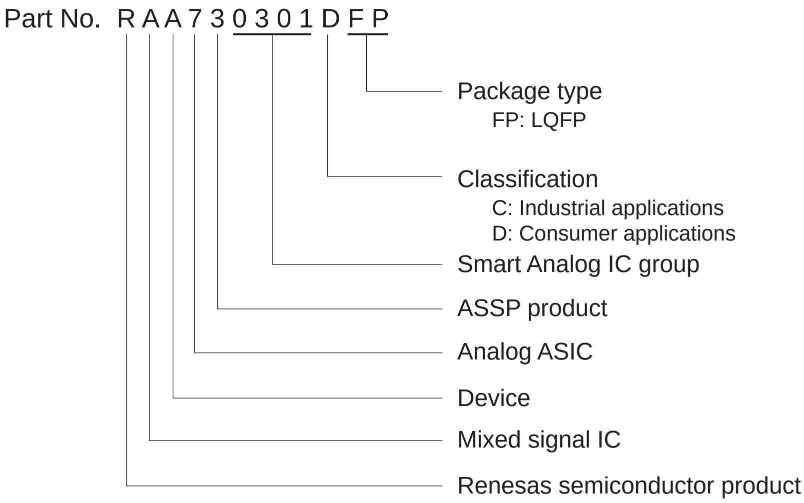
- On-chip instrumentation amplifier × 1 ch
- On-chip D/A converter × 1 ch
- On-chip variable output voltage regulator × 1 ch
- On-chip temperature sensor × 1 ch
- On-chip SPI × 1 ch
- Includes a low-current mode.
- Operating voltage range: 2.2 V ≤ V_{DD} ≤ 3.6 V
- Operating temperature range: –40°C ≤ T_A ≤ 105°C
- Package: 48-pin plastic LQFP (fine pitch) (7 × 7)

Applications

- Home appliances
- Industrial equipment
- Healthcare equipment

Ordering Information

Pin count	Package	Part Number
48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	RAA730301CFP, RAA730301DFP



How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electrical engineering, electronic circuits.

- To gain a general understanding of functions:
  →Read this manual in the order of the CONTENTS.
- To check the revised points :
  →The mark <R> shows major revised points. The revised points can be easily searched by copying an “<R>” in the PDF file and specifying it in the “Find what: ” field.

Conventions

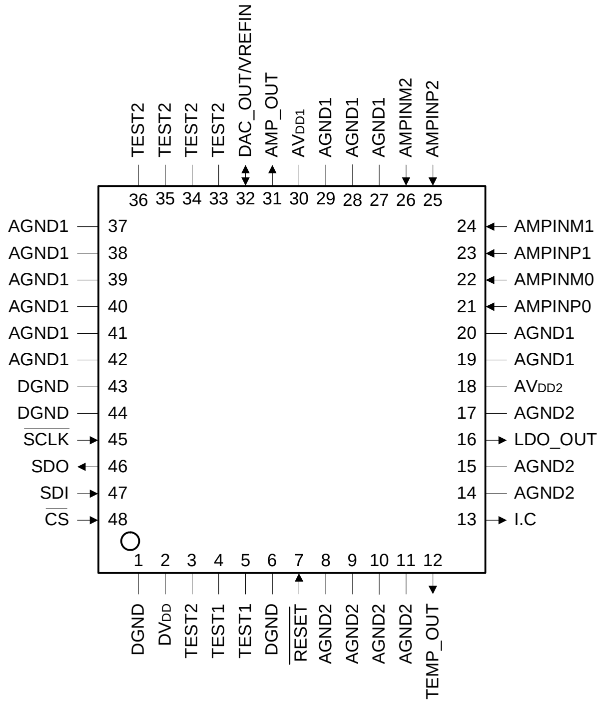
Data significance	: Higher digits on the left and lower digits on the right
Active low representations	: $\overline{\text{xxx}}$ (overscore over pin and signal name)
Note	: Footnote for item marked with Note in the text
Caution	: Information requiring particular attention
Remark	: Supplementary information
Numerical representations	: Binary ...xxxx or xxxxB Decimal ...xxxx Hexadecimal ...xxxxH

Contents

1. Pin Configuration

1.1 Pin Layout

- 48-pin plastic LQFP (fine pitch) (7 x 7)



Cautions 1. Make the potential of AGND1, AGND2 and DGND the same.

2. Make the potential of AV_{DD1}, AV_{DD2} and DV_{DD} the same.

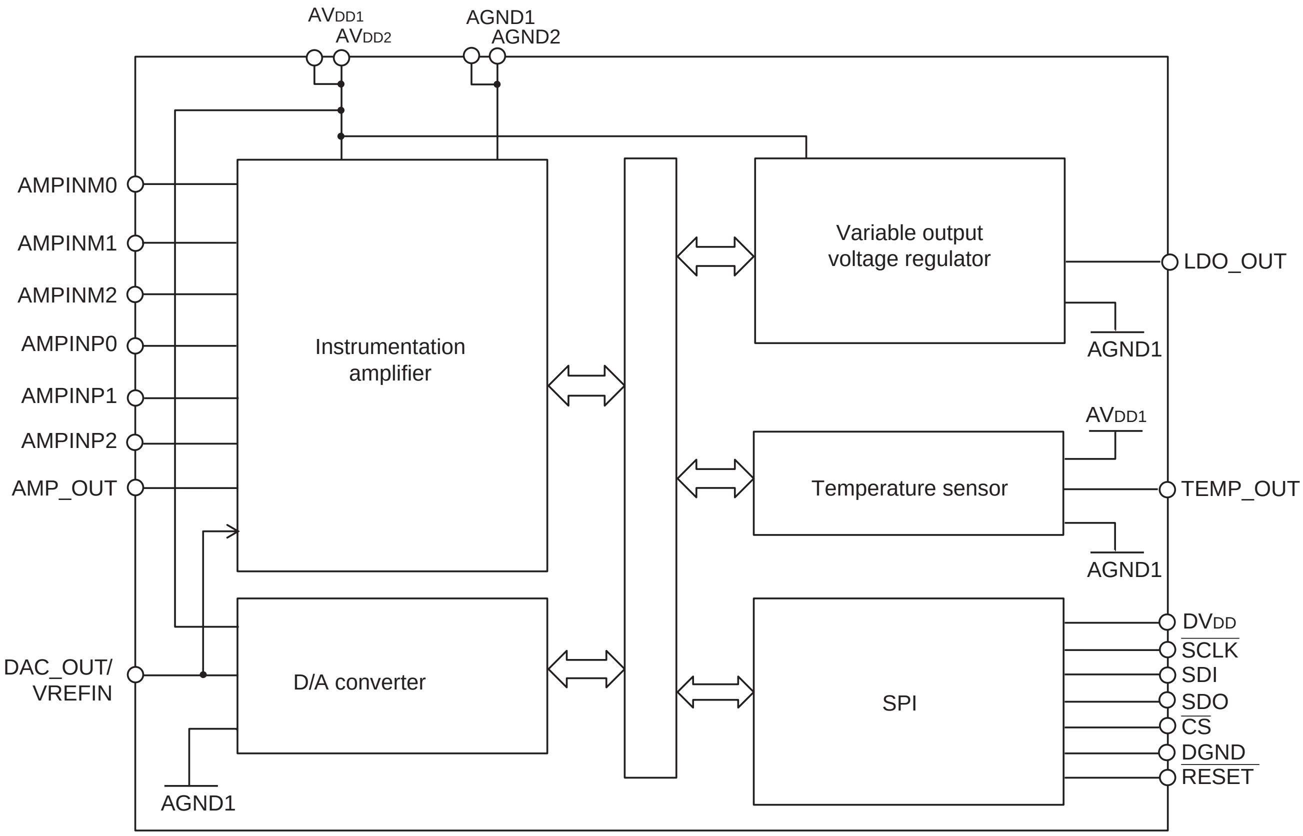
3. Connect the LDO_OUT pin to AGND2 via a capacitor (1.0 μF: recommended).

4. Connect the TEST1 pins to DGND.

5. Connect the I.C pin to AGND2.

6. Leave the TEST2 pins open.

1.2 Block Diagram



1.3 Pin Functions

Table 1-1 Pin Functions (1/2)

Pin No.	Pin Name	I/O	Pin Functions
1	DGND	–	GND pin for SPI
2	DV_{DD}	–	Power supply pin for SPI
3	TEST2	–	Test pins
4	TEST1	–	
5	TEST1	–	
6	DGND	–	GND pin for SPI
7	$\overline{RESET}$	Input	External reset pin
8	AGND2	–	GND pins for analog block (instrumentation amplifier, D/A converter, variable output voltage regulator, temperature sensor)
9	AGND2	–	
10	AGND2	–	
11	AGND2	–	
12	TEMP_OUT	Output	Temperature sensor output pin
13	I.C	–	–
14	AGND2	–	GND pins for analog block (instrumentation amplifier, D/A converter, variable output voltage regulator, temperature sensor)
15	AGND2	–	
16	LDO_OUT	Output	Variable output voltage regulator output pin
17	AGND2	–	GND pin for analog block (instrumentation amplifier, D/A converter, variable output voltage regulator, temperature sensor)
18	AV_{DD2}	–	Power supply pin for analog block (instrumentation amplifier, D/A converter, variable output voltage regulator, temperature sensor)
19	AGND1	–	GND pins for analog block (instrumentation amplifier, D/A converter, variable output voltage regulator, temperature sensor)
20	AGND1	–	
21	AMPINP0	Input	Instrumentation amplifier input pin 0 (+)
22	AMPINM0	Input	Instrumentation amplifier input pin 0 (–)
23	AMPINP1	Input	Instrumentation amplifier input pin 1 (+)
24	AMPINM1	Input	Instrumentation amplifier input pin 1 (–)
25	AMPINP2	Input	Instrumentation amplifier input pin 2 (+)
26	AMPINM2	Input	Instrumentation amplifier input pin 2 (–)
27	AGND1	–	GND pins for analog block (instrumentation amplifier, D/A converter, variable output voltage regulator, temperature sensor)
28	AGND1	–	
29	AGND1	–	
30	AV_{DD1}	–	Power supply pin for analog block (instrumentation amplifier, D/A converter, variable output voltage regulator, temperature sensor)
31	AMP_OUT	Output	Instrumentation amplifier output pin
32	DAC_OUT/ VREFIN	Output /Input	D/A converter analog voltage output pin/instrumentation amplifier reference voltage input pin
33	TEST2	–	Test pins
34	TEST2	–	
35	TEST2	–	
36	TEST2	–	

Table 1-1 Pin Functions (2/2)

Pin No.	Pin Name	I/O	Pin Functions
37	AGND1	–	GND pins for analog block (instrumentation amplifier, D/A converter, variable output voltage regulator, temperature sensor)
38	AGND1	–	
39	AGND1	–	
40	AGND1	–	
41	AGND1	–	
42	AGND1	–	
43	DGND	–	GND pins for SPI
44	DGND	–	
45	$\overline{\text{SCLK}}$	Input	Serial clock input pin for SPI
46	SDO	Output	Serial data output pin for SPI
47	SDI	Input	Serial data input pin for SPI
48	$\overline{\text{CS}}$	Input	Chip select input pin for SPI

1.4 Connection of Unused Pins

Table 1-2 Connection of Unused Pins

Pin No.	I/O	Recommended Connection of Unused Pins
TEMP_OUT	Output	Leave open.
AMPINP0	Input	Connect to AGND1.
AMPINM0	Input	
AMPINP1	Input	
AMPINM1	Input	
AMPINP2	Input	
AMPINM2	Input	
AMP_OUT	Output	Leave open.
DAC_OUT/VREFIN	Output /Input	
$\overline{\text{SCLK}}$	Input	Connect to Ground.[Note]
SDO	Output	Leave open.
SDI	Input	Connect to Ground.[Note]
$\overline{\text{CS}}$	Input	
LDO_OUT	Output	Leave open.
$\overline{\text{RESET}}$	Input	Connect to DV_{DD} directly or via a resistor.

Note Ground means the same electrical potential as AGND1, AGND2 and DGND.

1.5 Pin I/O Circuits

Figure 1-1. Pin I/O Circuit Type (1/2)

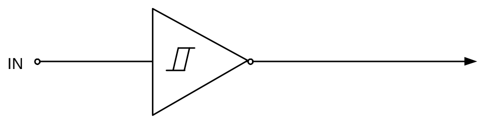
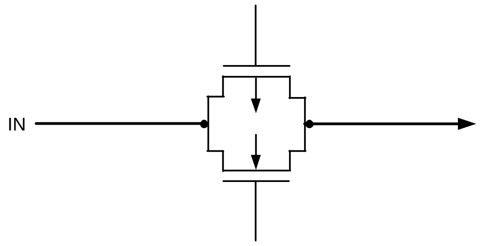
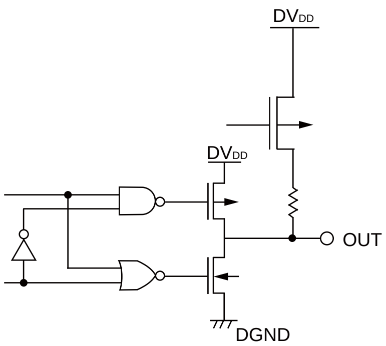
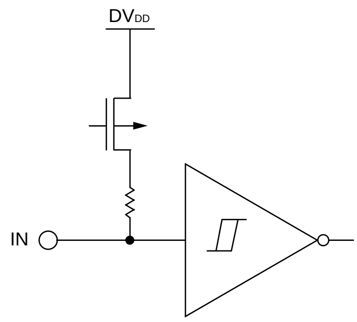
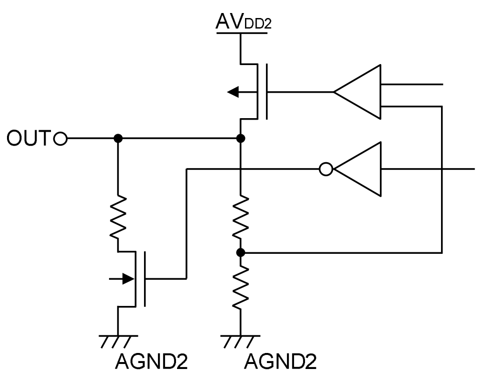
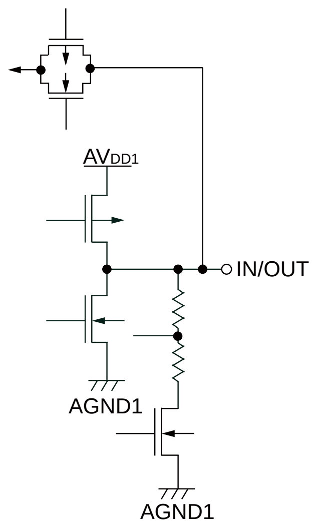
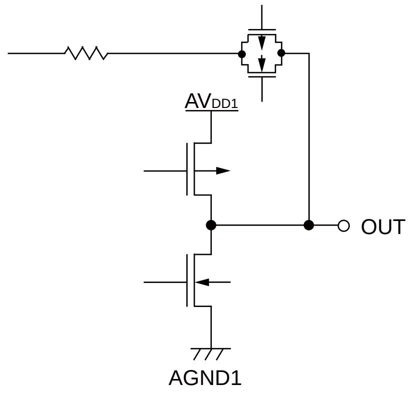
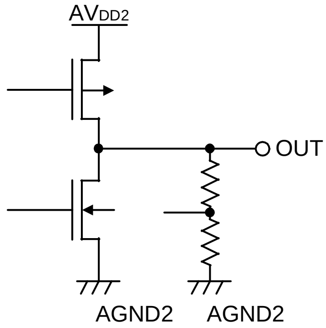
Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
$\overline{RESET}$	 Schmitt-triggered input with hysteresis characteristics	AMPINP0 AMPINM0 AMPINP1 AMPINM1 AMPINP2 AMPINM2	
SDO		$\overline{SCLK}$ SDI $\overline{CS}$	 Schmitt-triggered input with hysteresis characteristics
LDO_OUT		DAC_OUT/ VREFIN	

Figure 1-1. Pin I/O Circuit Type (2/2)

Pin Name	Equivalent Circuit	Pin Name	Equivalent Circuit
AMP_OUT		TEMP_OUT	

2. Instrumentation Amplifier

The RAA730301 has one on-chip instrumentation amplifier channel.

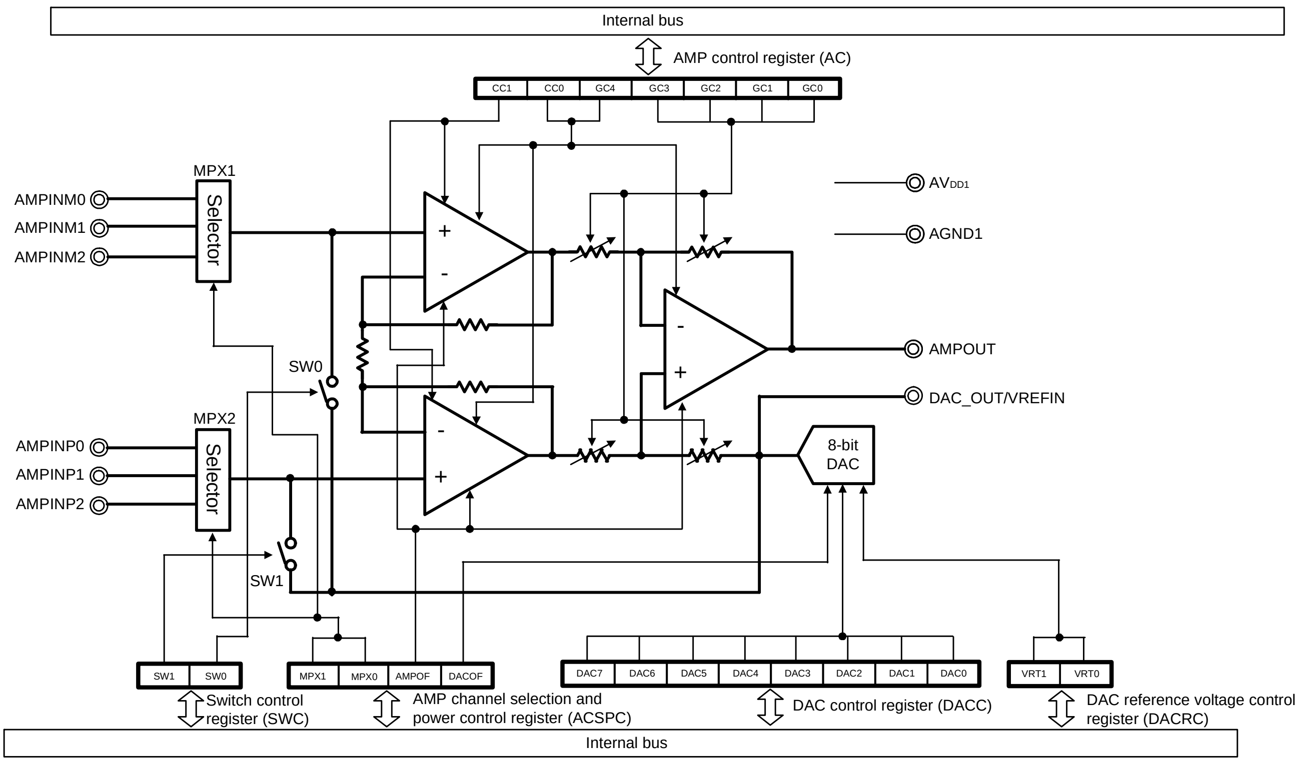
<R> 2.1 Overview of Instrumentation Amplifier Features

The instrumentation amplifier has the following features:

- The gain can be specified between 6 dB and 34 dB in 15 steps.
- Includes an input mode switching function.
- Four operating modes are available.
- Includes a power-off function.

And also, the output signal from D/A converter can be used as the reference voltage for instrumentation amplifier. If D/A converter is powered off, the external reference voltage is to be input to DAC_OUT/VREFIN pin. For details about use of D/A converter, see **3. D/A Converter**.

2.2 Block Diagram



2.3 Registers Controlling the Instrumentation Amplifier

The instrumentation amplifier is controlled by the following 3 registers:

- AMP control register (AC)
- AMP channel selection and power control register (ACSPC)
- Switch control register (SWC)

(1) AMP control register (AC)

This register is used to specify the operating mode, input mode, and the gain of the instrumentation amplifier.
Reset signal input clears this register to 00H.

Address: 01H Reset: 00H R/W

	7	6	5	4	3	2	1	0
AC	AIMS	CC1	CC0	0	GC3	GC2	GC1	GC0

AIMS	Input mode of instrumentation amplifier
0	Rail-to-rail input mode
1	P-ch single-ended input mode

CC1	CC0	Operation mode of instrumentation amplifier
0	0	High-speed mode
0	1	Mid-speed mode 2
1	0	Mid-speed mode 1
1	1	Low-speed mode

GC3	GC2	GC1	GC0	Gain (Typ.)
0	0	0	0	6 dB
0	0	0	1	8 dB
0	0	1	0	10 dB
0	0	1	1	12 dB
0	1	0	0	14 dB
0	1	0	1	16 dB
0	1	1	0	18 dB
0	1	1	1	20 dB
1	0	0	0	22 dB
1	0	0	1	24 dB
1	0	1	0	26 dB
1	0	1	1	28 dB
1	1	0	0	30 dB
1	1	0	1	32 dB
1	1	1	0	34 dB
Other than above				Setting prohibited

Remark Bit 4 can be set to 1, but this has no effect on the function.

(2) AMP channel selection and power control register (ACSPC)

This register is used to select the instrumentation amplifier input channel and enable or disable operation of the instrumentation amplifier, D/A converter, variable output voltage regulator, and temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When using the instrumentation amplifier, be sure to set bit 3 to 1.
Reset signal input clears this register to 00H.

Address: 04H Reset: 00H R/W

	7	6	5	4	3	2	1	0
ACSPC	MPX1	MPX0	0	0	AMPOF	DACOF	LDOOF	TEMOF

MPX1	MPX0	Source of instrumentation amplifier input
0	0	AMPINP0 pin and AMPINM0 pin
0	1	AMPINP1 pin and AMPINM1 pin
1	0	AMPINP2 pin and AMPINM2 pin
1	1	Open pin

AMPOF	Operation of instrumentation amplifier
0	Stop operation of the instrumentation amplifier.
1	Enable operation of the instrumentation amplifier.

Remark Bits 5 and 4 can be set to 1, but this has no effect on the function.

(3) Switch control register (SWC)

This register is used to specify whether to turn on or off switches SW0 and SW1, which are used to measure the offset voltage of the instrumentation amplifier.
Reset signal input clears this register to 00H.

Address: 06H After reset: 00H R/W

	7	6	5	4	3	2	1	0
SWC	0	0	0	0	0	0	SW1	SW0

SW1	Control of SW1
0	Turn off SW1.
1	Turn on SW1.

SW0	Control of SW0
0	Turn off SW0.
1	Turn on SW0.

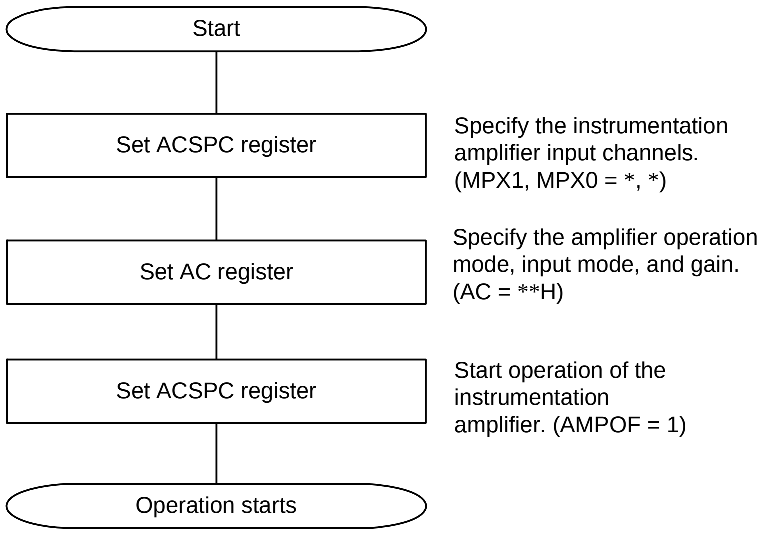
Remark Bits 7 to 2 can be set to 1, but this has no effect on the function.

Caution Be sure to set both bit 7 and bit 6 of the ACSPC register to 1, before setting bit 1 or bit 0 of the SWC register to 1.

2.4 Procedure for Operating the Instrumentation Amplifier

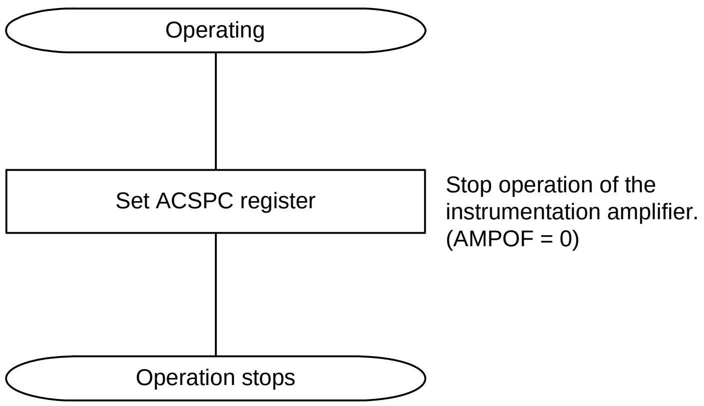
Follow the procedures below to start and stop the instrumentation amplifier.

Example of procedure for starting the instrumentation amplifier



Remark *: don't care

Example of procedure for stopping the instrumentation amplifier



3. D/A Converter

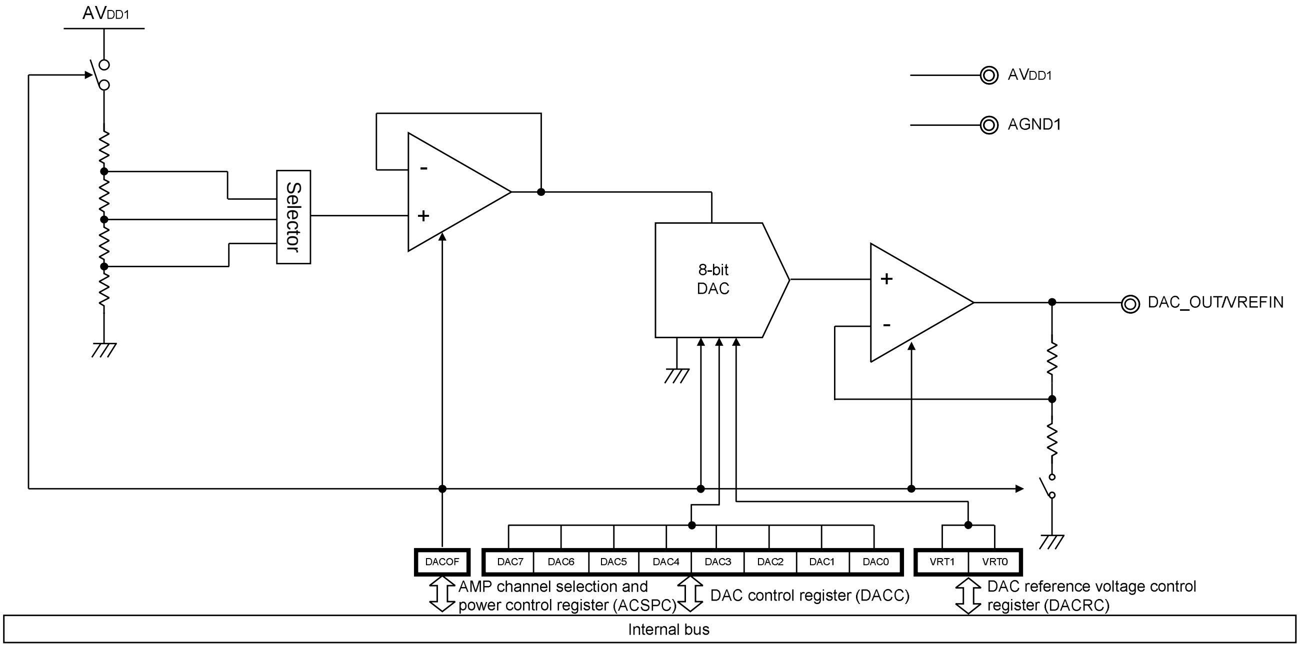
The RAA730301 has one on-chip D/A converter channel.

<R> 3.1 Overview of D/A Converter Features

The D/A converter is an 8-bit resolution converter that converts digital input signals into analog signals.
The D/A converter has the following features:

- 8-bit resolution
- R-2R ladder method
- Analog output voltage: Output voltage can be calculated with the equation shown below.
  Output voltage = Reference voltage upper limit × m/256 (m = 0 to 255: Value set to DACC register)
- Controls the reference voltage for the instrumentation amplifier
- Includes a power-off function

3.2 Block Diagram



3.3 Registers Controlling the D/A Converter

The D/A converter is controlled by the following 3 registers:

- DAC control register (DACC)
- DAC reference voltage control register (DACRC)
- AMP channel selection and power control register (ACSPC)

(1) DAC control register (DACC)

This register is used to specify the analog voltage output from D/A converter.
The output signal from D/A converter can be used as the reference voltage for the instrumentation amplifier.
Reset signal input sets this register to 80H.

Address: 00H Reset: 80H R/W

	7	6	5	4	3	2	1	0
DACC	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

Remark To calculate the output voltage, see **3. 1 Overview of D/A converter features**.

<R> (2) DAC reference voltage control register (DACRC)

This register is used to specify the upper limit (VRT) of the reference voltage for the D/A converter.
Reset signal input clears this register to 00H.

Address: 03H Reset: 00H R/W

	7	6	5	4	3	2	1	0
DACRC	0	0	0	0	0	0	VRT1	VRT0

VRT1	VRT0	Reference voltage upper limit (Typ.)
0	0	AV_{DD1}
0	1	$AV_{DD1} \times 4/5$
1	0	$AV_{DD1} \times 3/5$
1	1	AV_{DD1}

Remark Bits 7 to 2 can be set to 1, but this has no effect on the function.

(3) AMP channel selection and power control register (ACSPC)

This register is used to select the instrumentation amplifier input channel and enable or disable operation of the instrumentation amplifier, D/A converter, variable output voltage regulator, and temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When using the D/A converter, be sure to set bit 2 to 1.
Reset signal input clears this register to 00H.

Address: 04H Reset: 00H R/W

	7	6	5	4	3	2	1	0
ACSPC	MPX1	MPX0	0	0	AMPOF	DACOF	LDOOF	TEMOF

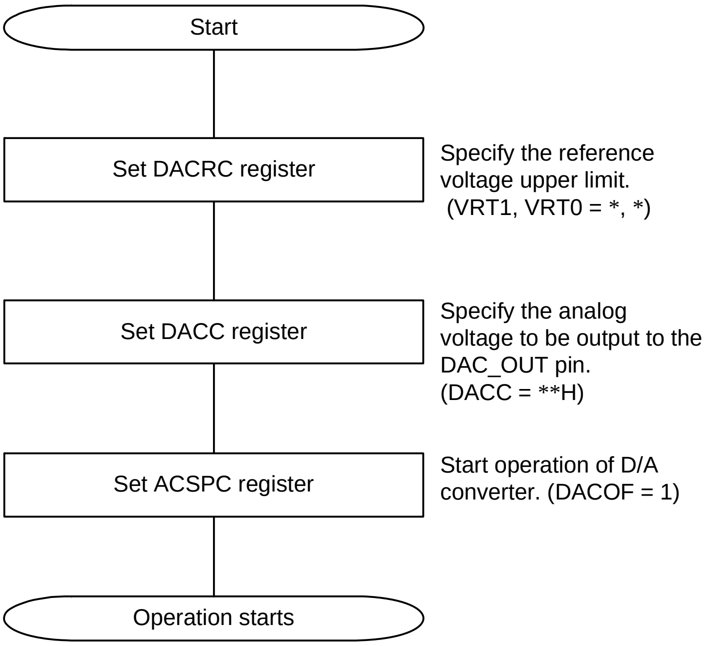
DACOF	Operation of D/A converter
0	Stop operation of the D/A converter.
1	Enable operation of the D/A converter.

Remark Bits 5 and 4 can be set to 1, but this has no effect on the function.

3.4 Procedure for Operating the D/A Converter

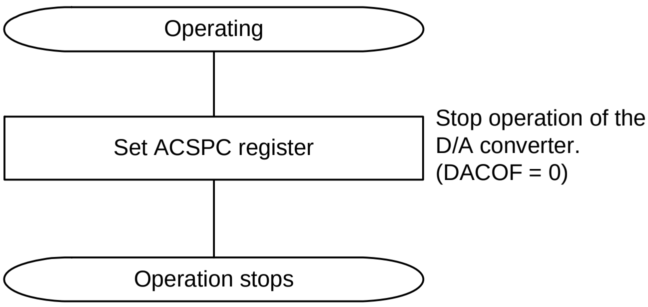
Follow the procedures below to start and stop the D/A converter.

Example of procedure for starting the D/A converter



Remark *: don't care

Example of procedure for stopping the D/A converter



3.5 Notes on Using the D/A Converter

Observe the following points when using the D/A converter:

(1) Only a very small current can flow from the DAC_OUT pin because the output impedance of the D/A converter is high. If the load input impedance is low, insert a follower amplifier between the load and the DAC_OUT pin. Also, make sure that the wiring between the pin and the follower amplifier or load is as short as possible (because of the high output impedance). If it is not possible to keep the wiring short, take measures such as surrounding the pin with a ground pattern.

(2) If inputting an external reference power supply to the VREFIN pin, be sure to set the DACOF bit to 0.

4. Temperature Sensor

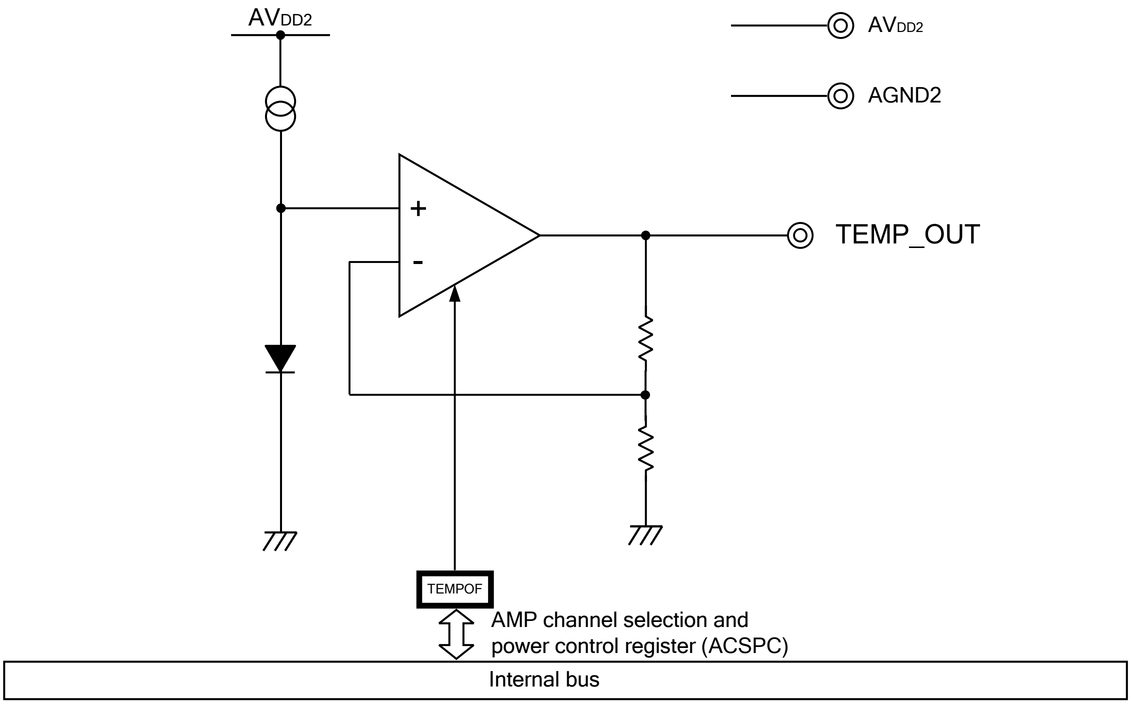
The RAA730301 has one on-chip temperature sensor channel.

4.1 Overview of Temperature Sensor Features

The temperature sensor has the following features:

- Output voltage temperature coefficient: –4 mV/°C (Typ.)
- Includes a power-off function

4.2 Block Diagram



4.3 Registers Controlling the Temperature Sensor

The temperature sensor is controlled by the AMP channel selection and power control register (ACSPC).

(1) AMP channel selection and power control register (ACSPC)

This register is used to select the instrumentation amplifier input channel and enable or disable operation of the instrumentation amplifier, D/A converter, variable output voltage regulator, and temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When selecting the signal to be input to the temperature sensor, be sure to set bit 0 to 1.
Reset signal input clears this register to 00H.

Address: 04H Reset: 00H R/W

	7	6	5	4	3	2	1	0
ACSPC	MPX1	MPX0	0	0	AMPOF	DACOF	LDOOF	TEMPOF

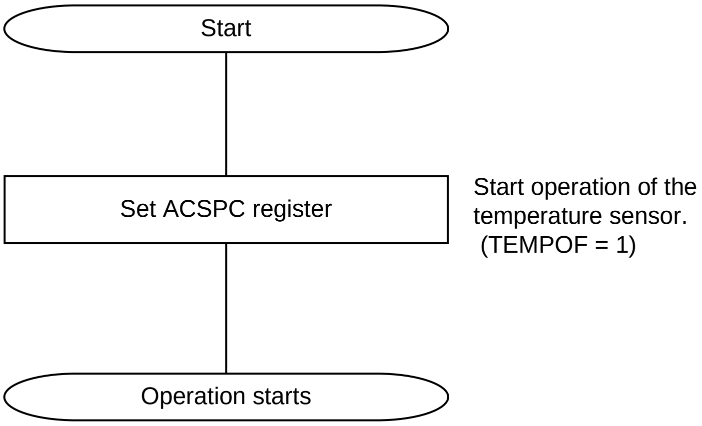
TEMPOF	Operation of temperature sensor
0	Stop operation of the temperature sensor.
1	Enable operation of the temperature sensor.

Remark Bits 5 to 4 can be set to 1, but this has no effect on the function.

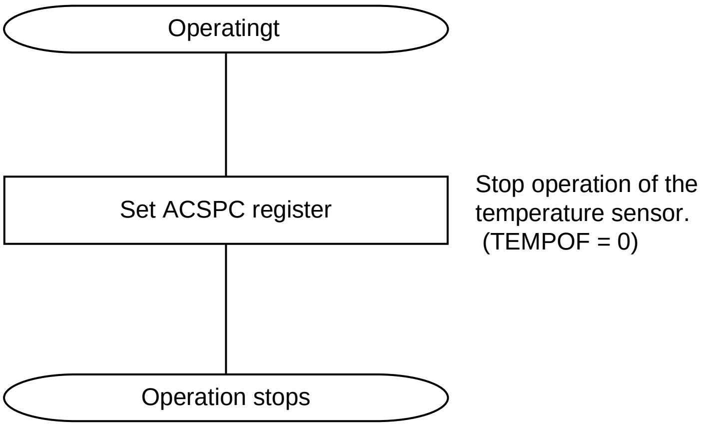
4.4 Procedure for Operating the Temperature Sensor

Follow the procedures below to start and stop the temperature sensor.

Example of procedure for starting the temperature sensor



Example of procedure for stopping the temperature sensor



5. Variable Output Voltage Regulator

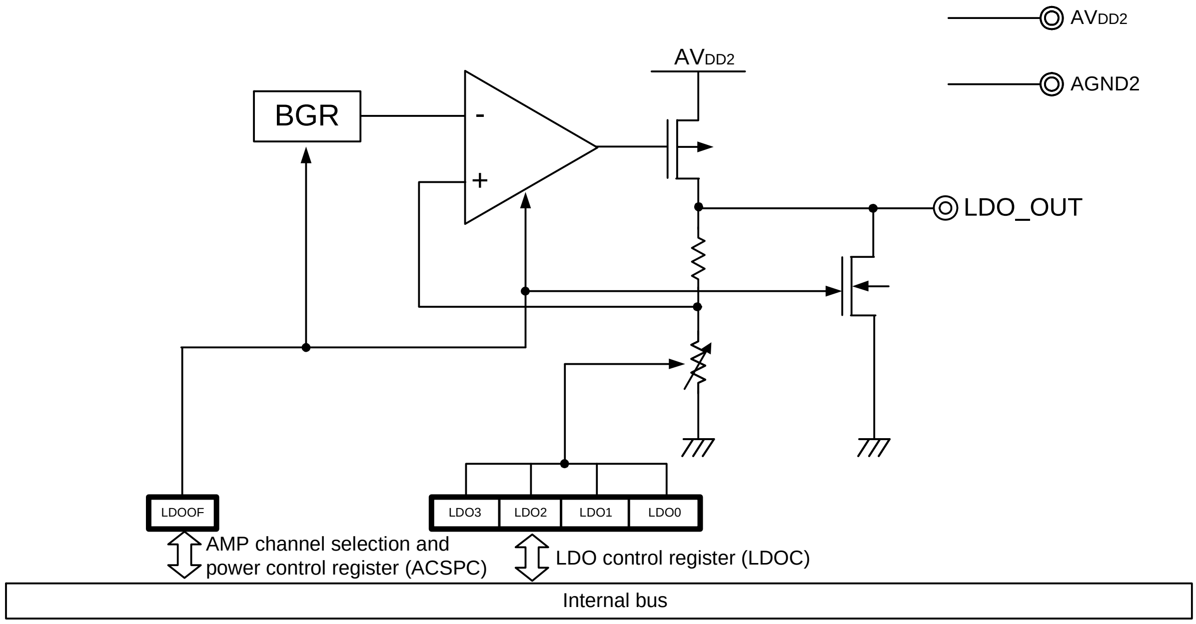
The RAA730301 has one on-chip variable output voltage regulator channel. This is a series regulator that generates a voltage of 1.8 V (default) from a supplied voltage of 3 V.

5.1 Overview of Variable Output Voltage Regulator Features

The variable output voltage regulator has the following features:

- Output voltage range: 1.8 to 3.1 V (Typ.)
- Output current: 15 mA (Max.)
- Includes a power-off function.

5.2 Block Diagram



5.3 Registers Controlling the Variable Output Voltage Regulator

The variable output voltage regulator is controlled by the following 2 registers:

- LDO control register (LDOC)
- AMP channel selection and power control register (ACSPC)

(1) LDO control register (LDOC)

This register is used to specify the output voltage of the variable output voltage regulator.
Reset signal input sets this register to 00H.

Address: 02H Reset: 00H R/W

	7	6	5	4	3	2	1	0
LDOC	0	0	0	0	LDO3	LDO2	LDO1	LDO0

LDO3	LDO2	LDO1	LDO0	Output voltage of variable output voltage regulator (Typ.)[Note]
0	0	0	0	1.8 V
0	0	0	1	1.9 V
0	0	1	0	2.0 V
0	0	1	1	2.1 V
0	1	0	0	2.2 V
0	1	0	1	2.3 V
0	1	1	0	2.4 V
0	1	1	1	2.5 V
1	0	0	0	2.6 V
1	0	0	1	2.7 V
1	0	1	0	2.8 V
1	0	1	1	2.9 V
1	1	0	0	3.0 V
1	1	0	1	3.1 V
Other than above				Setting prohibited

Note Output voltage is determined in consideration of dropout voltage.

Remark Bits 7 to 4 can be set to 1, but this has no effect on the function.

(2) AMP channel selection and power control register (ACSPC)

This register is used to select the instrumentation amplifier input channel and enable or disable operation of the instrumentation amplifier, D/A converter, variable output voltage regulator, and temperature sensor.
Use this register to stop unused functions to reduce power consumption and noise.
When using the variable output voltage regulator, be sure to set bit 1 to 1.
Reset signal input clears this register to 00H.

Address: 04H Reset: 00H R/W

	7	6	5	4	3	2	1	0
ACSPC	MPX1	MPX0	0	0	AMPOF	DACOF	LDOOF	TMPOF

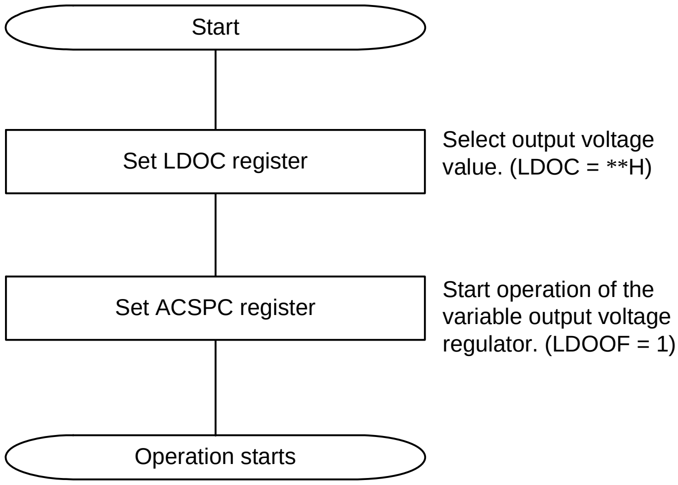
LDOOF	Operation of variable output voltage regulator
0	Stop operation of the variable output voltage regulator.
1	Enable operation of the variable output voltage regulator.

Remark Bits 5 and 4 can be set to 1, but this has no effect on the function.

5.4 Procedure for Operating the Variable Output Voltage Regulator

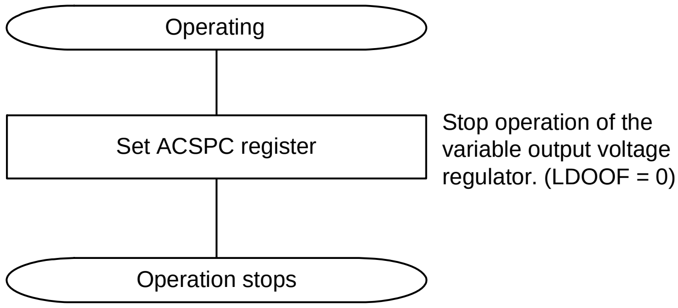
Follow the procedures below to start and stop the variable output voltage regulator.

Example of procedure for starting the variable output voltage regulator



Remark *: don't care

Example of procedure for stopping the variable output voltage regulator



<R> 6. SPI

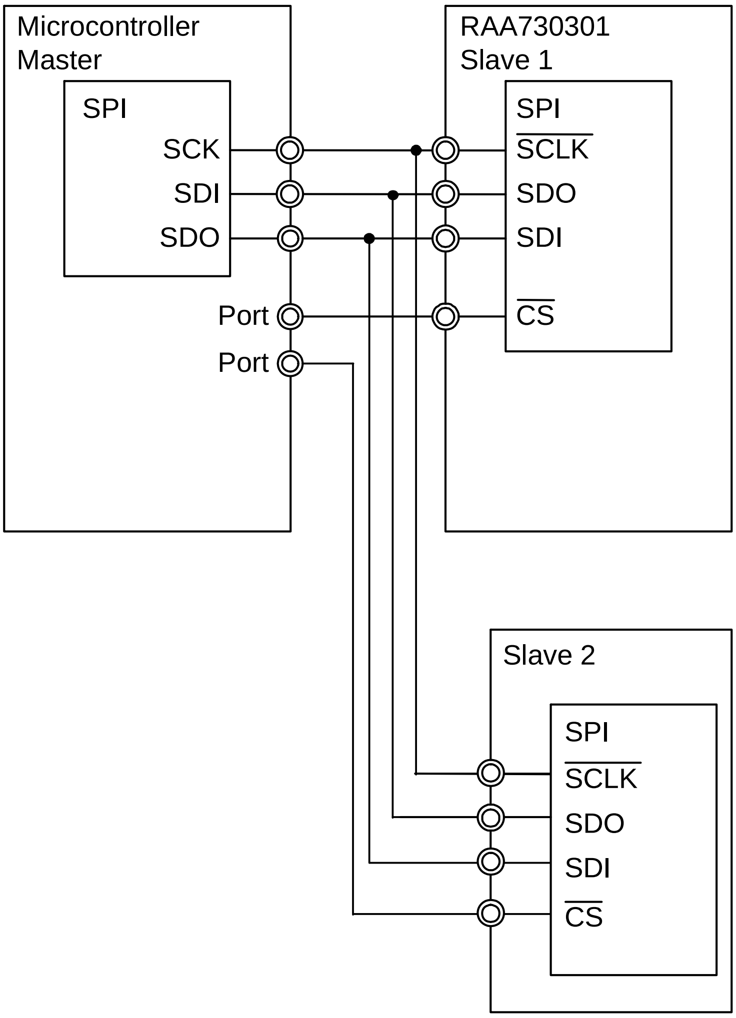
6.1 Overview of SPI Features

The SPI is used to allow control from external devices by using clocked communication via four lines: a serial clock line ($\overline{SCLK}$), two serial data lines (SDI and SDO), and a chip select input line ($\overline{CS}$).

Data transmission/reception:

- 16-bit data unit
- MSB first

Figure 6-1. SPI Configuration Example



Caution After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{RESET}$ pin before starting SPI communication. For details, see 7 Reset.

6.2 SPI Communication

The SPI transmits and receives data in 16-bit units. Data can be transmitted and received when $\overline{\text{CS}}$ is low. Data is transmitted one bit at a time in synchronization with the falling edge of the serial clock, and is received one bit at a time in synchronization with the rising edge of the serial clock. When the R/W bit is 1, data is written to the SPI control register in accordance with the address/data setting after the 16th rising edge of $\overline{\text{SCLK}}$ has been detected following the fall of $\overline{\text{CS}}$. The operation specified by the data is then executed. When the R/W bit is 0, the data is output from the register in accordance with the address/data setting in synchronization with the 9th and later falling edges of $\overline{\text{SCLK}}$ following the fall of $\overline{\text{CS}}$.

Figure 6-2. SPI Communication Timing

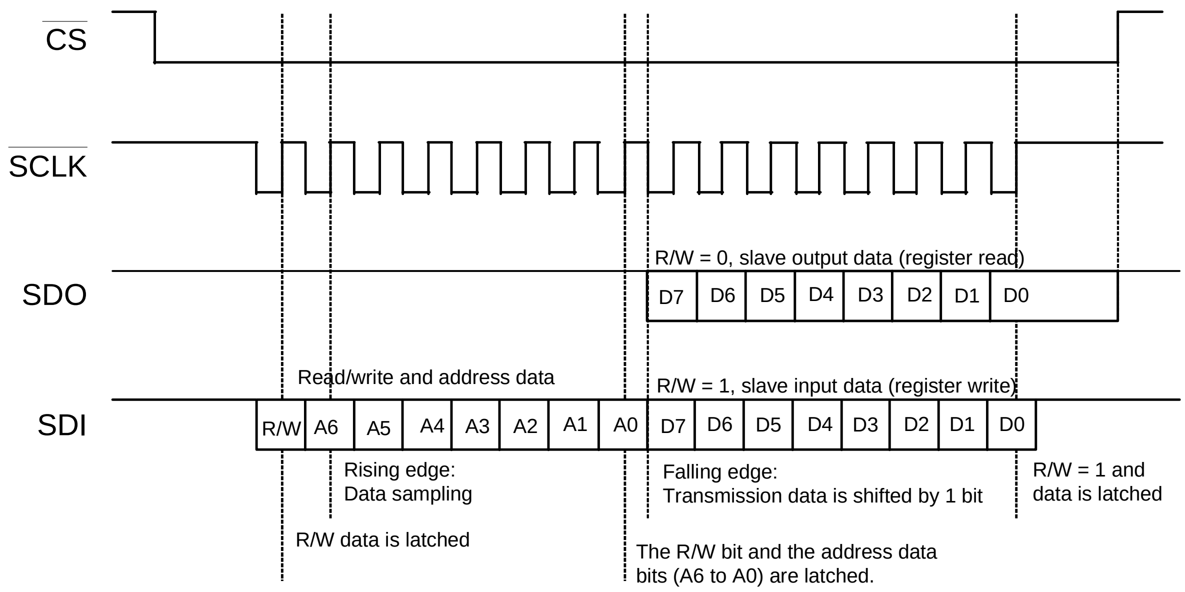


Table 6-1. SPI Control Registers

	Address	SPI Control Registers	R/W	After Reset
	00H	DAC control register (DACC)	R/W	80H
	01H	AMP control register (AC)	R/W	00H
	02H	LDO control register (LDOC)	R/W	00H
	03H	DAC reference voltage control register (DACRC)	R/W	00H
	04H	AMP channel selection and power control register (ACSPC)	R/W	00H
<R>	05H	Reset control register (RC)	R/W	00H[Note]
<R>	06H	Switch control register (SWC)	R/W	00H

Note The reset control register (RC) is not initialized to 00H by generating internal reset of the reset control register (RC). For details, see **7. Reset**.

<R> 7. Reset

7.1 Overview of Reset Feature

The RAA730301 has an on-chip reset function. The SPI control registers are initialized by reset. A reset can be generated in the following two ways:

- External reset by inputting an external reset signal to the $\overline{\text{RESET}}$ pin
- Internal reset by writing 1 to the RESET bit of the reset control register (RC)

The functions of the external reset and the internal reset are described below.

- After turning on DV_{DD}, be sure to generate external reset by inputting a reset signal to $\overline{\text{RESET}}$ pin before starting SPI communication.
- During reset, each function is shifted to the status shown in Table 7-1. The status of each SPI control register after reset has been acknowledged is shown in Table 7-2. After reset, the status of each pin is shown in Table 7-3.
- External reset is generated when a low-level signal is input to the $\overline{\text{RESET}}$ pin. On the other hand, internal reset is generated when 1 is written to the RESET bit of the reset control register (RC).
- External reset is subsequently cancelled by inputting a high-level signal to $\overline{\text{RESET}}$ pin after a low-level signal is input to this pin. On the other hand, internal reset is subsequently cancelled by writing 0 to the RESET bit of the reset control register (RC) after 1 is written to the same bit of this register.

Caution When generating an external reset, input a low-level signal to the $\overline{\text{RESET}}$ pin for at least 10 μs.

Table 7-1. Statuses During Reset

Function Block	External Reset from $\overline{\text{RESET}}$ Pin	Internal Reset by Reset Control Register (RC)
Instrumentation amplifier	Operation stops.	
D/A converter	Operation stops.	
Temperature sensor	Operation stops.	
Variable output voltage regulator	Operation stops.	
SPI	Operation stops.	Operation is enabled.

Table 7-2. Statuses of SPI Control Registers After a Reset Is Acknowledged

Address	SPI Control Register	Status After a Reset Is Acknowledged	
		External Reset	Internal Reset
00H	DAC control register (DACC)	80H	80H
01H	AMP control register (AC)	00H	00H
02H	LDO control register (LDOC)	00H	00H
03H	DAC reference voltage control register (DACRC)	00H	00H
04H	AMP channel selection and power control register (ACSPC)	00H	00H
05H	Reset control register (RC)	00H	01H[Note]
06H	Switch control register (SWC)	00H	00H

Note The reset control register (RC) is not initialized by generating internal reset of the reset control register (RC), but it can be done to 00H by generating external reset from $\overline{\text{RESET}}$ pin or by writing 0 to the RESET bit of the reset control register (RC).

Table 7-3. Pin Statuses After a Reset

Pin Name	External Reset from $\overline{\text{RESET}}$ Pin	Internal Reset by Reset Control Register (RC)
TEMP_OUT	Pull-down	Pull-down
LDO_OUT	Pull-down	Pull-down
AMPINP0	Hi-Z	Hi-Z
AMPINM0	Hi-Z	Hi-Z
AMPINP1	Hi-Z	Hi-Z
AMPINM1	Hi-Z	Hi-Z
AMPINP2	Hi-Z	Hi-Z
AMPINM2	Hi-Z	Hi-Z
AMP_OUT	Hi-Z	Hi-Z
DAC_OUT/VREFIN	Hi-Z	Hi-Z
$\overline{\text{SCLK}}$	Pull-up input	Hi-Z
SDO	Pull-up	Hi-Z
SDI	Pull-up input	Hi-Z
$\overline{\text{CS}}$	Pull-up input	Hi-Z

7.2 Registers Controlling the Reset Feature

(1) Reset control register (RC)

This register is used to control the reset feature.

An internal reset can be generated by writing 1 to the RESET bit. The reset control register (RC) is initialized to 00H by generating external reset from $\overline{\text{RESET}}$ pin or by writing 0 to the RESET bit of the reset control register (RC).

Address: 05H Reset: 00H[Note] R/W

	7	6	5	4	3	2	1	0
RC	0	0	0	0	0	0	0	RESET

RESET	Reset request by internal reset signal
0	Do not make a reset request by using the internal reset signal, or cancel the reset.
1	Make a reset request by using the internal reset signal, or the reset signal is currently being input.

Note The reset control register (RC) is not initialized by generating internal reset of the reset control register (RC), but it can be done to 00H by generating external reset from $\overline{\text{RESET}}$ pin or by writing 0 to the RESET bit of the reset control register (RC).

Caution When the RESET bit is 1, writing to any register other than the reset control register (RC) is ignored. Initializing the reset control register (RC) to 00H by external reset, or writing 0 to the RESET bit enable writing to all the registers.

Remark Bits 7 to 1 are fixed at 0 of read only.

8. Electrical Specifications

8.1 Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	AV_{DD}	AV_{DD1}, AV_{DD2}	–0.3 to +4.0	V
	DV_{DD}	DV_{DD}	–0.3 to +4.0	V
	AGND	AGND1, AGND2	–0.3 to +0.3	V
	DGND	DGND	–0.3 to +0.3	V
Input voltage	V_{I1}	AMPINM0, AMPINM1, AMPINM2, AMPINP0, AMPINP1, AMPINP2, $\overline{\text{RESET}}$, VREFIN	-0.3 to AV_{DD} + 0.3 Note	V
	V_{I2}	$\overline{\text{SCLK}}$, SDI, $\overline{\text{CS}}$, TEST	–0.3 to DV_{DD} + 0.3 Note	V
Output voltage	V_{O1}	AMP_OUT, DAC_OUT, TEMP_OUT, LDO_OUT	–0.3 to AV_{DD} + 0.3 Note	V
	V_{O2}	SDO	–0.3 to DV_{DD} + 0.3 Note	V
Output current	I_{O1}	AMP_OUT, DAC_OUT, TEMP_OUT	1	mA
	I_{O2}	SDO	±4	mA
	V_{LDO}	LDO_OUT	15	mA
Operating ambient temperature	T_A		–40 to +105	°C
<R> Storage temperature	T_{stg}		–40 to +125	°C

Note Must be 4.0 V or lower

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

<R> 8.2 Operating Condition

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Power supply voltage range	V_{DDOP}	AV_{DD1}, AV_{DD2}, DV_{DD}	+2.2	–	3.6	V
Operating temperature range	T_{OP}		–40	–	105	°C

8.3 Supply Current Characteristics

(–40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = DV_{DD} = 3.0 V)

Parameter	Symbol	Conditions		Ratings			Unit
				MIN	TYP	MAX	
Supply current	I_{stby1}[Note]	AMPOF = DACOF = LDOOF = TEMPOF = 0	T_A = 25°C	–	0.07	0.3	µA
			T_A = 85°C	–	0.4	2.1	µA
			T_A = 105°C	–	0.9	4.2	µA
	I_{m1}[Note]	AMPOF = DACOF = LDOOF = TEMPOF = 1, (instrumentation amplifier, D/A converter, variable output voltage regulator, and temperature sensor are operating), CC1, CC0 = 0, 0		–	1.25	1.9	mA
	I_{m2}[Note]	AMPOF = DACOF = LDOOF = TEMPOF = 1, (instrumentation amplifier, D/A converter, variable output voltage regulator, and temperature sensor are operating), CC1, CC0 = 0, 1		–	1.05	1.6	mA
	I_{m3}[Note]	AMPOF = DACOF = LDOOF = TEMPOF = 1, (instrumentation amplifier, D/A converter, variable output voltage regulator, and temperature sensor are operating), CC1, CC0 = 1, 0		–	0.85	1.3	mA
	I_{m4}[Note]	AMPOF = DACOF = LDOOF = TEMPOF = 1, (instrumentation amplifier, D/A converter, variable output voltage regulator, and temperature sensor are operating), CC1, CC0 = 1, 1		–	0.6	0.95	mA

Note Total current flowing to internal power supplies AV_{DD1}, AV_{DD2}, and DV_{DD}. Current flowing through the pull-up resistor is not included. The input leakage current flowing when the level of the input pin is fixed to AV_{DD1}, AV_{DD2} or DV_{DD}, or AGND1, AGND2 or DGND is included.

8.4 Electrical Specifications of Each Block

(1) Instrumentation amplifier

(–40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = DV_{DD} = 3.0 V, VREFIN = 1.5 V, AMPOF = 1, DACOF = 0)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	Icc00	CC1, CC0 = 0, 0	–	960	1400	μA
	Icc01	CC1, CC0 = 0, 1	–	750	1100	μA
	Icc10	CC1, CC0 = 1, 0	–	520	750	μA
	Icc11	CC1, CC0 = 1, 1	–	310	450	μA
Input voltage 1	VINL1	AIMS = 0	AGND1 – 0.05	–	–	V
	VINH1	AIMS = 0	–	–	AV_{DD1} + 0.1	V
Input voltage 2	VINL2	AIMS = 1	AGND1 – 0.05	–	–	V
	VINH2	AIMS = 1	–	–	AV_{DD1} – 1.4	V
Output voltage	VOUTL	IOL = –200 μA	–	–	AGND1 + 0.05	V
	VOUTH	IOH = 200 μA	AV_{DD1} – 0.05	–	–	V
Settling time	t_{SET_AMP00}	AC = 00H (6 dB), CC1, CC0 = 0, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	13	μs
	t_{SET_AMP01}	AC = 20H (6 dB), CC1, CC0 = 0, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	18	μs
	t_{SET_AMP10}	AC = 40H (6 dB), CC1, CC0 = 1, 0, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	32	μs
	t_{SET_AMP11}	AC = 60H (6 dB), CC1, CC0 = 1, 1, CL = 30 pF, output voltage = $1V_{PP}$, output convergence voltage V_{PP} = 999 mV	–	–	89	μs
Gain bandwidth	GBW00	C_{LMAX} = 30 pF, AC = 0EH (34 dB)	–	1.9	–	MHz
	GBW01	C_{LMAX} = 30 pF, AC = 2EH (34 dB)	–	1.65	–	MHz
	GBW10	C_{LMAX} = 30 pF, AC = 4EH (34 dB)	–	1.1	–	MHz
	GBW11	C_{LMAX} = 30 pF, AC = 6EH (34 dB)	–	0.5	–	MHz
Equivalent input noise	En00	AC = 0EH (34 dB), f = 1 kHz, CC1, CC0 = 0, 0	–	95	–	nV/√ Hz
	En01	AC = 2EH (34 dB), f = 1 kHz, CC1, CC0 = 0, 1	–	105	–	nV/√ Hz
	En10	AC = 4EH (34 dB), f = 1 kHz, CC1, CC0 = 1, 0	–	130	–	nV/√ Hz
	En11	AC = 6EH (34 dB), f = 1 kHz, CC1, CC0 = 1, 1	–	220	–	nV/√ Hz

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Input conversion offset voltage	VOFF00	T_A = 25°C, CC1, CC0 = 0, 0, GC3 to GC0 = 1, 0, 1, 0 (26 dB)	–7	–	7	mV
	VOFF01	T_A = 25°C, CC1, CC0 = 0, 1, GC3 to GC0 = 1, 0, 1, 0 (26 dB)	–10	–	10	mV
	VOFF10	T_A = 25°C, CC1, CC0 = 1, 0, GC3 o GC0 = 1, 0, 1, 0 (26 dB)	–10	–	10	mV
	VOFF11	T_A = 25°C, CC1, CC0 = 1, 1, GC3 to GC0 = 1, 0, 1, 0 (26 dB)	–12	–	12	mV
Input conversion offset voltage temperature coefficient	VOTC00	CC1, CC0 = 0, 0	–	±2.5	–	μV/°C
	VOTC01	CC1, CC0 = 0, 1	–	±2.5	–	μV/°C
	VOTC10	CC1, CC0 = 1, 0	–	±3.0	–	μV/°C
	VOTC11	CC1, CC0 = 1, 1	–	±4.0	–	μV/°C
Slew rate	SR00	CC1, CC0 = 0, 0, CL = 30 pF AC = 00H (6 dB)	–	1.2	–	V/μs
	SR01	CC1, CC0 = 0, 1, CL = 30 pF AC = 20H (6 dB)	–	0.9	–	V/μs
	SR10	CC1, CC0 = 1, 0, CL = 30 pF AC = 40H (6 dB)	–	0.55	–	V/μs
	SR11	CC1, CC0 = 1, 1, CL = 30 pF AC = 60H (6 dB)	–	0.25	–	V/μs
Common mode rejection ratio	CMRR00	AC = 0EH (34 dB), f = 1 kHz, CC1, CC0 = 0, 0	–	85	–	dB
	CMRR01	AC = 2EH (34 dB), f = 1 kHz, CC1, CC0 = 0, 1	–	85	–	dB
	CMRR10	AC = 4EH (34 dB), f = 1 kHz, CC1, CC0 = 1, 0	–	80	–	dB
	CMRR11	AC = 6EH (34 dB), f = 1 kHz, CC1, CC0 = 1, 1	–	75	–	dB
Power supply rejection ratio	PSRR00	AC = 00H (6 dB), f = 1 kHz, CC1, CC0 = 0, 0	–	70	–	dB
	PSRR01	AC = 20H (6 dB), f = 1 kHz, CC1, CC0 = 0, 1	–	70	–	dB
	PSRR10	AC = 40H (6 dB), f = 1 kHz, CC1, CC0 = 1, 0	–	70	–	dB
	PSRR11	AC = 60H (6 dB), f = 1 kHz, CC1, CC0 = 1, 1	–	70	–	dB
Gain setting error	GAIN_Accu1	T_A = 25°C	–0.8	–	0.8	dB
	GAIN_Accu2	T_A = –40 to 105°C	–1.2	–	1.2	dB

(2) D/A converter

(–40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = DV_{DD} = 3.0 V, DACOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
DAC ON current consumption	I_{DAC_ON}		–	270	400	µA
Resolution	R_{ES}		–	–	8	bit
Settling time	t_{SET}		–	–	50	µs
Differential non-linearity error Note	DNL	VRT1 = VRT0 = 0	–2	–	2	LSB
Integral non-linearity error	INL	VRT1 = VRT0 = 0	–2	–	2	LSB

Note Guaranteed monotonic.

(3) Temperature sensor

(–40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = DV_{DD} = 3.0 V, TEMPOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccA		–	90	140	µA
Output voltage	V_O	T_A = 25°C	–	1.28	–	V
Temperature sensitivity	T_{SE}		–	–4.0	–	mV/°C

(4) Variable output voltage regulator

(–40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = DV_{DD} = 3.0 V, LDOOF = 1)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Current consumption	IccON	Iout = 0 mA	–	80	120	µA
Output voltage accuracy	V_Accu	Iout = 0 mA	–10	–	10	%
Load current characteristics	Vout_load	Iout = 0 to 5 mA	–	15	30	mV
Output current	Iout		–	–	15	mA
Dropout voltage Note1	Vd	Iout = 15 mA	–	–	0.4	V
Power supply rejection ratio	PSRR	f = 1 kHz, CL = 1.0 µ F, Iout = 5 mA, AV_{DD2} = 3.0 V, LDOC = 08H (2.6 V)	–	45	–	dB
Discharge resistance	Rs	LDOOF = 0	–	1.0	1.5	kΩ
Settling time	Tset_rise Note2	CL = 1.0 µ F, Iout = 0 mA, LDOC = 08H (2.6 v)	–	–	200	µs
	Tset_fall Note3	CL = 1.0 µ F, Iout = mA, LDOC = 08H (2.6 v)	–	–	5	ms

Notes1. The output voltage range is determined not only by dropout voltage but also by output voltage accuracy.

2. Tset_rise is defined as the time between operation enabled by power control register ACSPC to output voltage being at 90% of its nominal value.

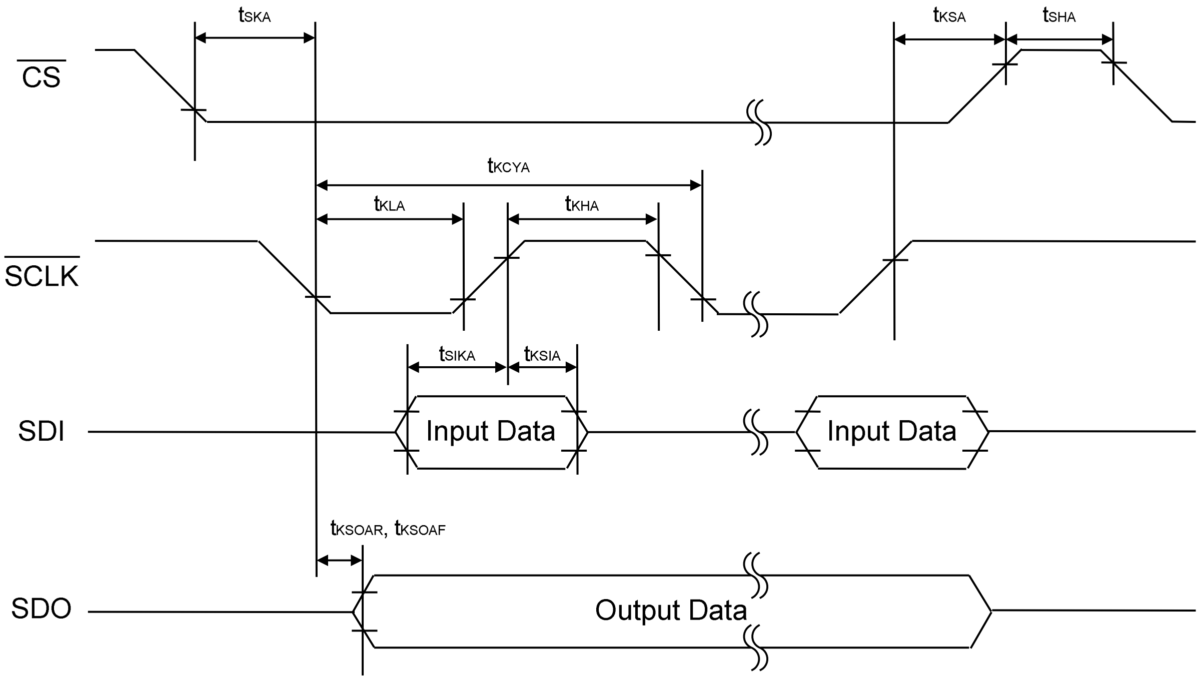
3. Tset_fall is defined as the time between operation disabled by power control register ACSPC to output voltage being at 10% of its nominal value.

(5) SPI

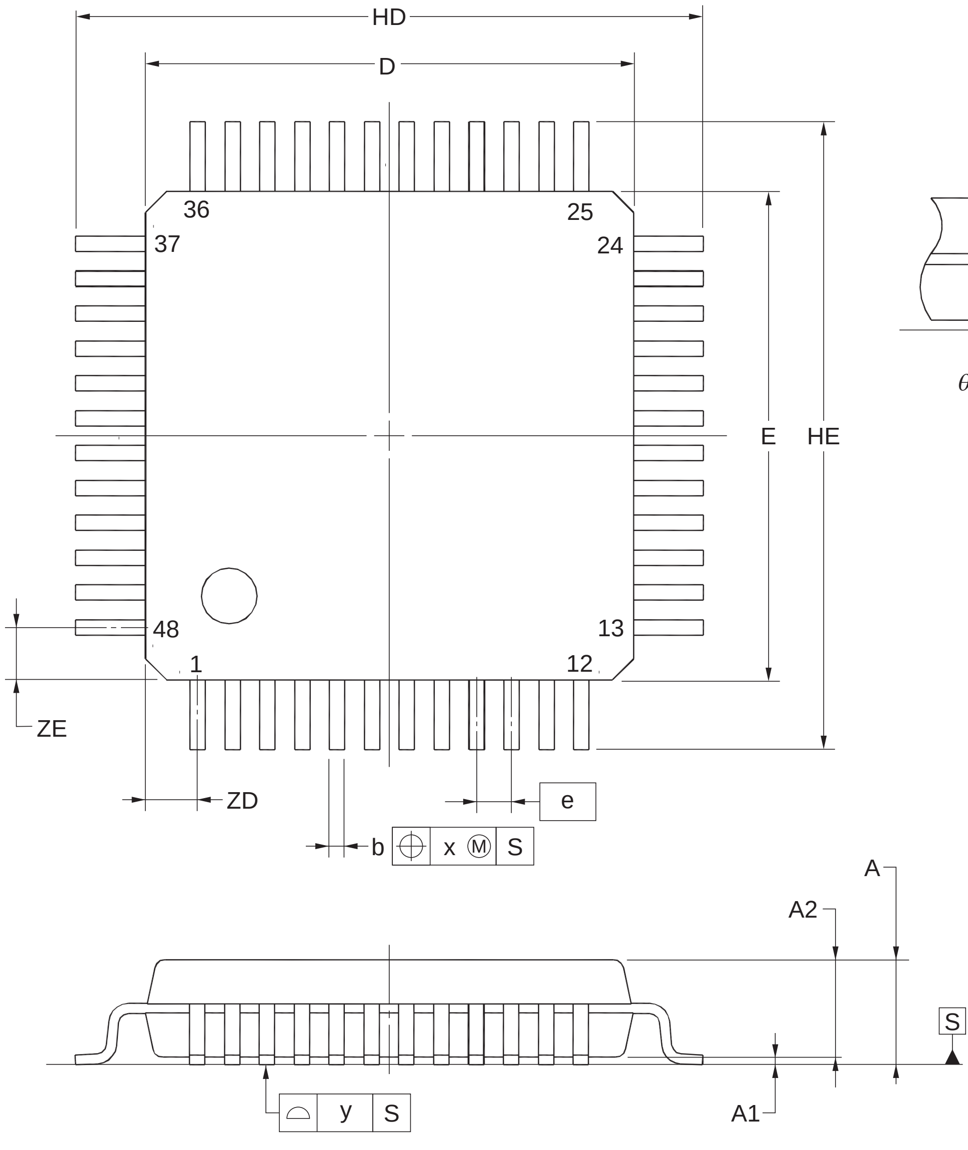
(–40°C ≤ T_A ≤ 105°C, AV_{DD1} = AV_{DD2} = DV_{DD} = 3.0 V)

Parameter	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
High-level input voltage	V_{IH}	$\overline{\text{CS}}$ pin, SDI pin, $\overline{\text{SCLK}}$ pin, $\overline{\text{RESET}}$ pin	DV_{DD} × 0.7	–	DV_{DD} + 0.1	V
Low-level input voltage	V_{IL}	$\overline{\text{CS}}$ pin, SDI pin, $\overline{\text{SCLK}}$ pin, $\overline{\text{RESET}}$ pin	DGND – 0.1	–	DV_{DD} × 0.3	V
Leakage current during high level input	I_{leak_Hi1}	$\overline{\text{CS}}$ pin, SDI pin, $\overline{\text{SCLK}}$ pin	–2	–	2	μA
	I_{leak_Hi2}	$\overline{\text{RESET}}$ pin	–2	–	2	μA
Leakage current during low level input	I_{leak_Lo1}	$\overline{\text{CS}}$ pin, SDI pin, $\overline{\text{SCLK}}$ pin	–2	–	2	μA
	I_{leak_Lo2}	$\overline{\text{RESET}}$ pin	–2	–	2	μA
Low-level output voltage at SDO pin	V_{SDO_Lo}	Io = -4 mA	–	250	400	mV
Leakage current when SDO is off	I_{leak_SDO}		–2	–	2	μA
Pull-up resistance	R_{SPI}	$\overline{\text{CS}}$ pin, SDI pin, $\overline{\text{SCLK}}$ pin, RESET = L	–	50	75	kΩ
$\overline{\text{SCLK}}$ cycle time	t_{KCYA}		100	–	–	ns
$\overline{\text{SCLK}}$ high-level width low-level width	t_{KHA}, t_{KLA}		$0.8t_{KCYA}/2$	–	–	ns
SDI setup time (to $\overline{\text{SCLK}}$↑)	t_{SIKA}		40	–	–	ns
SDI hold time (from $\overline{\text{SCLK}}$↑)	t_{KSIA}		10	–	–	ns
Delay time from $\overline{\text{SCLK}}$↓ to SDO	t_{KSOAR}	CL = 5 pF, VSDO = 3 V	–	–	40	ns
	t_{KSOAF}	CL = 5 pF, VSDO = 3 V	–	–	40	ns
$\overline{\text{CS}}$ high-level width	t_{SHA}		200	–	–	ns
Delay time from $\overline{\text{CS}}$↓ to $\overline{\text{SCLK}}$↓	t_{SKA}		200	–	–	ns
Delay time from $\overline{\text{SCLK}}$↑ to $\overline{\text{CS}}$↑	t_{KSA}		200	–	–	ns

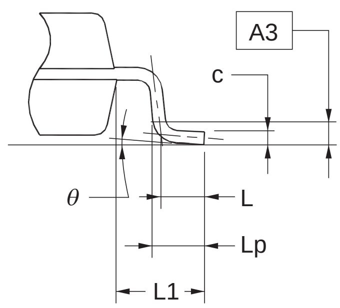
SPI transfer clock timing



9. Package Drawing



detail of lead end



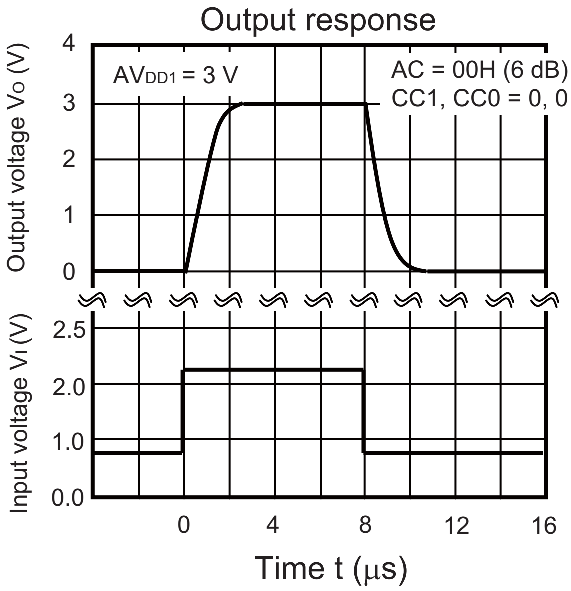
(UNIT:mm)

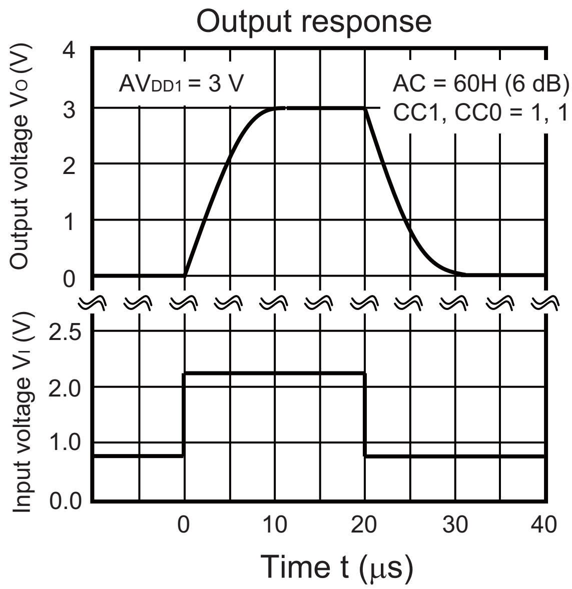
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

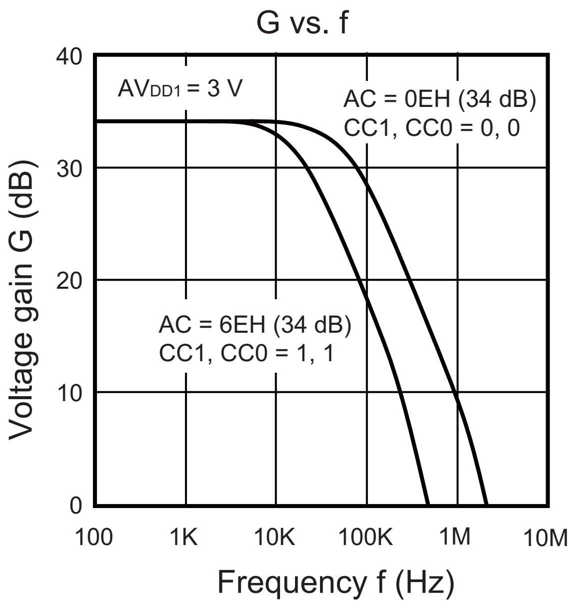
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

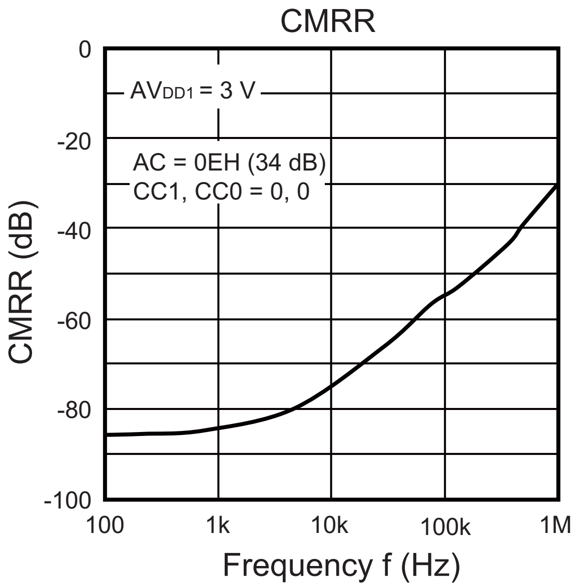
Characteristics Curve (T_A = 25°C, TYP.) (reference value)

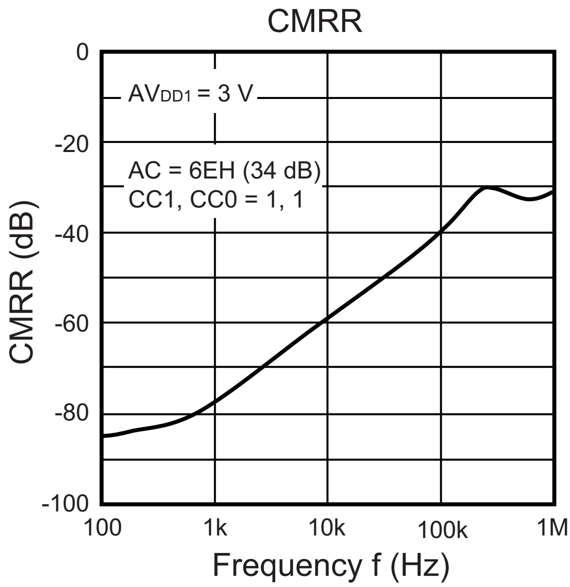
- Instrumentation amplifier

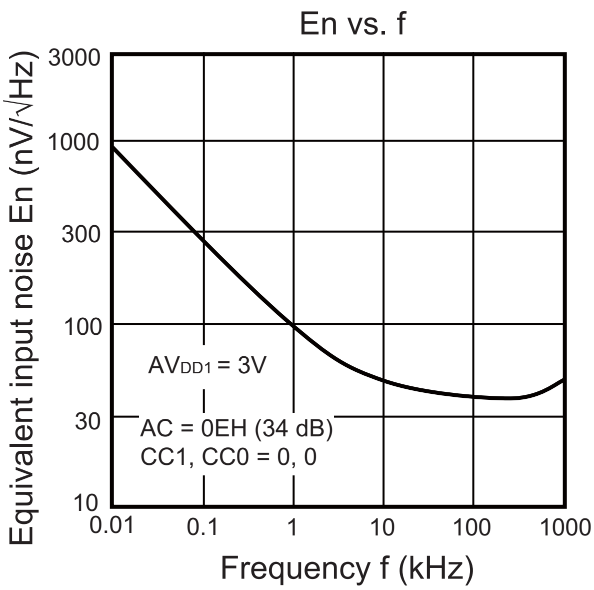


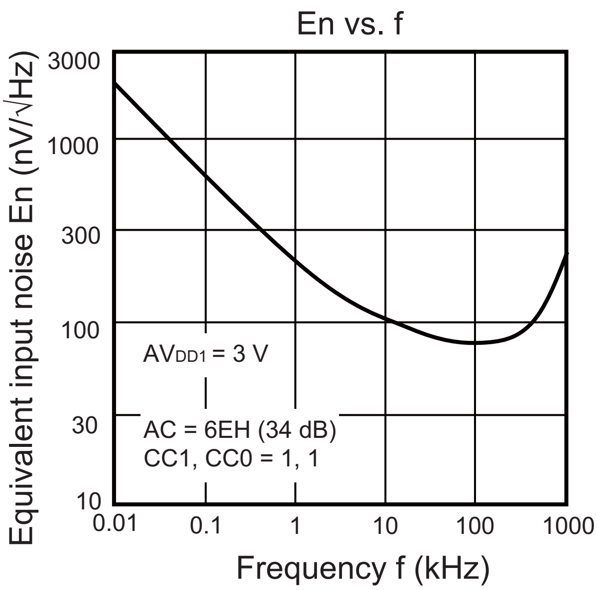




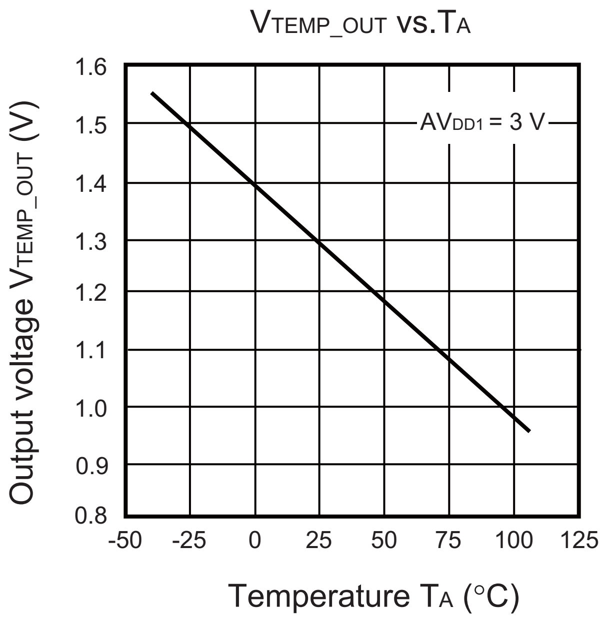

CMRR
AVDD1 = 3 V
AC = 0EH (34 dB)
CC1, CC0 = 0, 0
CMRR (dB)
0
-20
-40
-60
-80
-100
100
1k
10k
100k
1M
Frequency f (Hz)


CMRR
AVDD1 = 3 V
AC = 6EH (34 dB)
CC1, CC0 = 1, 1
CMRR (dB)
0
-20
-40
-60
-80
-100
100
1k
10k
100k
1M
Frequency f (Hz)

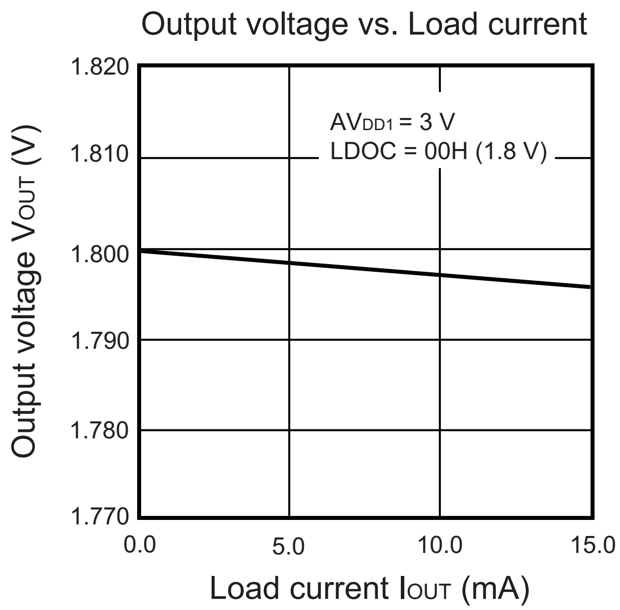

En vs. f
AVDD1 = 3V
AC = 0EH (34 dB)
CC1, CC0 = 0, 0
Equivalent input noise En (nV/√Hz)
3000
1000
300
100
30
10
0.01
0.1
1
10
100
1000
Frequency f (kHz)

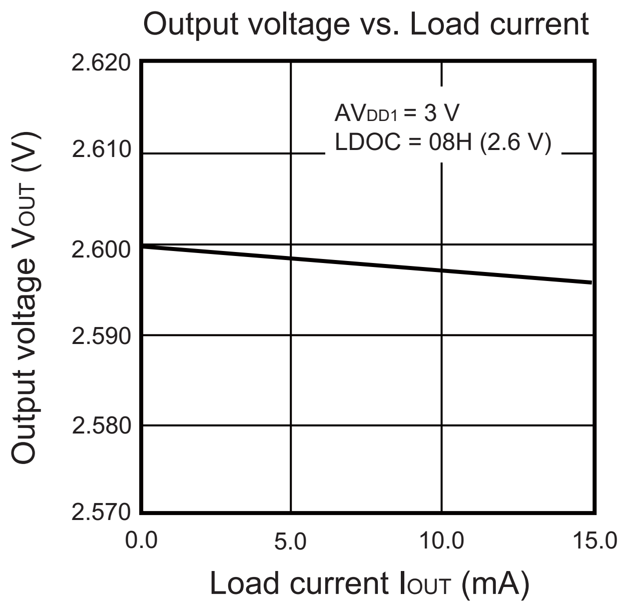

En vs. f
AVDD1 = 3 V
AC = 6EH (34 dB)
CC1, CC0 = 1, 1
Equivalent input noise En (nV/√Hz)
3000
1000
300
100
30
10
0.01
0.1
1
10
100
1000
Frequency f (kHz)

- Temperature sensor



- Variable output voltage regulator





Revision History	RAA730301 Monolithic Programmable Analog IC

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 29, 2013	–	First edition issued.
1.10	May. 31, 2014	11	Change of description about reference voltage in *2. 1 Instrumentation Amplifier*
		15	Change of the calculating formula about output voltage in *3. 1 D/A Converter*
		16	Change of description in *3. 3 (2) DAC reference voltage control register (DACRC)*
		27	Addition of Caution about external reset to *6. SPI*
		28	Correction of *Table 6-1 SPI Control Registers*
		29	Change of description in *7. Reset*
		32	Deletion of Junction temperature from *8. 1 Absolute Maximum Ratings*
		33	Change of the title to "*Operation condition"* in *8. 2*

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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