RAJ306000GFT

General purpose Motor control IC

R18DS0028EJ0101
Rev.01.01
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1 Over View

RAJ306000GFT is general-purpose Motor control IC for three phase Brush less DC motor applications. RAJ306000GFT has built in MCU(RL78/G1F) and a pre-driver. This has three half bridge circuits and can drive two N channel-MOSFET (High-side & Low-side). This enable effective motor drive control by detecting a rotor position by a signal from hall IC and optimally changing three phase energization timing. And is also capable for sensor-less control. In addition, this is equipped a safety function for overheat, overvoltage, and overcurrent and the lock detection for motor. Built-in MCU supports H/W of the safe standard of IEC60730. This can realize motor performance depending on application by the setting of the parameter for motor output by the built-in MCU.

This can support up to 500mA as a drive peak current of external MOSFET.

Built-in MCU are correspond the development tool of the RL78 family.

2 Features

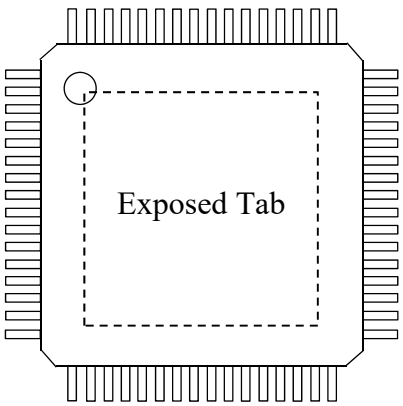
Applications

Power Tools and Lawn Equipment,
Printers, Fans and Valves

Total

(1) Operating Power Supply Voltage: 6V to 30V
(2) Operating temperature : Ta = -40 to +85degC
(3) Support function of Input terminal
for Speed control signal and signal of Start/Stop.
(4) Built-in 5V Regulator
(5) Low power consumption
VM current (Excluding 5V/7V Regulator & Charge-pump) :
[MCU block]: +5.2mA(HS Mode : fIH=32MHz, VDD=5V)
[pre-Driver Block]: + 13.5mA [VM = 22.5V]
VM standby current : 64uA (Typ.)
(6) GPIO : 28ch, Port for Input : 2ch

Pin alignment image
(64pin 7mm x 7mm, 0.4mm pitch,
1.0mm Body thickness)



P-HTFQFP64 [JEITA] (7x7)

Controller Function

(1) CPU: 16bit CISC CPU (RL78/G1F)
(2) Flash ROM: 64KB
(3) Data Flash: 4KB
(4) RAM: 5.5KB
(5) CSI: 2Chanel ----SPI:2ch, IIC:2ch, UART:1ch
(6) Timer
- Timer Array Unit: 1 unit ----------16bit, 4 channel
- Timer RD for Motor Control ------16bit, 2 channel
- Timer RG with Encoding function
----------16bit, 1 channel
- 64 MHz motor control input capture timer (Timer RX)

(7) 10-bit resolution A/D Converter: 9ch
Set of Internal reference Voltage and External reference Voltage is possible.

(8) Event Link Controller (ELC) : 6ch (External terminal)

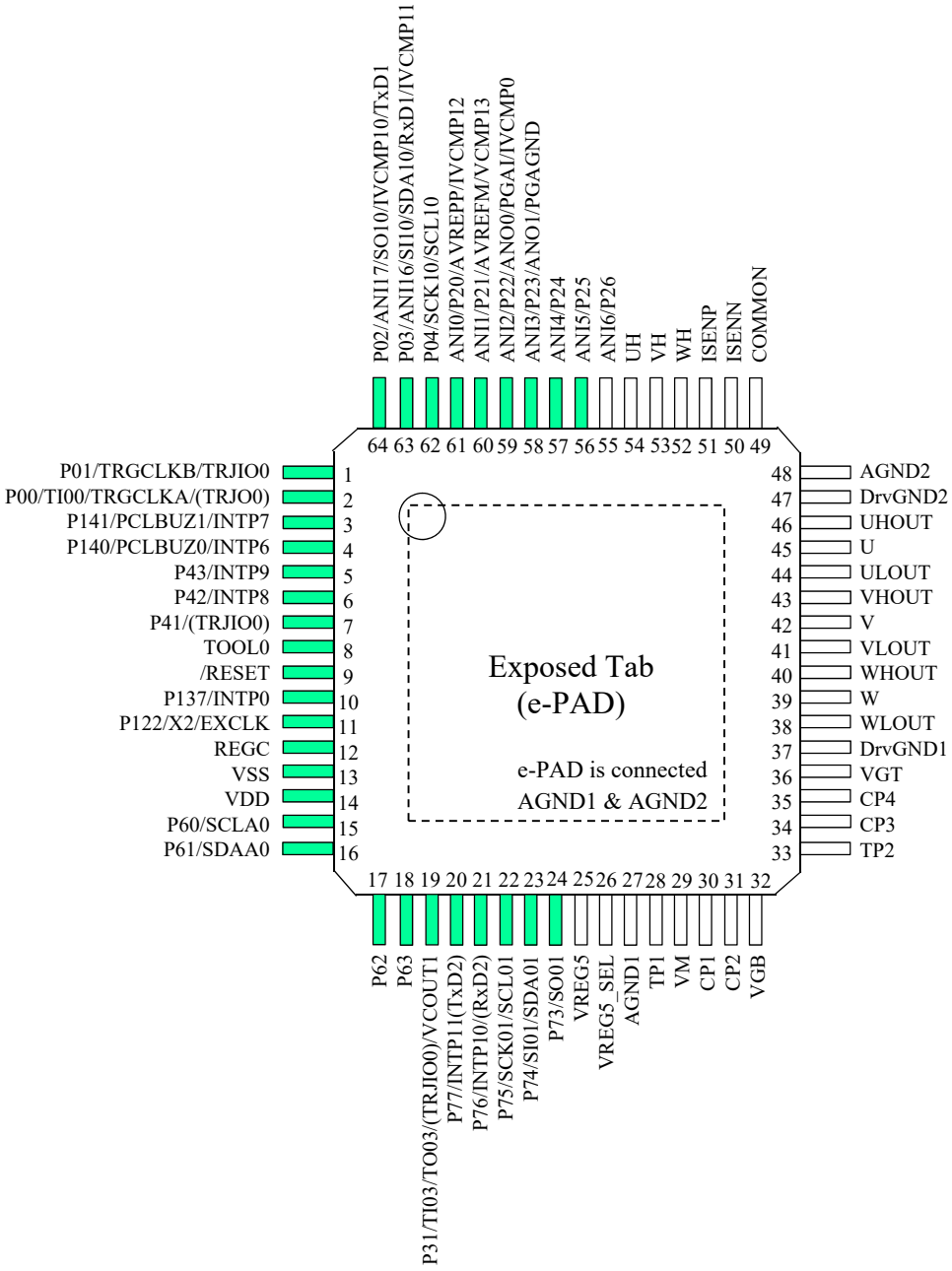
Pre-Driver Function

(1) Three-Phase Brushless DC Motor Controller
- Support Hall IC type & Hall sensor-less type
- Support the setting for Gain amp level
- The Self-align dead off time generator function.
- Gate drive peak current of 500mA.

(2) Drive of 6 N-Channel MOSFET is available.
(3) Gate drive current for MOSFET is up to 500mA
Support Charge pump function.
(4) Safety function:
Overheat, Overvoltage,
Overcurrent of the output phase, UVLO
(5) Setting the threshold level of the hall IC signal input level is possible.
(6) Output wave form mode for motor control :
PWM Output : 2 mode
(Support a commutation mode)
(7) Built in TSD(Thermal shut down)
Temperature Monitoring

3 PIN FUNCTION

PIN ASSIGNMENT [P-HTFQFP64 [JEITA] (7x7)]



Note : RL78/G1F Pins

Pin Functions-1 [P-HTFQFP64 [JEITA] (7x7)]

PIN Number	PIN Name	Sub Function	I/O level	IN/OUT or Power/GND	Initial Condition	Function	Remarks
1	P01	TO00/ TRGCLKB/ TRJIO0/ (INTP10)	VDD	I/O	INPUT	GPIO / TAU output / TRG external clock B input / TRJ input,output / (INTP10)	1
2	P00	TI00/ TRGCLKA/ (TRJO0)/(INTP8)	VDD	I/O	INPUT	GPIO / The pins for inputting an external count clock, capture trigger for TAU / TRG external clock A input / (TRJ output) / (INTP8)	1
3	P141	PCLBUZ1/ INTP7	VDD	I/O	INPUT	GPIO / Output Clock / INTP7	1
4	P140	PCLBUZ0/ INTP6	VDD	I/O	INPUT	GPIO / Output Clock / INTP6	1
5	P43	INTP9	VDD	I/O	INPUT	GPIO / INTP9	1
6	P42	INTP8	VDD	I/O	INPUT	GPIO / INTP8	1
7	P41	(TRJIO0)	VDD	I/O	INPUT	GPIO / (Output for TRJ)	1
8	P40	TOOL0	VDD	I/O	INPUT	GPIO / TOOL0 for E1 on-chip debugging	1
9	/RESET	-	VDD	-	INPUT	Enternal Reset	1
10	P137	INTP0	VDD	INPUT	INPUT	Only input / INTP0	1
11	P122	X2/EXCLK	VDD	INPUT	INPUT	Only input / Input of Main clock from External	1
12	REGC		VDD	-	-	Pin for connecting regulator output stabilization capacitance for internal operation of MCU.	1
13	VSS		VDD	GND		Ground potential for MCU	1
14	VDD		VDD	Power		Positive power supply for MCU	1
15	P60	SCLA0	VDD	I/O	INPUT	GPIO / Serial clock I/O pins of serial interface IICA0	1
16	P61	SDAA0	VDD	I/O	INPUT	GPIO / Serial data I/O pins of serial interface IICA0	1
17	P62	/SSI00	VDD	I/O	INPUT	GPIO / Chip select input pin of serial interface CSI00 [*1]	1
18	P63	-	VDD	I/O	INPUT	GPIO	1
19	P31	TI03/TO03/ (TRJIO0)/ (PCLBUZ0)/ VCOUT1	VDD	I/O	INPUT	GPIO / TAU input / TAU output / (TRJ input/output) / (Output clock) / Comparator 1 output	1
20	P77	KR7/INTP11	VDD	I/O	INPUT	GPIO / KR7 / INTP11	1
21	P76	KR6/INTP10	VDD	I/O	INPUT	GPIO / KR6 / INTP10	1
22	P75	KR5 / SCK01/ SCL01	VDD	I/O	INPUT	GPIO / KR5 / Serial clock I/O pins of serial interface CSI01 / Serial clock output pins of serial interface IIC01	1
23	P74	KR4 / SI01/ SDA01	VDD	I/O	INPUT	GPIO / KR4 / Serial data input pins of serial interface CSI01 / Serial data I/O pins of serial interface IIC01	1
24	P73	KR3 / SO01	VDD	I/O	INPUT	GPIO / KR3 / Serial data output pins of serial interface CSI01	1
25	VREG5		VREG5(5V)	IN/OUT	IN/OUT	VREG5 pin function is depends on VREG5_SEL pin level	
26	VREG5_SEL		VREG5	IN	IN	VREG5_SEL=GND: Built-in 5V regulator is selected.(Output 5V) VREG5_SEL=5V: External 5V regulator is selected(Input 5V)	
27	AGND1		GND	GND	GND	Ground potential 1 for analog and logic circuits of Pre-Driver	
28	TP1		VREG5	IN	IN	Terminal for Test. (Usually conect to GND)	
29	VM		VM	POWER	POWER	Power Supply input	
30	CP1		VGB	-	-	Charge pump Pin 1 (CP1)	
31	CP2		VGB	-	-	Charge pump Pin 2 (CP2)	
32	VGB		VGB	OUT	OUT	Gate drive voltage for Low-side	
33	TP2		VREG5	IN	IN	Terminal for Test. (Usually conect to GND)	
34	CP3		VM	-	-	Charge pump Pin 3 (CP3)	
35	CP4		VGT	-	-	Charge pump Pin 4 (CP4)	
36	VGT		VGT	OUT	OUT	Gate drive voltage for High-side	
37	DrvGND1		GND	GND	GND	Ground potential 1 for driving circuits of Pre-Driver	
38	WLOUT		VGB	OUT	OUT	Output of Pre-driver for W phase Low-side (Nch MOSFET)	
39	W		VM	IN	IN	Detection of BEMF level for W phase	
40	WHOUT		VGT	OUT	OUT	Output of Pre-driver for W phase High-side (Nch MOSFET)	
41	VLOUT		VGB	OUT	OUT	Output of Pre-driver for V phase Low-side (Nch MOSFET)	
42	V		VM	IN	IN	Detection of BEMF level for V phase	
43	VHOUT		VGT	OUT	OUT	Output of Pre-driver for V phase High-side (Nch MOSFET)	
44	ULOUT		VGB	OUT	OUT	Output of Pre-driver for U phase Low-side (Nch MOSFET)	
45	U		VM	IN	IN	Detection of BEMF level for U phase	
46	UHOUT		VGT	OUT	OUT	Output of Pre-driver for U phase High-side (Nch MOSFET)	
47	DrvGND2		GND	GND	GND	Ground potential 2 for driving circuits of Pre-Driver	

*1: RL78/G1F terminal. And Please refer to “RL78/G1F User’s manual: Hardware” (R01UH0516EJ0110) about Terminal function of RL78/G1F.
*2: The nullification of the SSI00 function is necessary.

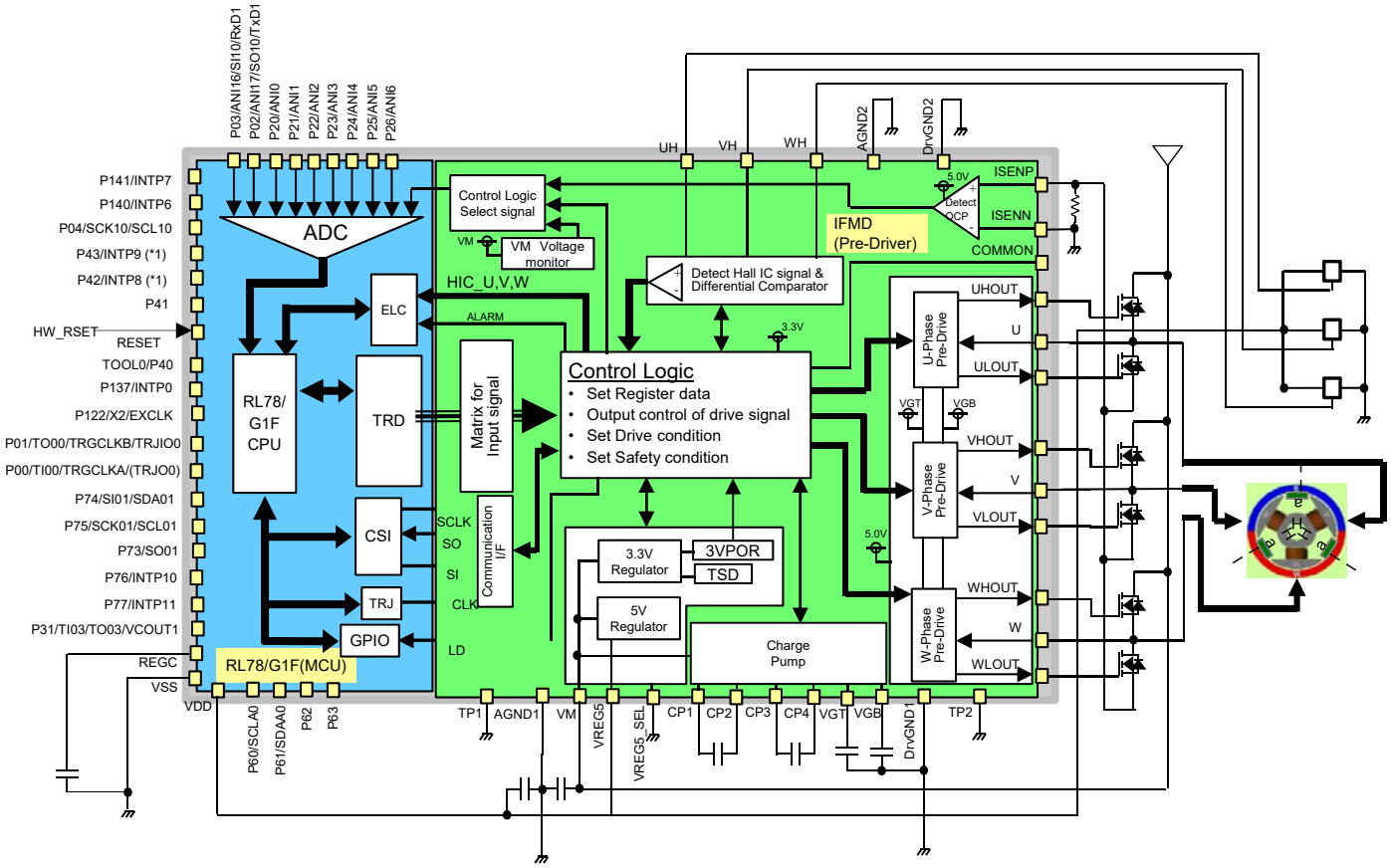
Pin Functions-2 [P-HTFQFP64 [JEITA] (7x7)]

PIN		Sub	I/O level	IN/OUT or	Initial	Function	Remarks
Number	Name	Function		Power/GND	Condition		
48	AGND2		GND	GND	GND	Ground potential 2 for analog and logic circuits of Pre-Driver.	
49	COMMON		VM	IN	IN	Input for Common signal of Motor	
50	ISENN		VREG5	IN	IN	Connect Negative side of Shunt resistor	
51	ISENP		VREG5	IN	IN	Connect Positive side of Shunt resistor	
52	WH		VREG5	IN	IN	Input of Hall IC signal for W phase	
53	VH		VREG5	IN	IN	Input of Hall IC signal for V phase	
54	UH		VREG5	IN	IN	Input of Hall IC signal for U phase	
55	P26	ANI6	VDD	I/O	ANALOG	A/D converter analog input / GPIO	1
56	P25	ANI5	VDD	I/O	ANALOG	A/D converter analog input / GPIO	1
57	P24	ANI4	VDD	I/O	ANALOG	A/D converter analog input / GPIO	1
58	P23	ANI3 / ANO1/ PGAGND	VDD	I/O	ANALOG	GPIO / A/D converter analog input / D/A converter output / PGA reference voltage input	1
59	P22	ANI2 /ANO0/ PGAI/IVCMP0	VDD	I/O	ANALOG	GPIO / A/D converter analog input / D/A converter output / PGA voltage input / Comparator 0 analog voltage input	1
60	P21	ANI1/AVREFM/ IVCMP13	VDD	I/O	ANALOG	GPIO / A/D converter analog input / A/D converter reference potential (- side) input / Comparator 1 analog voltage input/reference	1
61	P20	ANI0 /AVREFP/ IVCMP12 / (INTP11)	VDD	I/O	ANALOG	GPIO / A/D converter analog input / A/D converter reference potential (+ side) input / Comparator 1 analog voltage input/reference voltage input / (INTP11)	1
62	P04	SCK10/SCL10	VDD	I/O	ANALOG	GPIO / Serial clock I/O pins of serial interface CSI10 / Serial clock output pins of serial interface IIC10	1
63	P03	SI10 /ANI16/ RxD1/SI10/ SDA10/ IVCMP11	VDD	I/O	ANALOG	GPIO / Serial data input pins of serial interface CSI10 / A/D converter analog input / Serial data input pins of serial interface UART1 / Serial data input pins of serial interface CSI10 / Serial data I/O pins of serial interface IIC10 / Comparator 1 analog voltage input/reference voltage input	1
64	P02	SO10 /ANI17/ TxD1/ IVCMP10	VDD	I/O	ANALOG	GPIO / Serial data output pins of serial interface CSI10 / Serial data output pins of serial interface CSI10 / Serial data output pins of serial interface UART1 / Comparator 1 analog voltage input/reference voltage input	1

*1: RL78/G1F terminal. And Please refer to “RL78/G1F User’s manual: Hardware” (R01UH0516EJ0110) about Terminal function of RL78/G1F.

4 BLOCK DIAGRAM

(Incase of using Hall IC)



IFMD : Intelligent Front-end Motor Driver

- GPIO terminal: 28ch
  (Include ADC:9ch & Terminal for External interrupt: 6ch)
- Input terminal: 2ch

*1) PIOCR00 = 01 [Setting required]

*2) SSIE00 = 0 [Setting required]----Invalidation of $\overline{\text{SSI00}}$

Note : Please refer to “RL78/G1F User’s manual: Hardware (R01UH0516EJ0110) ”.

5 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATING (Ta=25 degC) [P-HTFQFP64 [JEITA] 1)

ITEM	SYMBOL	RATING	UNIT	NOTES
Power dissipation	Pd	5180	mW	
Thermal derating	Kθ	-41.5	mW/degC	Condition: refer to P.8
Power supply for motor drive	VM	-0.3 to +60	V	Refer to Note 4
Power supply	VDD	- 0.3 to +6.5	V	Port: VDD(MCU)
REGC terminal input voltage range	VIREGC	-0.3 to +2.8 Note1	V	Port: REGC
VREG5 terminal input voltage range	VIVREG5	-0.3 to +6.5	V	Port: VREG5
VGT output voltage range	VVGT	-0.3 to +48.0	V	Port :VGT
CP4 terminal voltage range	VCP4	-0.3 to +48.0	V	Port :CP4
CP3 terminal voltage range	VCP3	-0.3 to +48.0	V	Port :CP3
VGB output voltage range	VVGB	-0.3 to +18.0	V	Port :VGB
CP2 terminal voltage range	VCP2	-0.3 to +18.0	V	Port :CP2
CP1 terminal voltage range	VCP1	-0.3 to +18.0	V	Port :CP1
UHOUT, VHOUT, WHOUT output voltage range	VH_OUT	-0.5 to +48.0	V	Port :UHOUT, VHOUT, WHOUT
UHOUT, VHOUT, WHOUT output voltage range	Vphase	-0.5 to +48.0	V	Port :U, V, W, COMMON
ULOUT, VLOUT, WLOUT output voltage range	VL_OUT	-0.5 to +18.0	V	Port :ULOUT, VLOUT, WLOUT
Sense current terminal	ISEN	-0.3 to VREG5 + 0.3	V	Port : ISENP, ISENN
Digital terminal Input voltage range	DVIN1	-0.3 to VDD + 0.3 Note2	V	Port :P00 to P04, P20~P26, P31, P40 to P43, P73 to P77, P122, P137, P140, P141, EXCLK, /RESET
	DVIN2	-0.3 to +6.5	V	Port: P60 to P63 (Nch open-drain)
Output Voltage	DVOUT	-0.3 to VDD + 0.3 Note2	V	Port: P00 to P04, p20 to P26, P31, P40 to P43, P73 to P77, P140, P141
Analog input voltage	AVIN1	-0.3 to VDD + 0.3 And -0.3 to AVREF(+) + 0.3 Note2, 3	V	Port: ANI0 to ANI6, ANI16, ANI17
	AVIN2	-0.3 to VREG5 + 0.3	V	Port :VREG5_SEL, TP1, TP2
Hall sensor input terminal voltage	HVIN	-0.3 to VREG5 + 0.3	V	Port : UH, VH, WH
Hall sensor input terminal voltage1	DIOH1	-40	mA/Terminal	Port :P00 to P04, P31, P40 to P43, P73 to P77, P140, P141
		-70	mA/Total	Port : P00 to P04, P40 to P43, P140, P141
		-100	mA/Total	Port :P31, P73 to P77

1) Not subject to production test, specified by design.

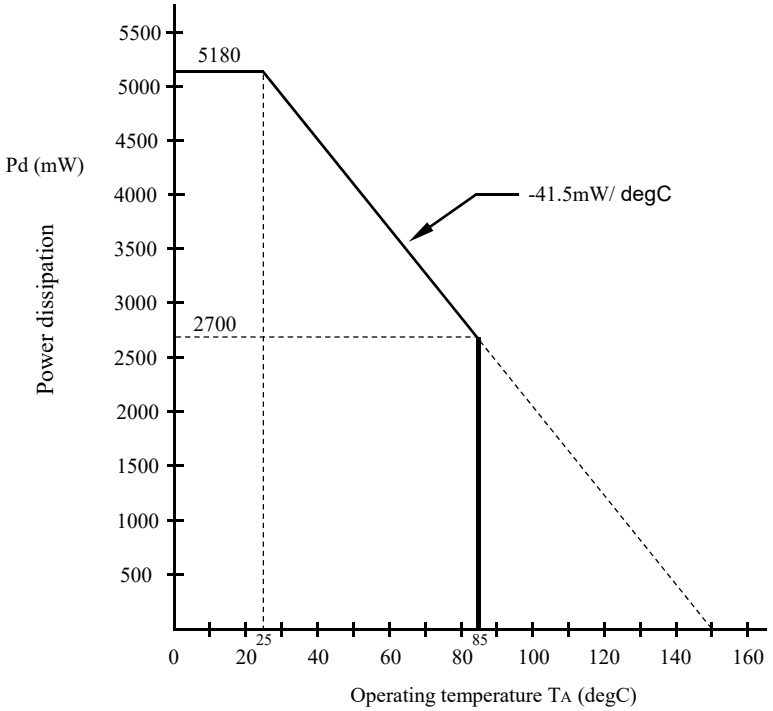
ABSOLUTE MAXIMUM RATING (Ta=25 degC) [P-HTFQFP64 [JEITA] 1)

ITEM	SYMBOL	RATING	UNIT	NOTES
Hall sensor input terminal voltage2	DIOH2	-0.5	mA/Terminal	Port : P20 to P26 (Total current of these terminal: 1.7mA)
Digital output current of Low level 1	DIOL1	+40	mA/Terminal	Port :P00 to P04, P31, P40 to P43, P60 to P63, P73 to P77, P140, P141
		+70	mA/Total	Port :P00 to P04, P40 to P43, P140, P141
		+100	mA/Total	Port :P31, P73 to P77
Digital output current of Low level 2	DIOL2	+1	mA/Terminal	Port : P20 to P26 (Total current of their terminal: 4.3mA)
Maximum junction temperature	Tj	+150	degC	IFMD chip
Operating temperature	Tope	-40 to +85	degC	
Storage temperature	Tstg	-65 to +150	degC	

1) Not subject to production test, specified by design.

Note 1. Connect the REGC pin to VSS via a capacitor (0.47 to 1 uF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
Note 2. Must be 6.5 V or lower.
Note 3. Do not exceed AVREF (+) + 0.3 V in case of A/D conversion target pin.
Note 4. Please do not apply the voltage more than 48V to VM terminal more than 1us.
In addition, when the VM voltage is as above 48V at DC level, the serge protective circuit of this IC works, and the applied voltage is clamped.
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
Remark 2. AVREF (+): + side reference voltage of the A/D converter.
Remark 3. VSS, GND: Reference voltage.
Port of GND: Drive block: DrvGND1, DrvGND2, Analog block: AGND1, AGND2
Port of VSS: VSS (MCU)

ABSOLUTE MAXIMUM RATING (TA=25 degC)



Notes) Glass epoxy board: 76.2mm x 114.5mm x 1.6mm, copper-occupancy ratio in a 4-layer board: 50% in layers 1 and 4, 95% in layers 2 and 3.
[Note that the allowable power consumption changes according to the conditions imposed on the board.]

Thermal Information

ITEM	SYMBOL RATING UNIT	NOTES
ψjt	1.99 degC/W	junction-to-case (package top surface) thermal resistance
θja	24.1 degC/W	junction-to-ambient thermal resistance
Exposed power pad / heat slug area	28.1 mm^2	---

Note1: Glass epoxy board: 76.2mm x 114.5mm x 1.6mm, copper-occupancy ratio in a 4-layer board: 50% in layers 1 and 4, 95% in layers 2 and 3.
[Note that the allowable power consumption changes according to the conditions imposed on the board.]

RECOMMENDED OPERATING CONDITIONS (TA=25 degC)

ITEM	SYMBOL	RATING	UNIT	NOTES
Power voltage for motor drive	VM	+6 to +30	V	
Output current of 5V Regulator	IVREG5	30 [Max]	mA	Total: 60mA [Max] Note1

Note1) Breakdown of 60mA(Max)

For External parts: 30mA(Max), For RAJ306000GFT IC 30mA

Electrical Characteristics (Ta = 25 degC, VM = 22.5V, VSS = GND = 0V)

Parameter	Symbol	Condition	Rated level			Unit	Notes
			MIN	TYP	MAX		
Power Supply Block							
VM operation current	I_{VM}	VREG5,VREG7 and Charge Pump	-	13.5	19	mA	Pre Driver block (Using Hall IC)
VM Standby currents	I_{STBY}	Motor: OFF, PS Register (04h): 00h, System clock: Stop	-	64	96	uA	
VREG5 Output voltage	V_{VREG5}	IOUT = 1 to 30mA	4.75	5	5.25	V	
VREG5 Output current	I_{VREG5}		-	-	30	mA	
Gate Driver Block							
Charge pump voltage for High side	Vvgt	IO=100uA	VM+10	-	VM+15	V	VM=22.5V
Charge pump voltage for Low side	Vvgb	IO=100uA	10	-	15	V	
Gate drive output voltage for High side	V_{OUTH}	IO=100uA	VM+10	-	VM+15	V	VM=22.5V
Gate drive output voltage for Low side	V_{OUTL}	IO=100uA	10	-	15	V	
Overcurrent Detection Block							
Input voltage level of connection terminal for Shunt resistance	VISEN	Port: ISENP	0.0	-	1.0	V	Note1)

Note 1) Please use ISENP terminal detecting a potential difference of the Shunt resistance at the range of a standard to show as above.
In addition, Please use the electric potential of ISENP terminal and the ISENN terminal
by relation condition of "ISENP>ISENN".

These note item is relate to the limitation of the input range for the AMP operation.

Electrical Characteristics (Ta = 25 degC, VM = 22.5V, VSS = GND = 0V)

Parameter	Symbol	Condition	Rated level MIN	Rated level TYP	Rated level MAX	Unit	Notes
Hall signal Block							
Hall IC input signal Threshold voltage level	HAIC_TH	HAIC_TH: 000	+ 0.32	+ 0.40	+ 0.48	V	
		HAIC_TH: 001	+ 0.56	+ 0.70	+ 0.84		
		HAIC_TH: 010	+ 0.80	+ 1.00	+ 1.20		
		HAIC_TH: 011	+ 1.04	+ 1.30	+ 1.56		
		HAIC_TH: 100	+ 1.28	+ 1.60	+ 1.92		
		HAIC_TH: 101	+ 1.52	+ 1.90	+ 2.28		
		HAIC_TH: 110	+ 1.76	+ 2.20	+ 2.64		
		HAIC_TH: 111	+ 2.00	+ 2.50	+ 3.00		
Hystersis	HIU_V_W_hys	HAIC_HYS: 00	-	0	-	mV	
		HAIC_HYS: 01	-	50	-		
		HAIC_HYS: 10	-	100	-		

IC Thermal characteristics

Parameter	Symbol	Condition	Rated Level MIN	Rated Level TYP	Rated Level MAX	UNIT	Notes
Safety protection block							
Overheat protection operating temperature	TSD			150		degC	Note 2)

Note 2) The targeted TSD temperature of the above is the design targeted value of this IC, and Renesas can not guarantees an operating temperature of the above. (Renesas can not inspect all product operation at the temperature of the above.)

Reference data of device characteristics (Ta = 25 degC, VM = 22.5V, VSS = GND = 0V)

Parameter	Symbol	Condition	Rated level MIN	Rated level TYP	Rated level MAX	Unit	Notes
Gate Driver Block							
Impedance of the gate drive output (High side)	ROUTH	IDR_H_P = 111	Typ. - 20%	9.5	Typ. + 20%	Ω	Note 3)
		IDR_H_P = 100		14.0		Ω	
		IDR_H_P = 000		65.0		Ω	
		IDR_H_N = 111	Typ. - 25%	38.5	Typ. + 25%	Ω	
		IDR_H_N = 100		10.0		Ω	
		IDR_H_N = 000		5.0		Ω	
Impedance of the gate drive output (Low side)	ROUTL	IDR_L_P = 111	Typ. - 20%	5.0	Typ. + 20%	Ω	Note 3)
		IDR_L_P = 100		7.0		Ω	
		IDR_L_P = 000		27.0		Ω	
		IDR_L_N = 111	Typ. - 25%	17.5	Typ. + 25%	Ω	
		IDR_L_N = 100		5.0		Ω	
		IDR_L_N = 000		2.5		Ω	

Note 3) The Impedance for the gate drive output of the above is the design targeted value of this IC, and Renesas can not guarantees a resistance level of the above.

6 BLOCK EXPLANATION

Serial Array Unit

The constitution of the serial unit array for RAJ306000GFT are the following.
Channel of CSI00: CSI00 is used for the communication of RL78/G1F MCU and the Pre-driver at the inside of RAJ306000GFT.

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I²C
0	0 A: [For internal communication]	CSI00(Slave select function is invalid.) A: [For internal communication]		
	1	CSI01		IIC01
	2	CSI10	UART1(TxD1)	IIC10
	3		UART1(RxD1)	
1	0			
	1			

A: CSI00 is used for the communication of RL78/G1F MCU and the analog device

CSI00 specification

Communication between RL78/G1F(MCU) and the analog device by the CSI mode is possible. The write setting of each register for the Pre-driver and the reading of register state for the Pre-driver are possible by using CSI mode communication.
CSI00 is assigned to the communication between RL78/G1F(MCU) and the Pre-driver. Therefore, CSI00 of RAJ306000GFT can not use for the communication with external parts. In addition, input function for the slave select of CSI00 is also invalid.
[SSIE00 = 0 [Setting required]----Invalidation of SSI00]

Shown about specification of CSI00(SCK00), CSI01 and CSI10 as follows.

- During communication at same potential (CSI mode) (master mode, SCKp... external clock input)

◆ Target Products: RAJ306000GFT (TA = -40 to +85degC)

(TA = 25degC, 4.06V <= VDD <= 5.25V , Vss = 0V) HS(High-speed main) mode

parameter	Symbol	Condition		CSI00		CSI01, CSI10		Unit
				MIN	MAX	MIN	MAX	
SCKp cycle time	t_{KCY1}	t_{KCY1}>=4/fCLK	4.06V <= VDD <= 5.25V	1000	-	250	-	ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.06V <= VDD <= 5.25V		t_{KCY1}/2 – 24	-	t_{KCY1}/2 – 24	-	ns
SIp setup time (to SCKp↑) * Note1	t_{SIK1}	4.06V <= VDD <= 5.25V		66	-	66	-	ns
SIp hold time (from SCKp↑) * Note1	t_{KSI1}	-		38	-	38	-	ns
Delay time from SCKp↓ to SOp output * Note1	t_{KSO1}	C = 30pF *Note2		-	50	-	50	ns

Note 1. When DAPmn = 0 ,CKPmn = 0, or DAPmn = 1 , CKPmn = 1.
"Edge polarty of SCKp" reveresed when DAPmn = 0 ,CKPmn = 1 or DAPmn = 1 , CKPmn = 0.

Note 2. C is the loDAPmn = 0 and ad capacitance of the SCKp and SOp output lines.

Remark 1. p: CSI number (p = 01,10), m: Unit number (m = 0), n: Channel number (n = 1,2)

- During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

◆ Target Products: RAJ306000GFT (TA = -40 to +85degC) (TA = 25degC, 4.06V <= VDD <= 5.25V , Vss = 0V)

Parameter	Symbol	Condition		HS(High-speed main) mode		Unit
				MIN	MAX	
SCKp cycle time	tKCY2	4.06V <= VDD <= 5.25V	20MHz >= 4/fMCK	16/f_{MCK}	-	ns
			fMCK >= 20MHz	12/f_{MCK}	-	ns
SCKp high-/low-level width	tKH2, tKL2	4.06V <= VDD <= 5.25V		t_{KCY2}/2 – 24	-	ns
SIp setup time (to SCKp↑) * Note1	tSIK1	4.06V <= VDD <= 5.25V		1/f_{MCK} + 40	-	ns
SIp hold time (from SCKp↑) * Note1	tKSI1	-		1/f_{MCK} + 62	-	ns
Delay time from SCKp↓ to SOp output * Note1	tKSO1	C = 30pF *Note2		-	2/f_{MCK} + 66	ns

Note 1. When DAPmn = 0 ,CKPmn = 0, or DAPmn = 1 , CKPmn = 1.
"Edge polarty of SCKp" reveresed when DAPmn = 0 ,CKPmn = 1 or DAPmn = 1 , CKPmn = 0.

Note 2. C is the load capacitance of the SOp output lines.

Note 4. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Remark 1. p: CSI n umber (p = 01, 10), m: Unit number (m = 0), n: Channel number (n = 1, 2), g: PIM number (g = 0, 1, 3, 5, 7)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,n: Channel number (mn = 10, 11))

Note : Please refer to "RL78/G1F User's manual: Hardware (R01UH0516EJ0110) " about Terminal function of RL78/G1F About specification of "simplified I2C mode".

- During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

◆ Target Products: RAJ306000GFT (TA = -40 to +85degC)

(TA = 25degC, 4.06V <= VDD <= 5.25V , Vss = 0V)

Parameter	Symbol	Condition		HS(High-speed main) mode		Unit
				MIN	MAX	
SCKp cycle time	tKCY2	4.06V <= VDD <= 5.25V	20MHz >= 4/fMCK	16/f_{MCK}	-	ns
			fMCK >= 20MHz	12/f_{MCK}	-	ns
SCKp high-/low-level width	tKH2, tKL2	4.06V <= VDD <= 5.25V		t_{KCY2}/2 – 24	-	ns
SIp setup time (to SCKp↑) * Note1	tSIK1	4.06V <= VDD <= 5.25V		1/f_{MCK} + 40	-	ns
SIp hold time (from SCKp↑) * Note1	tKSI1	-		1/f_{MCK} + 62	-	ns
Delay time from SCKp↓ to SOp output * Note1	tKSO1	C = 30pF *Note2		-	2/f_{MCK} + 66	ns

Note 1. When DAPmn = 0 ,CKPmn = 0, or DAPmn = 1 , CKPmn = 1.
"Edge polarty of SCKp" reveresed when DAPmn = 0 ,CKPmn = 1 or DAPmn = 1 , CKPmn = 0.

Note 2. C is the load capacitance of the SOp output lines.

Note 3. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

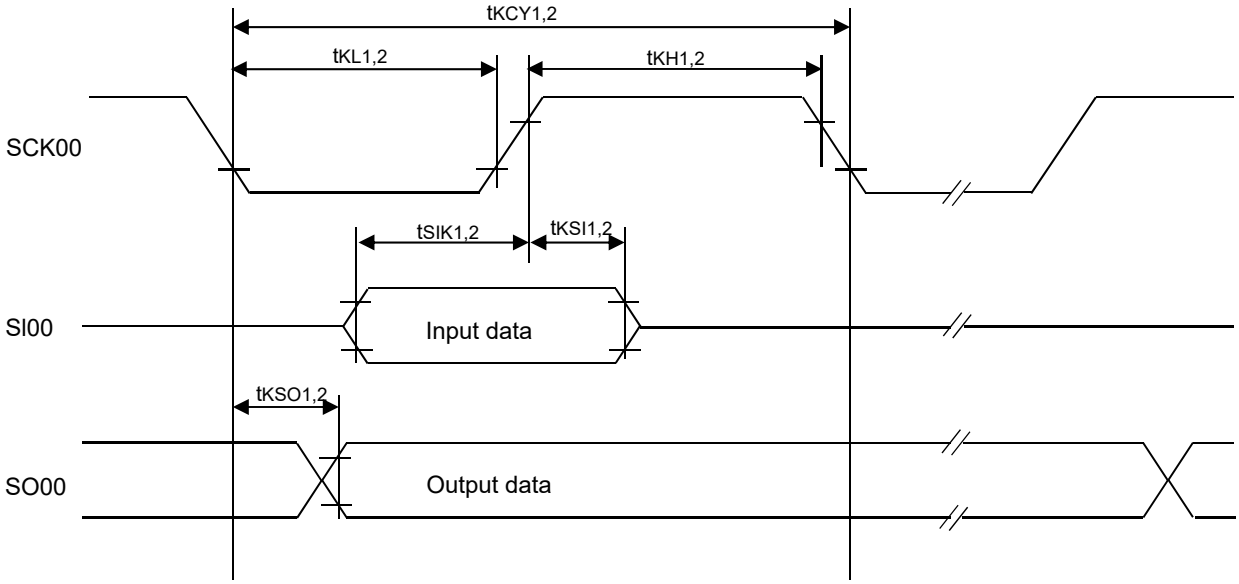
Remark 1. p: CSI number (p = 01, 10), m: Unit number (m = 0), n: Channel number (n = 1, 2), g: PIM number (g = 0, 1, 3, 5, 7)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 10, 11))

Note : Please refer to "RL78/G1F User's manual: Hardware (R01UH0516EJ0110) " about Terminal function of RL78/G1F
About specification of "simplified I2C mode".

CSI mode serial transfer timing (during communication at same potential)

1) When DAPmn = 0, CKPmn = 0 or DAPmn = 1, CKPmn = 1



Edge polarty of SCK00 reversed) when DAPmn = 0, CKPmn = 1 or DAPmn = 1, CKPmn = 0.

Shown about specification of UART1 as follows.

- During communication at same potential (UART mode)

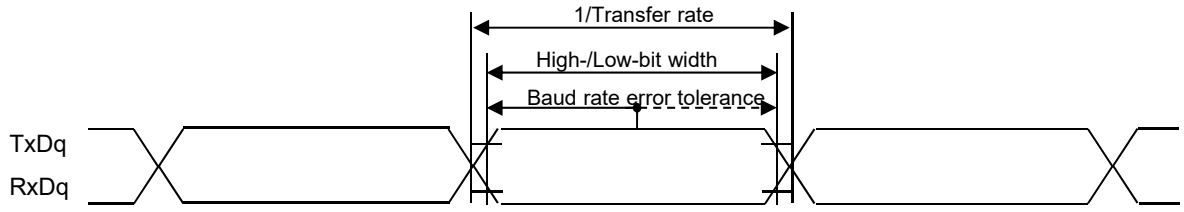
◆ Target Products: RAJ306000GFT (TA = -40 to +85degC)

(TA = 25deg, 4.06V <= VDD <= 5.25V, Vss = 0V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN	MAX	
Transfer rate Note1	-	4.06V <= VDD<= 5.25V	-	fMCK/12	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note2	-	2.6	Mbps

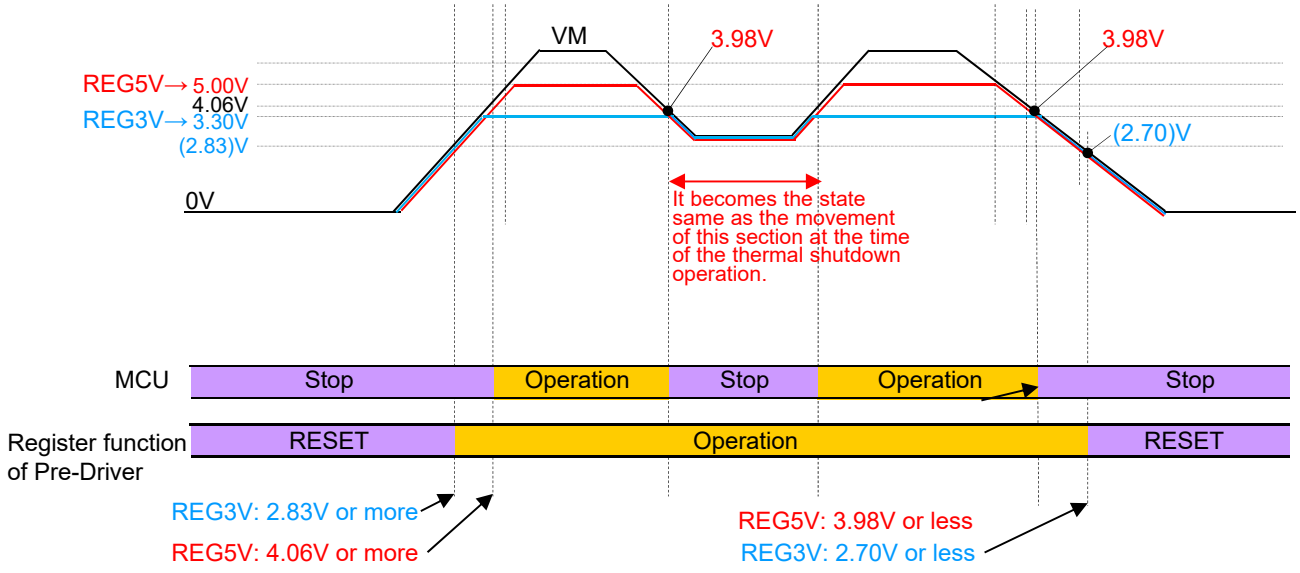
Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:
HS (high-speed main) mode: 32 MHz (4.06V <= VDD<= 5.25V)



Remark 1. fMCK: Serial array unit operation clock frequency

About a power-on sequence after Reset of MCU.

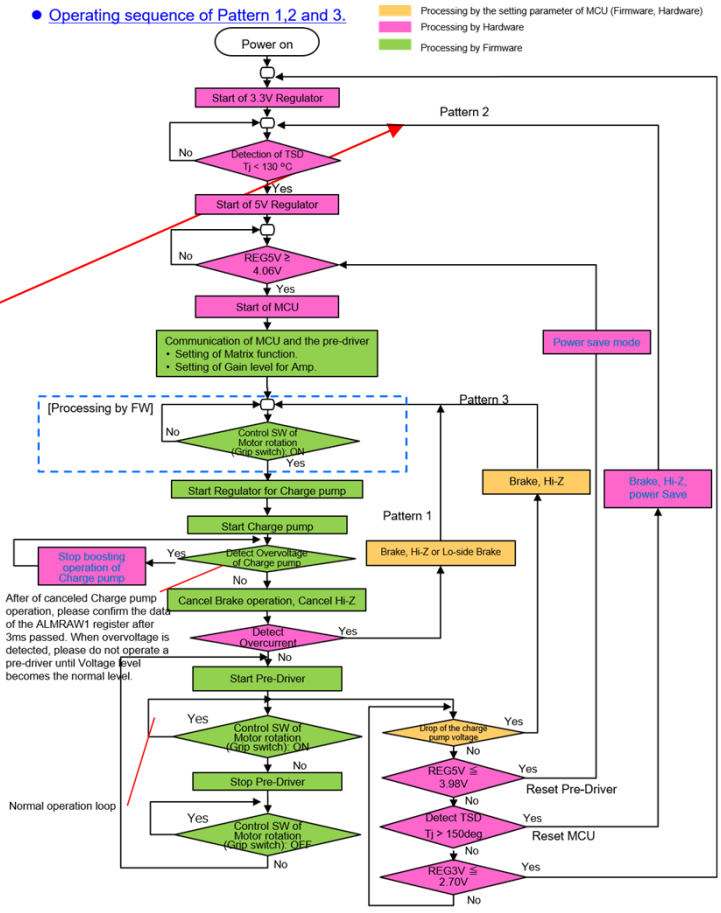


*1 When a user writes in data of Firmware to Flash, it is necessary for the user to set MCU as follows.
- Functions of Voltage Detector: Enable
  (Please refer to"RL78/G1F User's Manual: Hardware (R01UH0516EJ0110) CHAPTER 27 RESET FUNCTION" and "CHAPTER 29 VOLTAGE DTECTOR" about VLVD.)
- Setting "Reset mode" of Functions of Voltage Detector.
- Setting '4.06V of Rising edge' and '3.98V of Falling edge' on Detection voltage(VLVD).

*2 When a level of VM is less than 6V, the voltage up level of the charge pump becomes less than 10V.

When TSD operated

5V Regulator function is stop.
3V Regulator is operating.
In this case the register data written to Pre-Driver is maintained.



Functions of Clock Generator

The clock generator generates the clock to be supplied to the CPU and peripheral hardware. RL78/G1F MCU is mounted on RAJ306000GFT is support the high-speed on-chip oscillator (High-speed OCO). The frequency
at which to oscillate can be selected from among fHOCO = 64, 48, 32, 24, 16, 12, 8, 6, 4, 3, 2, or 1 MHz (TYP.) by using the option byte (000C2H). When 64 MHz or 48 MHz is selected as fHOCO, fIH is set to 32 MHz or 24 MHz, respectively. When 32 MHz or less is selected as fHOCO, fIH is not divided and set to the same frequency as fHOCO. After a reset release, the CPU always starts operating with this high-speed on-chip oscillator clock. Oscillation can be stopped by executing the STOP instruction or setting of the HIOSTOP bit (bit 0 of the CSC register).
The frequency specified by using an option byte can be changed by using the high-speed on-chip oscillator frequency select register (HOCODIV).
For details about the frequency, refer to Chapter 5 Clock Generator in "RL78/G1F user's Manual: hardware (R01UH0516EJ0110) ".

- On-chip oscillator characteristics

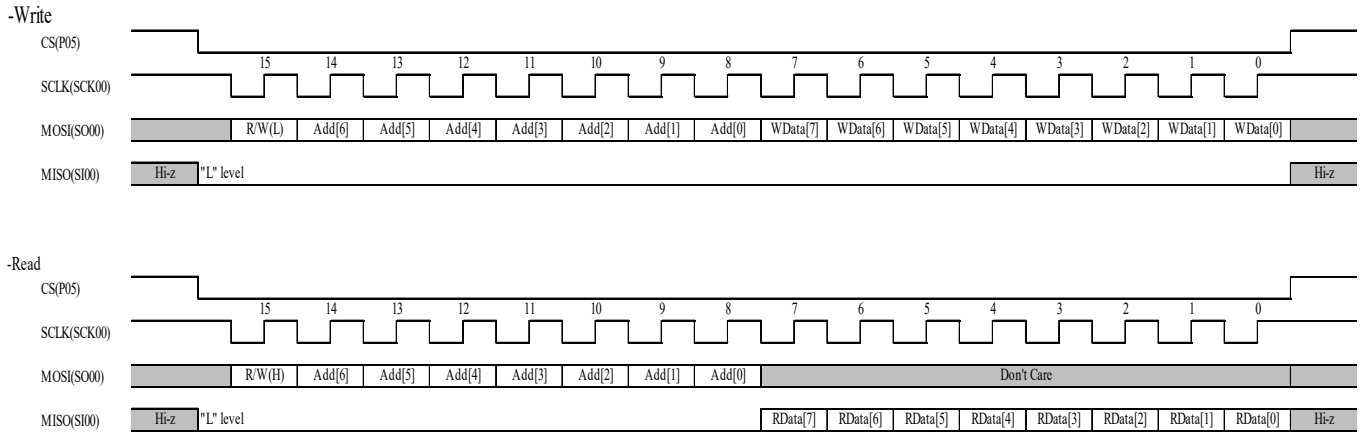
(TA = -40 to +85 degC, 4.06V <= VDD <= 5.25V , Vss = 0V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	fIH	4.06V <= VDD <= 5.25V	1	-	32	MHz
High-speed on-chip oscillator clock frequency accuracy	-	TA = -20 to +85 degC	-1	-	+1	%
		TA = -40 to -20 degC	-1.5	-	1.5	%
Low-speed on-chip oscillator clock frequency	fIL	-	-	15	-	kHz
Low-speed on-chip oscillator clock frequency accuracy	-	-	-15	-	+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H/010C2H) and bits 0 to 2 of the HOCODIV register.
Note 2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Communication Format

Shown a communication format of the 3-wire serial I/O communication as follows.
The data when the communication format except the following communication format was used become invalid.



Control Registers

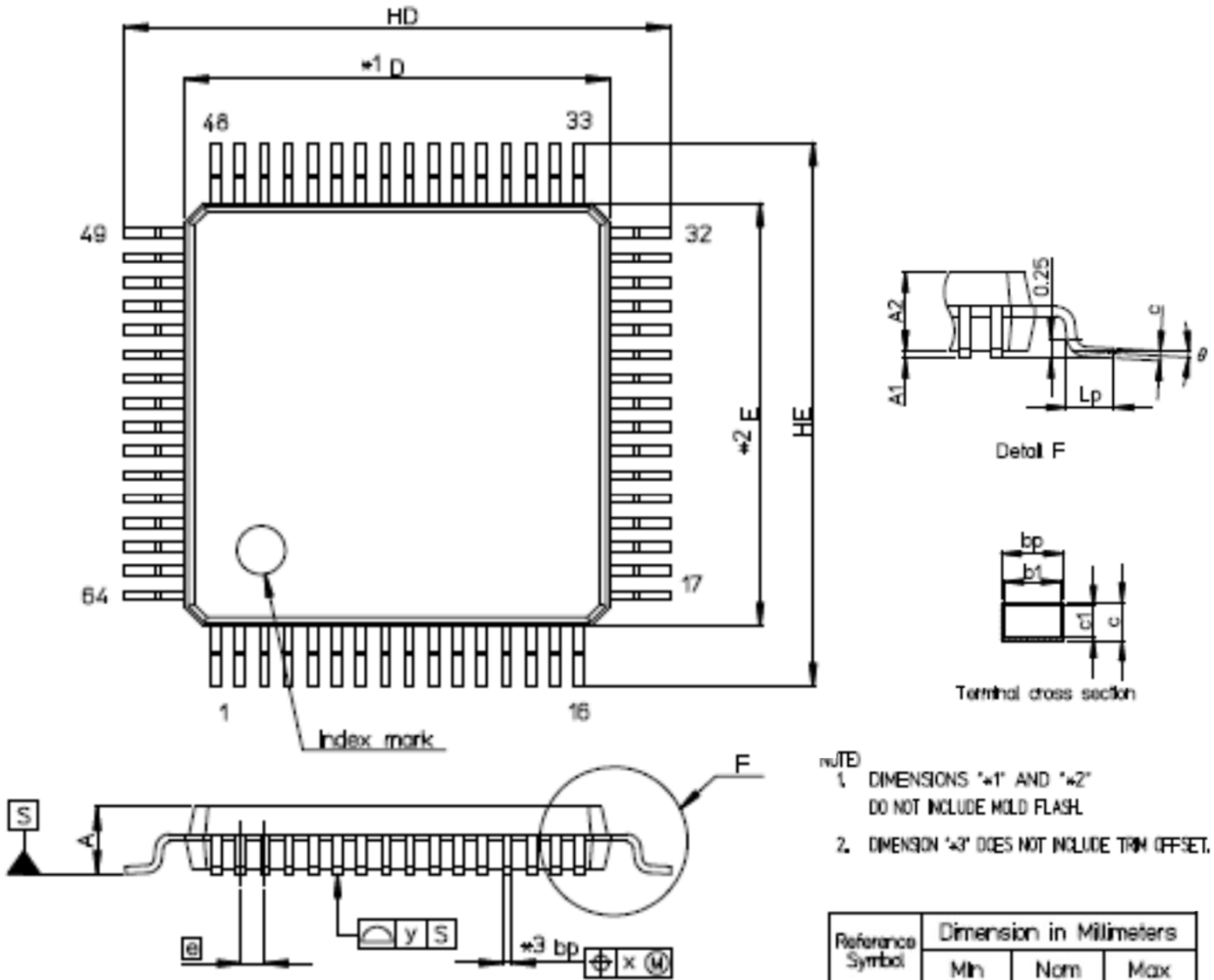
Shown Register Map as follows.

Add.	Register Name	Symbol	Initial value	7	6	5	4	3	2	1	0
02h	Power Save Control Register	PS_ALL	00h	0	0	0	0	0	0	0	PS_ALL_N
04h	By Function Power Save Control Setting Register	PS	00h	PS_PRE_N	0	PS_BMF_N	PS_CSAMP_N	PS_VMC_N	PS_HALL_N	PS_CPREG_N	PS_CP_N
06h	Software Reset Register	SW_RESET	00h	0	0	0	0	0	0	0	SW_RESET
08h	ADC Selector Register	ADC_SEL	00h	0	0	0	0	ADC_CH_SEL3 to 0			
0Ah	U Phase Moter Control Signal Select Register	SELSIG_U	03h	0	SELSIG_U_H2 to 0			0	SELSIG_U_L2 to 0		
0Ch	V Phase Moter Control Signal Select Register	SELSIG_V	14h	0	SELSIG_V_H2 to 0			0	SELSIG_V_L2 to 0		
0Eh	W Phase Moter Control Signal Select Register	SELSIG_W	25h	0	SELSIG_W_H2 to 0			0	SELSIG_W_L2 to 0		
10h	Hall Signal Processing Setting Register	HALL_SIG	00h	BEMF_MODE_SEL	CENTERTAP_SEL	HALL_MODE_SEL	PWM_SEL	HALL_POLA	HALL_SEL2 to 0		
12h	ALARM Status Register1	ALMSTS1	FFh	VREG5_OVP_N	VGT_OVP1_N	VGT_OVP2_N	VGT_UVP_N	VGB_OVP_N	VGB_UVP_N	OCP_N	TSDOP_N
14h	ALARM Operation Setting Register1	ALMOPE1	00h	0	0	0	VGT_UVP_OPE_N	0	VGB_UVP_OPE_N	OCP_OPE_N	TSD_OPE_N
16h	ALARM Pin Output Setting Register1	ALMOUT1	00h	REGV5_OVP_ALE_N	VGT_OVP1_ALE_N	VGT_OVP2_ALE_N	VGT_UVP_ALE_N	VGB_OVP_ALE_N	VGB_UVP_ALE_N	OCP_ALE_N	TSD_ALE_N
18h	ALARM Status Register2	ALMSTS2	FFh	1	1	1	1	1	1	1	VM_UVP_N
1Ah	Current Sense setting Register2	CS_SET2	00h	CSAMP_IREF1 to 0		CSAMP_ATT	0	0	0	0	0
1Ch	ALARM Pin Output Setting Register2	ALMOUT2	00h	0	0	0	0	0	0	0	VM_UVP_ALE_N
1Eh	Error Detection Wait Time Setting Register	ERROR_WAIT	00h	0	0	0	REGV5_OVP_WAIT	UVCP_WAIT1 to 0		OCPWAIT1 to 0	
20h	Current Sense setting Register1	CS_SET1	00h	0	SHUNT_SEL2 to 0			OCP_SEL_H3 to 0			
22h	Hall IC Threshold Adjustment Register	HAIC_TH	00h	0	0	HAIC_HYS1 to 0		0	HAIC_TH2 to 0		
24h	Pre-Driver Drive Status Register	PDDSTS	F0h	1	1	1	LDS_N	FG	HALL_MONI_U	HALL_MONI_V	HALL_MONI_W
26h	LD Judgment Wait Time Register	LDWAIT	00h	LD_ALE_N	0	0	0	0	LD_WAIT2 to 0		
28h	Motor Drive Control Setting Register	DRIVE_SET	00h	OCP_HYS_N	ALM_LATCH_CLR	0	DECAY_MODE_SEL	DT_REG_N	OCP_ERR_SEL	DIR_SEL	MOT_EN
2Ah	-	-	-	0	0	0	0	0	0	0	0
2Ch	High Side Output Current Capability Setting Register	IDRCNT_H	00h	0	IDR_H_P2 to 0			0	IDR_H_N2 to 0		
2Eh	Low Side Output Current Capability Setting Register	IDRCNT_L	00h	0	IDR_L_P2 to 0			0	IDR_L_N2 to 0		
30h	Pch Slew Rate Setting Register	TRCNT_P	00h	0	TR_H_P2 to 0			0	TP_L_P2 to 0		
32h	Charge Pump Setting Register1	CPSET1	01h	0	0	0	0	0	0	CP_CLK_DIV1 to 0	
34h	Charge Pump Setting Register2	CPSET2	02h	0	0	0	0	CP_BOOST_N	VREG10_OUT	VREG6P5_OUT	0
36h	Cahrge Pump Trimming Register	CP_TRIM	00h	CP_TRIM7 - CP_TRIM0							
38h to 3Eh	-	-	-	0	0	0	0	0	0	0	0
40h	5V Regulator Voltage Setting	VREG5_TRIM	00h	VREG5_TRIM7 - VREG5_TRIM0							
42h	Ext. FET Curent Detect AMP Setting Register	CSAMP_TRIM	00h	CSAMP_TRIM7 - CSAMP_TRIM0							
44h to 56h	-	-	-	0	0	0	0	0	0	0	0
58h	ALARM Raw Status Monitor Register1	ALMRAW1	FFh	1	VGT_OVP1_RAW_N	VGT_OVP2_RAW_N	VGT_UVP_RAW_N	VGT_OVP_RAW_N	VGB_UVP_RAW_N	1	1
5Ah	-	-	-	0	0	0	0	0	0	0	0
5Ch	TOIN Pin Monitor Register	TOIN_MONI	-	TOINA	TOINB	TOINC	TOIND	TOINE	TOINF	TOING	TOINH
5Eh	WHO_AM_I	WHO_AM_I	6Ah	0	1	1	0	1	0	1	0
60h	Trimming Protect Register	TRIM_PT	00h	TRIM_PT7 - TRIM_PT0							
62h to 72h	-	-	-	0	0	0	0	0	0	0	0
74h	Trimming Data Valid Regsiter	TRIM_EN	00h	0	0	0	0	0	0	0	TRIM_EN
76h	-	-	-	0	0	0	0	0	0	0	0
78h	High Precise BGR Temp. Correction Register	BGR_TRIM	FFh	BGR_TRIM_7 - BGR_TRIM0							
7Ah	BUFFAMP Absolute Vaue Correction Register	BFAMP_TRIM	FFh	BFAMP_TRIM_7 - BFAMP_TRIM_0							
7Ch to 7Eh	-	-	-	0	0	0	0	0	0	0	0

The detail is shown in "RL78/G1F User's manual: Hardware" (R01UH0516EJ0110), so please see it.

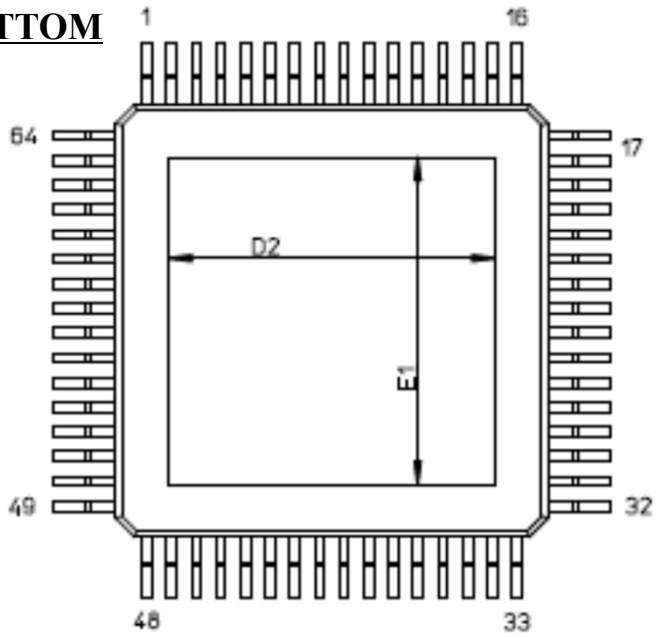
7 PACKAGE SPECIFICATION[P-HTFQFP64 [JEITA]

TOP



NOTE
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

BOTTOM



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
A2	0.95	1.00	1.05
HD	—	9.0	—
HE	—	9.0	—
A	—	—	1.20
A1	0.05	—	0.15
bp	0.13	—	0.23
b1	0.13	0.16	0.19
c	0.09	—	0.20
c1	0.09	—	0.16
θ	0°	—	7°
e	—	0.4	—
x	—	—	0.07
y	—	—	0.08
Lp	0.45	0.6	0.75
D2	—	5.3	—
E1	—	5.3	—

8 BUILT-IN RL78/G1F PIN SPEC

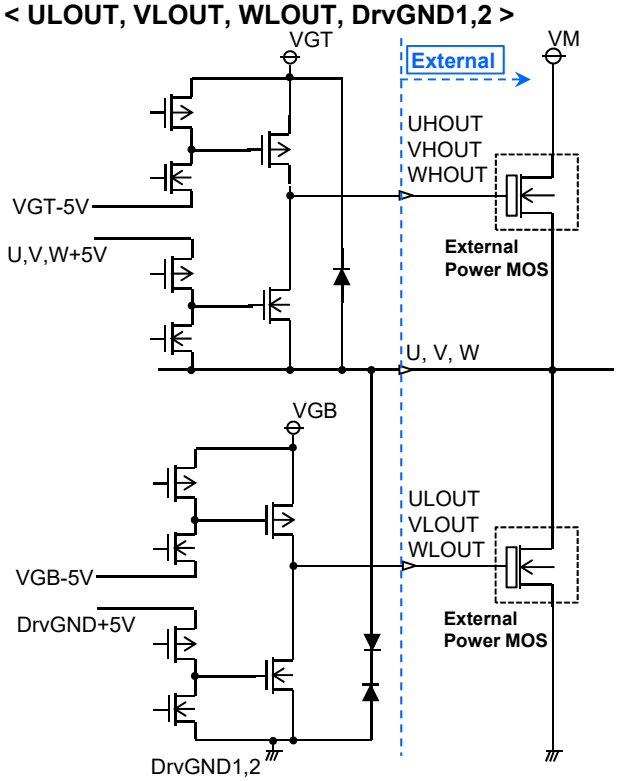
RL78/G1F 64Pin specification						RAJ306000 Series		
Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function	Function	Alternate Function	Terminal No.
P00	7-1-4	I/O	Input port	TI00/TRGCLKA/(TRJO0)/(INTP8)	Port 0. 7-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a softw are setting at input port. Input of P01, P03 and P04 can be set to TTL input buffer. Output of P00 and P02 to P04 can be set to N-ch open-drain output (EVDD tolerance). P02 and P03 can be set to analog input[Note].	P00	TI00/TRGCLKA/(TRJO0)/(INTP8)	2
P01	8-1-3			TO00/TRGCLKB/TRJIO0/(INTP10)		P01	TO00/TRGCLKB/TRJIO0/(INTP10)	1
P02	7-9-2		Analog function	ANI17/SO10/TxD1/IVCMP10		SO10	P02/ANI17/TxD1/IVCMP10	64
P03	8-9-2			ANI16/SI10/RxD1/SDA10/IVCMP11		SI10	P03/ANI16/RxD1/SI10/SDA10/IVCMP11	63
P04	8-1-4		Input port	SCK10/SCL10		SCK10	P04/SCL10	62
P05	7-1-3			(INTP10)				
P06				(INTP11)/(TRJIO0)		Interconnect		CLK
P10	8-3-8	I/O	Analog function	ANI20/SCK11/SCL11/TRDIOD1	Port 1. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a softw are setting at input port. Input of P10, P14 to P17 can be set to TTL input buffer. Output of P10, P11, P13 to P15, and P17 can be set to N-ch open-drain output (EVDD tolerance). P10 to P14 can be set to analog input[Note].	Interconnect		TOINF
P11	7-3-8			ANI21/SI11/SDA11/TRDIOC1		Interconnect		TOINE
P12	7-3-7			ANI22/SO11/TRDIOB1/(INTP5)		Interconnect		TOINC
P13	7-3-8			ANI23/TxD2/SO20/TRDIOA1/IrTxD		Interconnect		TOINB
P14	8-3-8			ANI24/RxD2/SI20/SDA20/TRDIOD0/(SCLA0)/IrRxD		Interconnect		TOIND
P15	8-1-8			SCK20/SCL20/TRDIOB0/(SDAA0)		Interconnect		TOINA
P16	8-1-7			TI01/TO01/INTP5/TRDIOC0/(SI00/RxD0)/(TRDIOA1)		Interconnect		TOINH
P17	8-1-8			TI02/TO02/TRDIOA0/TRDCLK/(SO00/TxD0)/(TRDIOD0)		Interconnect		TOING
P20	4-9-1	I/O	Analog function	ANI0/AVREFP/IVCMP12/(INTP11)	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units. Can be set to analog input[Note].	ANI0	P20/AVREFP/IVCMP12	61
P21				ANI1/AVREFM/IVCMP13		ANI1	AVREFM/P21/VCMP13	60
P22	4-16-1			ANI2/ANO0/PGAI/IVCMP0		ANI2	P22/ANO0/PGAI/IVCMP0	59
P23	4-15-1			ANI3/ANO1/PGAGND		ANI3	P23/ANO1/PGAGND	58
P24	4-3-3			ANI4		ANI4	P24	57
P25				ANI5		ANI5	P25	56
P26				ANI6		ANI6	P26	55
P27				ANI7		Interconnect		ISENADIN
P30	8-1-4	I/O	Input port	INTP3/RTC1HZ/SCK00/SCL00/TRJO0/(TRDIOB1)	Port 3. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a softw are setting at input port. Input of P30 can be set to TTL input buffer. Output of P30 can be set to N-ch open-drain output (EVDD tolerance).	Interconnect		SPI
P31	7-1-3			TI03/TO03/INTP4/(TRJIO0)/(PCLBUZ0)/VCOUT1		P31	TI03/TO03/INTP4/(TRJIO0)//VCOUT1	19
P40	7-1-3	I/O	Input port	TOOL0	Port 4. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a softw are setting at input port.	TOOL0	P40	8
P41				(TRJIO0)		P41	(TRJIO0)	7
P42				(INTP8)		P42	INTP8 [Note 2]	6
P43				(INTP9)		P43	INTP9 [Note 2]	5
P50	8-1-4	I/O	Input port	INTP1/SI00/RxD0/TOOLRxD/SDA00/TRGIOA/(TRJO0)/(TRDIOC1)	Port 5. 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a softw are setting at input port. Input of P50 and P55 can be set to TTL input buffer. Output of P50, P51, and P55 can be set to N-ch open-drain output (EVDD tolerance).	Interconnect		SPI
P51	7-1-4			INTP2/SO00/TxD0/TOOLTxD/TRGIOB/(TRDIOD1)		Interconnect		SPI
P52	7-1-3			(INTP1)		Interconnect		HIC_U
P53				(INTP2)		Interconnect		HIC_V
P54				(INTP3)		Interconnect		HIC_W
P55	8-1-4			(INTP4)/(PCLBUZ1)/(SCK00)		Interconnect		ALARM
P60	12-1-2	I/O	Input port	SCLA0	Port 6. 4-bit I/O port. Input/output can be specified in 1-bit units. Output of P60 to P63 is N-ch open-drain output (6 V tolerance).	P60	SCLA0	15
P61				SDAA0		P61	SDAA0	16
P62				/SSI00		P62	/SSI00 (Need to set SSIE00 = 0)	17
P63				—		P63	—	18
P70	7-1-3	I/O	Input port	KR0/SCK21/SCL21/(VCOUT1)	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a softw are setting at input port. Output of P71 and P74 can be set to N-ch opendrain output (EVDD tolerance).			
P71	7-1-4			KR1/SI21/SDA21/(VCOUT0)				
P72	7-1-3			KR2/SO21				
P73				KR3/SO01		P73	SO01	24
P74	7-1-4			KR4/INTP8/SI01/SDA01		P74	SI01/SDA01 [Note 2]	23
P75	7-1-3			KR5/INTP9/SCK01/SCL01		P75	SCK01/SCL01 [Note 2]	22
P76				KR6/INTP10/(RxD2)		P76	INTP10	21
P77				KR7/INTP11/(TxD2)		P77	INTP11	20
P120	7-3-3	I/O	Analog function	ANI19/VCOUT0	Port 12. 1-bit I/O port and 4-bit input-only port. P120 can be set to analog input. For only P120, input/output can be specified. For only P120, use of an on-chip pull-up resistor can be specified by a softw are setting at input port. P120 can be set to analog input[Note].			
P121	2-2-1	Input	Input port	X1				
P122				X2/EXCLK		P122	X2/EXCLK	11
P123				XT1				
P124				XT2/EXCLKS				
P130	1-1-1	Output	Output port	—	Port 13.			
P137	2-1-2	Input	Input port	INTP0	1-bit output-only port and 1-bit input-only port.	P137	INTP0	10
P140	7-1-3	I/O	Input port	PCLBUZ0/INTP6	Port 14. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a softw are setting at input port. P147 can be set to analog input[Note].	P140	PCLBUZ0/INTP6	4
P141				PCLBUZ1/INTP7		P141	PCLBUZ1/INTP7	3
P146				—		Interconnect		LD
P147	7-3-3		Analog function	ANI18/IVREF0				
/RESET	2-1-1	Input	—	—	Input-only pin for external reset. Connect to VDD directly or via a resistor w hen external reset is not used.	/RESET	-	9

Note : Each pin can be specified as either digital or analog by setting port mode control register x (PMCx) (Can be specified in 1-bit units).

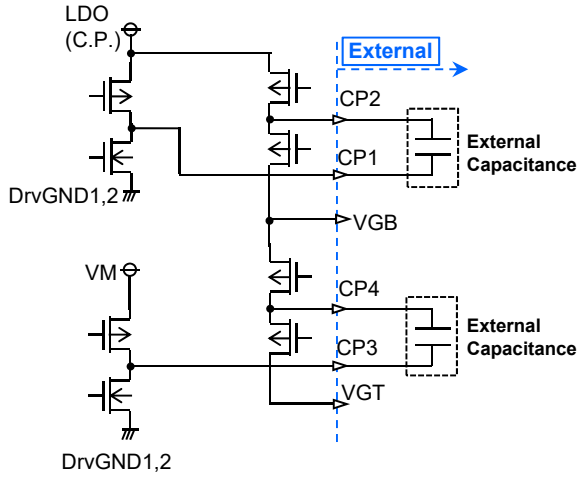
Remark : Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection registers 0 to 2 (PIOR0 to PIOR2).

8 PRE-DRIVER I/O CIRCUIT

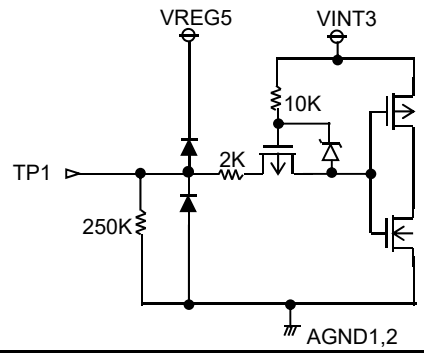
< UHOUT, U, VHOUT, V, WHOUT, W >
< ULOUT, VLOUT, WLOUT, DrvGND1,2 >



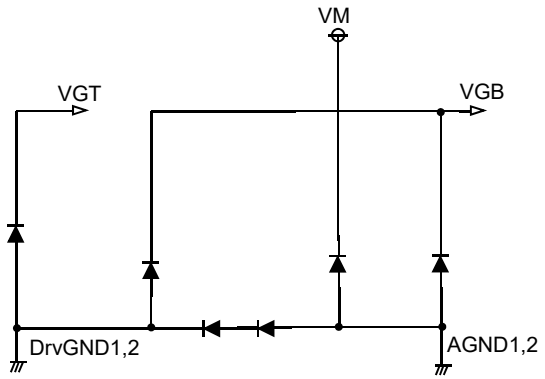
< CP1, CP2, VGB, CP3, CP4, VGT , VM >



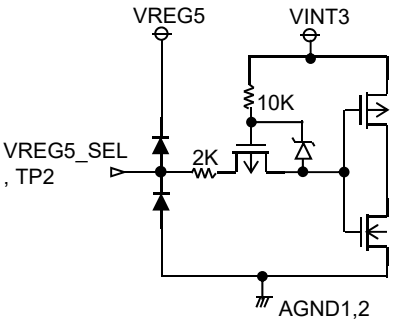
< TP1 >



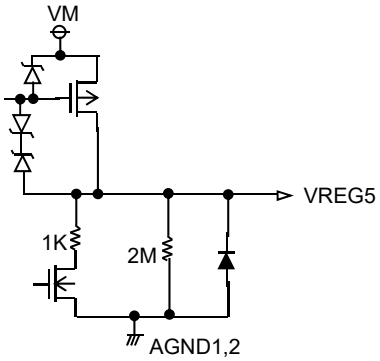
< VM / VGB / VGT / GND structure >



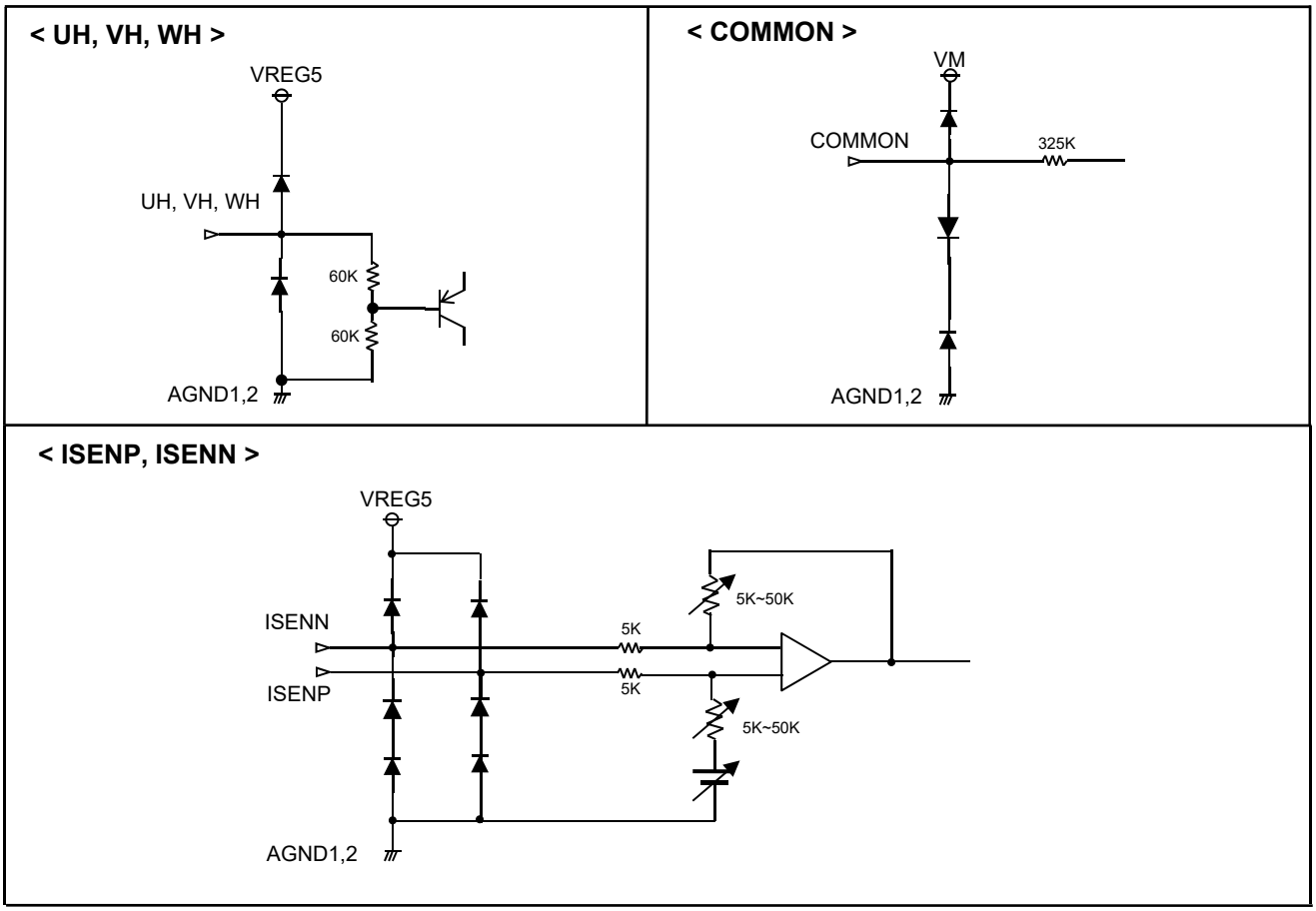
< VREG5_SEL, TP2 >



< VREG5 >



I/O Circuit



*1: On RL78/G1F terminal, please refer to “RL78/G1F User’s manual: Hardware” (R01UH0516EJ0110).

Revision History	RAJ306000GFT Data Sheet

Rev	Date	Description	
		Page	Summary
1.00	2017.09.06	-	
1.01	2017.09.26	3, 4, 5, 13, 14, 17~19, 23	"RL78/G1F User's manual: Hardware" (IMB-PB-170186 -> R01UH0516EJ0110)

Notes for CMOS devices

(1) Voltage application waveform at input pin:	Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
(2) Handling of unused input pins:	Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
(3) Precaution against ESD:	A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
(4) Status before initialization:	Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
(5) Power ON/OFF sequence:	In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
(6) Input of signal during power off state:	Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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