

# READ2351J

Ultra-Small Low Voltage Drive Input Output Full Range

CMOS Dual Operational Amplifier

R03DS0098EJ0200

Rev.2.00

$V_{IO} \leq \pm 6\text{mV}$ ,  $\text{SR} = 0.35\text{V}/\mu\text{s}$ ,  $\text{GBW} = 550\text{kHz}$

Apr. 17, 2017

## Description

The READ2351J is input and output full range dual CMOS Operational Amplifier realizing low voltage and low current consumption operation. This IC can be used in minimum operating supply voltage from 1.8V, and in wide ambient temperature range from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

Available in ultra-small 8 pins TSSOP package.

## Features

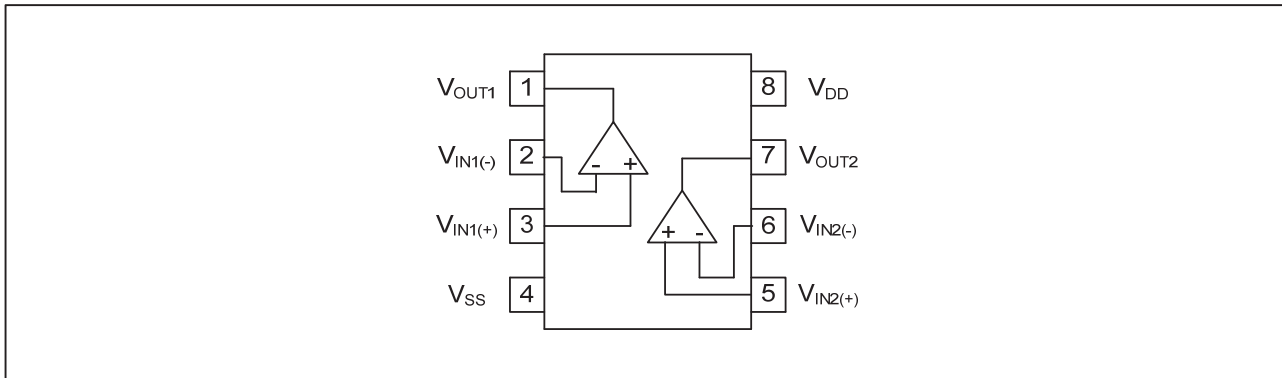
- Low voltage single supply operation  $V_{DD} = 1.8\text{V}$  to  $5.5\text{V}$
- Low input offset voltage  $V_{IO} \leq \pm 6.0\text{mV}$
- Low input bias current  $I_B \leq (1\text{pA})$ .
- Wide output voltage range  $V_{OUT} : V_{SS} + 0.1\text{V}$  to  $V_{DD} - 0.1\text{V} (@I_O = 1\text{mA})$
- Supply current (per channel)  $I_{DD} = 40\mu\text{A}$  Typ.
- High slew rate  $\text{SR} = 0.35\text{V}/\mu\text{s}$  Typ.

( ) reference value of design

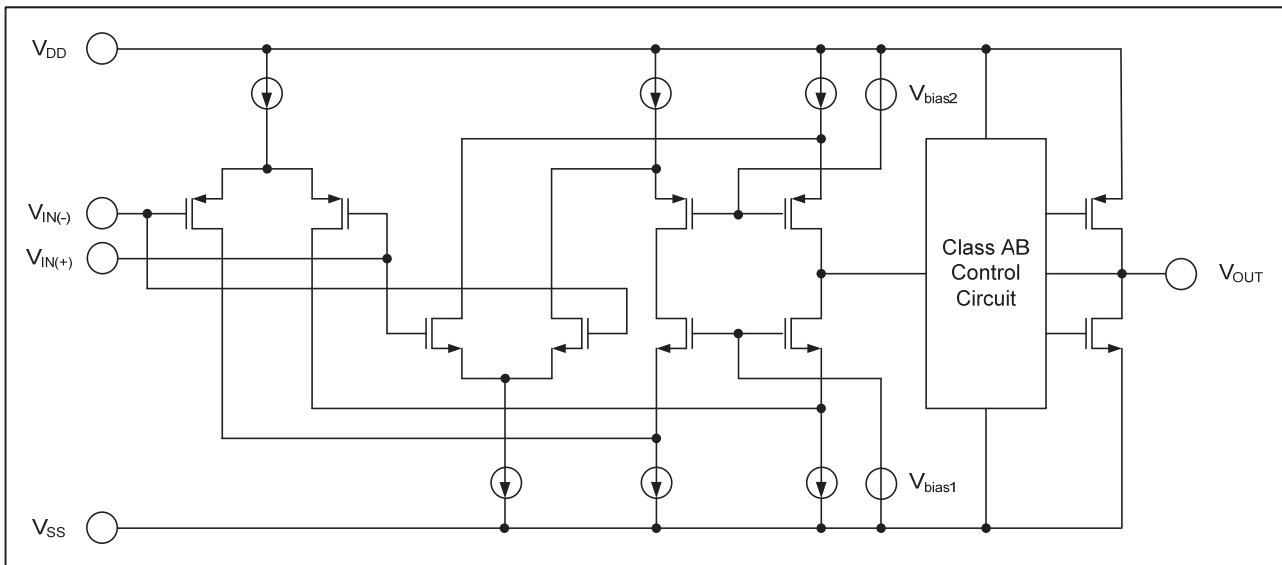
## Product Line-up

Type name	Product type quality level	Package
READ2351JSP	Low consumption current with high quality level	8 pins plastic TSSOP

Pin Arrangement



Equivalent Circuit (per one channel)



Absolute Maximum Ratings

<T<sub>A</sub>=25 °C >

Items	Symbol	Ratings	Unit
Supply voltage <sup>Note.1</sup>	V <sub>DD</sub>	-0.3 to +6.5	V
Differential input voltage	V <sub>ID</sub>	-V <sub>DD</sub> to +V <sub>DD</sub>	V
Input voltage <sup>Note.2</sup>	V <sub>I</sub>	-0.3 to V <sub>DD</sub> +0.3	V
Maximum output current	I <sub>O</sub>	10	mA
Power dissipation <sup>Note.3</sup>	P <sub>T</sub>	440	mW
Junction temperature	T <sub>J</sub>	+150	°C
Operating temp. range	T <sub>A</sub>	-40 to +125	°C
Storage temp. range	T <sub>stg</sub>	-55 to +150	°C

Note 1. Please take note that reverse connection of a power supply may cause destruction.

2. Stresses above these ratings may cause permanent damage such as characteristics degradation or destruction. Please do not exceed voltage below of GND-0.3V as it is bottom limit. In addition, operation amplifier is operated as normal when input voltage for electrical characteristics is in common mode input voltage range.

3. The value is measured under mounted on a glass epoxy base board (size 100mm×100mm, 1mm thickness, copper foiled surface base board area with 15% solid pattern). Please take note that every package has derating rate's restriction reception.

**Electrical Characteristics**<V<sub>DD</sub>=3.3V, T<sub>A</sub>=25°C >

Items	Symbol	MIN.	TYP.	MAX.	Unit	Test Condition
Supply voltage	V <sub>DD</sub> - V <sub>SS</sub>	1.8		5.5	V	
Input offset voltage	V <sub>IO</sub>			±6.0	mV	
Input offset current	I <sub>IO</sub>			(1)	pA	
Input bias current	I <sub>B</sub>			(1)	pA	
Output high voltage	V <sub>OH</sub>	V <sub>DD</sub> -0.1			V	I <sub>L</sub> = 1mA
Output low voltage	V <sub>OL</sub>			V <sub>SS</sub> +0.1	V	I <sub>L</sub> = 1mA
Voltage gain	A <sub>v</sub>	80	120		dB	R <sub>L</sub> ≥100kΩ
Channel supply current	I <sub>DD</sub> /ch		40	80	μA	R <sub>L</sub> =∞, I <sub>O</sub> =0
Common mode rejection ratio	CMRR	60	80		dB	
Supply voltage rejection ratio	SVRR	60	80		dB	
Common mode input voltage range	V <sub>ICM</sub>	V <sub>SS</sub>		V <sub>DD</sub>	V	
Gain bandwidth product	GBW		550		kHz	C <sub>L</sub> =20pF
Slew rate	SR		0.35		V/μs	C <sub>L</sub> =20pF

( ) reference value of design

## Notes

Output terminal : The over-current protection feature is not built in the output terminal of this product.

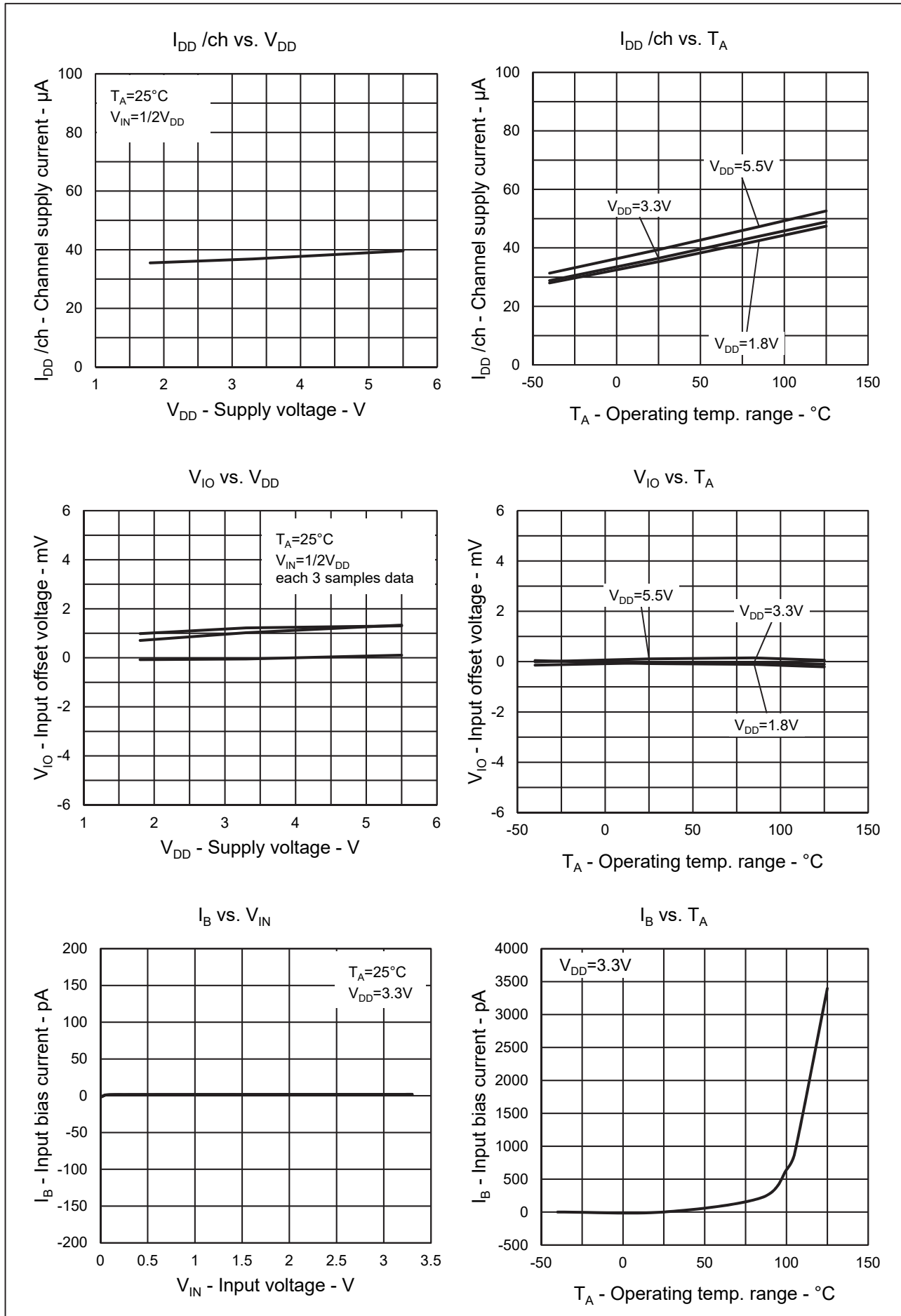
Therefore, please insert resistance to output port.

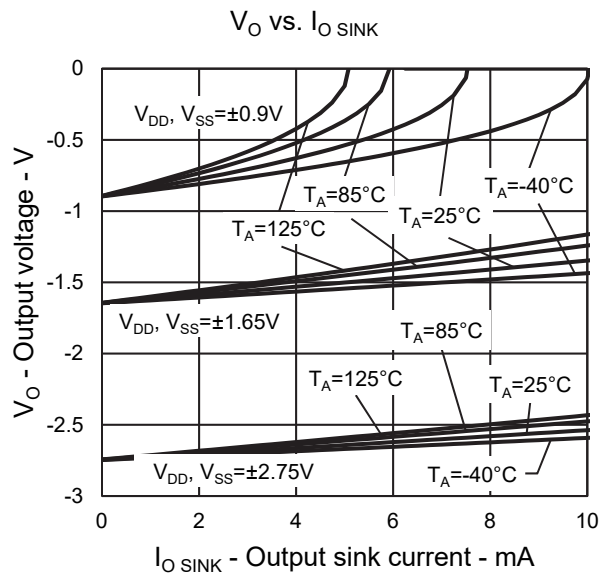
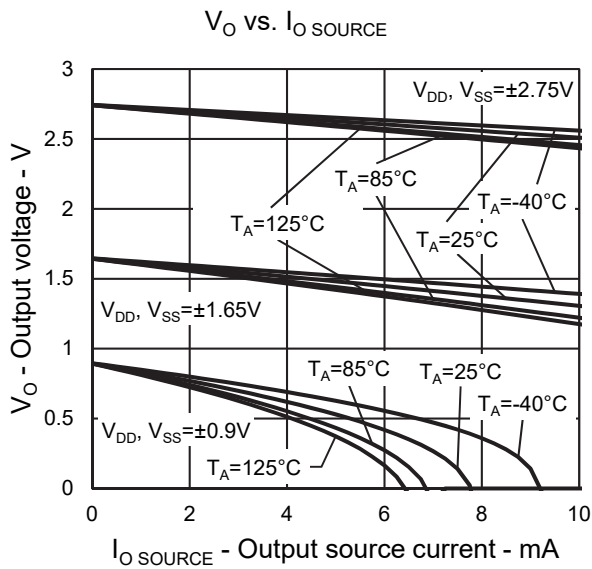
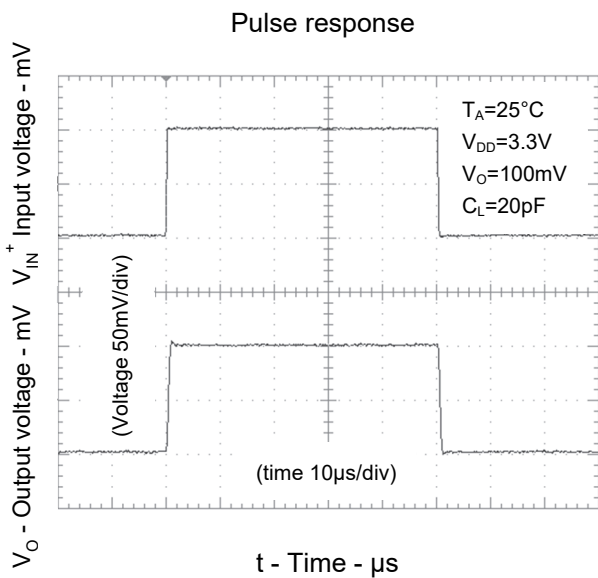
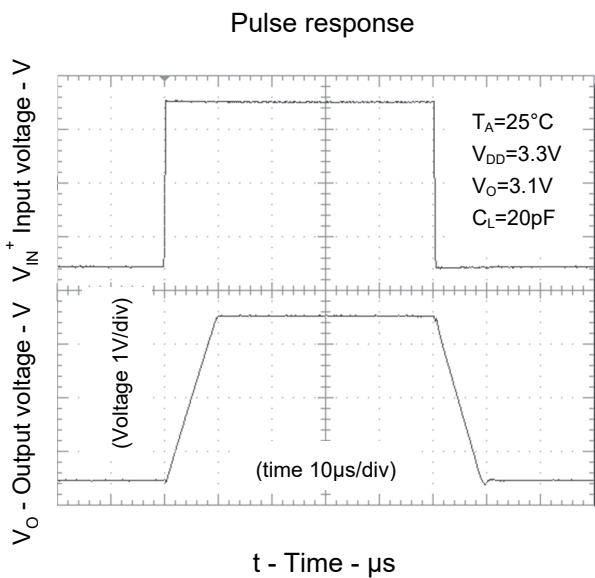
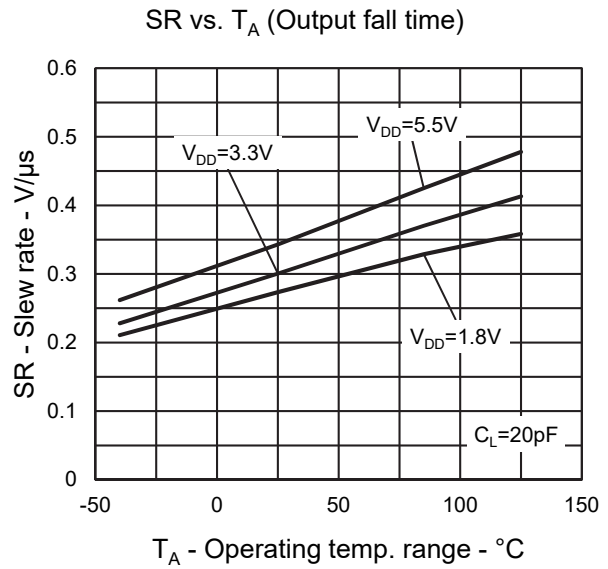
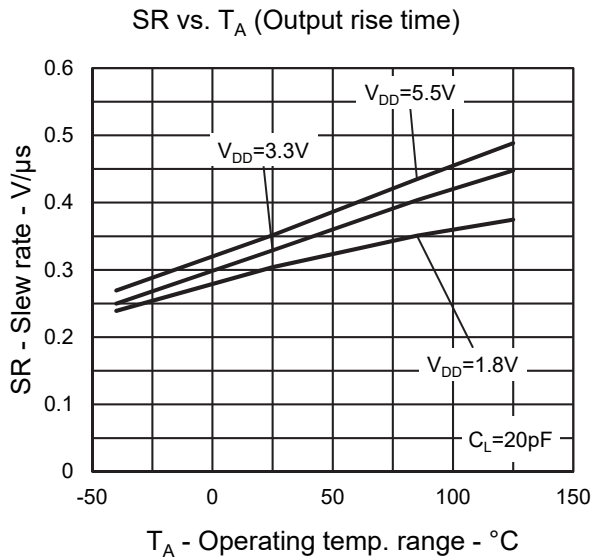
Input offset voltage : the amplifier circuit of the first block of operational amplifier.

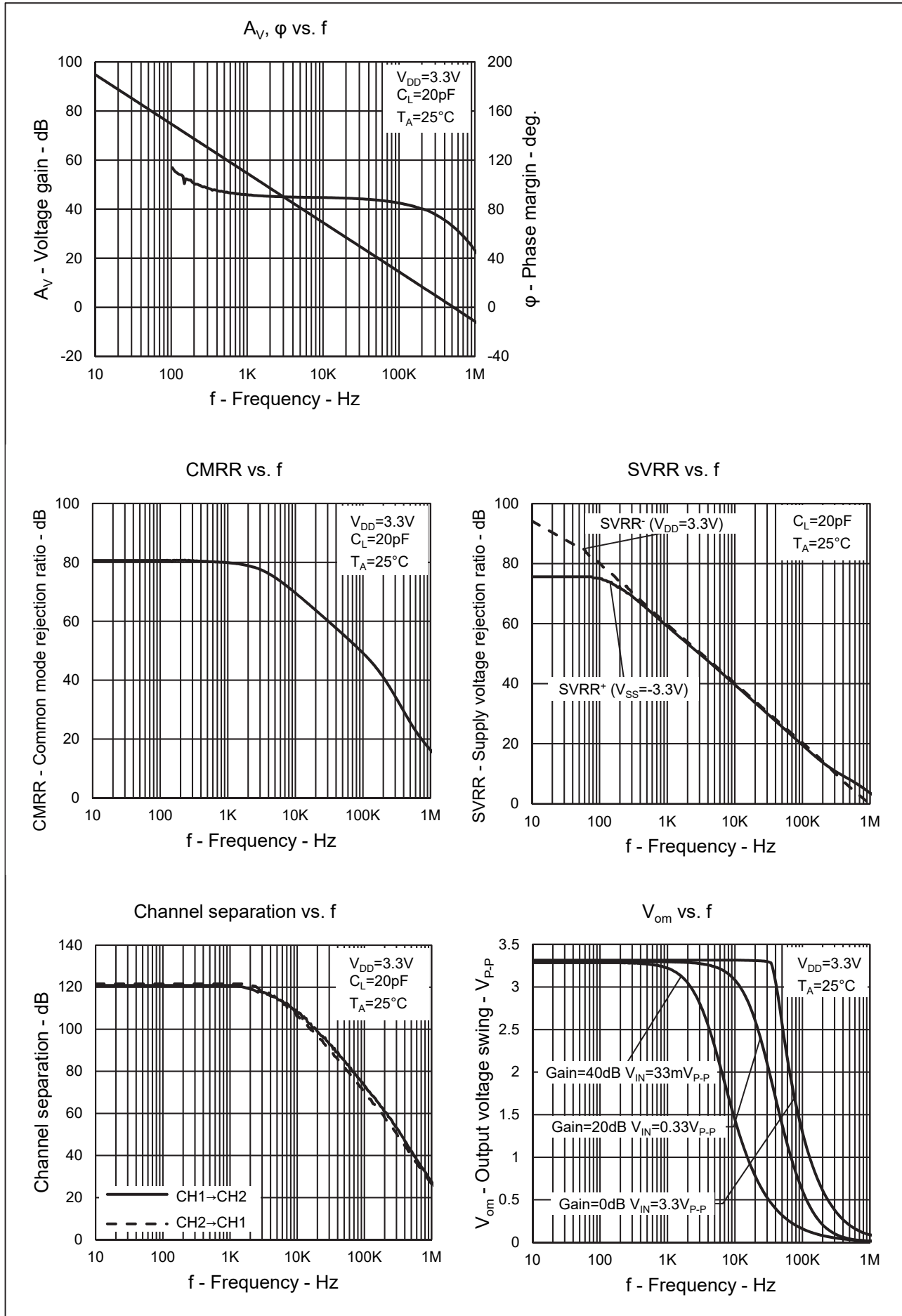
A circuit suitable for operation near GND, and a circuit suitable for operation near +power supply.

in case of input voltage of overlap point output port has a minute voltage shift or distortion.

Electrical Characteristics





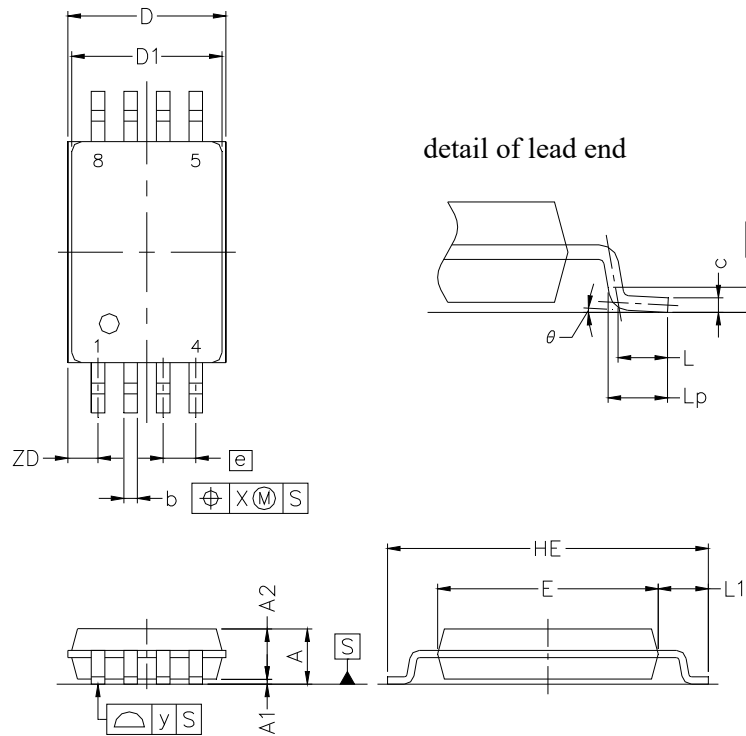


### Package Dimensions

#### 8-PIN PLASTIC TSSOP

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-TSSOP8-0225-0.65	PTSP0008JD-A	P8GR-65-9LG	-

Unit:mm



**NOTE**

Each lead centerline is located within 0.10 mm of its true position at maximum material condition.

ITEM	MILLIMETERS
D	3.15 ±0.15
D1	3.00 ±0.10
E	4.40 ±0.10
HE	6.40 ±0.20
A	1.20 MAX.
A1	0.10 ±0.05
A2	1.00 ±0.05
A3	0.25
b	0.24 <sup>+0.06</sup> <sub>-0.05</sub>
c	0.145 ±0.055
L	0.5
Lp	0.60 ±0.15
L1	1.00 ±0.20
$\theta$	3° <sup>+5°</sup> <sub>-3°</sub>
e	0.65
x	0.10
y	0.10
ZD	0.60

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