To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RJK2555DPA

Silicon N Channel MOS FET
High Speed Power Switching

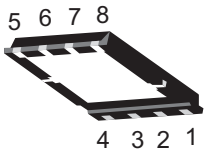
REJ03G1776-0200
Rev.2.00
Apr 09, 2009

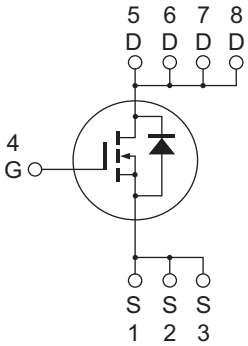
Features

- Low on-resistance
- Low drive current
- High density mounting

Outline

RENESAS Package code: PWSN0008DA-A
(Package name: WPAK)





1, 2, 3	Source
4	Gate
5, 6, 7, 8	Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	250	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	17	A
Drain peak current	$I_{D\ (pulse)}$ Note1	34	A
Body-drain diode reverse drain current	I_{DR}	17	A
Body-drain diode reverse drain peak current	$I_{DR\ (pulse)}$ Note1	34	A
Avalanche current	I_{AP} Note3	7	A
Avalanche energy	E_{AR} Note3	3.0	mJ
Channel dissipation	Pch Note2	30	W
Channel to case thermal impedance	θch-c	4.17	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. STch = 25°C, Tch ≤ 150°C

Electrical Characteristics

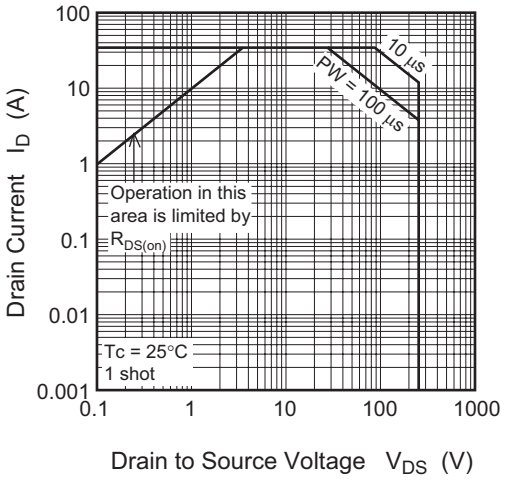
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	250	—	—	V	I_D = 10 mA, V_{GS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	µA	V_{DS} = 250 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±1	µA	V_{GS} = ±30 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	2.5	—	4.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	0.083	0.104	Ω	I_D = 8.5 A, V_{GS} = 10 V Note4
Input capacitance	Ciss	—	2400	—	pF	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	210	—	pF	
Reverse transfer capacitance	Crss	—	49	—	pF	
Turn-on delay time	$t_{d(on)}$	—	61	—	ns	I_D = 8.5 A V_{GS} = 10 V R_L = 14.7 Ω Rg = 10 Ω
Rise time	t_r	—	42	—	ns	
Turn-off delay time	$t_{d(off)}$	—	100	—	ns	
Fall time	t_f	—	33	—	ns	
Total gate charge	Qg	—	39	—	nC	V_{DD} = 200 V V_{GS} = 10 V I_D = 17 A
Gate to source charge	Qgs	—	12.4	—	nC	
Gate to drain charge	Qgd	—	10.5	—	nC	
Body-drain diode forward voltage	V_{DF}	—	0.90	1.35	V	I_F = 17 A, V_{GS} = 0 Note4
Body-drain diode reverse recovery time	t_{rr}	—	165	—	ns	I_F = 17 A, V_{GS} = 0 di_F/dt = 100 A/µs

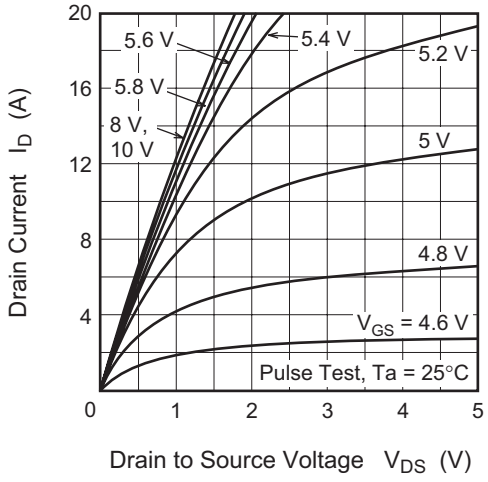
Notes: 4. Pulse test

Main Characteristics

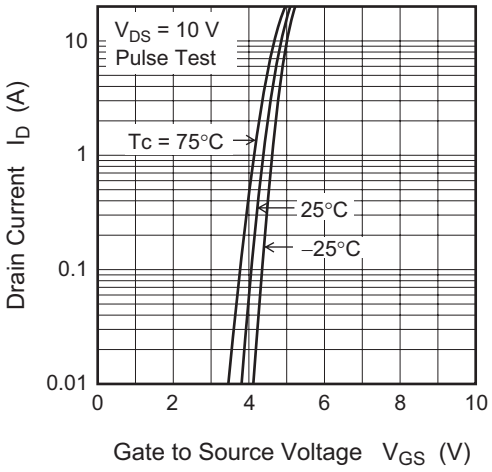
Maximum Safe Operation Area



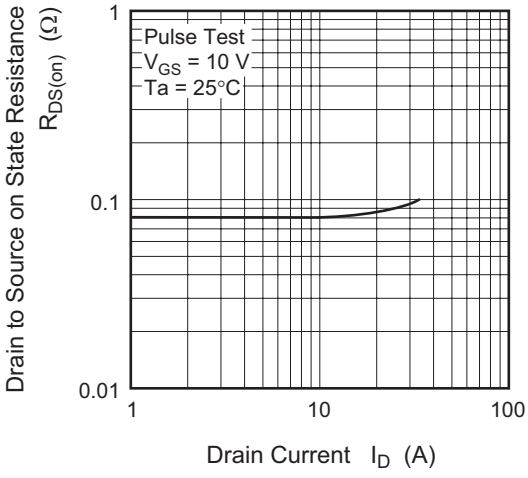
Typical Output Characteristics



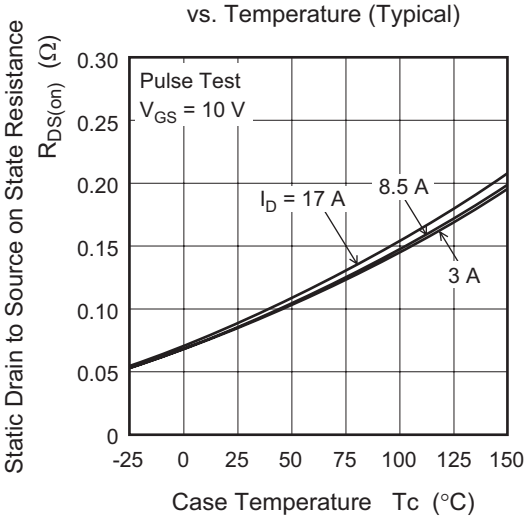
Typical Transfer Characteristics



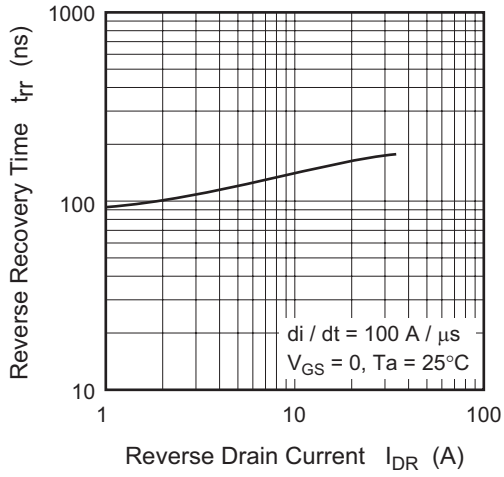
Static Drain to Source on State Resistance vs. Drain Current (Typical)



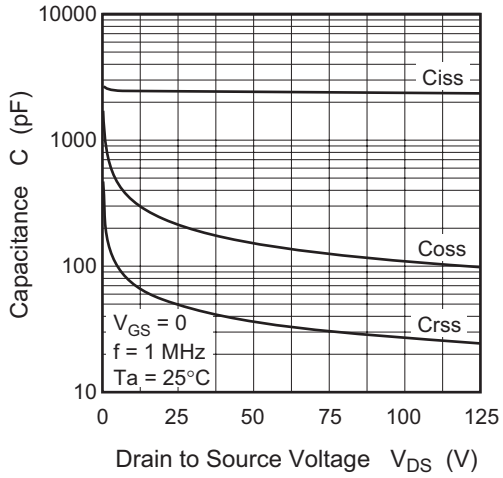
Static Drain to Source on State Resistance vs. Temperature (Typical)



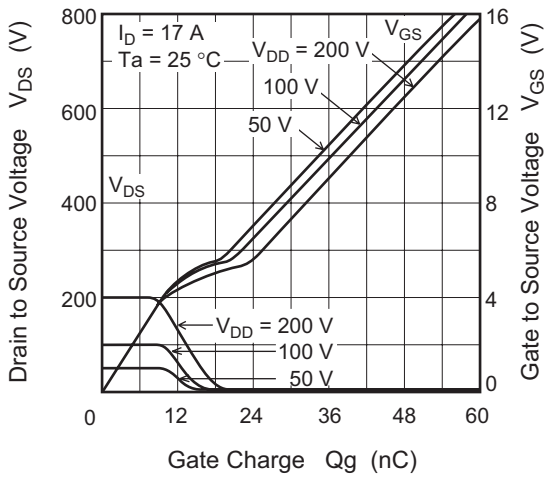
Body-Drain Diode Reverse Recovery Time (Typical)



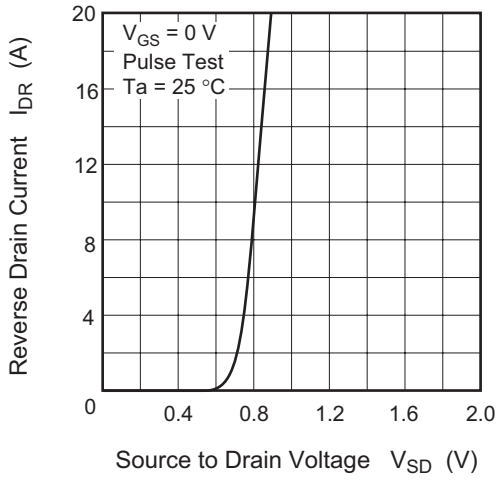
Typical Capacitance vs.
Drain to Source Voltage (Typical)



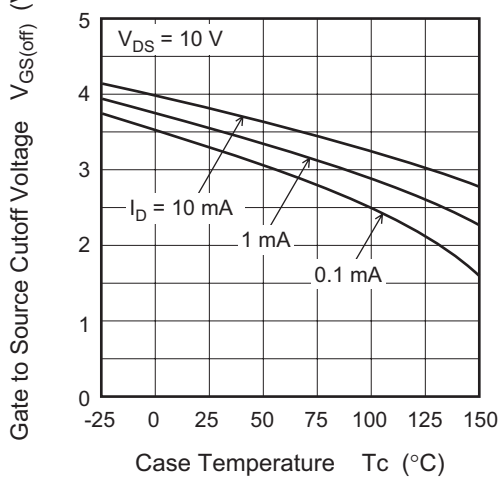
Dynamic Input Characteristics (Typical)



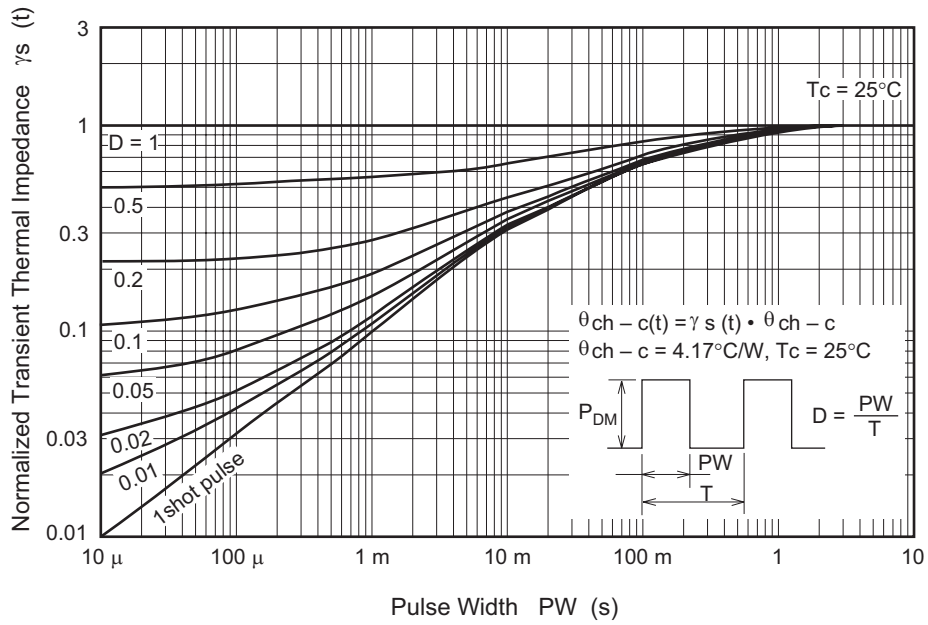
Reverse Drain Current vs.
Source to Drain Voltage (Typical)



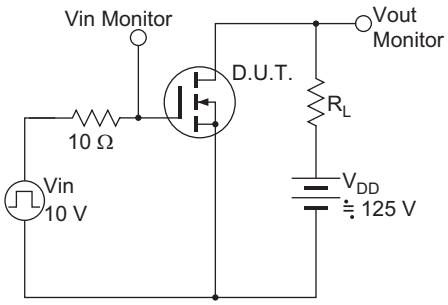
Gate to Source Cutoff Voltage
vs. Case Temperature (Typical)



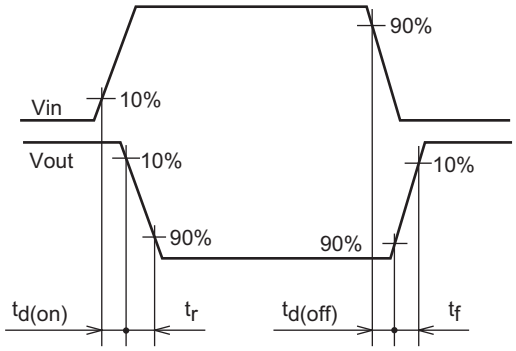
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



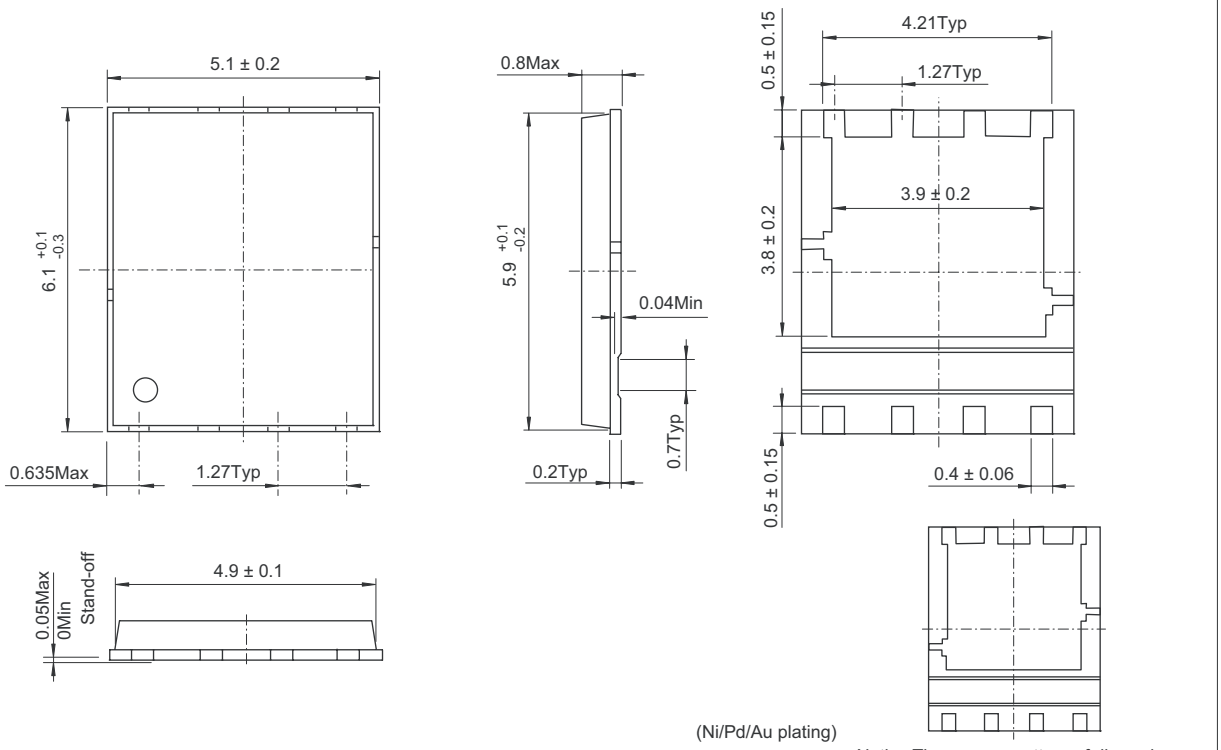
Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
WPAK	–	PWSN0008DA-A	WPAKV	0.075g

Unit: mm



Ordering Information

Part No.	Quantity	Shipping Container
RJK2555DPA-00-J0	2500 pcs	Taping

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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http://www.renesas.com

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Colophon .7.2