RJP1CS08DWA / RJP1CS08DWS

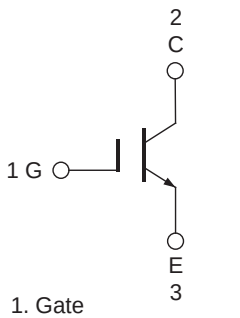
1250V - 200A - IGBT
Application: Inverter

R07DS0831EJ0400
Rev.4.00
Sep 30, 2015

Features

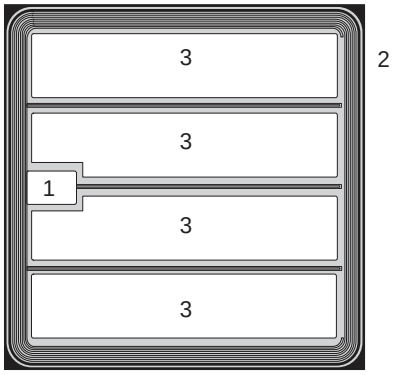
- Low collector to emitter saturation voltage
  $V_{CE(sat)}$ = 1.8 V typ. (at I_C = 200 A, V_{GE} = 15 V, Tc = 25°C)
- High speed switching
- Short circuit withstands time (10 μs min.)

Outline

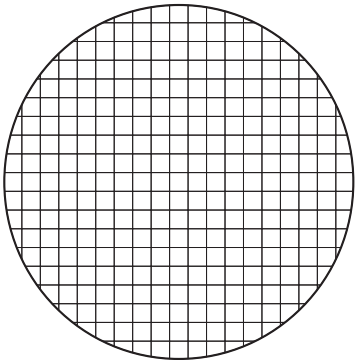


1. Gate
2. Collector (The back)
3. Emitter

Die



Wafer



Absolute Maximum Ratings

(Tc = 25°C unless otherwise noted)

Item		Symbol	Ratings	Unit
Collector to emitter voltage		V_{CES}	1250	V
Gate to emitter voltage		V_{GES}	±30	V
Collector current	Tc = 25°C	I_C	400	A
	Tc = 100°C	I_C	200	A
Junction temperature		Tj	175 Note1	°C

Notes: 1. Please use this device in the thermal conditions where the junction temperature does not exceed 175°C.
IGBT Application Note is disclosed about reliability test and application condition up to Tj = 175°C.

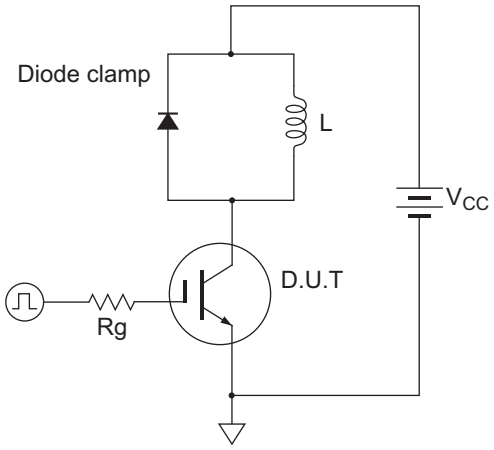
Electrical Characteristics (These data are actual measurement values in an evaluation package.)

(Tc = 25°C unless otherwise noted)

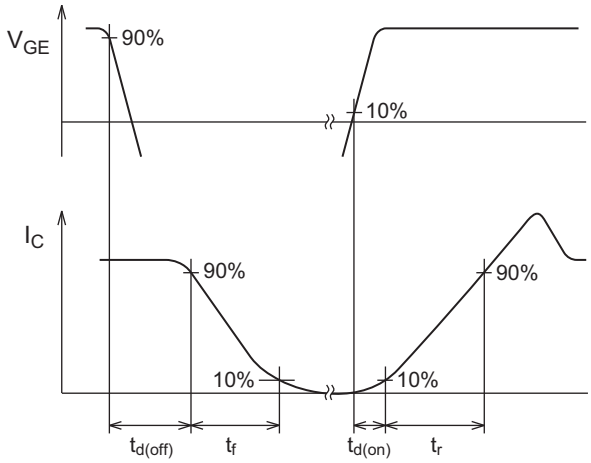
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero gate voltage collector current	I_{CES}	—	—	1	μA	V_{CE} = 1250 V, V_{GE} = 0
Gate to emitter leak current	I_{GES}	—	—	±1	μA	V_{GE} = ±30 V, V_{CE} = 0
Gate to emitter cutoff voltage	$V_{GE(off)}$	5.0	—	6.8	V	V_{CE} = 10 V, I_C = 6.7 mA
Collector to emitter saturation voltage	$V_{CE(sat)}$	—	1.80	2.25	V	I_C = 200 A, V_{GE} = 15 V Note2
Input capacitance	Cies	—	19.5	—	nF	V_{CE} = 25 V V_{GE} = 0 f = 1 MHz
Output capacitance	Coes	—	0.56	—	nF	
Reveres transfer capacitance	Cres	—	0.46	—	nF	
Total gate charge	Qg	—	1270	—	nC	V_{GE} = 15 V V_{CE} = 600 V I_C = 200 A
Gate to emitter charge	Qge	—	185	—	nC	
Gate to collector charge	Qgc	—	720	—	nC	
Switching time Note3	$t_{d(on)}$	—	140	—	ns	V_{CC} = 600 V I_C = 200 A V_{GE} = ±15 V Rg = 10 Ω, Tc = 150 °C Inductive load
	t_r	—	120	—	ns	
	$t_{d(off)}$	—	730	—	ns	
	t_f	—	140	—	ns	
Short circuit withstand time Note4	t_{sc}	10	—	—	μs	V_{CC} ≤ 720 V , V_{GE} = 15 V Tc = 150 °C

Notes: 2. Pulse test.
3. Switching time test circuit and waveform are shown below.
4. Verified by design.

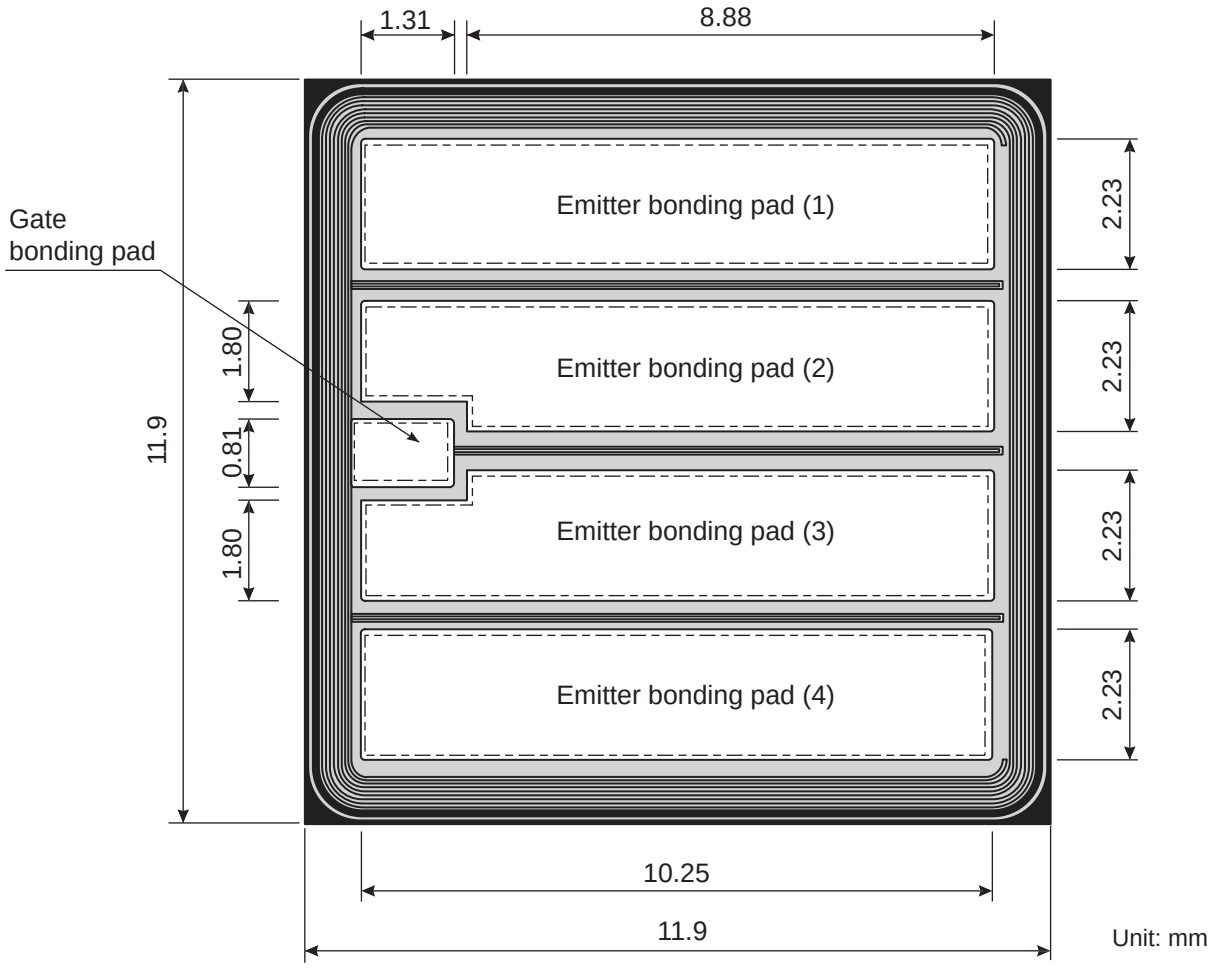
Switching Time Test Circuit



Waveform



Die Dimension



Note 1.

Illustration	Definition
Part of white	Al pattern
Part of dotted line	Bonding area
Part of gray	Final passivation

Note 2. The back of the chip is processed with Au evaporation.

Note 3. Recognition, target and any other patterns which are not related to IGBT operation, may be changed without notice.

Ordering Information

Orderable Part Number	Shipment form
RJP1CS08DWA-80#W0	Unsawn wafer
RJP1CS08DWS-80#W0	Sawn wafer

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HALII Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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