

## RL78/G24

R01DS0432EJ0110

RENESAS MCU

Rev.1.10

Nov 1, 2023

High-performance with 48-MHz CPU operation on true low-power platform, 50- $\mu$ A/MHz operating current, flexible application accelerator (FAA), enhanced timers and analog functions for motor control, digital power supply, and lighting applications, providing PMBus/SMBus, and DALI-2 communications, from 20 to 64 pins, 1.6- to 5.5-V operation

## 1. Outline

### 1.1 Features

Ultra-low power consumption technology

- VDD = single power supply voltage of 1.6 to 5.5 V
- HALT mode
- STOP mode
- High-speed wakeup from the STOP mode is possible.
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- The minimum instruction execution time can be changed from high to ultra-low speed.
  - High speed: 0.02083  $\mu$ s at 48 MHz operation with the high-speed on-chip oscillator clock or the PLL clock
  - Ultra-low speed: 30.5  $\mu$ s at 32.768 kHz operation with the subsystem clock
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 Mbyte
- General-purpose registers: (8-bit register  $\times$  8)  $\times$  4 banks
- On-chip RAM: 12 Kbytes

FAA core

- Multiplication: 32-bit signed  $\times$  32-bit signed  $\rightarrow$  32-bit signed
- Results of 64-bit multiplication can be right-shifted by a desired number of bits.
- Addition: 32-bit signed + 32-bit signed  $\rightarrow$  32-bit signed (internally calculated with 33-bit precision)
- Subtraction: 32-bit signed - 32-bit signed  $\rightarrow$  32-bit signed (internally calculated with 33-bit precision)
- Limit operation: Operation parameter registers (33 bits  $\times$  4) in which upper and lower limits can be set.
- Operation parameter registers (32 bits  $\times$  6)
- Address pointer registers (12 bits  $\times$  6)
- On-chip code RAM: 4 Kbytes
- On-chip data RAM: 2 Kbytes
- Multiple interrupts available

- A 32-byte shared memory is included for sharing of data by the RL78 CPU and FAA core.

Divider

- 32-bit  $\div$  32-bit = 32-bit unsigned

Code flash memory

- 64 or 128 Kbytes
- Block size: 2 Kbytes
- Security function: Prohibition of block erase and rewriting
- On-chip debugging
- Self-programming with boot swapping and flash shield window

Data flash memory

- 4 Kbytes
- Background operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (typ.)

High-speed on-chip oscillator

- Selectable from among 64 MHz, 48 MHz, 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy:
  - $\pm 1.0\%$  (VDD = 1.8 to 5.5 V, TA =  $-20$  to  $+85^\circ\text{C}$ )

Middle-speed on-chip oscillator

- Selectable from among 4 MHz, 2 MHz, and 1 MHz with adjustability

Low-speed on-chip oscillator

- 32.768 kHz (typ.) with adjustability

Operating ambient temperature

- TA =  $-40$  to  $+85^\circ\text{C}$  (2D: Consumer applications)
- TA =  $-40$  to  $+105^\circ\text{C}$  (3C: Industrial applications)
- TA =  $-40$  to  $+125^\circ\text{C}$  (4C: Industrial applications)

## Power management and resetting

- On-chip power-on-reset (POR) circuit
- On-chip voltage detectors (LVD0 and LVD1)

## Data transfer controller (DTC)

- Transfer modes: Normal transfer mode, repeat transfer mode, and block transfer mode
- Activated by interrupt sources
- Chain transfer

## Event link controller (ELC)

- 34 event signals can be set up between specified peripheral functions.

## Serial interfaces

- Two to six simplified SPIs (CSIs<sup>Note 1</sup>)
- Two to three UART/UART (LIN-bus supported) interfaces
- Two to six I<sup>2</sup>C/Simplified I<sup>2</sup>C interfaces
- Single digital addressable lighting interface (DALI)
- Single I<sup>2</sup>C (SM/PM bus) interface

## Timers

- 16-bit timers:
  - 4-channel timer array unit (TAU)
  - Single-channel timer RJ
  - 2-channel timer RD2 with PWMOPA
  - Single-channel timer RG2
  - Single-channel timer RX
- 32-bit interval timer:
  - Single channel in 32-bit counter mode
  - Two channels in 16-bit counter mode
  - Four channels in 8-bit counter mode
- Single-channel realtime clock: Counting of one second to 99 years, alarm interrupt, and clock correction
- Single-channel watchdog timer: Operates with the low-speed on-chip oscillator clock

- Three 16-bit timers KB30, KB31, and KB32:

Two outputs each (up to six outputs), complementary output timers for power control, timer restart, smooth start, PWM output gating, dithering, fast and asynchronous forced output stop triggered by a comparator or external interrupt, single or interleaved power factor correction (PFC) control, maximum frequency limit, fixed off control, pulse characteristics measurement, multi-phase operation, output with 651-ps average resolution (operation at 96 MHz and with the dithering being applied)

## A/D converter

- 8-/10-/12-bit resolution
- 12 to 23 analog input channels: Two channels include a sample and hold circuit each.
- Internal reference voltage (1.48 V) and temperature sensor

## D/A converter

- 8-/10-bit resolution (V<sub>DD</sub> = 2.7 to 5.5 V)
- Two to three analog output channels
- Output voltage: 0 V to V<sub>DD</sub>
- Realtime output

## Comparator module

- Four channels
- The external reference voltage and the D/A converter output are selectable as the reference voltage.
- Time window output functioning with the timer array unit

## Programmable gain amplifier

- Single amplifier

**Input/output port pins**

- Number of port pins: 26 to 120
- N-ch open drain I/O pins (withstand voltage of 6 V): 2 to 4
- N-ch open drain I/O pins (withstand voltage of  $V_{DD}$ <sup>Note 2</sup>/withstand voltage of  $E_{VDD}$ <sup>Note 3</sup>): 7 to 19
- Controlled current drive port pins: 2 to 8
- Can be set to N-ch open drain or TTL input buffer, and use of an on-chip pull-up resistor can be specified.
- Connectable to a device with different voltage (1.8, 2.5, or 3 V)

**Others**

- Key interrupt
- Clock output/buzzer output controller
- Binary-coded decimal (BCD) correction circuit

**Note 1.** Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

**Note 2.** This applies to the 20- to 52-pin products.

**Note 3.** This applies to the 64-pin products.

**Remark** The functions mounted depend on the product. See **1.6 Outline of Functions**.

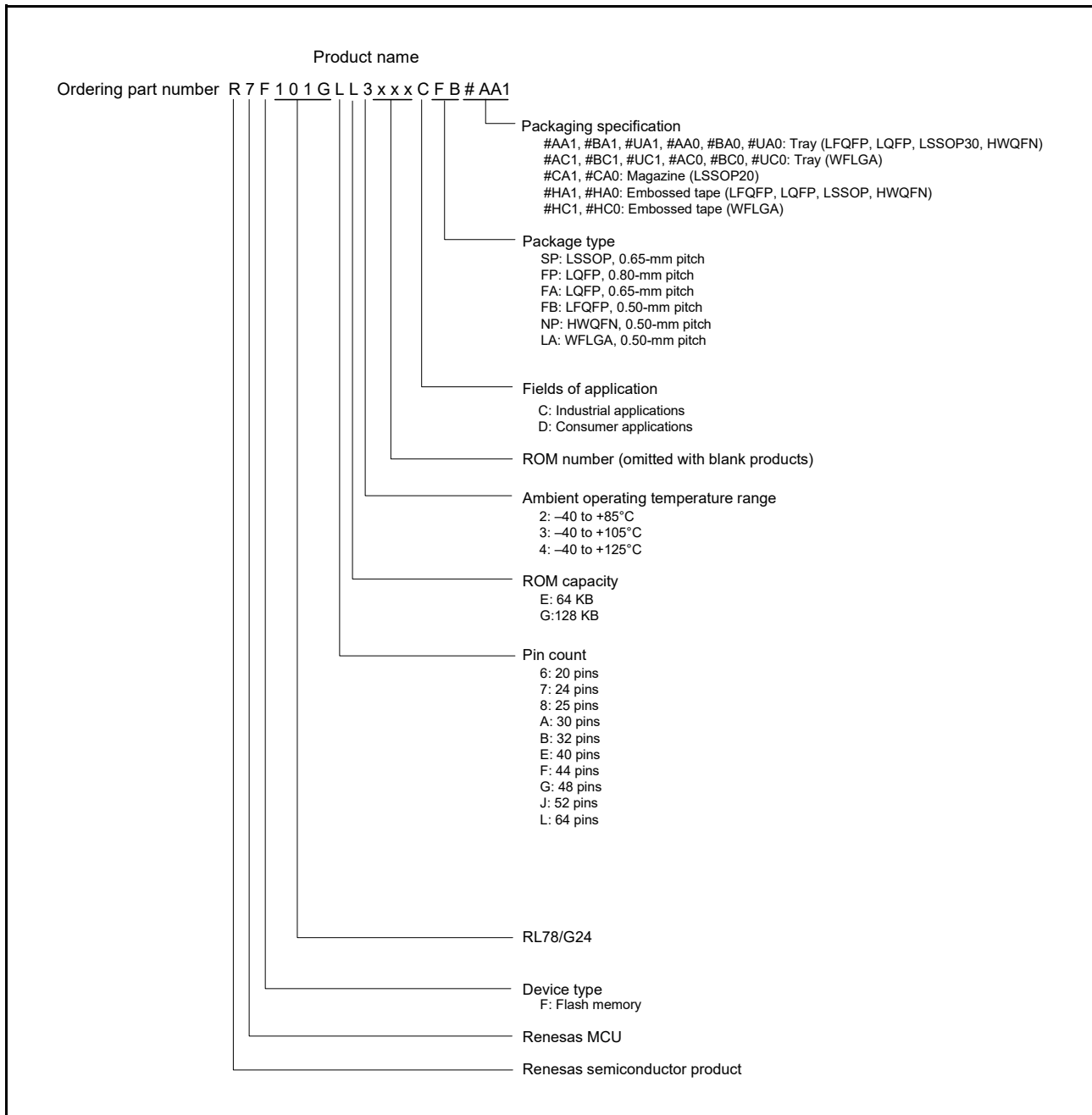
• ROM and RAM capacities

Flash ROM	Data flash memory	RAM	RL78/G24				
			20 pins	24 pins	25 pins	30 pins	32 pins
128 KB	4 KB	12 KB	R7F101G6G	R7F101G7G	R7F101G8G	R7F101GAG	R7F101GBG
64 KB			R7F101G6E	R7F101G7E	R7F101G8E	R7F101GAE	R7F101GBE

Flash ROM	Data flash memory	RAM	RL78/G24				
			40 pins	44 pins	48 pins	52 pins	64 pins
128 KB	4 KB	12 KB	R7F101GEG	R7F101GFG	R7F101GGG	R7F101GJG	R7F101GLG
64 KB			R7F101GEE	R7F101GFE	R7F101GGE	R7F101GJE	R7F101GLE

## 1.2 List of Part Numbers

<R> Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G24



&lt;R&gt; Table 1 - 1 List of Ordering Part Numbers

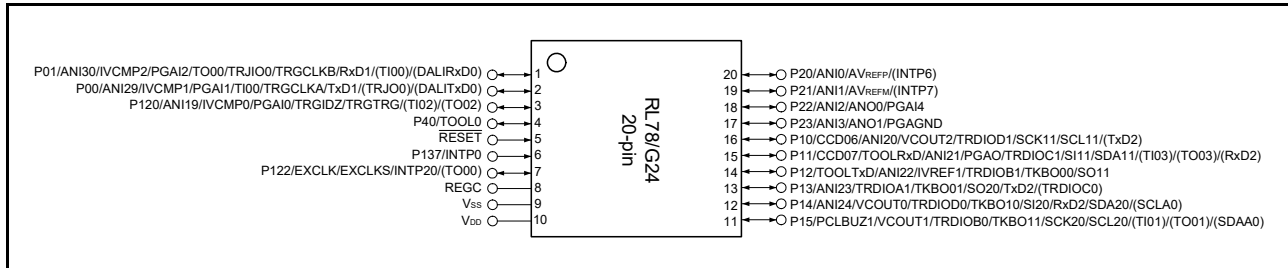
Pin Count	Package	Fields of Application Note	Ordering Part Number		Renesas Code
			Product Name	Packaging Specification	
20	20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)	C	R7F101G6G4CSP, R7F101G6E4CSP, R7F101G6G3CSP, R7F101G6E3CSP	#CA1, #CA0, #HA1, #HA0	PLSP0020JB-A
		D	R7F101G6G2DSP, R7F101G6E2DSP		
24	24-pin plastic HWQFN (4 × 4 mm, 0.50-mm pitch)	C	R7F101G7G4CNP, R7F101G7E4CNP, R7F101G7G3CNP, R7F101G7E3CNP	#AA1, #AA0, #BA1, #BA0, #UA1, #UA0, #HA1, #HA0	PWQN0024KG-A
		D	R7F101G7G2DNP, R7F101G7E2DNP		
25	25-pin plastic WFLGA (3 × 3 mm, 0.50-mm pitch)	C	R7F101G8G3CLA, R7F101G8E3CLA	#AC1, #AC0, #BC1, #BC0, #UC1, #UC0, #HC1, #HC0	PWL0025KB-A
		D	R7F101G8G2DLA, R7F101G8E2DLA		
30	30-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch)	C	R7F101GAG4CSP, R7F101GAE4CSP, R7F101GAG3CSP, R7F101GAE3CSP	#AA1, #AA0, #BA1, #BA0, #UA1, #UA0, #HA1, #HA0	PLSP0030JB-B
		D	R7F101GAG2DSP, R7F101GAE2DSP		
32	32-pin plastic HWQFN (5 × 5 mm, 0.50-mm pitch)	C	R7F101GBG4CNP, R7F101GBE4CNP, R7F101GBG3CNP, R7F101GBE3CNP	#AA1, #AA0, #BA1, #BA0, #UA1, #UA0, #HA1, #HA0	PWQN0032KE-A
		D	R7F101GBG2DNP, R7F101GBE2DNP		
	32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch)	C	R7F101GBG3CFP, R7F101GBE3CFP	#AA1, #AA0, #BA1, #BA0, #UA1, #UA0, #HA1, #HA0	PLQP0032GB-A
		D	R7F101GBG2DFP, R7F101GBE2DFP		
40	40-pin plastic HWQFN (6 × 6 mm, 0.50-mm pitch)	C	R7F101GEG4CNP, R7F101GEE4CNP, R7F101GEG3CNP, R7F101GEE3CNP	#AA1, #AA0, #BA1, #BA0, #UA1, #UA0, #HA1, #HA0	PWQN0040KD-A
		D	R7F101GEG2DNP, R7F101GEE2DNP		
44	44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)	C	R7F101GFG3CFP, R7F101GFE3CFP	#AA1, #AA0, #BA1, #BA0, #UA1, #UA0, #HA1, #HA0	PLQP0044GC-A
		D	R7F101GFG2DFP, R7F101GFE2DFP		
48	48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)	C	R7F101GGG4CFB, R7F101GGE4CFB, R7F101GGG3CFB, R7F101GGE3CFB	#AA1, #AA0, #BA1, #BA0, #UA1, #UA0, #HA1, #HA0	PLQP0048KB-B
		D	R7F101GGG2DFB, R7F101GGE2DFB		
	48-pin plastic HWQFN (7 × 7 mm, 0.50-mm pitch)	C	R7F101GGG3CNP, R7F101GGE3CNP	#AA1, #AA0, #BA1, #BA0, #UA1, #UA0, #HA1, #HA0	PWQN0048KC-A
		D	R7F101GGG2DNP, R7F101GGE2DNP		
52	52-pin plastic LQFP (10 × 10 mm, 0.65-mm pitch)	C	R7F101GJG4CFA, R7F101GJE4CFA, R7F101GJG3CFA, R7F101GJE3CFA	#AA1, #AA0, #BA1, #BA0, #UA1, #UA0, #HA1, #HA0	PLQP0052JA-A
		D	R7F101GJG2DFA, R7F101GJE2DFA		
64	64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch)	C	R7F101GLG3CFA, R7F101GLE3CFA	#AA1, #AA0, #BA1, #BA0, #UA1, #UA0, #HA1, #HA0	PLQP0064JA-A
		D	R7F101GLG2DFA, R7F101GLE2DFA		
	64-pin plastic LFQFP (10 × 10 mm, 0.50-mm pitch)	C	R7F101GLG3CFB, R7F101GLE3CFB	#AA1, #AA0, #BA1, #BA0, #UA1, #UA0, #HA1, #HA0	PLQP0064KB-C
		D	R7F101GLG2DFB, R7F101GLE2DFB		

**Note** For the fields of application, see **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G24**.

## 1.3 Pin Configuration (Top View)

### 1.3.1 20-pin products

- 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1  $\mu$ F).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register x (PIORx). Refer to **Figure 7 - 8 Format of Peripheral I/O Redirection Register 0 (PIOR0)** to **Figure 7 - 11 Format of Peripheral I/O Redirection Register 3 (PIOR3)** in the RL78/G24 User's Manual.

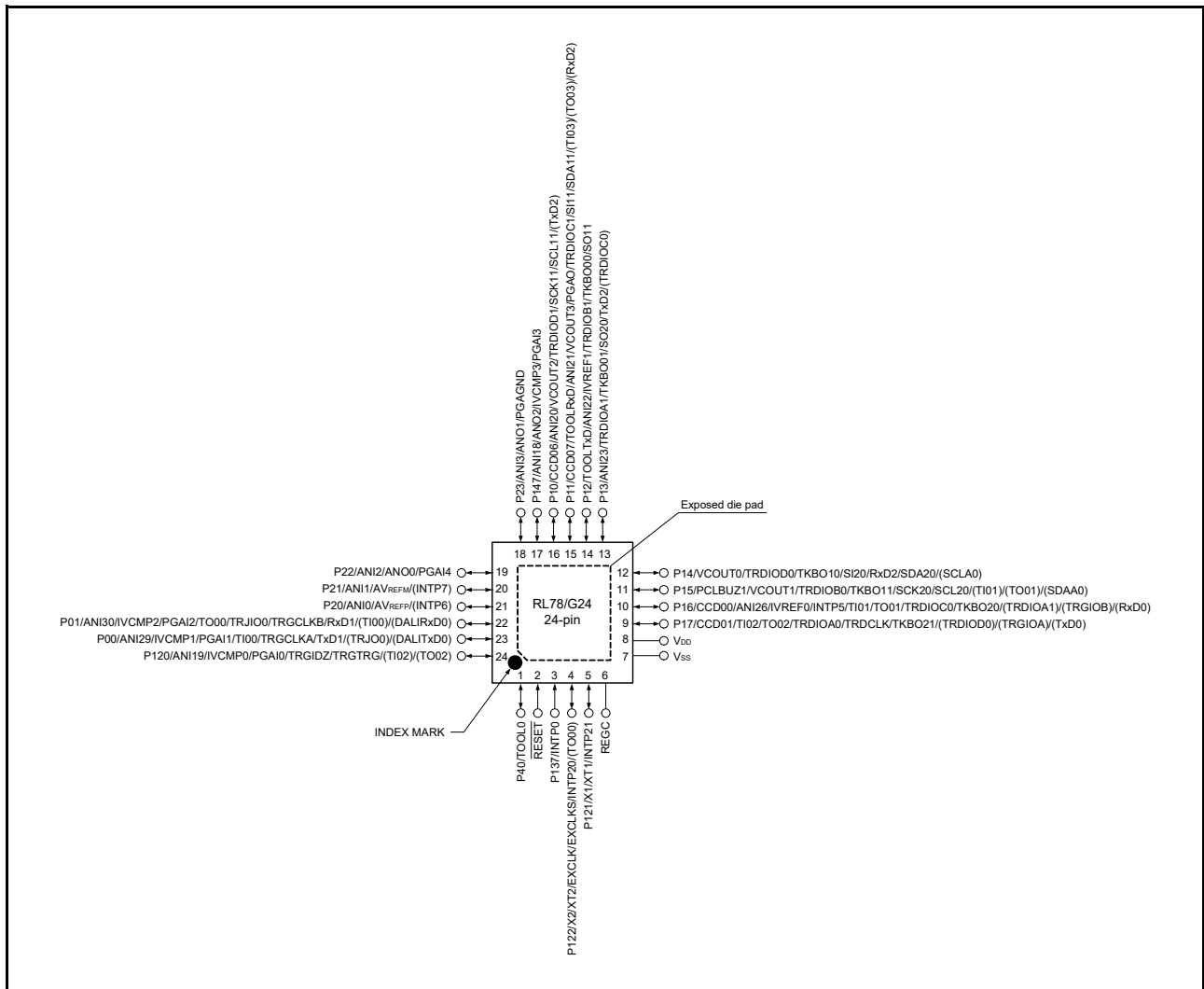
Table 1 - 2 Multiplexed Pin Functions of the 20-pin Products

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces			
	20LSSOP	Digital port Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Digital addressable lighting interface (DALI)
1	P01	—	—	ANI30	—	IVCMP2	PGA2	—	—	TO00/ (TI00)	TRJIO0	—	TRGCLKB	—	—	RxD1	—	(DALIRxD0)
2	P00	—	—	ANI29	—	IVCMP1	PGA1	—	—	TI00	(TRJO0)	—	TRGCLKA	—	—	TxD1	—	(DALITxD0)
3	P120	—	—	ANI19	—	IVCMP0	PGA0	—	—	(TI02)/ (TO02)	—	—	TRGIDZ/ TRGTRG	—	—	—	—	—
4	P40	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	P137	—	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—	—
7	P122	—	EXCLK/ EXCLKS	—	—	—	—	INTP20	—	(TO00)	—	—	—	—	—	—	—	—
8	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
9	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10	—	—	Vdd	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
11	P15	—	PCLBUZ1	—	—	VCOUT1	—	—	—	(TI01)/ (TO01)	TRDIOB0	—	TKBO11	—	—	SCK20/ SCL20	(SDAA0)	—
12	P14	—	—	ANI24	—	VCOUT0	—	—	—	—	TRDIOD0	—	TKBO10	—	—	SI20/ RxD2/ SDA20	(SCLA0)	—
13	P13	—	—	ANI23	—	—	—	—	—	—	TRDIOA1/ (TRDIOC0)	—	TKBO01	—	—	SO20/ TxD2	—	—
14	P12	—	TOOLTxD	ANI22	—	IVREF1	—	—	—	—	TRDIOB1	—	TKBO00	—	—	SO11	—	—
15	P11	CCD07	TOOLRxD	ANI21	—	—	PGAO	—	—	(TI03)/ (TO03)	TRDIOC1	—	—	—	—	SI11/ SDA11/ (RxD2)	—	—
16	P10	CCD06	—	ANI20	—	VCOUT2	—	—	—	—	TRDIOD1	—	—	—	—	SCK11/ SCL11/ (TxD2)	—	—
17	P23	—	—	ANI3	ANO1	—	PGAGND	—	—	—	—	—	—	—	—	—	—	—
18	P22	—	—	ANI2	ANO0	—	PGA4	—	—	—	—	—	—	—	—	—	—	—
19	P21	—	—	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	—	—	—	—	—	—	—	—
20	P20	—	—	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	—	—	—	—	—	—	—	—



### 1.3.2 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.50-mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register x (PIORx). Refer to Figure 7 - 8 Format of Peripheral I/O Redirection Register 0 (PIOR0) to Figure 7 - 11 Format of Peripheral I/O Redirection Register 3 (PIOR3) in the RL78/G24 User's Manual.

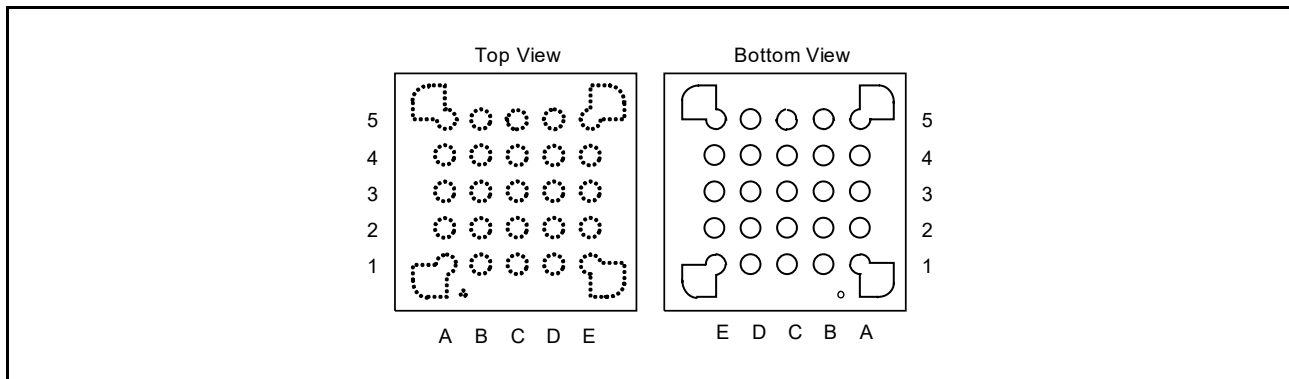
**Remark 3.** For the product in a QFN package, we recommend soldering the exposed die pad onto a plated area of the printed circuit board that has no electrical connections.

Table 1 - 3 Multiplexed Pin Functions of the 24-pin Products

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces		
	24HWQFN	Digital port Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
1	P40	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
2	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—
3	P137	—	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—
4	P122	—	X2/XT2/ EXCLK/ EXCLKS	—	—	—	—	INTP20	(TO00)	—	—	—	—	—	—	—	—
5	P121	—	X1/XT1	—	—	—	—	INTP21	—	—	—	—	—	—	—	—	—
6	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8	—	—	Vdd	—	—	—	—	—	—	—	—	—	—	—	—	—	—
9	P17	CCD01	—	—	—	—	—	—	TI02/ TO02	TRDIOA0/ (TRDIOA0)/ TRDCLK	(TRGIOA)	TKBO21	—	(TxD0)	—	—	—
10	P16	CCD00	—	ANI26	—	IVREF0	—	INTP5	TI01/ TO01	TRDIOC0/ (TRDIOA1)	(TRGIOB)	TKBO20	—	(RxD0)	—	—	—
11	P15	—	PCLBUZ1	—	—	VCOUT1	—	—	(TI01)/ (TO01)	TRDIOB0	—	TKBO11	—	SCK20/ SCL20	(SDAA0)	—	—
12	P14	—	—	—	—	VCOUT0	—	—	—	TRDIOD0	—	TKBO10	—	SI20/ RxD2/ SDA20	(SCLA0)	—	—
13	P13	—	—	ANI23	—	—	—	—	—	TRDIOA1/ (TRDIOC0)	—	TKBO01	—	SO20/ TxD2	—	—	—
14	P12	—	TOOLTxD	ANI22	—	IVREF1	—	—	—	TRDIOB1	—	TKBO00	—	SO11	—	—	—
15	P11	CCD07	TOOLRxD	ANI21	—	VCOUT3	PGAO	—	(TI03)/ (TO03)	TRDIOC1	—	—	—	SI11/ SDA11/ (RxD2)	—	—	—
16	P10	CCD06	—	ANI20	—	VCOUT2	—	—	—	TRDIOD1	—	—	—	SCK11/ SCL11/ (TxD2)	—	—	—
17	P147	—	—	ANI18	ANO2	IVCMP3	PGAI3	—	—	—	—	—	—	—	—	—	—
18	P23	—	—	ANI3	ANO1	—	PGAGND	—	—	—	—	—	—	—	—	—	—
19	P22	—	—	ANI2	ANO0	—	PGAI4	—	—	—	—	—	—	—	—	—	—
20	P21	—	—	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	—	—	—	—	—	—	—
21	P20	—	—	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	—	—	—	—	—	—	—
22	P01	—	—	ANI30	—	IVCMP2	PGAI2	—	TO00/ (TI00)	TRJIO0	—	TRGCLKB	—	RxD1	—	(DALIRxD0)	—
23	P00	—	—	ANI29	—	IVCMP1	PGAI1	—	TI00	(TRJO0)	—	TRGCLKA	—	TxD1	—	(DALITxD0)	—
24	P120	—	—	ANI19	—	IVCMP0	PGAI0	—	(TI02)/ (TO02)	—	—	TRGIDZ/ TRGTRG	—	—	—	—	—

### 1.3.3 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.50-mm pitch)



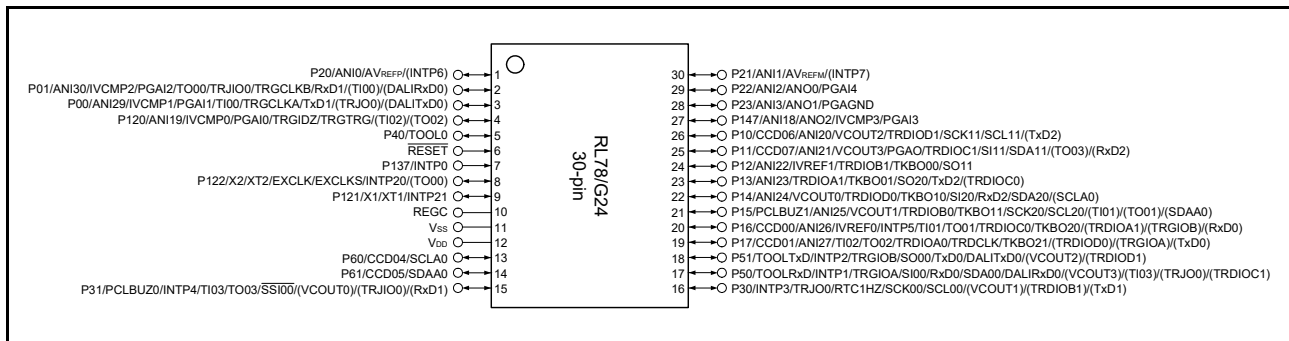
	A	B	C	D	E
5	P40/TOOL0	RESET	P01/ANI30/IVCMP2/PGAI2/ TO00/TRJIO0/TRGCLKB/ RxD1/(TI00)/(DALIRxD0)	P22/ANI2/ANO0/PGAI4	P147/ANI18/ANO2/ IVCMP3/PGAI3
4	P122/X2/XT2/EXCLK/ EXCLKS/INTP20/(TO00)	P137/INTP0	P00/ANI29/IVCMP1/PGAI1/ TI00/TRGCLKA/TxD1/ (TRJO0)/(DALITxD0)	P21/ANI1/AVREFM/(INTP7)	P10/CCD06/ANI20/ VCOUT2/TRDIOD1/SCK11/ SCL11/(TxD2)
3	P121/X1/XT1/INTP21	VDD	P20/ANI0/AVREFP/(INTP6)	P12/TOOLTxD/ANI22/ IVREF1/TRDIOB1/ TKBO00/SO11	P11/CCD07/TOOLRxD/ ANI21/VCOUT3/PGAO/ TRDIOC1/SI11/SDA11/ (TI03)/(TO03)/(RxD2)
2	REGC	VSS	P23/ANI3/ANO1/PGAGND	P14/ANI24/VCOUT0/ TRDIOD0/TKBO10/SI20/ RxD2/SDA20/(SCLA0)	P13/ANI23/TRDIOA1/ TKBO01/SO20/TxD2/ (TRDIOC0)
1	P17/CCD01/ANI27/TI02/ TO02/TRDIOA0/TRDCLK/ TKBO21/(TRDIOD0)/ (TRGIOA)/(TxD0)	P16/CCD00/ANI26/ IVREF0/INTP5/TI01/TO01/ TRDIOC0/TKBO20/ (TRDIOA1)/(TRGIOB)/ (RxD0)	P120/ANI19/IVCMP0/ PGAI0/TRGIDZ/TRGTRG/ (TI02)/(TO02)	P15/PCLBUZ1/ANI25/ VCOUT1/TRDIOB0/ TKBO11/SCK20/SCL20/ (TI01)/(TO01)/(SDAA0)	P130

Table 1 - 4 Multiplexed Pin Functions of the 25-pin Products

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces			
	25WFLGA	Digital port Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Digital addressable lighting interface (DALI)
A1	P17	CCD01	—	ANI27	—	—	—	—	—	TI02/ TO02	—	TRDIOA0/ (TRDIOD0)/ TRDCLK	(TRGIOA)	TKBO21	—	(TxD0)	—	—
A2	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
A3	P121	—	X1/XT1	—	—	—	—	INTP21	—	—	—	—	—	—	—	—	—	
A4	P122	—	X2/XT2/ EXCLK/ EXCLKS	—	—	—	—	INTP20	(TO00)	—	—	—	—	—	—	—	—	
A5	P40	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
B1	P16	CCD00	—	ANI26	—	IVREF0	—	INTP5	—	TI01/ TO01	—	TRDIOC0/ (TRDIOA1)	(TRGIOB)	TKBO20	—	(RxD0)	—	
B2	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
B3	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
B4	P137	—	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—	
B5	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
C1	P120	—	—	ANI19	—	IVCMP0	PGAI0	—	—	(TI02)/ (TO02)	—	—	TRGIDZ/ TRGTRG	—	—	—	—	
C2	P23	—	—	ANI3	ANO1	—	PGAGND	—	—	—	—	—	—	—	—	—	—	
C3	P20	—	—	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	—	—	—	—	—	—	—	
C4	P00	—	—	ANI29	—	IVCMP1	PGAI1	—	—	TI00	(TRJO0)	—	TRGCLKA	—	—	TxD1	(DALITxD0)	
C5	P01	—	—	ANI30	—	IVCMP2	PGAI2	—	—	TO00/ (TI00)	TRJIO0	—	TRGCLKB	—	—	RxD1	(DALIRxD0)	
D1	P15	—	PCLBUZ1	ANI25	—	VCOUT1	—	—	—	(TI01)/ (TO01)	—	TRDIOB0	—	TKBO11	—	SCK20/ SCL20	(SDAA0)	
D2	P14	—	—	ANI24	—	VCOUT0	—	—	—	—	—	TRDIOD0	—	TKBO10	—	SI20/ RxD2/ SDA20	(SCLA0)	
D3	P12	—	TOOLTxD	ANI22	—	IVREF1	—	—	—	—	—	TRDIOB1	—	TKBO00	—	SO11	—	
D4	P21	—	—	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	—	—	—	—	—	—	—	
D5	P22	—	—	ANI2	ANO0	—	PGAI4	—	—	—	—	—	—	—	—	—	—	
E1	P130	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
E2	P13	—	—	ANI23	—	—	—	—	—	—	—	TRDIOA1/ (TRDIOC0)	—	TKBO01	—	SO20/ TxD2	—	
E3	P11	CCD07	TOOLRxD	ANI21	—	VCOUT3	PGAO	—	—	(TI03)/ (TO03)	—	TRDIOC1	—	—	—	SI11/ SDA11/ (RxD2)	—	
E4	P10	CCD06	—	ANI20	—	VCOUT2	—	—	—	—	—	TRDIOD1	—	—	—	SCK11/ SCL11/ (TxD2)	—	
E5	P147	—	—	ANI18	ANO2	IVCMP3	PGAI3	—	—	—	—	—	—	—	—	—	—	

### 1.3.4 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch)



**Caution** Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register x (PIORx). Refer to **Figure 7 - 8 Format of Peripheral I/O Redirection Register 0 (PIOR0)** to **Figure 7 - 11 Format of Peripheral I/O Redirection Register 3 (PIOR3)** in the RL78/G24 User's Manual.

Table 1 - 5 Multiplexed Pin Functions of the 30-pin Products (1/2)

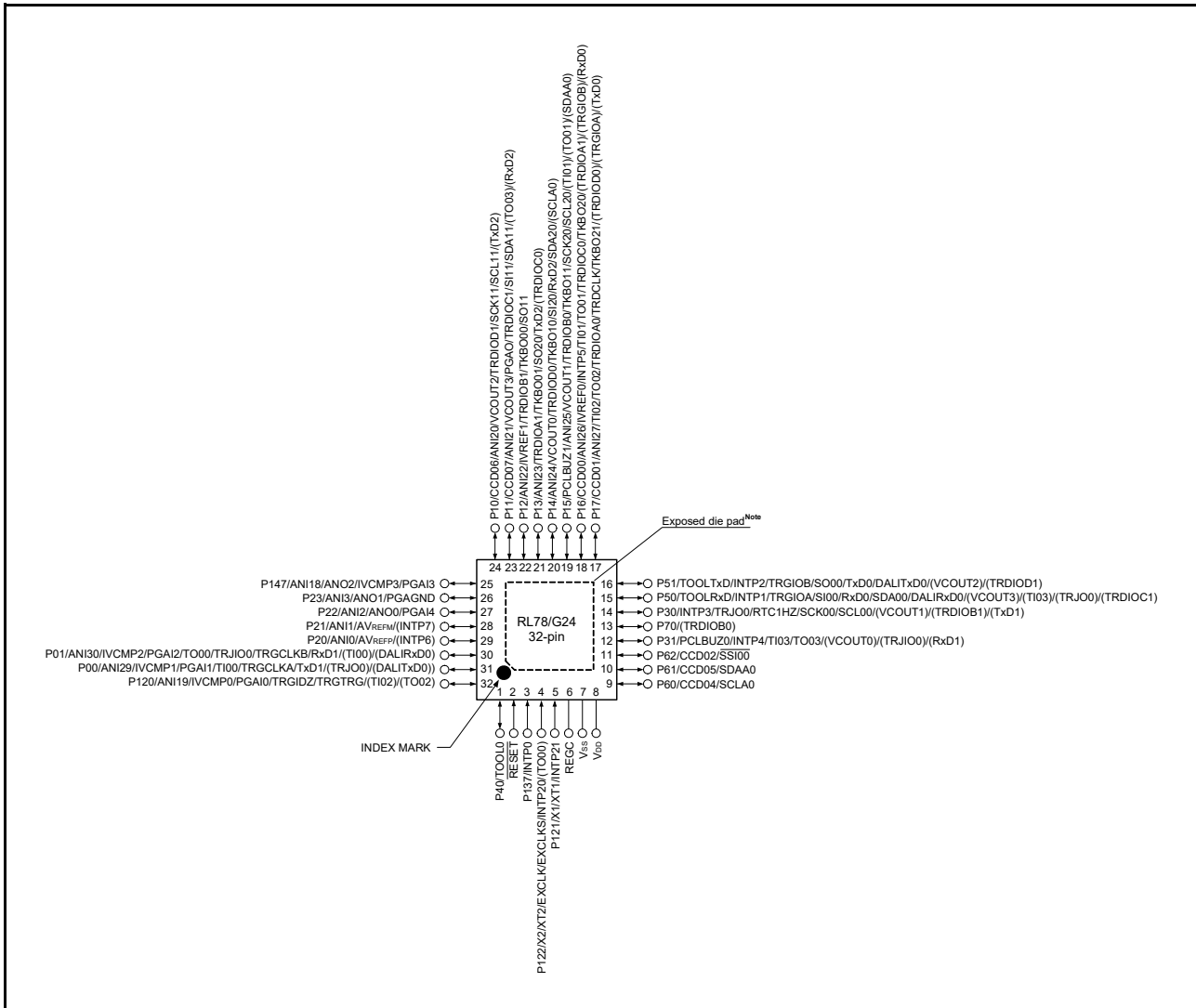
Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces		
	30LSSOP	Digital port Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
1	P20	—	—	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	—	—	—	—	—	—	—
2	P01	—	—	ANI30	—	IVCMP2	PGAI2	—	—	TO00/ (TI00)	TRJIO0	—	TRGCLKB	—	—	RxD1	(DALIRxD0)
3	P00	—	—	ANI29	—	IVCMP1	PGAI1	—	—	TI00	(TRJIO0)	—	TRGCLKA	—	—	TxD1	(DALITxD0)
4	P120	—	—	ANI19	—	IVCMP0	PGAI0	—	—	(TI02)/ (TO02)	—	—	TRGIDZ/ TRGTRG	—	—	—	—
5	P40	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	P137	—	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—
8	P122	—	X2/XT2/ EXCLK/ EXCLKS	—	—	—	—	INTP20	(TO00)	—	—	—	—	—	—	—	—
9	P121	—	X1/XT1	—	—	—	—	INTP21	—	—	—	—	—	—	—	—	—
10	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
11	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	—	—	Vdd	—	—	—	—	—	—	—	—	—	—	—	—	—	—
13	P60	CCD04	—	—	—	—	—	—	—	—	—	—	—	—	—	SCLA0	—
14	P61	CCD05	—	—	—	—	—	—	—	—	—	—	—	—	—	SDAA0	—
15	P31	—	PCLBUZ0	—	—	(VCOUT0)	—	INTP4	TI03/ TO03	(TRJIO0)	—	—	—	—	SSI00/ (RxD1)	—	—
16	P30	—	—	—	—	(VCOUT1)	—	INTP3	—	TRJ00	(TRDIOB1)	—	—	RTC1HZ	SCK00/ SCL00/ (TxD1)	—	—
17	P50	—	TOOLRxD	—	—	(VCOUT3)	—	INTP1	(TI03)	(TRJ00)	(TRDIOC1)	TRGIOA	—	—	SI00/ RxD0/ SDA00	—	DALIRxD0
18	P51	—	TOOLTxD	—	—	(VCOUT2)	—	INTP2	—	—	(TRDIOD1)	TRGIOB	—	—	SO00/ TxD0	—	DALITxD0
19	P17	CCD01	—	ANI27	—	—	—	—	TI02/ TO02	—	TRDIOA0/ (TRDIOD0)/ TRDCLK	(TRGIOA)	TKBO21	—	(TxD0)	—	—
20	P16	CCD00	—	ANI26	—	IVREF0	—	INTP5	TI01/ TO01	—	TRDIOC0/ (TRDIOA1)	(TRGIOB)	TKBO20	—	(RxD0)	—	—
21	P15	—	PCLBUZ1	ANI25	—	VCOUT1	—	—	(TI01)/ (TO01)	—	TRDIOB0	—	TKBO11	—	SCK20/ SCL20	(SDAA0)	—
22	P14	—	—	ANI24	—	VCOUT0	—	—	—	—	TRDIOD0	—	TKBO10	—	SI20/ RxD2/ SDA20	(SCLA0)	—
23	P13	—	—	ANI23	—	—	—	—	—	—	TRDIOA1/ (TRDIOC0)	—	TKBO01	—	SO20/ TxD2	—	—
24	P12	—	—	ANI22	—	IVREF1	—	—	—	—	TRDIOB1	—	TKBO00	—	SO11	—	—
25	P11	CCD07	—	ANI21	—	VCOUT3	PGAO	—	(TO03)	—	TRDIOC1	—	—	—	SI11/ SDA11/ (RxD2)	—	—
26	P10	CCD06	—	ANI20	—	VCOUT2	—	—	—	—	TRDIOD1	—	—	—	SCK11/ SCL11/ (TxD2)	—	—

Table 1 - 5 Multiplexed Pin Functions of the 30-pin Products (2/2)

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces		
	Digital port	Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
27	P147	—	—	ANI18	ANO2	IVCMP3	PGAI3	—	—	—	—	—	—	—	—	—	—
28	P23	—	—	ANI3	ANO1	—	PGAGND	—	—	—	—	—	—	—	—	—	—
29	P22	—	—	ANI2	ANO0	—	PGAI4	—	—	—	—	—	—	—	—	—	—
30	P21	—	—	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	—	—	—	—	—	—	—

### 1.3.5 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.50-mm pitch)
- 32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch)



**Note** The 32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch) products do not have an exposed die pad.

**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register x (PIORx). Refer to **Figure 7 - 8 Format of Peripheral I/O Redirection Register 0 (PIOR0)** to **Figure 7 - 11 Format of Peripheral I/O Redirection Register 3 (PIOR3)** in the RL78/G24 User's Manual.

**Remark 3.** For the product in a QFN package, we recommend soldering the exposed die pad onto a plated area of the printed circuit board that has no electrical connections.



Table 1 - 6 Multiplexed Pin Functions of the 32-pin Products (1/2)

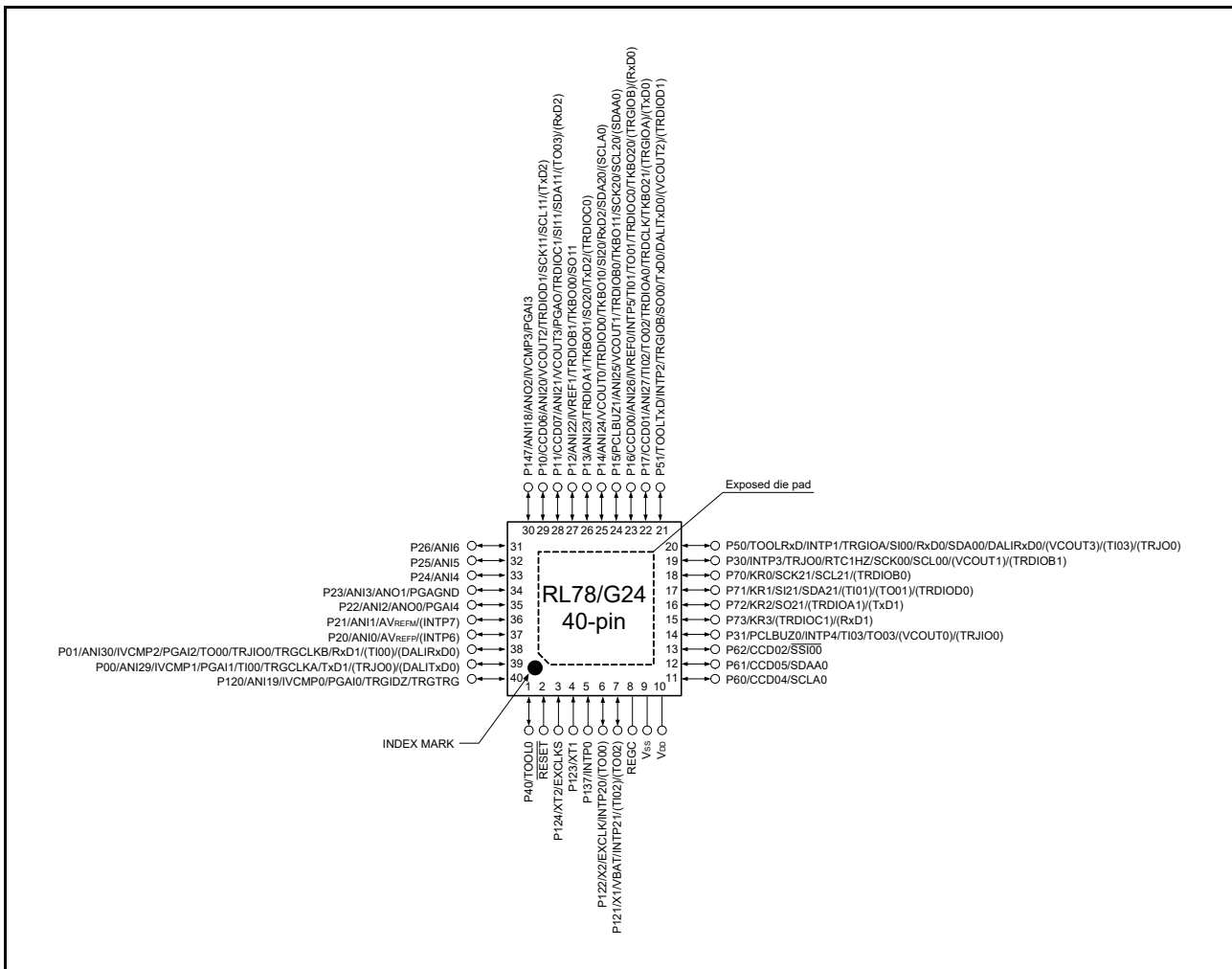
Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces		
	32HWQFN, 32LOFP	Digital port Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
1	P40	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
2	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—
3	P137	—	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—
4	P122	—	X2/XT2/ EXCLK/ EXCLKS	—	—	—	—	INTP20	(TO00)	—	—	—	—	—	—	—	—
5	P121	—	X1/XT1	—	—	—	—	INTP21	—	—	—	—	—	—	—	—	—
6	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8	—	—	Vdd	—	—	—	—	—	—	—	—	—	—	—	—	—	—
9	P60	CCD04	—	—	—	—	—	—	—	—	—	—	—	—	—	SCLA0	—
10	P61	CCD05	—	—	—	—	—	—	—	—	—	—	—	—	—	SDAA0	—
11	P62	CCD02	—	—	—	—	—	—	—	—	—	—	—	—	SSIO0	—	—
12	P31	—	PCLBUZ0	—	—	(VCOUT0)	—	INTP4	TI03/ TO03	(TRJIO0)	—	—	—	—	(RxD1)	—	—
13	P70	—	—	—	—	—	—	—	—	(TRDIOB0)	—	—	—	—	—	—	—
14	P30	—	—	—	—	(VCOUT1)	—	INTP3	—	TRJO0	(TRDIOB1)	—	—	RTC1HZ	SCK00/ SCL00/ (TxD1)	—	—
15	P50	—	TOOLRxD	—	—	(VCOUT3)	—	INTP1	(TI03)	(TRJO0)	(TRDIOC1)	TRGIOA	—	—	SI00/ RxD0/ SDA00	—	DALIRxD0
16	P51	—	TOOLTxD	—	—	(VCOUT2)	—	INTP2	—	—	(TRDIOD1)	TRGIOB	—	—	SO00/ TxD0	—	DALITxD0
17	P17	CCD01	—	ANI27	—	—	—	—	TI02/ TO02	—	TRDIOA0/ (TRDIOD0)/ TRDCLK	(TRGIOA)	TKBO21	—	(TxD0)	—	—
18	P16	CCD00	—	ANI26	—	IVREF0	—	INTP5	TI01/ TO01	—	TRDIOC0/ (TRDIOA1)	(TRGIOB)	TKBO20	—	(RxD0)	—	—
19	P15	—	PCLBUZ1	ANI25	—	VCOUT1	—	—	(TI01)/ (TO01)	—	TRDIOB0	—	TKBO11	—	SCK20/ SCL20	(SDAA0)	—
20	P14	—	—	ANI24	—	VCOUT0	—	—	—	—	TRDIOD0	—	TKBO10	—	SI20/ RxD2/ SDA20	(SCLA0)	—
21	P13	—	—	ANI23	—	—	—	—	—	—	TRDIOA1/ (TRDIOC0)	—	TKBO01	—	SO20/ TxD2	—	—
22	P12	—	—	ANI22	—	IVREF1	—	—	—	—	TRDIOB1	—	TKBO00	—	SO11	—	—
23	P11	CCD07	—	ANI21	—	VCOUT3	PGAO	—	(TO03)	—	TRDIOC1	—	—	—	SI11/ SDA11/ (RxD2)	—	—
24	P10	CCD06	—	ANI20	—	VCOUT2	—	—	—	—	TRDIOD1	—	—	—	SCK11/ SCL11/ (TxD2)	—	—
25	P147	—	—	ANI18	ANO2	IVCMP3	PGAI3	—	—	—	—	—	—	—	—	—	—
26	P23	—	—	ANI3	ANO1	—	PGAGND	—	—	—	—	—	—	—	—	—	—
27	P22	—	—	ANI2	ANO0	—	PGAI4	—	—	—	—	—	—	—	—	—	—

Table 1 - 6 Multiplexed Pin Functions of the 32-pin Products (2/2)

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces		
	Digital port	Controlled current drive port		AD converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
28	P21	—	—	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	—	—	—	—	—	—	—
29	P20	—	—	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	—	—	—	—	—	—	—
30	P01	—	—	ANI30	—	IVCMP2	PGAI2	—	—	TO00/ (TI00)	TRJ00	—	TRGCLKB	—	—	RxD1	(DALIRxD0)
31	P00	—	—	ANI29	—	IVCMP1	PGAI1	—	—	TI00	(TRJ00)	—	TRGCLKA	—	—	TxD1	(DALITxD0)
32	P120	—	—	ANI19	—	IVCMP0	PGAI0	—	—	(TI02)/ (TO02)	—	—	TRGIDZ/ TRGTRG	—	—	—	—

### 1.3.6 40-pin products

- 40 -pin plastic HWQFN (6 × 6 mm, 0.50-mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register x (PIORx). Refer to **Figure 7 - 8 Format of Peripheral I/O Redirection Register 0 (PIOR0)** to **Figure 7 - 11 Format of Peripheral I/O Redirection Register 3 (PIOR3)** in the RL78/G24 User's Manual.

**Remark 3.** For the product in a QFN package, we recommend soldering the exposed die pad onto a plated area of the printed circuit board that has no electrical connections.

Table 1 - 7 Multiplexed Pin Functions of the 40-pin Products (1/2)

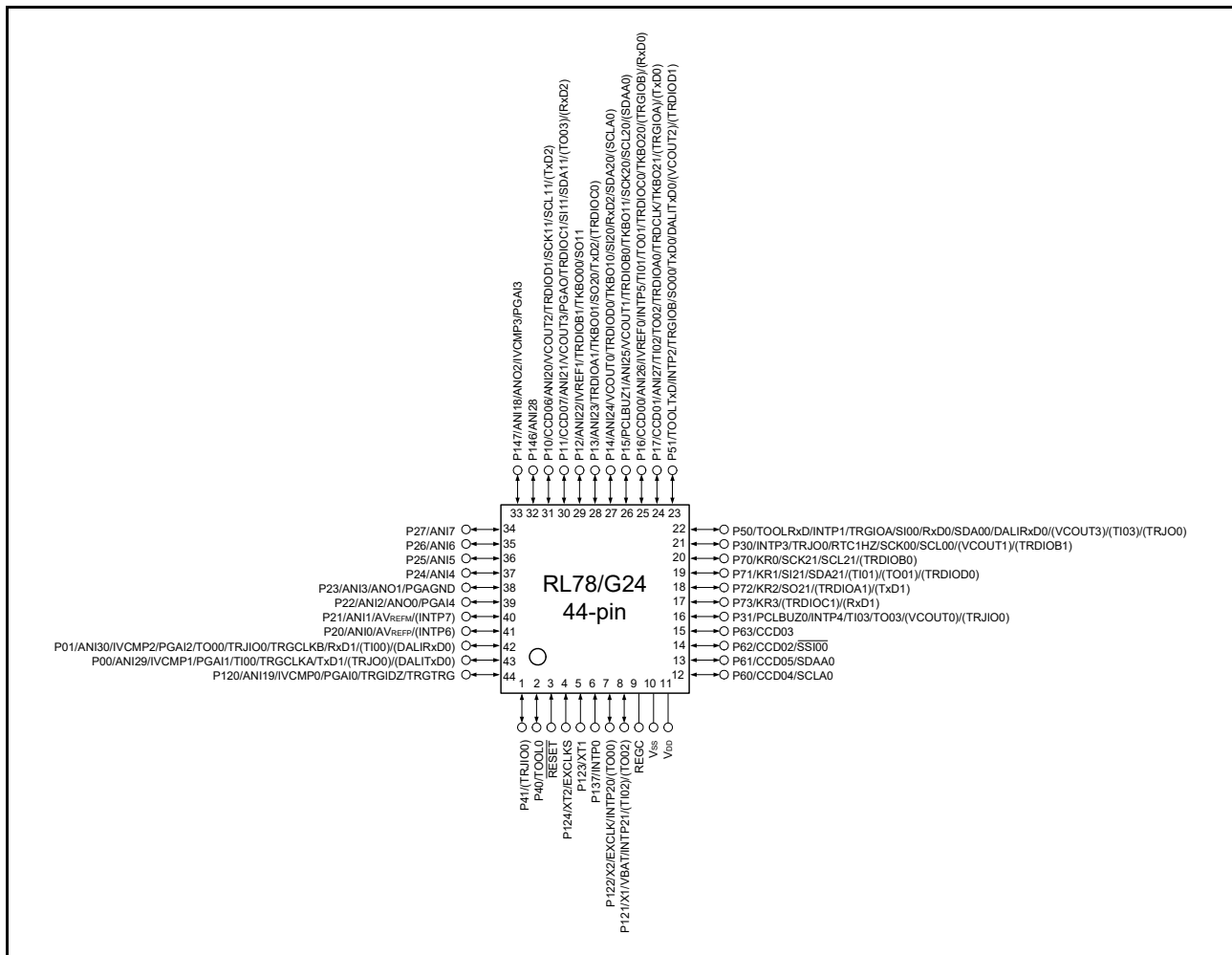
Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces		
	40HWQFN	Digital port Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
1	P40	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
2	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—
3	P124	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—	—
4	P123	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	P137	—	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—
6	P122	—	X2/EXCLK	—	—	—	—	INTP20	(TO00)	—	—	—	—	—	—	—	—
7	P121	—	X1/VBAT	—	—	—	—	INTP21	(TI02)/ (TO02)	—	—	—	—	—	—	—	—
8	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
9	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10	—	—	Vdd	—	—	—	—	—	—	—	—	—	—	—	—	—	—
11	P60	CCD04	—	—	—	—	—	—	—	—	—	—	—	—	—	SCLA0	—
12	P61	CCD05	—	—	—	—	—	—	—	—	—	—	—	—	—	SDAA0	—
13	P62	CCD02	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIO0	—
14	P31	—	PCLBUZ0	—	—	(VCOUT0)	—	INTP4	TI03/ TO03	(TRJIO0)	—	—	—	—	—	—	—
15	P73	—	—	—	—	—	—	KR3	—	—	(TRDIOC1)	—	—	—	(RxD1)	—	—
16	P72	—	—	—	—	—	—	KR2	—	—	(TRDIOA1)	—	—	—	SO21/ (TxD1)	—	—
17	P71	—	—	—	—	—	—	KR1	(TI01)/ (TO01)	—	(TRDIOD0)	—	—	—	SI21/ SDA21	—	—
18	P70	—	—	—	—	—	—	KR0	—	—	(TRDIOB0)	—	—	—	SCK21/ SCL21	—	—
19	P30	—	—	—	—	(VCOUT1)	—	INTP3	—	—	TRJO0	(TRDIOB1)	—	RTC1HZ	SCK00/ SCL00	—	—
20	P50	—	TOOLRxD	—	—	(VCOUT3)	—	INTP1	(TI03)	(TRJO0)	—	TRGIOA	—	—	SI00/ RxD0/ SDA00	—	DALIRxD0
21	P51	—	TOOLTxD	—	—	(VCOUT2)	—	INTP2	—	—	(TRDIOD1)	TRGIOB	—	—	SO00/ TxD0	—	DALITxD0
22	P17	CCD01	—	ANI27	—	—	—	—	TI02/ TO02	—	TRDIOA0/ TRDCLK	(TRGIOA)	TKBO21	—	(TxD0)	—	—
23	P16	CCD00	—	ANI26	—	IVREF0	—	INTP5	TI01/ TO01	—	TRDIOC0	(TRGIOB)	TKBO20	—	(RxD0)	—	—
24	P15	—	PCLBUZ1	ANI25	—	VCOUT1	—	—	—	—	TRDIOB0	—	TKBO11	—	SCK20/ SCL20	(SDAA0)	—
25	P14	—	—	ANI24	—	VCOUT0	—	—	—	—	TRDIOD0	—	TKBO10	—	SI20/ RxD2/ SDA20	(SCLA0)	—
26	P13	—	—	ANI23	—	—	—	—	—	—	TRDIOA1/ (TRDIOC0)	—	TKBO01	—	SO20/ TxD2	—	—
27	P12	—	—	ANI22	—	IVREF1	—	—	—	—	TRDIOB1	—	TKBO00	—	SO11	—	—
28	P11	CCD07	—	ANI21	—	VCOUT3	PGAO	—	(TO03)	—	TRDIOC1	—	—	—	SI11/ SDA11/ (RxD2)	—	—

Table 1 - 7 Multiplexed Pin Functions of the 40-pin Products (2/2)

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces		
	Digital port	Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
29	P10	CCD06	—	ANI20	—	VCOUT2	—	—	—	—	TRDIOD1	—	—	—	SCK11/ SCL11/ (Tx/D2)	—	—
30	P147	—	—	ANI18	ANO2	IVCMP3	PGAI3	—	—	—	—	—	—	—	—	—	—
31	P26	—	—	ANI6	—	—	—	—	—	—	—	—	—	—	—	—	—
32	P25	—	—	ANI5	—	—	—	—	—	—	—	—	—	—	—	—	—
33	P24	—	—	ANI4	—	—	—	—	—	—	—	—	—	—	—	—	—
34	P23	—	—	ANI3	ANO1	—	PGAGND	—	—	—	—	—	—	—	—	—	—
35	P22	—	—	ANI2	ANO0	—	PGAI4	—	—	—	—	—	—	—	—	—	—
36	P21	—	—	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	—	—	—	—	—	—	—
37	P20	—	—	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	—	—	—	—	—	—	—
38	P01	—	—	ANI30	—	IVCMP2	PGAI2	—	—	TO00/ (TI00)	TRJIO0	—	TRGCLKB	—	—	RxD1	(DALIRxD0)
39	P00	—	—	ANI29	—	IVCMP1	PGAI1	—	—	TI00	(TRJO0)	—	TRGCLKA	—	—	TxD1	(DALITxD0)
40	P120	—	—	ANI19	—	IVCMP0	PGAI0	—	—	—	—	—	TRGIDZ/ TRGTRG	—	—	—	—

### 1.3.7 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register x (PIORx). Refer to **Figure 7 - 8 Format of Peripheral I/O Redirection Register 0 (PIOR0)** to **Figure 7 - 11 Format of Peripheral I/O Redirection Register 3 (PIOR3)** in the RL78/G24 User's Manual.

Table 1 - 8 Multiplexed Pin Functions of the 44-pin Products (1/2)

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMI		Timers					Communications Interfaces		
	44LQFP	Digital port Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
1	P41	—	—	—	—	—	—	—	—	(TRJIO0)	—	—	—	—	—	—	—
2	P40	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
3	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—
4	P124	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	P123	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	P137	—	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—
7	P122	—	X2/EXCLK	—	—	—	—	INTP20	(TO00)	—	—	—	—	—	—	—	—
8	P121	—	X1/VBAT	—	—	—	—	INTP21	(TI02)/ (TO02)	—	—	—	—	—	—	—	—
9	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—	—	—
11	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	P60	CCD04	—	—	—	—	—	—	—	—	—	—	—	—	—	SCLA0	—
13	P61	CCD05	—	—	—	—	—	—	—	—	—	—	—	—	—	SDAA0	—
14	P62	CCD02	—	—	—	—	—	—	—	—	—	—	—	—	SSIO0	—	—
15	P63	CCD03	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
16	P31	—	PCLBUZ0	—	—	(VCOUT0)	—	INTP4	TI03/ TO03	(TRJIO0)	—	—	—	—	—	—	—
17	P73	—	—	—	—	—	—	KR3	—	—	(TRDIOC1)	—	—	—	(RxD1)	—	—
18	P72	—	—	—	—	—	—	KR2	—	—	(TRDIOA1)	—	—	—	SO21/ (TxD1)	—	—
19	P71	—	—	—	—	—	—	KR1	(TI01)/ (TO01)	—	(TRDIOD0)	—	—	—	SI21/S DA21	—	—
20	P70	—	—	—	—	—	—	KR0	—	—	(TRDIOB0)	—	—	—	SCK21/ SCL21	—	—
21	P30	—	—	—	—	(VCOUT1)	—	INTP3	—	TRJ00	(TRDIOB1)	—	—	RTC1HZ	SCK00/ SCL00	—	—
22	P50	—	TOOLRxD	—	—	(VCOUT3)	—	INTP1	(TI03)	(TRJ00)	—	TRGIOA	—	—	SI00/ RxD0/ SDA00	—	DALIRxD0
23	P51	—	TOOLTxD	—	—	(VCOUT2)	—	INTP2	—	—	(TRDIOD1)	TRGIOB	—	—	SO00/ TxD0	—	DALITxD0
24	P17	CCD01	—	ANI27	—	—	—	—	TI02/ TO02	—	TRDIOA0/ TRDCLK	(TRGIOA)	TKBO21	—	(TxD0)	—	—
25	P16	CCD00	—	ANI26	—	IVREF0	—	INTP5	TI01/ TO01	—	TRDIOC0	(TRGIOB)	TKBO20	—	(RxD0)	—	—
26	P15	—	PCLBUZ1	ANI25	—	VCOUT1	—	—	—	—	TRDIOB0	—	TKBO11	—	SCK20/ SCL20	—	(SDAA0)
27	P14	—	—	ANI24	—	VCOUT0	—	—	—	—	TRDIOD0	—	TKBO10	—	SI20/ RxD2/ SDA20	(SCLA0)	—
28	P13	—	—	ANI23	—	—	—	—	—	—	TRDIOA1/ (TRDIOC0)	—	TKBO01	—	SO20/ TxD2	—	—
29	P12	—	—	ANI22	—	IVREF1	—	—	—	—	TRDIOB1	—	TKBO00	—	SO11	—	—

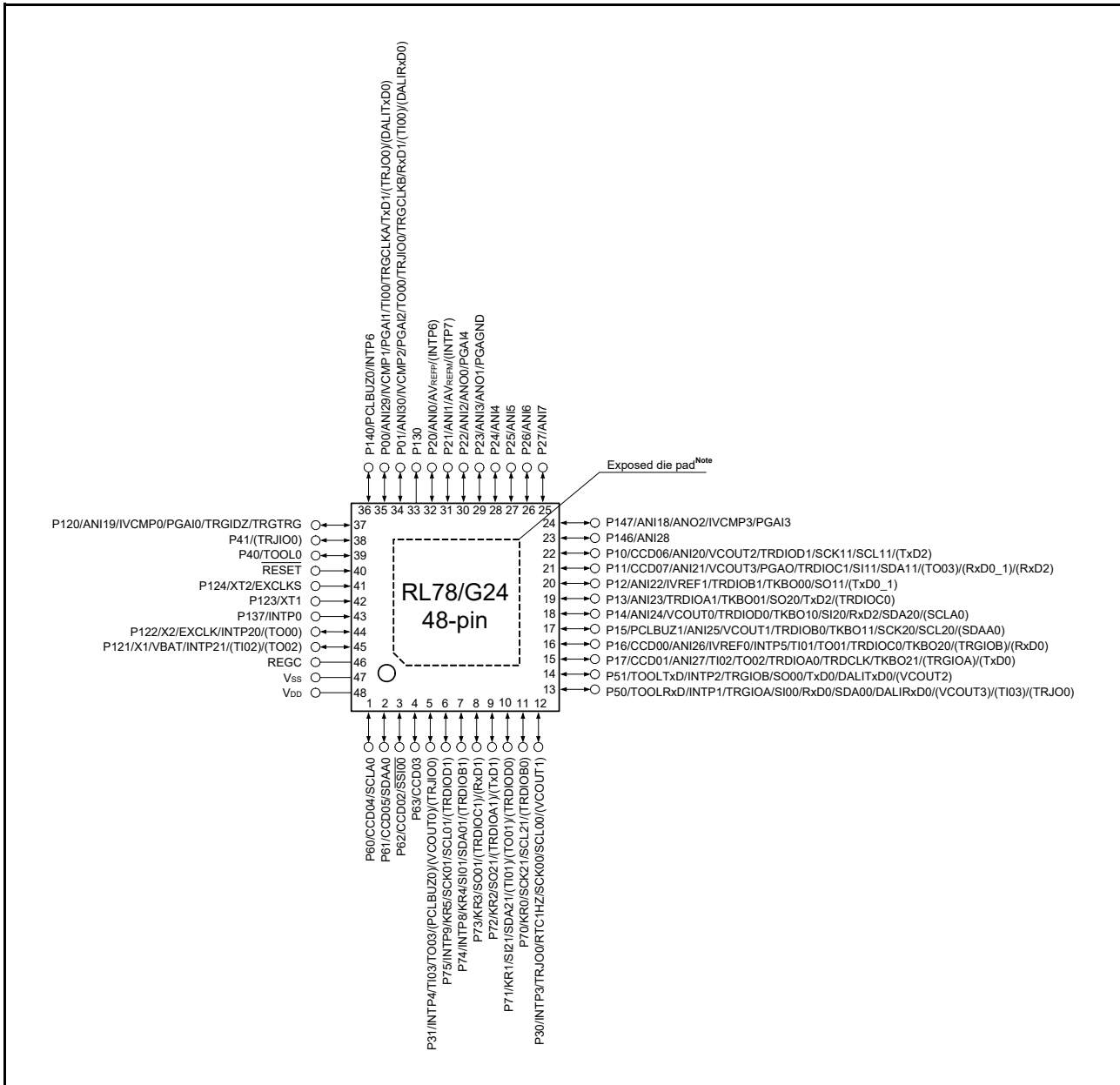
Table 1 - 8 Multiplexed Pin Functions of the 44-pin Products (2/2)

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits			HMIs		Timers					Communications Interfaces																					
	44LQFP	Digital port		Controlled current drive port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Digital addressable lighting interface (DALI)																
30	P11	CCD07	—	ANI21	—	VCOUT3	PGAO	—	—	(TO03)	—	TRDI0C1	—	—	—	—	—	—	—	—	—	S111/ SDA11/ (RxD2)	—	—	—										
31	P10	CCD06	—	ANI20	—	VCOUT2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCK11/ SCL11/ (TxD2)	—	—	—							
32	P146	—	—	ANI28	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—				
33	P147	—	—	ANI18	ANO2	IVCMP3	PGAI3	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—				
34	P27	—	—	ANI7	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—			
35	P26	—	—	ANI6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
36	P25	—	—	ANI5	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
37	P24	—	—	ANI4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
38	P23	—	—	ANI3	ANO1	—	PGAGND	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
39	P22	—	—	ANI2	ANO0	—	PGAI4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
40	P21	—	—	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
41	P20	—	—	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
42	P01	—	—	ANI30	—	IVCMP2	PGAI2	—	—	TO00/ (TI00)	TRJIO0	—	—	TRGCLKB	—	—	—	—	—	—	—	—	—	—	—	—	RxD1	—	—	(DALIRxD0)	—	—	—	—	
43	P00	—	—	ANI29	—	IVCMP1	PGAI1	—	—	TI00	(TRJO0)	—	—	TRGCLKA	—	—	—	—	—	—	—	—	—	—	—	—	TxD1	—	(DALITxD0)	—	—	—	—	—	
44	P120	—	—	ANI19	—	IVCMP0	PGAI0	—	—	—	—	—	—	TRGIDZ/ TRGTRG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—



### 1.3.8 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)
- 48-pin plastic HWQFN (7 × 7 mm, 0.50-mm pitch)



**Note** The 48-pin plastic LQFP (7 × 7 mm, 0.50-mm pitch) products do not have an exposed die pad.

**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register x (PIORx). Refer to **Figure 7 - 8 Format of Peripheral I/O Redirection Register 0 (PIOR0)** to **Figure 7 - 11 Format of Peripheral I/O Redirection Register 3 (PIOR3)** in the RL78/G24 User's Manual.

**Remark 3.** For the product in a QFN package, we recommend soldering the exposed die pad onto a plated area of the printed circuit board that has no electrical connections.

Table 1 - 9 Multiplexed Pin Functions of the 48-pin Products (1/2)

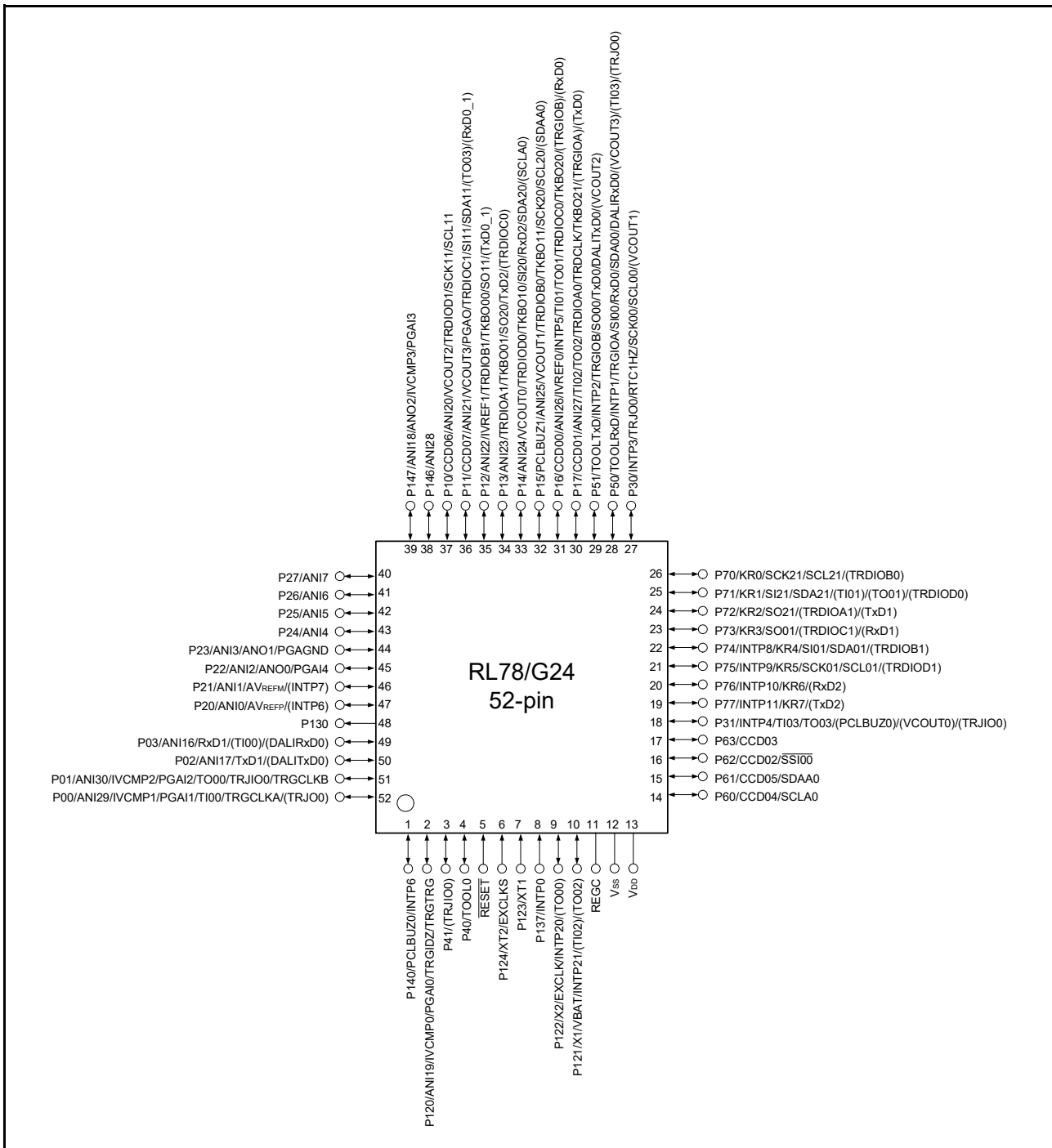
Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces		
	Digital port	Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
1	P60	CCD04	—	—	—	—	—	—	—	—	—	—	—	—	—	SCLA0	—
2	P61	CCD05	—	—	—	—	—	—	—	—	—	—	—	—	—	SDAA0	—
3	P62	CCD02	—	—	—	—	—	—	—	—	—	—	—	—	SSI00	—	—
4	P63	CCD03	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	P31	—	(PCLBUZ0)	—	—	(VCOUT0)	—	INTP4	—	TI03/ TO03	(TRJIO0)	—	—	—	—	—	—
6	P75	—	—	—	—	—	—	INTP9	KR5	—	—	(TRDIOD1)	—	—	—	SCK01/ SCL01	—
7	P74	—	—	—	—	—	—	INTP8	KR4	—	—	(TRDIOB1)	—	—	—	SI01/ SDA01	—
8	P73	—	—	—	—	—	—	—	KR3	—	—	(TRDIOC1)	—	—	—	SO01/ (RxD1)	—
9	P72	—	—	—	—	—	—	—	KR2	—	—	(TRDIOA1)	—	—	—	SO21/ (TxD1)	—
10	P71	—	—	—	—	—	—	—	KR1	(TI01)/ (TO01)	—	(TRDIOD0)	—	—	—	SI21/ SDA21	—
11	P70	—	—	—	—	—	—	—	KR0	—	—	(TRDIOB0)	—	—	—	SCK21/ SCL21	—
12	P30	—	—	—	—	(VCOUT1)	—	INTP3	—	—	TRJ00	—	—	RTC1HZ	SCK00/ SCL00	—	—
13	P50	—	TOOLRxD	—	—	(VCOUT3)	—	INTP1	—	(TI03)	(TRJ00)	—	TRGIOA	—	—	SI00/ RxD0/ SDA00	DALIRxD0
14	P51	—	TOOLTxD	—	—	(VCOUT2)	—	INTP2	—	—	—	—	TRGIOB	—	—	SO00/ TxD0	DALITxD0
15	P17	CCD01	—	ANI27	—	—	—	—	—	TI02/ TO02	—	TRDIOA0/ TRDCLK	(TRGIOA)	TKBO21	—	(TxD0)	—
16	P16	CCD00	—	ANI26	—	IVREF0	—	INTP5	—	TI01/ TO01	—	TRDIOC0	(TRGIOB)	TKBO20	—	(RxD0)	—
17	P15	—	PCLBUZ1	ANI25	—	VCOUT1	—	—	—	—	—	TRDIOB0	—	TKBO11	—	SCK20/ SCL20	(SDAA0)
18	P14	—	—	ANI24	—	VCOUT0	—	—	—	—	—	TRDIOD0	—	TKBO10	—	SI20/ RxD2/ SDA20	(SCLA0)
19	P13	—	—	ANI23	—	—	—	—	—	—	—	TRDIOA1/ (TRDIOC0)	—	TKBO01	—	SO20/ TxD2	—
20	P12	—	—	ANI22	—	IVREF1	—	—	—	—	—	TRDIOB1	—	TKBO00	—	SO11/ (TxD0_1)	—
21	P11	CCD07	—	ANI21	—	VCOUT3	PGAO	—	—	(TO03)	—	TRDIOC1	—	—	—	SI11/ SDA11/ (RxD0_1)/ (RxD2)	—
22	P10	CCD06	—	ANI20	—	VCOUT2	—	—	—	—	—	TRDIOD1	—	—	—	SCK11/ SCL11/ (TxD2)	—
23	P146	—	—	ANI28	—	—	—	—	—	—	—	—	—	—	—	—	—
24	P147	—	—	ANI18	ANO2	IVCMP3	PGA3	—	—	—	—	—	—	—	—	—	—

Table 1 - 9 Multiplexed Pin Functions of the 48-pin Products (2/2)

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers						Communications Interfaces		
	Digital port	Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Digital addressable lighting interface (DALI)
25	P27	—	—	ANI7	—	—	—	—	—	—	—	—	—	—	—	—	—	
26	P26	—	—	ANI6	—	—	—	—	—	—	—	—	—	—	—	—	—	
27	P25	—	—	ANI5	—	—	—	—	—	—	—	—	—	—	—	—	—	
28	P24	—	—	ANI4	—	—	—	—	—	—	—	—	—	—	—	—	—	
29	P23	—	—	ANI3	ANO1	—	PGAGND	—	—	—	—	—	—	—	—	—	—	
30	P22	—	—	ANI2	ANO0	—	PGAI4	—	—	—	—	—	—	—	—	—	—	
31	P21	—	—	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	—	—	—	—	—	—	—	
32	P20	—	—	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	—	—	—	—	—	—	—	
33	P130	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
34	P01	—	—	ANI30	—	IVCMP2	PGAI2	—	—	TO00/ (TI00)	TRJIO0	—	TRGCLKB	—	—	RxD1	— (DALIRxD0)	
35	P00	—	—	ANI29	—	IVCMP1	PGAI1	—	—	TI00	(TRJO0)	—	TRGCLKA	—	—	TxD1	— (DALITxD0)	
36	P140	—	PCLBUZ0	—	—	—	—	INTP6	—	—	—	—	—	—	—	—	—	
37	P120	—	—	ANI19	—	IVCMP0	PGAIO	—	—	—	—	—	TRGIDZ/ TRGTRG	—	—	—	—	
38	P41	—	—	—	—	—	—	—	—	—	(TRJIO0)	—	—	—	—	—	—	
39	P40	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
40	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
41	P124	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
42	P123	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
43	P137	—	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—	
44	P122	—	X2/EXCLK	—	—	—	—	INTP20	—	(TO00)	—	—	—	—	—	—	—	
45	P121	—	X1/VBAT	—	—	—	—	INTP21	—	(TI02)/ (TO02)	—	—	—	—	—	—	—	
46	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
47	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
48	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—	—	—	

### 1.3.9 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65-mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register x (PIORx). Refer to **Figure 7 - 8 Format of Peripheral I/O Redirection Register 0 (PIOR0)** to **Figure 7 - 11 Format of Peripheral I/O Redirection Register 3 (PIOR3)** in the RL78/G24 User's Manual.

Table 1 - 10 Multiplexed Pin Functions of the 52-pin Products (1/2)

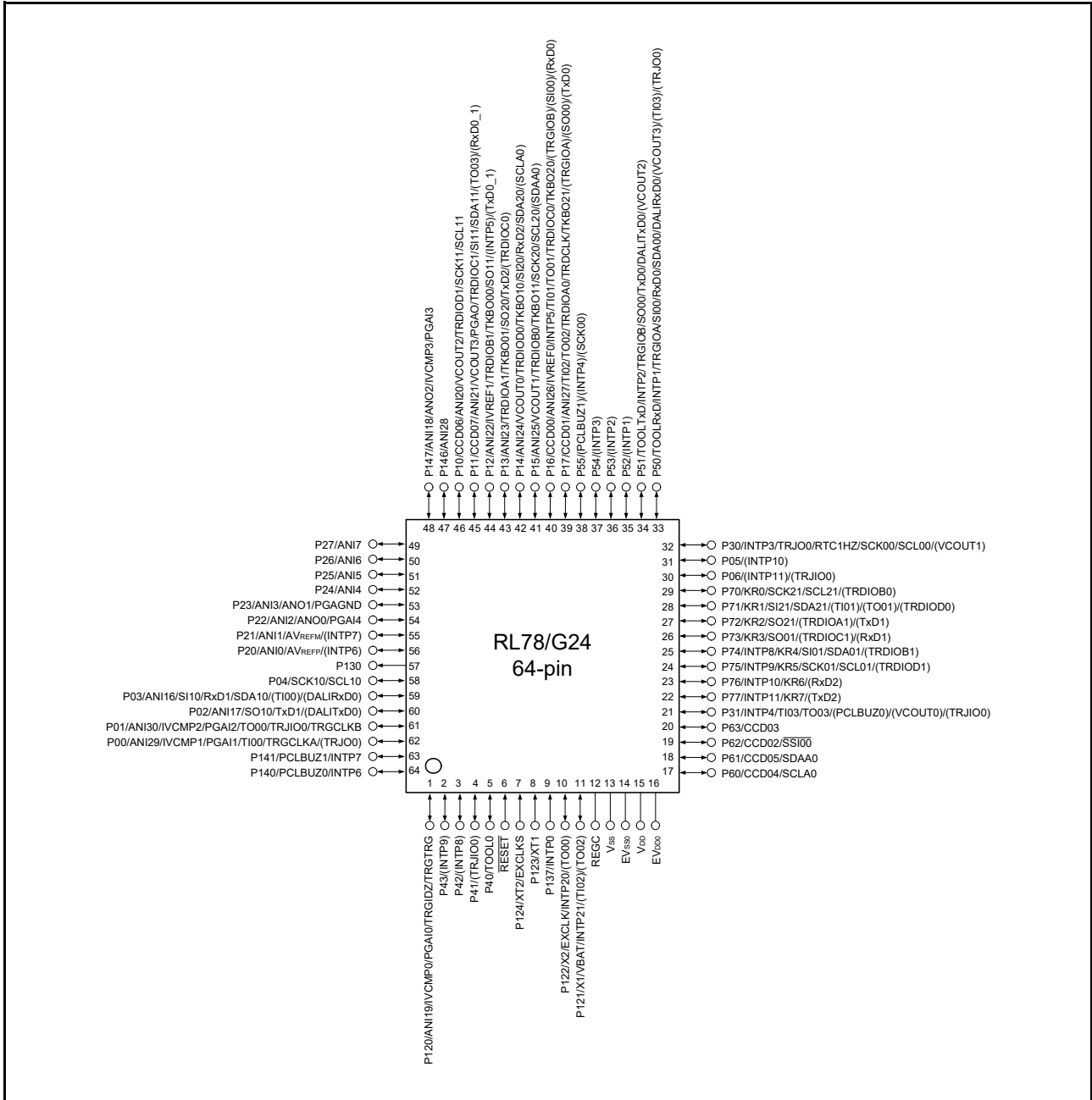
Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces		
	52LQFP	Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
1	P140	—	PCLBUZ0	—	—	—	—	INTP6	—	—	—	—	—	—	—	—	—
2	P120	—	—	ANI19	—	IVCMP0	PGAIO	—	—	—	—	TRGIDZ/ TRGTRG	—	—	—	—	—
3	P41	—	—	—	—	—	—	—	—	(TRJIO0)	—	—	—	—	—	—	—
4	P40	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	P124	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	P123	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8	P137	—	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—
9	P122	—	X2/EXCLK	—	—	—	—	INTP20	(TO00)	—	—	—	—	—	—	—	—
10	P121	—	X1/VBAT	—	—	—	—	INTP21	(TI02)/ (TO02)	—	—	—	—	—	—	—	—
11	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—	—	—
13	—	—	Vdd	—	—	—	—	—	—	—	—	—	—	—	—	—	—
14	P60	CCD04	—	—	—	—	—	—	—	—	—	—	—	—	—	SCLA0	—
15	P61	CCD05	—	—	—	—	—	—	—	—	—	—	—	—	—	SDAA0	—
16	P62	CCD02	—	—	—	—	—	—	—	—	—	—	—	—	SSI00	—	—
17	P63	CCD03	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
18	P31	—	(PCLBUZ0)	—	—	(VCOUT0)	—	INTP4	TI03/ TO03	(TRJIO0)	—	—	—	—	—	—	—
19	P77	—	—	—	—	—	—	INTP11	KR7	—	—	—	—	—	(TxD2)	—	—
20	P76	—	—	—	—	—	—	INTP10	KR6	—	—	—	—	—	(RxD2)	—	—
21	P75	—	—	—	—	—	—	INTP9	KR5	—	(TRDIOD1)	—	—	—	SCK01/ SCL01	—	—
22	P74	—	—	—	—	—	—	INTP8	KR4	—	(TRDIOB1)	—	—	—	SI01/ SDA01	—	—
23	P73	—	—	—	—	—	—	—	KR3	—	(TRDIOC1)	—	—	—	SO01/ (RxD1)	—	—
24	P72	—	—	—	—	—	—	—	KR2	—	(TRDIOA1)	—	—	—	SO21/ (TxD1)	—	—
25	P71	—	—	—	—	—	—	—	KR1	(TI01)/ (TO01)	(TRDIOD0)	—	—	—	SI21/ SDA21	—	—
26	P70	—	—	—	—	—	—	—	KR0	—	(TRDIOB0)	—	—	—	SCK21/ SCL21	—	—
27	P30	—	—	—	—	(VCOUT1)	—	INTP3	—	TRJO0	—	—	—	RTC1HZ	SCK00/ SCL00	—	—
28	P50	—	TOOLRxD	—	—	(VCOUT3)	—	INTP1	(TI03)	(TRJO0)	—	TRGIOA	—	—	SI00/ RxD0/ SDA00	—	DALIRxD0
29	P51	—	TOOLTxD	—	—	(VCOUT2)	—	INTP2	—	—	—	TRGIOB	—	—	SO00/ TxD0	—	DALITxD0

Table 1 - 10 Multiplexed Pin Functions of the 52-pin Products (2/2)

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMs		Timers					Communications Interfaces		
	52LQFP	Digital port Controlled current drive port		AD converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
30	P17	CCD01	—	ANI27	—	—	—	—	TI02/ TO02	—	TRDIOA0/ TRDCLK	(TRGIOA)	TKBO21	—	(TxD0)	—	—
31	P16	CCD00	—	ANI26	—	IVREF0	—	INTP5	—	TI01/ TO01	—	TRDIOC0	(TRGIOB)	TKBO20	—	(RxD0)	—
32	P15	—	PCLBUZ1	ANI25	—	VCOUT1	—	—	—	—	—	TRDIOB0	—	TKBO11	—	SCK20/ SCL20	(SDAA0)
33	P14	—	—	ANI24	—	VCOUT0	—	—	—	—	—	TRDIOD0	—	TKBO10	—	SI20/ RxD2/ SDA20	(SCLA0)
34	P13	—	—	ANI23	—	—	—	—	—	—	—	TRDIOA1/ (TRDIOC0)	—	TKBO01	—	SO20/ TxD2	—
35	P12	—	—	ANI22	—	IVREF1	—	—	—	—	—	TRDIOB1	—	TKBO00	—	SO11/ (TxD0_1)	—
36	P11	CCD07	—	ANI21	—	VCOUT3	PGAO	—	—	(TO03)	—	TRDIOC1	—	—	—	—	SI11/ SDA11/ (RxD0_1)
37	P10	CCD06	—	ANI20	—	VCOUT2	—	—	—	—	—	TRDIOD1	—	—	—	—	SCK11/ SCL11
38	P146	—	—	ANI28	—	—	—	—	—	—	—	—	—	—	—	—	—
39	P147	—	—	ANI18	ANO2	IVCMP3	PGA3	—	—	—	—	—	—	—	—	—	—
40	P27	—	—	ANI7	—	—	—	—	—	—	—	—	—	—	—	—	—
41	P26	—	—	ANI6	—	—	—	—	—	—	—	—	—	—	—	—	—
42	P25	—	—	ANI5	—	—	—	—	—	—	—	—	—	—	—	—	—
43	P24	—	—	ANI4	—	—	—	—	—	—	—	—	—	—	—	—	—
44	P23	—	—	ANI3	ANO1	—	PGAGND	—	—	—	—	—	—	—	—	—	—
45	P22	—	—	ANI2	ANO0	—	PGA4	—	—	—	—	—	—	—	—	—	—
46	P21	—	—	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	—	—	—	—	—	—	—
47	P20	—	—	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	—	—	—	—	—	—	—
48	P130	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
49	P03	—	—	ANI16	—	—	—	—	(TI00)	—	—	—	—	—	—	RxD1	(DALIRxD0)
50	P02	—	—	ANI17	—	—	—	—	—	—	—	—	—	—	—	TxD1	(DALITxD0)
51	P01	—	—	ANI30	—	IVCMP2	PGA2	—	TO00	TRJIO0	—	TRGCLKB	—	—	—	—	—
52	P00	—	—	ANI29	—	IVCMP1	PGA1	—	TI00	(TRJO0)	—	TRGCLKA	—	—	—	—	—

1.3.10 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.50-mm pitch)



- Caution 1.** Connect the EVSS0 pin to the same ground as the VSS pin.
- Caution 2.** Make sure that the voltage on the VDD pin is no less than that on the EVDD0 pin.
- Caution 3.** Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

- Remark 1.** For pin identification, see 1.4 Pin Identification.
- Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.
- Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register x (PIORx). Refer to **Figure 7 - 8 Format of Peripheral I/O Redirection Register 0 (PIOR0)** to **Figure 7 - 11 Format of Peripheral I/O Redirection Register 3 (PIOR3)** in the RL78/G24 User's Manual.

Table 1 - 11 Multiplexed Pin Functions of the 64-pin Products (1/3)

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces		
	64LQFP, 64LFQFP	Digital port Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
1	P120	—	—	ANI19	—	IVCMP0	PGA10	—	—	—	—	TRGIDZ/ TRGTRG	—	—	—	—	—
2	P43	—	—	—	—	—	—	(INTP9)	—	—	—	—	—	—	—	—	—
3	P42	—	—	—	—	—	—	(INTP8)	—	—	—	—	—	—	—	—	—
4	P41	—	—	—	—	—	—	—	—	(TRJIO0)	—	—	—	—	—	—	—
5	P40	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	P124	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8	P123	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
9	P137	—	—	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—
10	P122	—	X2/EXCLK	—	—	—	—	INTP20	(TO00)	—	—	—	—	—	—	—	—
11	P121	—	X1/VBAT	—	—	—	—	INTP21	(TI02)/ (TO02)	—	—	—	—	—	—	—	—
12	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
13	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—	—	—
14	—	—	EVSS0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
15	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—	—	—
16	—	—	EVDD0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
17	P60	CCD04	—	—	—	—	—	—	—	—	—	—	—	—	—	SCLA0	—
18	P61	CCD05	—	—	—	—	—	—	—	—	—	—	—	—	—	SDAA0	—
19	P62	CCD02	—	—	—	—	—	—	—	—	—	—	—	—	SSIO0	—	—
20	P63	CCD03	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
21	P31	—	(PCLBUZ0)	—	—	(VCOUT0)	—	INTP4	TI03/ TO03	(TRJIO0)	—	—	—	—	—	—	—
22	P77	—	—	—	—	—	—	INTP11	KR7	—	—	—	—	—	—	(TxD2)	—
23	P76	—	—	—	—	—	—	INTP10	KR6	—	—	—	—	—	—	(RxD2)	—
24	P75	—	—	—	—	—	—	INTP9	KR5	—	—	(TRDIOD1)	—	—	—	SCK01/ SCL01	—
25	P74	—	—	—	—	—	—	INTP8	KR4	—	—	(TRDIOB1)	—	—	—	SI01/ SDA01	—
26	P73	—	—	—	—	—	—	—	KR3	—	—	(TRDIOC1)	—	—	—	SO01/ (RxD1)	—
27	P72	—	—	—	—	—	—	—	KR2	—	—	(TRDIOA1)	—	—	—	SO21/ (TxD1)	—
28	P71	—	—	—	—	—	—	—	KR1	(TI01)/ (TO01)	—	—	—	—	—	SI21/ SDA21	—
29	P70	—	—	—	—	—	—	—	KR0	—	—	(TRDIOB0)	—	—	—	SCK21/ SCL21	—
30	P06	—	—	—	—	—	—	(INTP11)	—	(TRJIO0)	—	—	—	—	—	—	—
31	P05	—	—	—	—	—	—	(INTP10)	—	—	—	—	—	—	—	—	—



Table 1 - 11 Multiplexed Pin Functions of the 64-pin Products (2/3)

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces			
	Digital port	Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Digital addressable lighting interface (DALI)
32	P30	—	—	—	—	(VCOUT1)	—	INTP3	—	—	TRJ00	—	—	—	RTC1HZ	SCK00/ SCL00	—	—
33	P50	—	TOOLRxD	—	—	(VCOUT3)	—	INTP1	—	(TI03)	(TRJ00)	—	TRGIOA	—	—	SI00/ RxD0/ SDA00	—	DALIRxD0
34	P51	—	TOOLTxD	—	—	(VCOUT2)	—	INTP2	—	—	—	—	TRGIOB	—	—	SO00/ TxD0	—	DALITxD0
35	P52	—	—	—	—	—	—	(INTP1)	—	—	—	—	—	—	—	—	—	—
36	P53	—	—	—	—	—	—	(INTP2)	—	—	—	—	—	—	—	—	—	—
37	P54	—	—	—	—	—	—	(INTP3)	—	—	—	—	—	—	—	—	—	—
38	P55	—	(PCLBUZ1)	—	—	—	—	(INTP4)	—	—	—	—	—	—	(SCK00)	—	—	—
39	P17	CCD01	—	ANI27	—	—	—	—	—	TI02/ TO02	—	TRDIOA0/ TRDCLK	(TRGIOA)	TKBO21	—	(SO00)/ (TxD0)	—	—
40	P16	CCD00	—	ANI26	—	IVREF0	—	INTP5	—	TI01/ TO01	—	TRDIOC0	(TRGIOB)	TKBO20	—	(SI00)/ (RxD0)	—	—
41	P15	—	—	ANI25	—	VCOUT1	—	—	—	—	—	TRDIOB0	—	TKBO11	—	SCK20/ SCL20	(SDAA0)	—
42	P14	—	—	ANI24	—	VCOUT0	—	—	—	—	—	TRDIOD0	—	TKBO10	—	SI20/ RxD2/ SDA20	(SCLA0)	—
43	P13	—	—	ANI23	—	—	—	—	—	—	—	TRDIOA1/ (TRDIOC0)	—	TKBO01	—	SO20/ TxD2	—	—
44	P12	—	—	ANI22	—	IVREF1	—	(INTP5)	—	—	—	TRDIOB1	—	TKBO00	—	SO11/ (TxD0_1)	—	—
45	P11	CCD07	—	ANI21	—	VCOUT3	PGAO	—	—	(TO03)	—	TRDIOC1	—	—	—	SI11/ SDA11/ (RxD0_1)	—	—
46	P10	CCD06	—	ANI20	—	VCOUT2	—	—	—	—	—	TRDIOD1	—	—	—	SCK11/ SCL11	—	—
47	P146	—	—	ANI28	—	—	—	—	—	—	—	—	—	—	—	—	—	—
48	P147	—	—	ANI18	ANO2	IVCMP3	PGAI3	—	—	—	—	—	—	—	—	—	—	—
49	P27	—	—	ANI7	—	—	—	—	—	—	—	—	—	—	—	—	—	—
50	P26	—	—	ANI6	—	—	—	—	—	—	—	—	—	—	—	—	—	—
51	P25	—	—	ANI5	—	—	—	—	—	—	—	—	—	—	—	—	—	—
52	P24	—	—	ANI4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
53	P23	—	—	ANI3	ANO1	—	PGAGND	—	—	—	—	—	—	—	—	—	—	—
54	P22	—	—	ANI2	ANO0	—	PGAI4	—	—	—	—	—	—	—	—	—	—	—
55	P21	—	—	ANI1/ AVREFM	—	—	—	(INTP7)	—	—	—	—	—	—	—	—	—	—
56	P20	—	—	ANI0/ AVREFP	—	—	—	(INTP6)	—	—	—	—	—	—	—	—	—	—
57	P130	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
58	P04	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SCK10/ SCL10	—	—

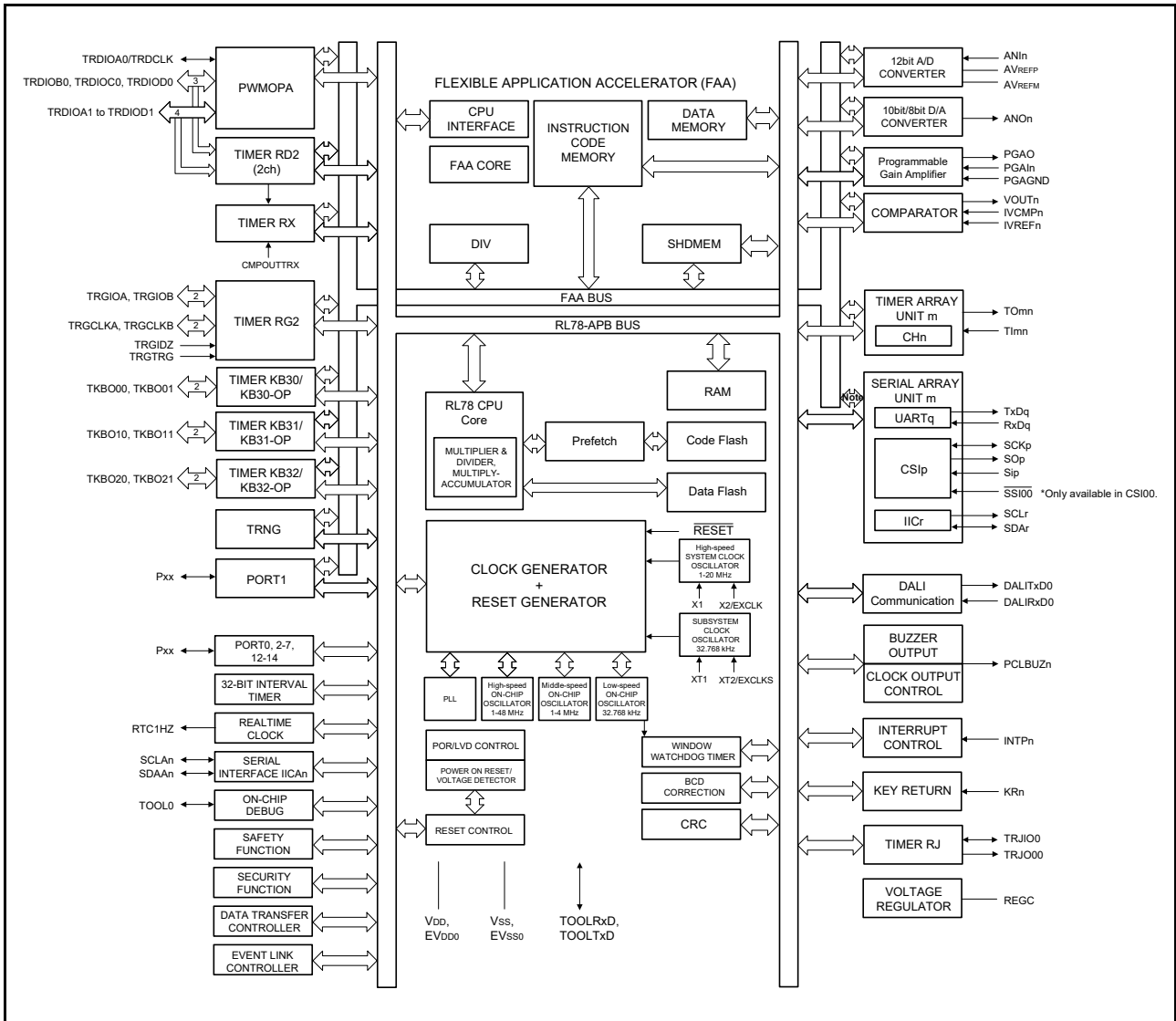
Table 1 - 11 Multiplexed Pin Functions of the 64-pin Products (3/3)

Pin Number	I/O		Power supply, system clock, and debugging	Analog Circuits				HMIs		Timers					Communications Interfaces		
	Digital port	Controlled current drive port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Programmable gain amplifier (PGA)	Interrupt (INTP)	Key interrupt (KR)	Timer array unit (TAU)	Timer RJ (TRJ)	Timer RD2 (TRD2)	Timer RG2 (TRG2)	16-bit timers KB30, KB31, and KB32 (TMKB3)	Realtime clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)
59	P03	—	—	ANI16	—	—	—	—	(T100)	—	—	—	—	—	SI10/RxD1/SDA10	—	(DALIRxD0)
60	P02	—	—	ANI17	—	—	—	—	—	—	—	—	—	—	SO10/TxD1	—	(DALITxD0)
61	P01	—	—	ANI30	—	IVCMP2	PGAI2	—	TO00	TRJIO0	—	TRGCLKB	—	—	—	—	—
62	P00	—	—	ANI29	—	IVCMP1	PGAI1	—	TI00	(TRJO0)	—	TRGCLKA	—	—	—	—	—
63	P141	—	PCLBUZ1	—	—	—	—	INTP7	—	—	—	—	—	—	—	—	—
64	P140	—	PCLBUZ0	—	—	—	—	INTP6	—	—	—	—	—	—	—	—	—

## 1.4 Pin Identification

ANI0 to ANI7,		SCL00, SCL01, SCL10,	
ANI16 to ANI30	: Analog input	SCL11, SCL20, SCL21	: Serial clock output
ANO0 to ANO2	: Analog output	SDAA0,	
AVREFM	: Analog reference voltage minus	SDA00, SDA01, SDA10,	
AVREFP	: Analog reference voltage plus	SDA11, SDA20, SDA21	: Serial data input/output
CCD00 to CCD07	: Controlled current drive output	SI00, SI01, SI10, SI11,	
DALIRxD0	: DALI receive data	SI20, SI21, SI30, SI31	: Serial data input
DALITxD0	: DALI transmit data	SO00, SO01, SO10,	
EVDD0	: Power supply for port	SO11, SO20, SO21	: Serial data output
EVSS0	: Ground for port	$\overline{SSI00}$	: Serial interface chip select input
EXCLK	: External clock input (main system clock)	TI00 to TI03	: Timer input
EXCLKS	: External clock input (subsystem clock)	TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21	: Timer KB3 output
INTP0 to INTP11,		TO00 to TO03	: Timer output
INTP20, INTP21	: Interrupt request from peripheral	TOOL0	: Data input/output for tool
IVCMP0 to IVCMP3	: Comparator input	TOOLRxD, TOOLTxD	: Data input/output for external device
IVREF0, IVREF1	: Comparator reference input	TRDCLK	: Timer RD2 external input clock
KR0 to KR7	: Key return	TRDIOA0, TRDIOB0,	
P00 to P06	: Port 0	TRDIOC0, TRDIOD0,	
P10 to P17	: Port 1	TRDIOA1, TRDIOB1,	
P20 to P27	: Port 2	TRDIOC1, TRDIOD1	: Timer RD2 input/output
P30, P31	: Port 3	TRGIOA, TRGIOB	: Timer RG2 input/output
P40 to P43	: Port 4	TRGCLKA, TRGCLKB	: Timer RG2 external input clock
P50 to P55	: Port 5	TRGIDZ, TRGTRG	: Timer RG2 external trigger input
P60 to P63	: Port 6	TRJIO0	: Timer RJ input/output
P70 to P77	: Port 7	TRJO0	: Timer RJ output
P120 to P124	: Port 12	TxD0 to TxD2	: Transmit data
P130, P137	: Port 13	VBAT	: Battery backup power supply
P140, P141, P146, P147	: Port 14	VCOUT0 to VCOUT3	: Comparator output
PCLBUZ0, PCLBUZ1	: Programmable clock output/buzzer output	VDD	: Power supply
PGAGND	: PGA ground	VSS	: Ground
PGAI0 to PGAI4	: PGA input	X1, X2	: Crystal oscillator (main system clock)
PGAO	: PGA output	XT1, XT2	: Crystal oscillator (subsystem clock)
REGC	: Regulator capacitance		
$\overline{RESET}$	: Reset		
RTC1HZ	: Realtime clock correction clock (1 Hz) output		
RxD0 to RxD2	: Receive data		
SCLA0,			
SCK00, SCK01, SCK10,			
SCK11, SCK20, SCK21	: Serial clock input/output		

### 1.5 Block Diagram



**Note** Serial array unit 0 is only connected to the FAA bus.

**Caution** The key return function is only incorporated in the 40- to 128-pin products.

**Remark** m: Unit number, n: Channel number, p: CSI number, q: UART number, r: Simplified I<sup>2</sup>C number, xx: Port number

## 1.6 Outline of Functions

[20-, 24-, 25-, 30-, and 32-pin products]

**Caution** This outline describes the functions at the time when peripheral I/O redirection register x (PIORx) is set to 00H.

(1/3)

Item		20-pin	24-pin	25-pin	30-pin	32-pin
		R7F101G6x	R7F101G7x	R7F101G8x	R7F101GAx	R7F101GBx
Code flash memory		64 or 128 Kbytes				
Data flash memory		4 Kbytes				
RAM		12 Kbytes				
Address space		1 Mbyte				
CPU/ peripheral hardware clock frequency (fCLK)	Main system clock	HS (high-speed main) mode: 1 to 48 MHz (VDD = 2.4 to 5.5 V) HS (high-speed main) mode: 1 to 32 MHz (VDD = 1.8 to 5.5 V) HS (high-speed main) mode: 1 to 4 MHz <sup>Note 1</sup> (VDD = 1.6 to 5.5 V) LS (low-speed main) mode: 1 to 24 MHz (VDD = 1.8 to 5.5 V) LS (low-speed main) mode: 1 to 4 MHz <sup>Note 1</sup> (VDD = 1.6 to 5.5 V) LP (low-power main) mode: 1 to 2 MHz <sup>Note 2</sup> (VDD = 1.6 to 5.5 V)				
	Subsystem clock	SUB mode: 32.768 kHz (VDD = 1.6 to 5.5 V)				
Main system clock	High-speed system clock (fmx)	1 to 20 MHz				
	High-speed on-chip oscillator clock (fIH)	1 MHz, 2 MHz, 3 MHz, 4 MHz, 6 MHz, 8 MHz, 12 MHz, 16 MHz, 24 MHz, 32 MHz, 48 MHz, 64 MHz				
	Middle-speed on-chip oscillator clock (fIM)	1 MHz, 2 MHz, 4 MHz				
	PLL clock	16 MHz, 32 MHz <sup>Note 3</sup> (VDD = 1.8 to 5.5 V) 24 MHz, 48 MHz <sup>Note 4</sup> (VDD = 2.4 to 5.5 V)				
Subsystem clock	Subsystem clock oscillator clock (fsx, fsXR)	32.768 kHz (VDD = 2.4 to 5.5 V)				
	Low-speed on-chip oscillator clock (fIL)	32.768 kHz (typ.)				
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.03125 μs (at the 32-MHz operation with the high-speed on-chip oscillator clock (fIH)) 0.02083 μs (at the 48-MHz operation with the high-speed on-chip oscillator clock (fIH)) <sup>Note 5</sup> 0.03125 μs (PLL clock: fPLL = 64 MHz, fIH = 16 or 32 MHz <sup>Note 3</sup> ) 0.02083 μs (PLL clock: fPLL = 96 MHz, fIH = 24 or 48 MHz <sup>Note 4</sup> ) <sup>Note 5</sup>				
Instruction set		<ul style="list-style-type: none"> <li>• Data transfer (8/16 bits)</li> <li>• Adder and subtractor/logical operation (8/16 bits)</li> <li>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)</li> <li>• Multiplication and accumulation (16 bits × 16 bits + 32 bits)</li> <li>• Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.</li> </ul>				

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Item	20-pin	24-pin	25-pin	30-pin	32-pin	
	R7F101G6x	R7F101G7x	R7F101G8x	R7F101GAx	R7F101GBx	
FAA core	<ul style="list-style-type: none"> <li>• Multiplication: 32-bit signed × 32-bit signed → 32-bit signed</li> <li>• Results of 64-bit multiplication can be right-shifted by a desired number of bits.</li> <li>• Addition: 32-bit signed + 32-bit signed → 32-bit signed (internally calculated with 33-bit precision)</li> <li>• Subtraction: 32-bit signed - 32-bit signed → 32-bit signed (internally calculated with 33-bit precision)</li> <li>• Limit operation: Operation parameter registers (33 bits × 4) in which upper and lower limits can be set.</li> <li>• Operation parameter registers (32 bits × 6)</li> <li>• Address pointer registers (12 bits × 6)</li> <li>• On-chip code RAM: 4 Kbytes</li> <li>• On-chip data RAM: 2 Kbytes</li> <li>• Multiple interrupts available</li> <li>• A 32-byte shared memory is included for sharing of data by the RL78 CPU and FAA core.</li> </ul>					
I/O port	Total number of pins	16	20	21	26	28
	CMOS I/O	15 (N-ch open drain I/O [withstand voltage of VDD]: 7)	19 (N-ch open drain I/O [withstand voltage of VDD]: 8)		23 (N-ch open drain I/O [withstand voltage of VDD]: 11)	25 (N-ch open drain I/O [withstand voltage of VDD]: 11)
	CMOS input	1				
	CMOS output	—		1	—	
	N-ch open drain I/O (withstand voltage: 6 V)	—			2	
	Controlled current drive port	2	4		6	7
Timers	16-bit timers TAU, timer RJ, timer RD2, timer RX, timer RG2	9 channels in total: 4-channel timer array unit (TAU) 1-channel timer RJ 2-channel timer RD2 with PWMOPA 1-channel timer RG2 1-channel timer RX				
	16-bit timer Timer KB3	2 channels (PWM outputs: 4)	3 channels (PWM outputs: 6)			
	Watchdog timer	1 channel				
	Realtime clock (RTC)	1 channel				
	32-bit interval timer (TML32)	1 channel in 32-bit counter mode, 2 channels in 16-bit counter mode, 4 channels in 8-bit counter mode				
	Timer outputs	11 (PWM outputs: 10 <sup>Note 6</sup> ), 19 (PWM outputs: 11 <sup>Note 6</sup> ) <sup>Note 7</sup>	17 (PWM outputs: 14 <sup>Note 6</sup> ), 22 (PWM outputs: 14 <sup>Note 6</sup> ) <sup>Note 7</sup>			
	RTC output	—			1	
Clock output/buzzer output	1				2	
	<ul style="list-style-type: none"> <li>• 3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (Main system clock: f<sub>MAIN</sub> = 32 MHz)</li> <li>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Low-speed peripheral clock: f<sub>SP</sub> = 32.768 kHz)</li> </ul>					
8-/10-/12-bit resolution A/D converter	12 channels	13 channels	16 channels			
	3-channel simultaneous sampling	2 channels				

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Item	20-pin	24-pin	25-pin	30-pin	32-pin
	R7F101G6x	R7F101G7x	R7F101G8x	R7F101GAx	R7F101GBx
8-/10-bit D/A converter	2 to 3 channels				
DAC outputs (ANOx)	2	3			
Programmable gain amplifier (PGA)	1 channel				
Comparator module	3 channels	4 channels			
Serial interfaces	<p>[20-pin products]</p> <ul style="list-style-type: none"> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> </ul> <p>[24- and 25-pin products]</p> <ul style="list-style-type: none"> <li>• UART (supporting LIN-bus): 1 channel</li> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> </ul> <p>[30- and 32-pin products]</p> <ul style="list-style-type: none"> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART (UART supporting LIN-bus): 1 channel</li> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> </ul>				
I <sup>2</sup> C bus	—			1	
I <sup>2</sup> C (SM/PM) bus	—			1	
DALI	—			1	
Data transfer controller (DTC)	42 sources	47 sources		52 sources	
Vectored interrupt sources	Internal	46	55		
	External	6	8	12	
Key interrupt	—				
Reset	<ul style="list-style-type: none"> <li>• Reset by <math>\overline{\text{RESET}}</math> pin</li> <li>• Internal reset by watchdog timer</li> <li>• Internal reset by power-on-reset</li> <li>• Internal reset by voltage detectors (LVD0 and LVD1)</li> <li>• Internal reset by illegal instruction execution<sup>Note 8</sup></li> <li>• Internal reset by RAM parity error</li> <li>• Internal reset by illegal-memory access</li> </ul>				
Power-on-reset circuit	<ul style="list-style-type: none"> <li>• Power-on reset: 1.51 V (typ.)</li> <li>• Power-down reset: 1.50 V (typ.)</li> </ul>				
Voltage detector	LVD0	Detection voltage <ul style="list-style-type: none"> <li>• Rising edge: 1.69 to 3.96 V (6 stages)</li> <li>• Falling edge: 1.65 to 3.88 V (6 stages)</li> </ul>			
	LVD1	Detection voltage <ul style="list-style-type: none"> <li>• Rising edge: 1.67 to 4.16 V (18 stages)</li> <li>• Falling edge: 1.63 to 4.08 V (18 stages)</li> </ul>			
On-chip debugging	Available (tracing supported)				
Power supply voltage	$V_{DD} = 1.6$ to $5.5$ V (2D: Consumer applications, 3C: Industrial applications) $V_{DD} = 2.7$ to $5.5$ V (4C: Industrial applications)				
Operating ambient temperature	$T_A = -40$ to $+85^\circ\text{C}$ (2D: Consumer applications), $T_A = -40$ to $+105^\circ\text{C}$ (3C: Industrial applications), $T_A = -40$ to $+125^\circ\text{C}$ (4C: Industrial applications)				

**Note 1.** Overwrite the flash memory during operation at a frequency of no higher than 4 MHz.

**Note 2.** When the flash memory is to be overwritten, switch to HS (high-speed main) mode or LS (low-speed main) mode.

**Note 3.** Applicable when the PLL clock frequency is 64 MHz. Select f<sub>PLL/2</sub> (32 MHz) or f<sub>PLL/4</sub> (16 MHz) as the system clock.

**Note 4.** Applicable when the PLL clock frequency is 96 MHz. Select f<sub>PLL/2</sub> (32 MHz) or f<sub>PLL/4</sub> (16 MHz) as the system clock.

**Note 5.** This applies when the prefetch buffer is enabled. For details on the operation of the prefetch buffer, refer to **Section 8**

**Operation State Control** in the RL78/G24 User's Manual.

- Note 6.** The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). For details, see **10.9.3 Operation for the multiple PWM output function** in the RL78/G24 User's Manual.
- Note 7.** This applies when the setting of the PIOR0 bit is 1.
- Note 8.** In normal operation, executing the instruction code FFH triggers an internal reset, but this is not the case during emulation by the in-circuit emulator or on-chip debugging emulator.



**[40-, 44-, 48-, 52-, and 64-pin products]**

**Caution** This outline describes the functions at the time when peripheral I/O redirection register x (PIORx) is set to 00H.

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Item		40-pin	44-pin	48-pin	52-pin	64-pin
		R7F101GEx	R7F101GFx	R7F101GGx	R7F101GJx	R7F101GLx
Code flash memory		64 or 128 Kbytes				
Data flash memory		4 Kbytes				
RAM		12 Kbytes				
Address space		1 Mbyte				
CPU/ peripheral hardware clock frequency (fCLK)	Main system clock	HS (high-speed main) mode: 1 to 48 MHz (VDD = 2.4 to 5.5 V) HS (high-speed main) mode: 1 to 32 MHz (VDD = 1.8 to 5.5 V) HS (high-speed main) mode: 1 to 4 MHz <sup>Note 1</sup> (VDD = 1.6 to 5.5 V) LS (low-speed main) mode: 1 to 24 MHz (VDD = 1.8 to 5.5 V) LS (low-speed main) mode: 1 to 4 MHz <sup>Note 1</sup> (VDD = 1.6 to 5.5 V) LP (low-power main) mode: 1 to 2 MHz <sup>Note 2</sup> (VDD = 1.6 to 5.5 V)				
	Subsystem clock	SUB mode: 32.768 kHz (VDD = 1.6 to 5.5 V)				
Main system clock	High-speed system clock (fMX)	1 to 20 MHz				
	High-speed on-chip oscillator clock (fIH)	1 MHz, 2 MHz, 3 MHz, 4 MHz, 6 MHz, 8 MHz, 12 MHz, 16 MHz, 24 MHz, 32 MHz, 48 MHz, 64 MHz				
	Middle-speed on-chip oscillator clock (fIM)	1 MHz, 2 MHz, 4 MHz				
	PLL clock	16 MHz, 32 MHz <sup>Note 3</sup> (VDD = 1.8 to 5.5 V) 24 MHz, 48 MHz <sup>Note 4</sup> (VDD = 2.4 to 5.5 V)				
Subsystem clock	Subsystem clock oscillator clock (fSX, fSXR)	32.768 kHz (VDD = 1.6 to 5.5 V)				
	Low-speed on-chip oscillator clock (fIL)	32.768 kHz (typ.)				
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.03125 μs (at the 32-MHz operation with the high-speed on-chip oscillator clock (fIH)) 0.02083 μs (at the 48-MHz operation with the high-speed on-chip oscillator clock (fIH)) <sup>Note 5</sup> 0.03125 μs (PLL clock: fPLL = 64 MHz, fIH = 16 or 32 MHz <sup>Note 3</sup> ) 0.02083 μs (PLL clock: fPLL = 96 MHz, fIH = 24 or 48 MHz <sup>Note 4</sup> ) <sup>Note 5</sup>				
Instruction set		<ul style="list-style-type: none"> <li>• Data transfer (8/16 bits)</li> <li>• Adder and subtractor/logical operation (8/16 bits)</li> <li>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)</li> <li>• Multiplication and accumulation (16 bits × 16 bits + 32 bits)</li> <li>• Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.</li> </ul>				
FAA core		<ul style="list-style-type: none"> <li>• Multiplication: 32-bit signed × 32-bit signed → 32-bit signed</li> <li>• Results of 64-bit multiplication can be right-shifted by a desired number of bits.</li> <li>• Addition: 32-bit signed + 32-bit signed → 32-bit signed (internally calculated with 33-bit precision)</li> <li>• Subtraction: 32-bit signed - 32-bit signed → 32-bit signed (internally calculated with 33-bit precision)</li> <li>• Limit operation: Operation parameter registers (33 bits × 4) in which upper and lower limits can be set.</li> <li>• Operation parameter registers (32 bits × 6)</li> <li>• Address pointer registers (12 bits × 6)</li> <li>• On-chip code RAM: 4 Kbytes</li> <li>• On-chip data RAM: 2 Kbytes</li> <li>• Multiple interrupts available</li> <li>• A 32-byte shared memory is included for sharing of data by the RL78 CPU and FAA core.</li> </ul>				

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Item		40-pin	44-pin	48-pin	52-pin	64-pin
		R7F101GEx	R7F101GFx	R7F101GGx	R7F101GJx	R7F101GLx
I/O port	Total number of pins	36	40	44	48	58
	CMOS I/O	31 (N-ch open drain I/O [withstand voltage of VDD]: 14)	35 (N-ch open drain I/O [withstand voltage of VDD]: 14)	38 (N-ch open drain I/O [withstand voltage of VDD]: 15)	42 (N-ch open drain I/O [withstand voltage of VDD]: 17)	52 (N-ch open drain I/O [withstand voltage of VDD]: 19)
	CMOS input	3				
	CMOS output	—			1	
	N-ch open drain I/O (withstand voltage: 6 V)	2				
	Controlled current drive port	7	8			
Timers	16-bit timers TAU, timer RJ, timer RD2, timer RX, timer RG2	9 channels in total: 4-channel timer array unit (TAU) 1-channel timer RJ 2-channel timer RD2 with PWMOPA 1-channel timer RG2 1-channel timer RX				
	16-bit timer Timer KB3	3 channels (PWM outputs: 6)				
	Watchdog timer	1 channel				
	Realtime clock (RTC)	1 channel				
	32-bit interval timer (TML32)	1 channel in 32-bit counter mode, 2 channels in 16-bit counter mode, 4 channels in 8-bit counter mode				
	Timer outputs	17 (PWM outputs: 14 <sup>Note 6</sup> ), 22 (PWM outputs: 14 <sup>Note 6</sup> ) <sup>Note 7</sup>				
	RTC output	1				
Clock output/buzzer output		2				
		<ul style="list-style-type: none"> <li>• 3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (Main system clock: f<sub>MAIN</sub> = 32 MHz)</li> <li>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Low-speed peripheral clock: f<sub>SXP</sub> = 32.768 kHz)</li> </ul>				
8-/10-/12-bit resolution A/D converter		19 channels	21 channels		23 channels	
	3-channel simultaneous sampling	2 channels				
8-/10-bit D/A converter		2 to 3 channels				
	DAC outputs (ANOx)	3				
Programmable gain amplifier (PGA)		1 channel				
Comparator module		4 channels				

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Item	40-pin	44-pin	48-pin	52-pin	64-pin
	R7F101GEx	R7F101GFx	R7F101GGx	R7F101GJx	R7F101GLx
Serial interfaces	[40- and 44-pin products] <ul style="list-style-type: none"> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART (UART supporting LIN-bus): 1 channel</li> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> <li>• Simplified SPI (CSI): 2 channels, simplified I<sup>2</sup>C: 2 channels, UART: 1 channel</li> </ul> [48- and 52-pin products] <ul style="list-style-type: none"> <li>• Simplified SPI (CSI): 2 channels, simplified I<sup>2</sup>C: 2 channels, UART (UART supporting LIN-bus): 1 channel</li> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> <li>• Simplified SPI (CSI): 2 channels, simplified I<sup>2</sup>C: 2 channels, UART: 1 channel</li> </ul> [64-pin products] <ul style="list-style-type: none"> <li>• Simplified SPI (CSI): 2 channels, simplified I<sup>2</sup>C: 2 channels, UART (UART supporting LIN-bus): 1 channel</li> <li>• Simplified SPI (CSI): 2 channels, simplified I<sup>2</sup>C: 2 channels, UART: 1 channel</li> <li>• Simplified SPI (CSI): 2 channels, simplified I<sup>2</sup>C: 2 channels, UART: 1 channel</li> </ul>				
	I <sup>2</sup> C bus	1			
	I <sup>2</sup> C (SM/PM) bus	1			
	DALI	1			
Data transfer controller (DTC)	53 sources				
Vectored interrupt sources	Internal	55			
	External	13	15		
Key interrupt	4		6	8	
Reset	<ul style="list-style-type: none"> <li>• Reset by <math>\overline{\text{RESET}}</math> pin</li> <li>• Internal reset by watchdog timer</li> <li>• Internal reset by power-on-reset</li> <li>• Internal reset by voltage detectors (LVD0 and LVD1)</li> <li>• Internal reset by illegal instruction execution<sup>Note 8</sup></li> <li>• Internal reset by RAM parity error</li> <li>• Internal reset by illegal-memory access</li> </ul>				
Power-on-reset circuit	<ul style="list-style-type: none"> <li>• Power-on reset: 1.51 V (typ.)</li> <li>• Power-down reset: 1.50 V (typ.)</li> </ul>				
Voltage detector	LVD0	Detection voltage <ul style="list-style-type: none"> <li>• Rising edge: 1.69 to 3.96 V (6 stages)</li> <li>• Falling edge: 1.65 to 3.88 V (6 stages)</li> </ul>			
	LVD1	Detection voltage <ul style="list-style-type: none"> <li>• Rising edge: 1.67 to 4.16 V (18 stages)</li> <li>• Falling edge: 1.63 to 4.08 V (18 stages)</li> </ul>			
On-chip debugging	Available (tracing supported)				
Power supply voltage	V <sub>DD</sub> = 1.6 to 5.5 V (2D: Consumer applications, 3C: Industrial applications) V <sub>DD</sub> = 2.7 to 5.5 V (4C: Industrial applications)				
Operating ambient temperature	T <sub>A</sub> = -40 to +85°C (2D: Consumer applications), T <sub>A</sub> = -40 to +105°C (3C: Industrial applications), T <sub>A</sub> = -40 to +125°C (4C: Industrial applications)				

**Note 1.** Overwrite the flash memory during operation at a frequency of no higher than 2 MHz.

**Note 2.** When the flash memory is to be overwritten, switch to HS (high-speed main) mode or LS (low-speed main) mode.

**Note 3.** Applicable when the PLL clock frequency is 64 MHz. Select f<sub>PLL/2</sub> (32 MHz) or f<sub>PLL/4</sub> (16 MHz) as the system clock.

**Note 4.** Applicable when the PLL clock frequency is 96 MHz. Select f<sub>PLL/2</sub> (32 MHz) or f<sub>PLL/4</sub> (16 MHz) as the system clock.

**Note 5.** This applies when the prefetch buffer is enabled. For details on the operation of the prefetch buffer, refer to **Section 8 Operation State Control** in the RL78/G24 User's Manual.

**Note 6.** The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). For details, see **10.9.3 Operation for the multiple PWM output function** in the RL78/G24 User's Manual.

**Note 7.** This applies when the setting of the PIOR0 bit is 1.

**Note 8.** In normal operation, executing the instruction code FFH triggers an internal reset, but this is not the case during emulation by the in-circuit emulator or on-chip debugging emulator.

## 2. Electrical Characteristics (TA = -40 to +105°C)

This section describes the electrical characteristics of the following types of products.

- 2D: Consumer applications, TA = -40 to +85°C  
R7F101Gxx2Dxx
- 3C: Industrial applications, TA = -40 to +105°C  
R7F101Gxx3Cxx
- 4C: Industrial applications, products of TA = -40 to +125°C, but under the condition TA = -40 to +105°C  
R7F101Gxx4Cxx

**Caution 1. RL78 microcontrollers have on-chip debugging functionality for use in the development and evaluation of user systems. Do not use on-chip debugging with products designated as part of mass production, because using this function may cause the guaranteed number of times the flash memory is rewritten to be exceeded, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when on-chip debugging is used with products designated as part of mass production.**

**Caution 2. For the consumer application products (2D), the ambient operating temperature of TA = -40°C to +85°C applies.**

**Caution 3. For products that do not have an EVDD0 or EVSS0 pin, read EVDD0 as VDD, and EVSS0 as VSS.**

**Caution 4. The present pins differ depending on the products. For details, see 2.1 Functions of Port Pins through 2.2.1 Functions for each product in the RL78/G24 User's Manual.**

## 2.1 Absolute Maximum Ratings

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Item	Symbols	Conditions	Ratings	Unit
Supply voltage	VDD		-0.5 to +6.5	V
	EVDD0		-0.5 to +6.5	V
	EVSS0		-0.5 to +0.3	V
REGC pin input voltage	VIREGC	REGC	-0.3 to +2.1 and -0.3 to VDD + 0.3 <sup>Note 1</sup>	V
Input voltage	Vi1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P140, P141, P146, P147	-0.3 to EVDD0 + 0.3 and -0.3 to VDD + 0.3 <sup>Note 2</sup>	V
	Vi2	P60, P61 (N-ch open drain)	-0.3 to +6.5	V
	Vi3	P20 to P27, P121 to P124, P137, EXCLK, EXCLKS, RESET	-0.3 to VDD + 0.3 <sup>Note 2</sup>	V
Output voltage	Vo1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147	-0.3 to EVDD0 + 0.3 and -0.3 to VDD + 0.3 <sup>Note 2</sup>	V
	Vo2	P20 to P27, P121, P122	-0.3 to VDD + 0.3 <sup>Note 2</sup>	V
Analog input voltage	VAI1	ANI16 to ANI30	-0.3 to EVDD0 + 0.3 and -0.3 to AVREFP + 0.3 <b>Notes 2, 3</b>	V
	VAI2	ANI0 to ANI7	-0.3 to VDD + 0.3 and -0.3 to AVREFP + 0.3 <b>Notes 2, 3</b>	V

**Note 1.** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). The listed value is the absolute maximum rating of the REGC pin. Do not apply a specific voltage to this pin.

**Note 2.** This voltage must be no higher than 6.5 V.

**Note 3.** The voltage on a pin in use for A/D conversion must not exceed AVREFP + 0.3.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark 1.** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

**Remark 2.** AVREFP refers to the positive reference voltage of the A/D converter.

**Remark 3.** The reference voltage is Vss.

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Item	Symbols	Conditions		Ratings	Unit
High-level output current	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P62, P63, P70 to P77, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P121, P122	-5	mA
		Total of all pins		-20	mA
	Low-level output current	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147	40
Total of all pins 170 mA			P00 to P04, P40 to P43, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77, P146, P147	100	mA
IOL2		Per pin	P20 to P27, P121, P122	10	mA
		Total of all pins		20	mA
Ambient operating temperature		TA	In normal operation mode	3C: Industrial applications	-40 to +105
	2D: Consumer applications			-40 to +85	°C
	In flash memory programming mode		3C: Industrial applications	-40 to +105	°C
			2D: Consumer applications	-40 to +85	°C
Storage temperature	T <sub>stg</sub>			-65 to +150	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

## 2.2 Characteristics of the Oscillators

### 2.2.1 Characteristics of the X1 and XT1 oscillators

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V (20- to 32-pin products), 1.6 V ≤ VDD ≤ 5.5 V (40- to 64-pin products), VSS = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time <sup>Note</sup>	Ceramic resonator/ crystal resonator		0.05		1	μs
XT1 clock oscillation frequency (f <sub>XT</sub> ) <sup>Note</sup>	Crystal resonator			32.768		kHz

**Note** The listed time and frequency indicate permissible ranges of the oscillators. For actual applications, request the resonator manufacturer for evaluation of the resonators on the oscillator circuit mounted on a board so you can use appropriate values. Refer to **2.4 AC Characteristics** for instruction execution time.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Sufficiently evaluate the oscillation stabilization time with the resonator to be used, and then specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS).



## 2.2.2 Characteristics of the on-chip oscillators

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f <sub>ih</sub>				1		48	MHz
High-speed on-chip oscillator clock frequency accuracy <sup>Note 1</sup>		HIPREC = 1	+85 to +105°C	1.8 V ≤ VDD ≤ 5.5 V	-1.5		+1.5	%
				1.6 V ≤ VDD ≤ 5.5 V	-6.0		+6.0	%
			-20 to +85°C	1.8 V ≤ VDD ≤ 5.5 V	-1.0		+1.0	%
				1.6 V ≤ VDD ≤ 5.5 V	-5.0		+5.0	%
			-40 to -20°C	1.8 V ≤ VDD ≤ 5.5 V	-1.5		+1.5	%
				1.6 V ≤ VDD ≤ 5.5 V	-5.5		+5.5	%
		HIPREC = 0 <sup>Note 4</sup>			-15		0	%
High-speed on-chip oscillator clock correction resolution						0.05		%
Middle-speed on-chip oscillator clock frequency <sup>Note 2</sup>	f <sub>im</sub>				1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy <sup>Note 1</sup>					-12		+12	%
Middle-speed on-chip oscillator clock correction resolution						0.15		%
Middle-speed on-chip oscillator frequency temperature coefficient							±0.17 <sup>Note 3</sup>	%/°C
Low-speed on-chip oscillator clock frequency <sup>Note 2</sup>	f <sub>il</sub>					32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy <sup>Note 1</sup>					-15		+15	%
Low-speed on-chip oscillator clock correction resolution						0.3		%
Low-speed on-chip oscillator frequency temperature coefficient							±0.21 <sup>Note 3</sup>	%/°C

**Note 1.** The accuracy values were obtained in testing of this product.

**Note 2.** The listed values only indicate the characteristics of the oscillators. Refer to **2.4 AC Characteristics** for instruction execution time.

**Note 3.** These values were obtained in the evaluation.

**Note 4.** This condition applies when the setting of the FRQSEL3 bit is 1.

### 2.2.3 Characteristics of the PLL oscillator

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
PLL input frequency	f <sub>PLLIN</sub>	High-speed system clock (f <sub>MX</sub> ) or high-speed on-chip oscillator clock (f <sub>IH</sub> )		8		MHz
PLL output frequency	f <sub>PLL</sub>	f <sub>PLLIN</sub> × 12		96		MHz
		f <sub>PLLIN</sub> × 8		64		MHz
Lock-up wait time		Wait time after PLL output is enabled until the output frequency is stabilized	50			μs
Interval wait time		Wait time after PLL stop until PLL operation is set again	4			μs
Setting wait time		Required wait time after the PLL input clock is stabilized and the PLL setting is determined until startup settings are made	1			μs

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit		
Allowable high-level output current <b>Note 1</b>	IOH1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70-P77, P120, P130, P140, P141, P146, P147	1.6 V ≤ EVDD0 ≤ 5.5 V			-10.0 <b>Note 2</b>	mA	
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (when duty ≤ 70% <b>Note 3</b> )	4.0 V ≤ EVDD0 ≤ 5.5 V			-55.0 <b>Note 4</b>	mA	
			2.7 V ≤ EVDD0 < 4.0 V			-10.0	mA	
			1.8 V ≤ EVDD0 < 2.7 V			-5.0	mA	
			1.6 V ≤ EVDD0 < 1.8 V			-2.5	mA	
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P62, P63, P70 to P77, P146, P147 (when duty ≤ 70% <b>Note 3</b> )	4.0 V ≤ EVDD0 ≤ 5.5 V			-80.0 <b>Note 5</b>	mA	
			2.7 V ≤ EVDD0 < 4.0 V			-19.0 <b>Note 7</b>	mA	
			1.8 V ≤ EVDD0 < 2.7 V			-10.0	mA	
			1.6 V ≤ EVDD0 < 1.8 V			-5.0	mA	
		Total of all pins (when duty ≤ 70% <b>Note 3</b> )	1.6 V ≤ EVDD0 ≤ 5.5 V			-135.0 <b>Note 6</b>	mA	
		IOH2	Per pin for P20 to P27, P121, P122	4.0 V ≤ VDD ≤ 5.5 V			-3.0 <b>Note 2</b>	mA
				2.7 V ≤ VDD < 4.0 V			-1.0 <b>Note 2</b>	mA
				1.8 V ≤ VDD < 2.7 V			-1.0 <b>Note 2</b>	mA
	1.6 V ≤ VDD < 1.8 V					-0.5 <b>Note 2</b>	mA	
	Total of all pins (when duty ≤ 70% <b>Note 3</b> )		4.0 V ≤ VDD ≤ 5.5 V			-20.0 <b>Note 8</b>	mA	
			2.7 V ≤ VDD < 4.0 V			-10.0 <b>Note 9</b>	mA	
			1.8 V ≤ VDD < 2.7 V			-5.0	mA	
			1.6 V ≤ VDD < 1.8 V			-5.0	mA	

(Notes, Caution, and Remark are listed on the next page.)

- Note 1.** Device operation is guaranteed at the listed currents even if current is flowing from the EVDD0 or VDD pin to an output pin.
- Note 2.** The combination of these and other pins must not exceed the total current value.
- Note 3.** The listed output current values apply when the duty cycle is no greater than 70%.  
Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle (%).
- Total output current from all pins =  $(I_{OH} \times 0.7)/(n \times 0.01)$   
Example when  $I_{OH} = -10.0$  mA,  $n = 80\%$   
Total output current from all pins =  $(-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7$  mA  
Note that the duty cycle has no effect on the current that is allowed to flow into a single pin.
- Note 4.** The maximum value is –30 mA in products for industrial applications (R7F101Gxx3Cxx) with an ambient operating temperature range of +85°C to +105°C.  
The maximum value is –24 mA in products for industrial applications (R7F101Gxx4Cxx) with an ambient operating temperature range of –40°C to +105°C.
- Note 5.** The maximum value is –50 mA in products for industrial applications (R7F101Gxx3Cxx) with an ambient operating temperature range of +85°C to +105°C.  
The maximum value is –42 mA in products for industrial applications (R7F101Gxx4Cxx) with an ambient operating temperature range of –40°C to +105°C.
- Note 6.** The maximum value is –60 mA with an ambient operating temperature range of +85°C to +105°C and -100 mA with an ambient operating temperature range of –40°C to +85°C in products for industrial applications (R7F101Gxx3Cxx).  
The maximum value is –54 mA in products for industrial applications (R7F101Gxx4Cxx) with an ambient operating temperature range of –40°C to +105°C.
- Note 7.** The maximum value is –17 mA in products for industrial applications (R7F101Gxx4Cxx) with an ambient operating temperature range of –40°C to +105°C.
- Note 8.** The maximum value is –14 mA in products for industrial applications (R7F101Gxx4Cxx) with an ambient operating temperature range of –40°C to +105°C.
- Note 9.** The maximum value is –8 mA in products for industrial applications (R7F101Gxx4Cxx) with an ambient operating temperature range of –40°C to +105°C.

**Caution** The following pins do not output high-level signals in the N-ch open-drain mode.  
**P00, P02 to P04, P10 to P15, P17, P30, P50, P51, P55, and P71 to P74**

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Allowable low-level output current <sup>Note 1</sup>	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147			20.0 <b>Notes 2, 8</b>	mA	
		Per pin for P60, P61			15.0 <b>Note 2</b>	mA	
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (when duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EVDD0 ≤ 5.5 V			70.0 <b>Note 4</b>	mA
			2.7 V ≤ EVDD0 < 4.0 V			15.0	mA
			1.8 V ≤ EVDD0 < 2.7 V			9.0	mA
			1.6 V ≤ EVDD0 < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P62, P63, P70 to P77, P146, P147 (when duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EVDD0 ≤ 5.5 V			80.0 <b>Note 4</b>	mA
			2.7 V ≤ EVDD0 < 4.0 V			35.0 <b>Note 6</b>	mA
			1.8 V ≤ EVDD0 < 2.7 V			20.0	mA
			1.6 V ≤ EVDD0 < 1.8 V			10.0	mA
	Total of all pins (when duty ≤ 70% <sup>Note 3</sup> )				150.0 <b>Note 5</b>	mA	
	IOL2	Per pin for P20 to P27, P121, P122	4.0 V ≤ VDD ≤ 5.5 V			8.5 <b>Note 2</b>	mA
			2.7 V ≤ VDD < 4.0 V			1.5 <b>Note 2</b>	mA
			1.8 V ≤ VDD < 2.7 V			0.6 <b>Note 2</b>	mA
			1.6 V ≤ VDD < 1.8 V			0.4 <b>Note 2</b>	mA
		Total of all pins (when duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ VDD ≤ 5.5 V			20 <b>Note 7</b>	mA
			2.7 V ≤ VDD < 4.0 V			20 <b>Note 7</b>	mA
			1.8 V ≤ VDD < 2.7 V			15.0	mA
			1.6 V ≤ VDD < 1.8 V			10.0	mA

(Notes and Remark are listed on the next page.)

- Note 1.** Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the EVSS0 or VSS pin.
- Note 2.** The combination of these and other pins must not exceed the total current value.
- Note 3.** The listed output current values apply when the duty cycle is no greater than 70%.  
Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle (%).
- Total output current from all pins =  $(I_{OH} \times 0.7)/(n \times 0.01)$   
Example when  $I_{OH} = -10.0$  mA,  $n = 80\%$   
Total output current from all pins =  $(-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7$  mA  
Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. No current higher than the absolute maximum rating must not flow into a single pin.
- Note 4.** The maximum value is 40 mA in products for industrial applications (R7F101Gxx3Cxx) with an ambient operating temperature range of +85°C to +105°C.  
The maximum value is 34 mA in products for industrial applications (R7F101Gxx4Cxx) with an ambient operating temperature range of -40°C to +105°C.
- Note 5.** The maximum value is 80 mA in products for industrial applications (R7F101Gxx3Cxx) with an ambient operating temperature range of +85°C to +105°C.  
The maximum value is 68 mA in products for industrial applications (R7F101Gxx4Cxx) with an ambient operating temperature range of -40°C to +105°C.
- Note 6.** The maximum value is 15 mA in products for industrial applications (R7F101Gxx4Cxx) with an ambient operating temperature range of -40°C to +105°C.
- Note 7.** The maximum value is 14 mA in products for industrial applications (R7F101Gxx4Cxx) with an ambient operating temperature range of -40°C to +105°C.
- Note 8.** The maximum value is 17 mA in products for industrial applications (R7F101Gxx4Cxx) with an ambient operating temperature range of -40°C to +105°C.
- Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input voltage, high	VIH1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer	0.8 EVDD0		EVDD0	V
	VIH2	P01, P03, P04, P10, P11, P14 to P17, P30, P50, P55, P73	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2		EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0		EVDD0	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	1.5		EVDD0	V
	VIH3	P20 to P27		0.7 VDD		VDD	V
	VIH4	P60, P61	I/O port mode	0.7 EVDD0		6.0	V
	VIH5	P121 to P124, P137, EXCLK, EXCLKS, RESET		0.8 VDD		VDD	V
VIH6	P60, P61	SMBus input mode 2.7 V ≤ EVDD0 ≤ 5.5 V	1.35		EVDD0	V	
Input voltage, low	UIL1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer	0		0.2 EVDD0	V
	UIL2	P01, P03, P04, P10, P11, P14 to P17, P30, P50, P55, P73	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	0		0.32	V
	UIL3	P20 to P27		0		0.3 VDD	V
	UIL4	P60, P61	I/O port mode	0		0.3 EVDD0	V
	UIL5	P121 to P124, P137, EXCLK, EXCLKS, RESET		0		0.2 VDD	V
UIL6	P60, P61	SMBus input mode 2.7 V ≤ EVDD0 ≤ 5.5 V			0.8	V	

**Caution** The maximum value of VIH of pins P00, P02 to P04, P10 to P15, P17, P30, P50, P51, P55, and P71 to P74 is EVDD0, even in the N-ch open-drain mode.

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage, high	VOH1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -10.0 mA	EVDD0 - 1.5		V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -3.0 mA	EVDD0 - 0.7		V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -2.0 mA	EVDD0 - 0.6		V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -1.5 mA	EVDD0 - 0.5		V
			1.6 V ≤ EVDD0 < 5.5 V, IOH1 = -1.0 mA	EVDD0 - 0.5		V
	VOH2	P20 to P27, P121, P122	4.0 V ≤ VDD ≤ 5.5 V, IOH2 = -3.0 mA	VDD - 0.7		V
			2.7 V ≤ VDD < 4.0 V, IOH2 = -1.0 mA	VDD - 0.5		V
			1.8 V ≤ VDD < 2.7 V, IOH2 = -1.0 mA	VDD - 0.5		V
			1.6 V ≤ VDD < 1.8 V, IOH2 = -0.5 mA	VDD - 0.5		V

**Caution** Pins P00, P02 to P04, P10 to P15, P17, P30, P50, P51, P55, P71 to P74 do not output high-level signals in the N-ch open-drain mode.

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(5/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Output voltage, low	VOL1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 20.0 mA			1.3	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 8.5 mA			0.7	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 3.0 mA			0.6	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 1.5 mA			0.4	V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 0.6 mA			0.4	V
			1.6 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 0.3 mA			0.4	V
	VOL2	P20 to P27, P121, P122	4.0 V ≤ VDD ≤ 5.5 V, IOL2 = 8.5 mA			0.7	V
			2.7 V ≤ VDD < 4.0 V, IOL2 = 1.5 mA			0.5	V
			1.8 V ≤ VDD < 2.7 V, IOL2 = 0.6 mA			0.4	V
			1.6 V ≤ VDD < 1.8 V, IOL2 = 0.4 mA			0.4	V
	VOL3	P60, P61	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 15.0 mA			2.0	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 5.0 mA			0.4	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 3.0 mA			0.4	V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 2.0 mA			0.4	V
			1.6 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 1.0 mA			0.4	V

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.



(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	
Output current <sup>Note</sup>	CCDIOL	P10, P11, P16, P17, P60 to P63	CCSm = 01H	4.0 V ≤ EVDD0 ≤ 5.5 V	1.0	1.8	2.6	mA
				2.7 V ≤ EVDD0 < 4.0 V	0.8	1.5	2.3	mA
			CCSm = 02H	4.0 V ≤ EVDD0 ≤ 5.5 V	3.0	4.9	6.5	mA
				3.0 V ≤ EVDD0 < 4.0 V	2.7	4.3	5.9	mA
			CCSm = 03H	4.0 V ≤ EVDD0 ≤ 5.5 V	6.6	10.0	13.2	mA
				3.3 V ≤ EVDD0 < 4.0 V	6.0	9.1	12.1	mA
		P60, P61	CCSm = 04H	4.0 V ≤ EVDD0 ≤ 5.5 V	10.2	15.0	19.8	mA
				3.3 V ≤ EVDD0 < 4.0 V	9.4	13.8	18.2	mA

**Note** The listed currents apply when the output current control function is enabled.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(7/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input leakage current, high	ILI1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P140, P141, P146, P147	VI = EVDD0			1	μA
	ILI2	P20 to P27, P137, RESET	VI = VDD			1	μA
	ILI3	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	VI = VDD			1	μA
Input leakage current, low	ILIL1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147	VI = EVSS0			1	μA
	ILIL2	P20 to P27, P137, RESET	VI = VSS			1	μA
	ILIL3	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	VI = VSS			1	μA
On-chip pull-up resistance	RU	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120 to P122, P140, P141, P146, P147	VI = EVSS0, input port	10	20	100	kΩ

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

## 2.3.2 Supply current characteristics

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/5)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f <sub>PLL</sub> = 96 MHz f <sub>CLK</sub> = 48 MHz (MCM0 = 0)Note 2	Normal operation	VDD = 5.0 V	5.5	17.6	mA
						VDD = 2.4 V	5.5	17.6	
				f <sub>PLL</sub> = 96 MHz f <sub>CLK</sub> = 48 MHz (MCM = 1)Note 4	Normal operation	VDD = 5.0 V	5.3	17.4	mA
						VDD = 2.4 V	5.3	17.4	
				f <sub>IH</sub> = 48 MHzNote 2	Normal operation	VDD = 5.0 V	4.6	11.9	mA
						VDD = 2.4 V	4.6	11.9	
				f <sub>PLL</sub> = 64 MHz f <sub>CLK</sub> = 32 MHz (MCM0 = 0)Note 2	Normal operation	VDD = 5.0 V	3.9	12.1	mA
						VDD = 1.8 V	3.9	12.1	
				f <sub>PLL</sub> = 64 MHz f <sub>CLK</sub> = 32 MHz (MCM = 1)Note 4	Normal operation	VDD = 5.0 V	3.7	11.9	mA
						VDD = 1.8 V	3.7	11.9	
				f <sub>IH</sub> = 32 MHzNote 2	Basic operation	VDD = 5.0 V	1.6	—	mA
						VDD = 1.8 V	1.6	—	
			Normal operation		VDD = 5.0 V	3.3	8.3	mA	
					VDD = 1.8 V	3.3	8.3		
			LS (low-speed main) mode	f <sub>IH</sub> = 24 MHzNote 2	Normal operation	VDD = 5.0 V	2.5	6.3	mA
						VDD = 1.8 V	2.5	6.3	
				f <sub>IH</sub> = 16 MHzNote 2	Normal operation	VDD = 5.0 V	1.8	4.4	mA
						VDD = 1.8 V	1.8	4.4	
				f <sub>IM</sub> = 4 MHzNote 3	Normal operation	VDD = 5.0 V	0.5	1.3	mA
						VDD = 1.6 V	0.5	1.3	
			LP (low-power main) mode	f <sub>IM</sub> = 2 MHzNote 3	Normal operation	VDD = 5.0 V	215	707	μA
						VDD = 1.6 V	214	706	
				f <sub>IM</sub> = 1 MHzNote 3	Normal operation	VDD = 5.0 V	120	466	μA
						VDD = 1.6 V	119	464	
HS (high-speed main) mode	f <sub>MX</sub> = 20 MHzNote 4, Square wave input	Normal operation	VDD = 5.0 V	2.0	5.2	mA			
			VDD = 1.8 V	2.0	5.2				
LS (low-speed main) mode	f <sub>MX</sub> = 20 MHzNote 4, Square wave input	Normal operation	VDD = 5.0 V	1.9	5.1	mA			
			VDD = 1.8 V	1.9	5.0				
	f <sub>MX</sub> = 20 MHzNote 4, Resonator connection	Normal operation	VDD = 5.0 V	2.1	5.3	mA			
			VDD = 1.8 V	2.1	5.3				
	f <sub>MX</sub> = 10 MHzNote 4, Square wave input	Normal operation	VDD = 5.0 V	1.0	2.7	mA			
			VDD = 1.8 V	1.0	2.7				
	f <sub>MX</sub> = 10 MHzNote 4, Resonator connection	Normal operation	VDD = 5.0 V	1.1	2.9	mA			
			VDD = 1.8 V	1.1	2.9				
	f <sub>MX</sub> = 8 MHzNote 4, Square wave input	Normal operation	VDD = 5.0 V	0.8	2.2	mA			
			VDD = 1.8 V	0.8	2.2				

(Notes and Remarks are listed on the next page.)

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	LS (low-speed main) mode	fMX = 8 MHz <sup>Note 4</sup> , Resonator connection	Normal operation	VDD = 5.0 V	0.9	2.4	mA
						VDD = 1.8 V	0.9	2.4	

**Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The currents in the Typ. column do not include the peripheral operating current in the HS (high-speed main), LS (low-speed main), or LV (low-voltage main) mode. The currents in the Max. column include the peripheral operating current, but do not include those of the FAA, A/D converter, sample & hold circuit, D/A converter, PGA, comparator, TRNG, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing when the data flash memory is being rewritten.

**Note 2.** The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

**Note 3.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

**Note 4.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

**Remark 1.** f<sub>ih</sub>: High-speed on-chip oscillator clock frequency

**Remark 2.** f<sub>im</sub>: Middle-speed on-chip oscillator clock frequency

**Remark 3.** f<sub>mx</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 4.** f<sub>pll</sub>: PLL clock frequency (up to 96 MHz)

**Remark 5.** f<sub>clk</sub>: CPU/peripheral hardware clock frequency

**Remark 6.** The typical value for the ambient operating temperature (TA) is 25°C unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	Subsystem clock operation mode	fsUB = 32.768 kHz <sup>Note 2</sup> , Low-speed on-chip oscillator operation	Normal operation	TA = -40°C		3.9	16.8	μA
						TA = +25°C		4.7	17.4	
						TA = +50°C		6.3	30.9	
						TA = +70°C		9.7	52.3	
						TA = +85°C		15.3	83.2	
						TA = +105°C		30.6	177.3	
				fsUB = 32.768 kHz <sup>Note 3</sup> , Square wave input	Normal operation	TA = -40°C		3.5	16.3	μA
						TA = +25°C		4.9	22.0	
						TA = +50°C		5.9	31.7	
						TA = +70°C		9.2	53.9	
						TA = +85°C		14.7	81.8	
				fsUB = 32.768 kHz <sup>Note 3</sup> , Resonator connection	Normal operation	TA = -40°C		3.6	13.4	μA
						TA = +25°C		4.3	14.1	
						TA = +50°C		5.8	27.2	
						TA = +70°C		9.2	50.0	
TA = +85°C		14.9	79.7							
				TA = +105°C		30.0	174.3			

**Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The currents in the Typ. and Max. columns do not include the peripheral operating current when the CPU is operating with the sub-system clock.

**Note 2.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

**Note 3.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 11B). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

**Remark 1.** fil: Low-speed on-chip oscillator clock frequency

**Remark 2.** fsUB: Subsystem clock frequency (XT1 clock oscillation frequency)

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions				Min.	Typ.	Max.	Unit	
Supply current <b>Note 1</b>	<b>IDD2</b> <b>Note 2</b>	HALT mode	HS (high-speed main) mode	f <sub>PLL</sub> = 96 MHz f <sub>CLK</sub> = 48 MHz (MCM0 = 0) <b>Note 2</b>	VDD = 5.0 V		1.57	12.84	mA	
					VDD = 2.4 V		1.57	12.84		
				f <sub>PLL</sub> = 96 MHz f <sub>CLK</sub> = 48 MHz (MCM = 1) <b>Note 4</b>	VDD = 5.0 V		1.39	12.62	mA	
					VDD = 2.4 V		1.39	12.62		
				f <sub>IH</sub> = 48 MHz <b>Note 2</b>	VDD = 5.0 V		0.73	7.13	mA	
					VDD = 2.4 V		0.73	7.12		
				f <sub>PLL</sub> = 64 MHz f <sub>CLK</sub> = 32 MHz (MCM0 = 0) <b>Note 2</b>	VDD = 5.0 V		1.19	8.79	mA	
					VDD = 1.8 V		1.18	8.78		
				f <sub>PLL</sub> = 64 MHz f <sub>CLK</sub> = 32 MHz (MCM = 1) <b>Note 4</b>	VDD = 5.0 V		1.01	8.58	mA	
					VDD = 1.8 V		0.99	8.56		
				f <sub>IH</sub> = 32 MHz <b>Note 3</b>	VDD = 5.0 V		0.62	4.98	mA	
					VDD = 1.8 V		0.61	4.96		
				LS (low-speed main) mode	f <sub>IH</sub> = 24 MHz <b>Note 3</b>	VDD = 5.0 V		0.51	3.83	mA
						VDD = 1.8 V		0.50	3.82	
			f <sub>IH</sub> = 16 MHz <b>Note 3</b>		VDD = 5.0 V		0.48	2.79	mA	
					VDD = 1.8 V		0.47	2.78		
			f <sub>IM</sub> = 4 MHz <b>Note 4</b>		VDD = 5.0 V		0.10	0.82	mA	
					VDD = 1.6 V		0.09	0.81		
			LP (low-power main) mode	f <sub>IM</sub> = 2 MHz <b>Note 4</b>	VDD = 5.0 V		39	493	μA	
					VDD = 1.6 V		40	494		
				f <sub>IM</sub> = 1 MHz <b>Note 4</b>	VDD = 5.0 V		32	358	μA	
					VDD = 1.6 V		31	357		
			HS (high-speed main) mode	f <sub>MX</sub> = 20 MHz <b>Note 5</b> , Square wave input	VDD = 5.0 V		0.25	3.02	mA	
					VDD = 1.8 V		0.23	2.99		
			LS (low-speed main) mode	f <sub>MX</sub> = 20 MHz <b>Note 5</b> , Square wave input	VDD = 5.0 V		0.26	3.03	mA	
					VDD = 1.8 V		0.23	2.99		
				f <sub>MX</sub> = 20 MHz <b>Note 5</b> , Resonator connection	VDD = 5.0 V		0.44	3.25	mA	
					VDD = 1.8 V		0.43	3.23		
f <sub>MX</sub> = 10 MHz <b>Note 5</b> , Square wave input	VDD = 5.0 V			0.16	1.65	mA				
	VDD = 1.8 V			0.13	1.62					
f <sub>MX</sub> = 10 MHz <b>Note 5</b> , Resonator connection	VDD = 5.0 V			0.30	1.82	mA				
	VDD = 1.8 V			0.29	1.81					
f <sub>MX</sub> = 8 MHz <b>Note 5</b> , Square wave input	VDD = 5.0 V			0.14	1.37	mA				
	VDD = 1.8 V			0.12	1.35					
f <sub>MX</sub> = 8 MHz <b>Note 5</b> , Resonator connection	VDD = 5.0 V		0.23	1.49	mA					
	VDD = 1.8 V		0.22	1.47						

(Notes and Remarks are listed on the next page.)

- Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The currents in the Typ. column do not include the peripheral operating current when the CPU is placed in the HS (high-speed main), LS (low-speed main), or LV (low-voltage main) mode. The currents in the Max. column include the peripheral operating current, but do not include those of the FAA, A/D converter, sample & hold circuit, D/A converter, PGA, comparator, TRNG, LVD circuit, I/O port, and on-chip pull-up-/pull-down resistors, and those flowing when the data flash memory is being rewritten. The currents in the Max. column include that of the RTC when the CPU is placed in the HALT mode.
- Note 2.** The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.
- Note 3.** The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
- Note 4.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.
- Note 5.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
- Remark 1.** f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
- Remark 2.** f<sub>IM</sub>: Middle-speed on-chip oscillator clock frequency
- Remark 3.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 4.** f<sub>PLL</sub>: PLL clock frequency (up to 96 MHz)
- Remark 5.** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency
- Remark 6.** The typical value for the ambient operating temperature (TA) is 25°C unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions			Min.	Typ.	Max.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	Subsystem clock operation mode	fSUB = 32.768 kHz Note 3, Low-speed on-chip oscillator operation	TA = -40°C		0.97	12.31	μA
					TA = +25°C		1.55	12.61	
					TA = +50°C		2.80	25.50	
					TA = +70°C		5.54	45.88	
					TA = +85°C		10.41	75.70	
					TA = +105°C		23.12	165.88	
				fSUB = 32.768 kHz, Square wave input Note 4	TA = -40°C		0.27	11.34	μA
					TA = +25°C		1.48	16.73	
					TA = +50°C		2.19	26.04	
					TA = +70°C		4.93	47.32	
					TA = +85°C		9.37	73.70	
					TA = +105°C		22.71	168.71	
				fSUB = 32.768 kHz, Resonator connection Note 5	TA = -40°C		0.40	8.83	μA
					TA = +25°C		0.94	9.53	
					TA = +50°C		2.16	22.41	
					TA = +70°C		4.91	43.76	
					TA = +85°C		9.71	72.66	
					TA = +105°C		22.43	163.33	
IDD3	STOP mode	Realtime clock stopped Note 6	TA = -40°C		0.16	10.00	μA		
			TA = +25°C		0.63	10.00			
			TA = +50°C		1.80	20.00			
			TA = +70°C		4.30	40.00			
			TA = +85°C		9.30	70.00			
			TA = +105°C		22.00	160.00			
			128-Hz realtime clock operation Note 7	TA = -40°C		0.24	11.00	μA	
				TA = +25°C		0.71	11.00		
				TA = +50°C		1.95	22.00		
				TA = +70°C		4.60	45.00		
				TA = +85°C		9.50	80.00		
				TA = +105°C		23.00	170.00		

(Notes and Remarks are listed on the next page.)

- Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The currents in the Typ. and Max. columns do not include the peripheral operating current when the CPU is operating with the sub-system clock, or when the CPU is placed in the STOP mode, but include that of the RTC when in the HALT mode.
- Note 2.** The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.
- Note 3.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped, including the current flowing into the RTC. They do not include the currents flowing into the 32-bit interval timer and watchdog timer.
- Note 4.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, including the current flowing into the RTC. They do not include the currents flowing into the 32-bit interval timer and watchdog timer.
- Note 5.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and when RTCLPC is set to 1 and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 11B), including the current flowing into the RTC. They do not include the currents flowing into the 32-bit interval timer and watchdog timer.
- Note 6.** The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. They do not include the currents flowing into the RTC, 32-bit interval timer and watchdog timer. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.
- Note 7.** The listed currents apply when the low-speed on-chip oscillator is stopped, and when RTCLPC is set to 1 and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 11B), including the current flowing into the RTC. They do not include the currents flowing into the 32-bit interval timer and watchdog timer.

**Remark 1.** f<sub>L</sub>: Low-speed on-chip oscillator clock frequency

**Remark 2.** f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)



## Peripheral Functions (Common to all products)

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	IFIH Note 1	HIPREC = 0			380	—	μA
		HIPREC = 1			240	—	μA
Middle-speed on-chip oscillator operating current	IFIM Note 1				20	—	μA
Low-speed on-chip oscillator operating current	IFIL Note 1				0.3	—	μA
RTC operating current	IRTC Notes 1, 2, 3	fRTCCLK = 32.768 kHz			0.005	—	μA
		fRTCCLK = 128 Hz			0.002	—	μA
32-bit interval timer operating current	IIT Notes 1, 2, 4				0.04	—	μA
Watchdog timer operating current	IWDT Notes 1, 2, 5	fil = 32.768 kHz (typ.)			0.32	—	μA
A/D converter operating current	IADC Notes 1, 6	Conversion at maximum speed	Normal mode, AVREFP = VDD = 5.0 V		0.95	1.6	mA
			Low-voltage mode, AVREFP = VDD = 3.0 V		0.54	0.81	mA
AVREFP current	IADREF Note 7	AVREFP = 5.0 V			60	—	μA
A/D converter internal reference voltage current	IADREF Note 1				114	—	μA
Temperature sensor operating current	ITMPS Note 1				110	—	μA
D/A converter operating current	IDAC Notes 1, 8	Per channel	10-bit DAC, VDD = 5.0 V		223	—	μA
			8-bit DAC, VDD = 5.0 V		120	—	μA
Comparator operating current	ICMP Notes 1, 9	Per channel			100	—	μA
PGA operating current	IPGA Notes 1, 10				460	—	μA
Sample & hold circuit operating current	ISH Notes 1, 11	Per channel			800	—	μA
LVD operating current	ILVD0 Notes 1, 12				0.03	—	μA
	ILVD1 Notes 1, 12				0.03	—	μA
FAA operating current	IFAA Notes 1, 13	fCLK = 48 MHz			11.0	—	mA
		fCLK = 32 MHz			7.3	—	mA
True random number generator operating current	ITRNG				1.6	—	mA
SMBus operating current	ISMBUS				250	—	μA
Self-programming operating current	IFSP Notes 1, 14				2.5	12.2	mA
Data flash rewrite operating current	IBGO Notes 1, 15				2.5	12.2	mA

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(Notes and Remarks are listed on the next page.)

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
SNOOZE operating current	ISNOZ <b>Note 1</b>	ADC to be in use	The ADC is shifting to the SNOOZE mode. <b>Note 16</b>		0.7	1.2	mA
			The ADC is operating in the low-voltage mode, AVREFF = VDD = 3.0 V		1.2	2.0	
		Simplified SPI (CSI)/UART to be in use			0.7	1.07	
Low-speed peripheral clock supply current	ISXP <b>Notes 1, 17</b>	RTCLPC = 0			0.27	—	μA
Output current control operating current	ICCDA <b>Notes 1, 18</b>	The setting of the CCDE register is not 00H.			100	—	μA
		ICCDP <b>Notes 19, 20</b>	Per single controlled current drive port	Low-level output current setting: Hi-Z		30	—
	Low-level output current setting: 2 to 15 mA				210	—	μA

**Note 1.** This current flows into VDD.

**Note 2.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.

**Note 3.** This current only flows to the realtime clock (RTC). It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and IRTC when the realtime clock is operating in the operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be included in the supply current. IDD2 in the subsystem clock operation mode includes the operating current of the realtime clock.

**Note 4.** This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and IIT when the 32-bit interval timer is operating or in the HALT mode.

**Note 5.** This current only flows to the watchdog timer. It includes the operating current of the low-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3, and IWDT when the watchdog timer is operating.

**Note 6.** This current only flows to the A/D converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and IADC when the A/D converter is operating or in the HALT mode.

**Note 7.** This current flows into AVREFF.

**Note 8.** This current only flows to the D/A converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and IDAC when the D/A converter is operating.

**Note 9.** This current only flows to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3, and ICMP when the comparator circuit is operating.

**Note 10.** This current only flows to the PGA circuit. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and IPGA when the PGA circuit is operating.

**Note 11.** This current only flows to the sample & hold circuit. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and ISH when the sample & hold circuit is operating.

**Note 12.** This current only flows to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3, and ILVD when the LVD circuit is operating.

**Note 13.** This current only flows to the FAA circuit. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and IFAA when the FAA circuit is operating.

**Note 14.** This current only flows during self-programming.

**Note 15.** This current only flows while the data flash memory is being rewritten.

**Note 16.** For shift time to the SNOOZE mode, see **20.9 SNOOZE Mode Function** in the RL78/G24 User's Manual.

**Note 17.** This current is added to the supply current in the STOP mode when the setting of RTCLPC is 0 with the subsystem clock X (fsx) oscillating, or in the HALT mode when the setting of RTCLPC is 0 with the subsystem clock X (fsx) selected as the CPU clock.

**Note 18.** This current is added to the supply current when the controlled current drive port is set.

**Note 19.** This current does not include the current flowing into the I/O ports.

**Note 20.** This current flows into EVDD0 and EVDD1.

**Remark 1.** fIL: Low-speed on-chip oscillator clock frequency

**Remark 2.** fsx: Subsystem clock X frequency

**Remark 3.** fCLK: CPU/peripheral hardware clock frequency

**Remark 4.** The typical value for the ambient operating temperature is 25°C.

## 2.4 AC Characteristics

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	
Instruction cycle	TCY	Main system clock (fMAIN) operation	HS (high-speed main) mode (Prefetch ON)	2.4 V ≤ VDD ≤ 5.5 V	0.02083		1	μs
			HS (high-speed main) mode (Prefetch OFF)	1.8 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ VDD ≤ 1.8 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.04167		1	μs
		1.6 V ≤ VDD ≤ 1.8 V		0.25		1	μs	
		LP (low-power main) mode	1.6 V ≤ VDD ≤ 5.5 V	0.5		1	μs	
		Subsystem clock (fSUB) operation	1.8 V ≤ VDD ≤ 5.5 V	26.041	30.5	31.3	μs	
Self-programming mode		HS (high-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.03125		1	μs	
			2.4 V ≤ VDD ≤ 5.5 V	0.02083		1	μs	
		LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.04167		1	μs	
External system clock frequency	fEX	1.8 V ≤ VDD ≤ 5.5 V		1.0		20.0	MHz	
		1.6 V ≤ VDD < 1.8 V		1.0		4.0	MHz	
	fEXS			32		38.4	kHz	
External system clock input high-level width, low-level width	tEXH, tEXL	1.8 V ≤ VDD ≤ 5.5 V		24			ns	
		1.6 V ≤ VDD < 1.8 V		120			ns	
	tEXHS, tEXLS			13.7			μs	
Ti00 to Ti03 input high-level width, low-level width	tTIH, tTIL			1/fMCK + 10			ns Note	
Timer RJ input cycle	tc	TRJIO	2.7 V ≤ EVDD0 ≤ 4.0 V	100			ns	
			1.8 V ≤ EVDD0 ≤ 2.7 V	300			ns	
			1.6 V ≤ EVDD0 ≤ 1.8 V	500			ns	
Timer RJ input high-level width, low-level width	tTJIH, tTJIL	TRJIO	2.7 V ≤ EVDD0 ≤ 4.0 V	40			ns	
			1.8 V ≤ EVDD0 ≤ 2.7 V	120			ns	
			1.6 V ≤ EVDD0 ≤ 1.8 V	200			ns	
Timer RD2 input high-level width, low-level width	tTDIH, tTDIL	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/fCLK			ns	
Timer RD2 forcible shut-off signal input low-level width	tTDSIL	P137/INTP0	2 MHz ≤ fCLK ≤ 48 MHz	1			μs	
			fCLK ≤ 2 MHz	1/fCLK + 1			μs	

(Note and Remark are listed on the next page.)

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(2/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Timer RG2 input high-level width, low-level width	tTGIH, tTGIL	TRGIOA, TRGIOB, TRGIDZ, TRGTRG		2.5/fCLK			ns
TO00 to TO03 TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TRJIO0, TRJIO1, TRGIOA, TRGIOB, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 output frequency	fTO	HS (high-speed main) mode LS (low-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
			2.7 V ≤ EVDD0 < 4.0 V			8	MHz
			1.8 V ≤ EVDD0 < 2.7 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
		LP (low-power main) mode	1.6 V ≤ EVDD0 ≤ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	fPCL	HS (high-speed main) mode LS (low-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
			2.7 V ≤ EVDD0 < 4.0 V			8	MHz
			1.8 V ≤ EVDD0 < 2.7 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
		LP (low-power main) mode	1.6 V ≤ EVDD0 < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0, INTP20, INTP21	1.6 V ≤ VDD ≤ 5.5 V	1			μs
		INTP1 to INTP11	1.6 V ≤ EVDD0 ≤ 5.5 V	1			μs
Key interrupt input high-level width, low-level width	tKRH, tKRL	KR0 to KR7	1.8 V ≤ EVDD0 ≤ 5.5 V	250			ns
			1.6 V ≤ EVDD0 < 1.8 V	1			μs
RESET low-level width	tRSL			10			μs

**Note** The following conditions are required for low-voltage interface when EVDD0 < VDD.

1.8 V ≤ EVDD0 < 2.7 V: 125 ns (min.)

1.6 V ≤ EVDD0 < 1.8 V: 250 ns (min.)

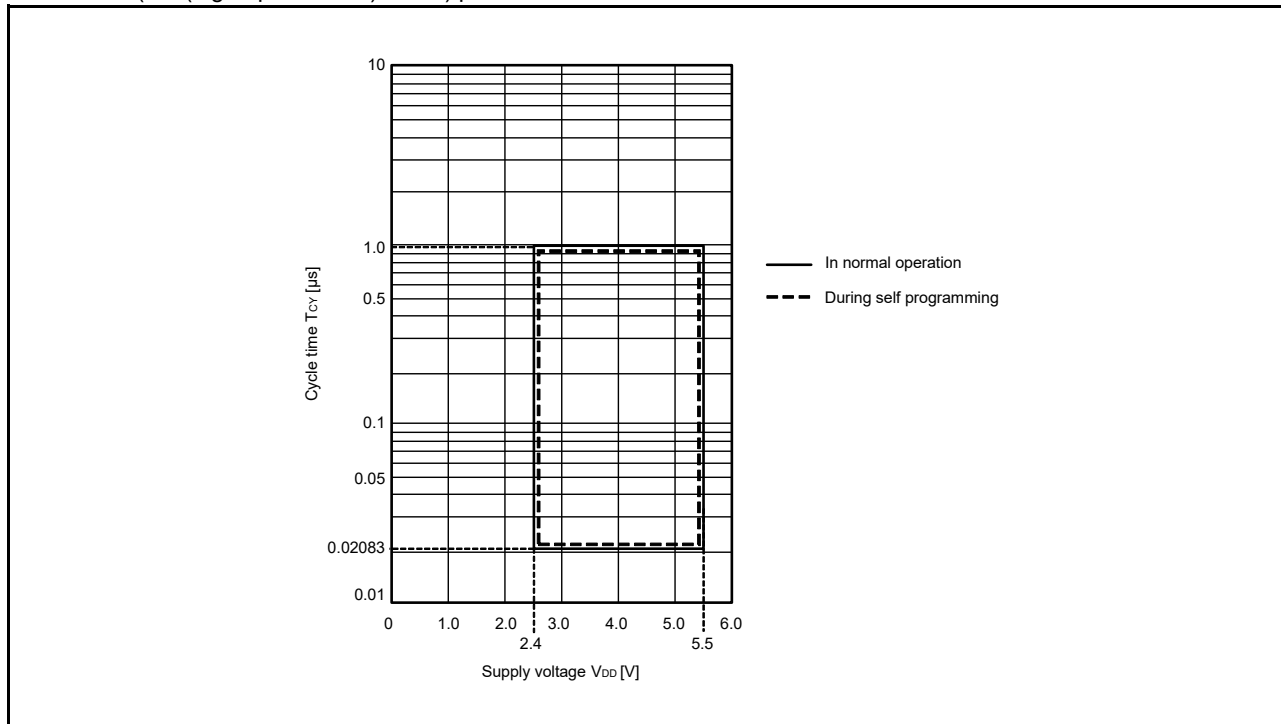
**Remark** fMCK: Timer array unit operating clock frequency

To set this operating clock, use the CKS<sub>mn</sub>0 and CKS<sub>mn</sub>1 bits of the timer mode register mn (TMR<sub>mn</sub>).

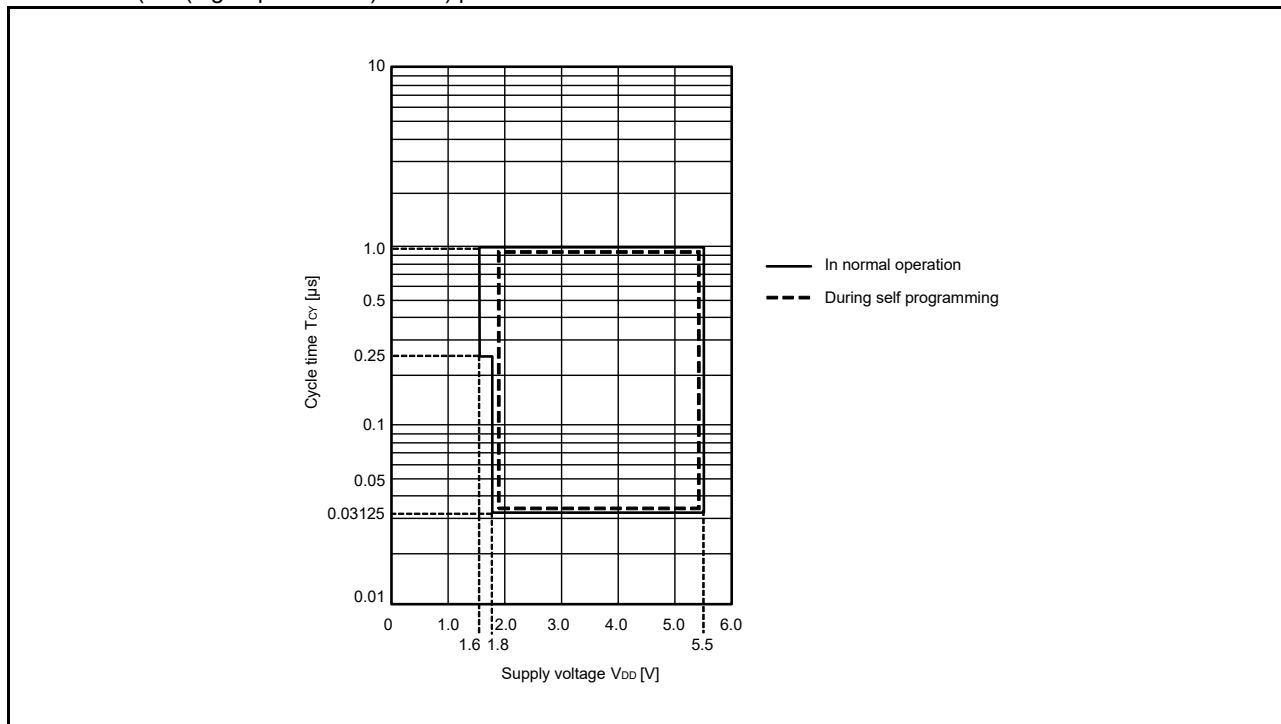
m: Unit number (m = 0), n: Channel number (n = 0 to 3)

Minimum Instruction Execution Time during Main System Clock Operation

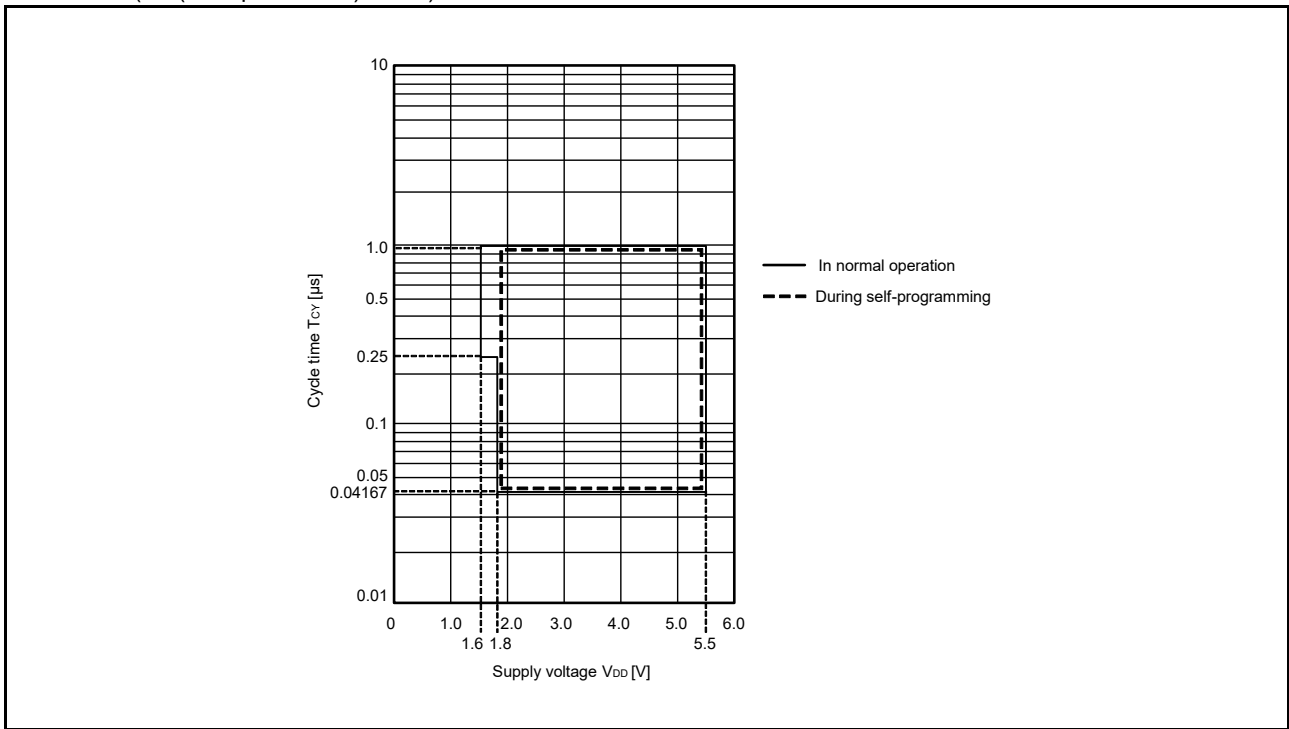
TCY vs VDD (HS (high-speed main) mode) prefetch ON



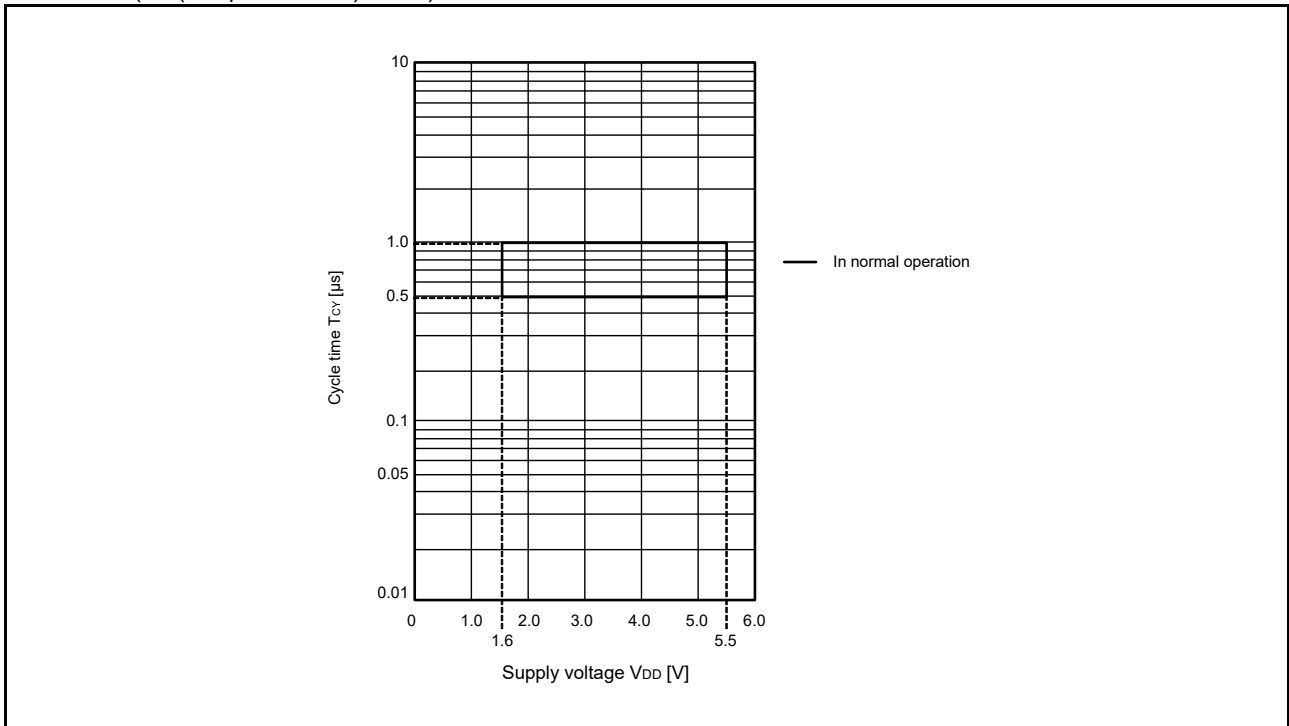
TCY vs VDD (HS (high-speed main) mode) prefetch OFF



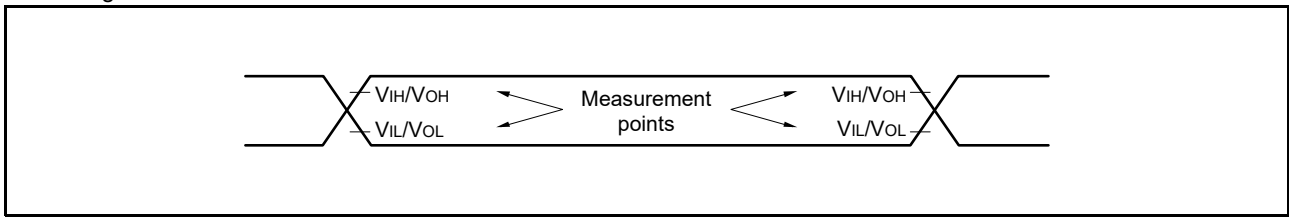
TCY vs VDD (LS (low-speed main) mode)



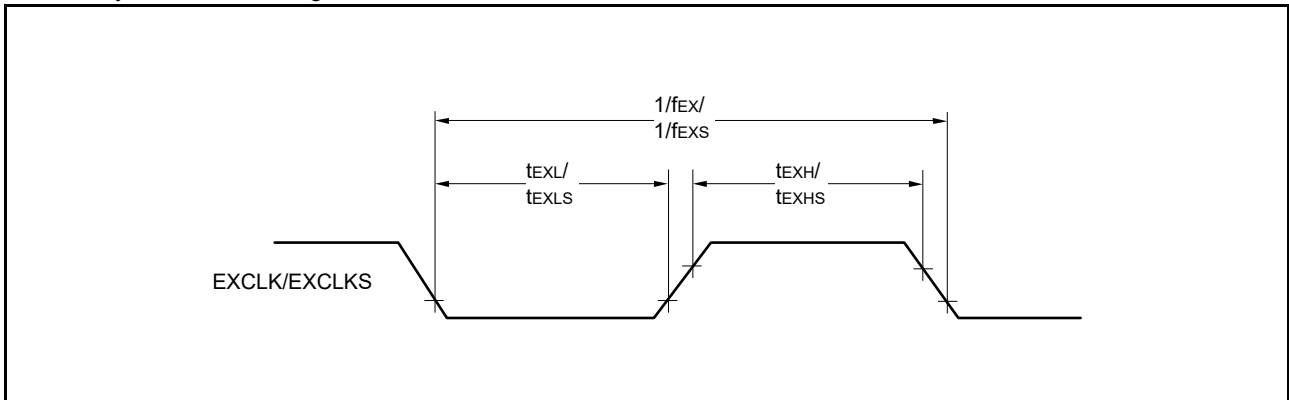
TCY vs VDD (LP (low-power main) mode)



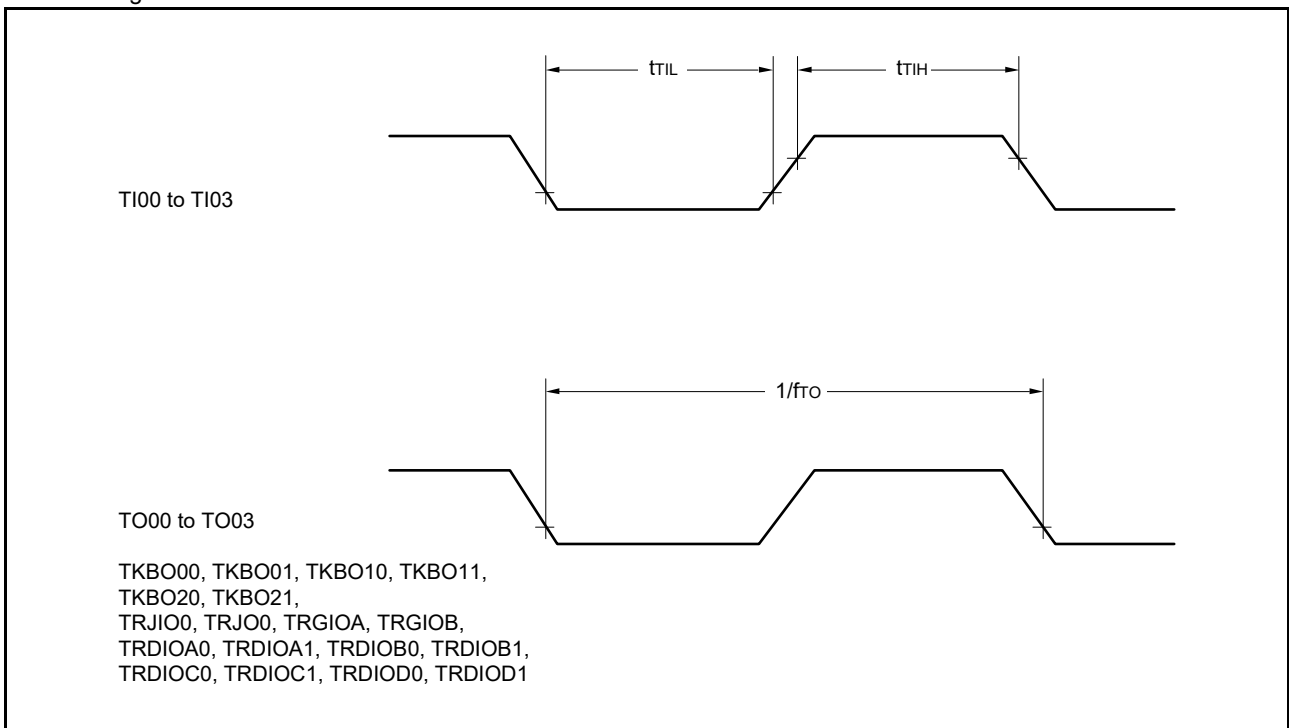
AC Timing Measurement Points



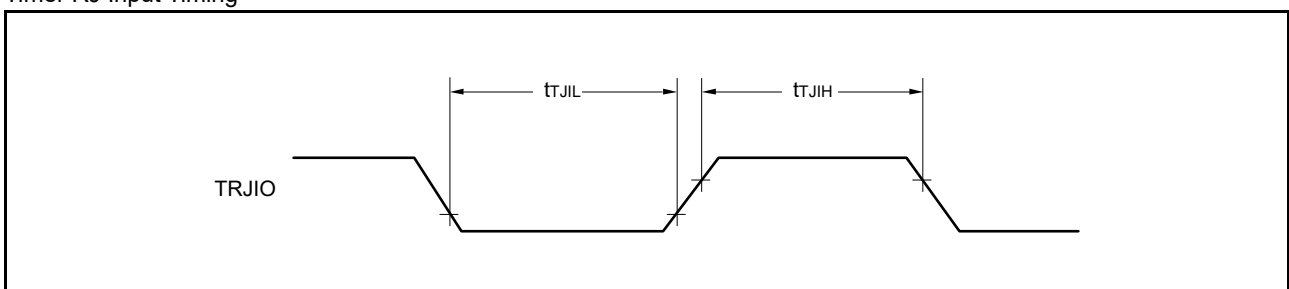
External System Clock Timing



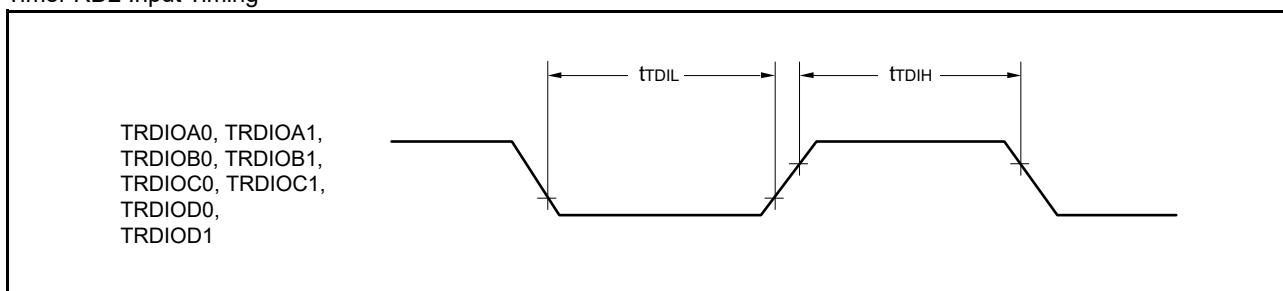
TI/TO Timing



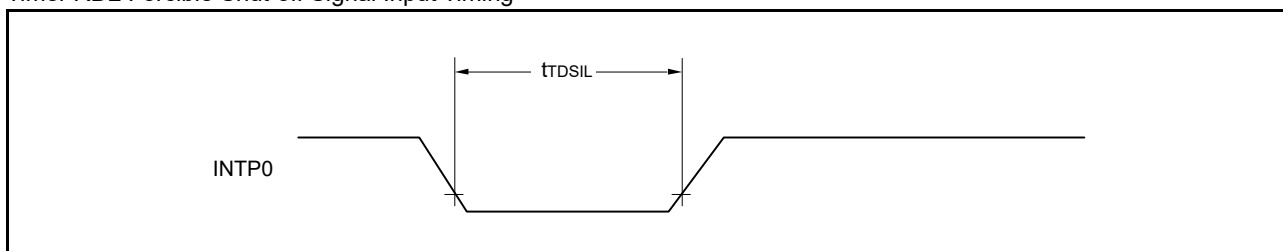
Timer RJ Input Timing



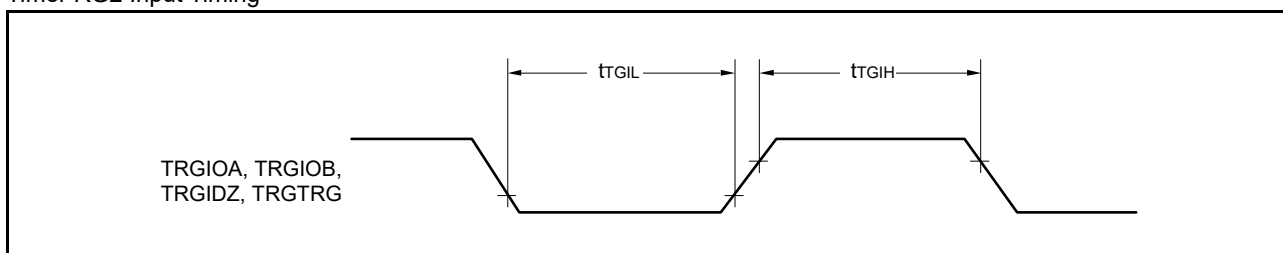
Timer RD2 Input Timing



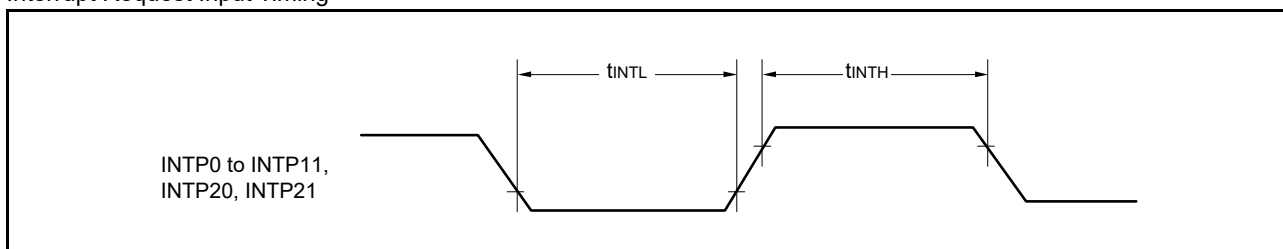
Timer RD2 Forcible Shut-off Signal Input Timing



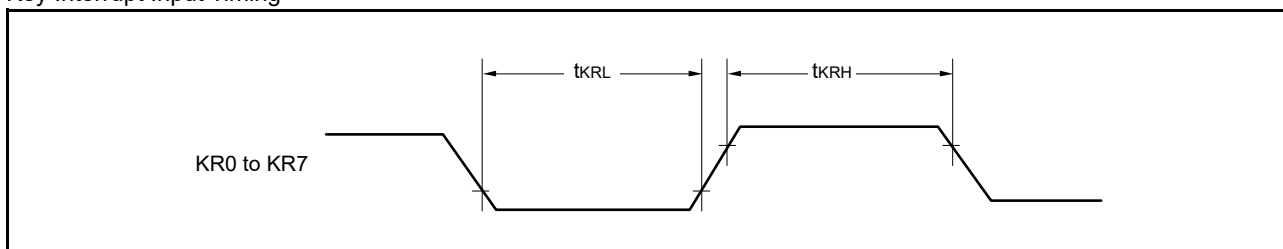
Timer RG2 Input Timing



Interrupt Request Input Timing

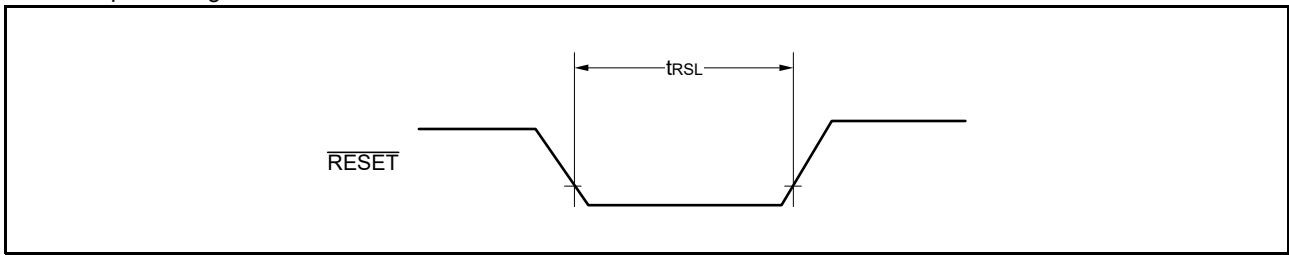


Key Interrupt Input Timing



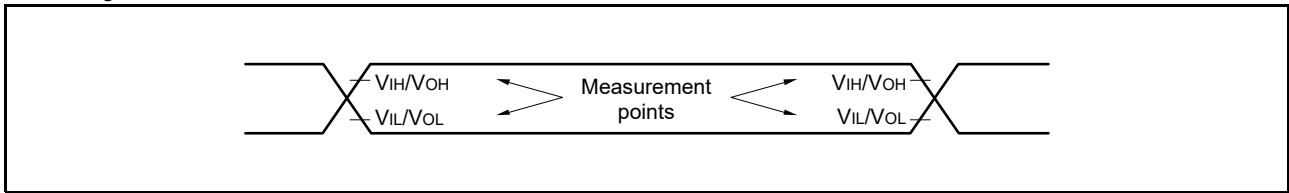


RESET Input Timing



## 2.5 Characteristics of the Peripheral Functions

### AC Timing Measurement Points



### 2.5.1 Serial array unit

- In UART communications with devices operating at same voltage levels

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate Note 1		1.6 V ≤ EVDD0 ≤ 5.5 V		fMCK/6 Note 2		fMCK/6 Note 2		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		5.3		4		0.33	Mbps

**Note 1.** The transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

**Note 2.** The following conditions are required for low-voltage interface when EVDD0 < VDD.

2.4 V ≤ EVDD0 < 2.7 V: 2.6 Mbps (max.)

1.8 V ≤ EVDD0 < 2.4 V: 1.3 Mbps (max.)

1.6 V ≤ EVDD0 < 1.8 V: 0.6 Mbps (max.)

**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are as follows.

HS (high-speed main) mode: 48 MHz (2.4 V ≤ VDD ≤ 5.5 V)

32 MHz (1.8 V ≤ VDD ≤ 5.5 V)

4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

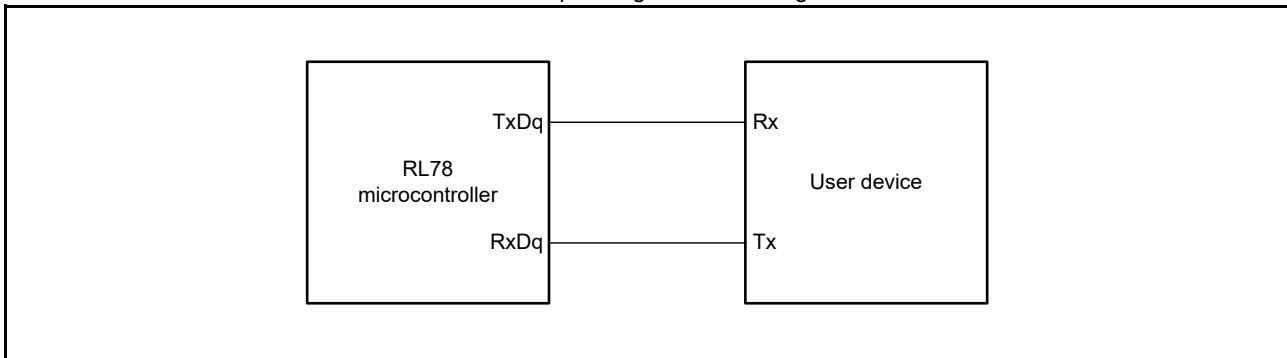
LS (low-speed main) mode: 24 MHz (1.8 V ≤ VDD ≤ 5.5 V)

4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

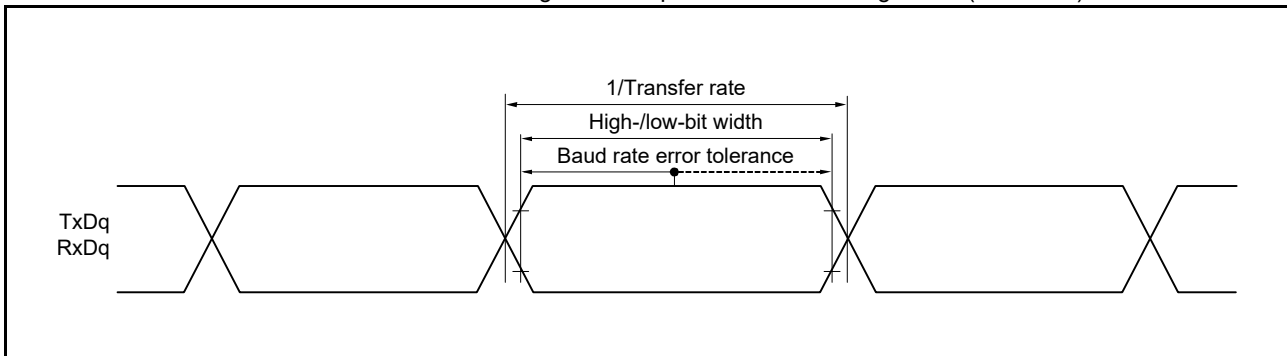
LP (low-power main) mode: 2 MHz (1.6 V ≤ VDD ≤ 5.5 V)

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Connection in UART communications with devices operating at same voltage levels



Bit width in UART communications when interfacing devices operate at same voltage level (reference)



**Remark 1.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** fMCK: Serial array unit operation clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

2. In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock (the ratings below are only applicable to CSI00)

(TA = -40 to +85°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	tkCY1	tkCY1 ≥ 2/fCLK	4.0 V ≤ EVDD0 ≤ 5.5 V	62.5		83.3		1000		ns
			2.7 V ≤ EVDD0 ≤ 5.5 V	83.3		125		1000		ns
SCKp high-/low-level width	tkH1, tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V		tkCY1/2 - 7		tkCY1/2 - 10		tkCY1/2 - 50		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V		tkCY1/2 - 10		tkCY1/2 - 15		tkCY1/2 - 50		ns
Slp setup time (to SCKp↑)Note 1	tsIK1	4.0 V ≤ EVDD0 ≤ 5.5 V		23		33		110		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V		33		50		110		ns
Slp hold time (from SCKp↑) Note 1	tkSI1	2.7 V ≤ EVDD0 ≤ 5.5 V		10		10		10		ns
Delay time from SCKp↓ to SOp outputNote 2	tkSO1	C = 20 pFNote 3			10		10		10	ns

**Note 1.** The setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes "to SCKp↓" and that for the Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and normal output mode for the SOp and SCKp pins by using the port input mode register g (PIMg) and the port output mode register g (POMg).

**Remark 1.** The listed values are only valid when the peripheral I/O redirect function of CSI00 is not in use.

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

**Remark 3.** fMCK: Serial array unit operating clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00)

3. In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	tkCY1	tkCY1 ≥ 4/fCLK	2.7 V ≤ EVDD0 ≤ 5.5 V	125		166		2000		ns
			2.4 V ≤ EVDD0 ≤ 5.5 V	250		250		2000		ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	500		500		2000		ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	1000		1000		2000		ns
SCKp high-/low-level width	tkH1, tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 12		tkCY1/2 - 21		tkCY1/2 - 50		ns	
		2.7 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 18		tkCY1/2 - 25		tkCY1/2 - 50		ns	
		2.4 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 38		tkCY1/2 - 38		tkCY1/2 - 50		ns	
		1.8 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns	
		1.6 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 100		tkCY1/2 - 100		tkCY1/2 - 100		ns	
Slp setup time (to SCKp↑) <sup>Note 1</sup>	tsIK1	4.0 V ≤ EVDD0 ≤ 5.5 V	44		54		110		ns	
		2.7 V ≤ EVDD0 ≤ 5.5 V	44		54		110		ns	
		2.4 V ≤ EVDD0 ≤ 5.5 V	75		75		110		ns	
		1.8 V ≤ EVDD0 ≤ 5.5 V	110		110		110		ns	
		1.6 V ≤ EVDD0 ≤ 5.5 V	220		220		220		ns	
Slp hold time (from SCKp↑) <sup>Note 1</sup>	tkSI1	1.6 V ≤ EVDD0 ≤ 5.5 V	19		19		19		ns	
Delay time from SCKp↓ to SOp output <sup>Note 2</sup>	tkSO1	1.6 V ≤ EVDD0 ≤ 5.5 V C = 30 pF <sup>Note 3</sup>		25		25		25	ns	

**Note 1.** The setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp↓” and that for the Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and normal output mode for the SOp and SCKp pins by using the port input mode register g (PIMg) and the port output mode register g (POMg).

**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** fMCK: Serial array unit operating clock frequency  
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

4. In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the external SCKp clock

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(1/2)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit	
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time Note 4	tkCY2	4.0 V ≤ EVDD0 ≤ 5.5 V	20 MHz < fMCK	8/fMCK		8/fMCK		—		ns	
			fMCK ≤ 20 MHz	6/fMCK		6/fMCK		6/fMCK		ns	
		2.7 V ≤ EVDD0 ≤ 5.5 V	16 MHz < fMCK	8/fMCK		8/fMCK		—		ns	
			fMCK ≤ 16 MHz	6/fMCK		6/fMCK		6/fMCK		ns	
		2.4 V ≤ EVDD0 ≤ 5.5 V			6/fMCK and 500		6/fMCK and 500		6/fMCK and 500		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V			6/fMCK and 750		6/fMCK and 750		6/fMCK and 750		ns
1.6 V ≤ EVDD0 ≤ 5.5 V			6/fMCK and 1500		6/fMCK and 1500		6/fMCK and 1500		ns		
SCKp high-/ low-level width	tkH2, tkL2	4.0 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 7		tkCY2/2 - 7		tkCY2/2 - 7		ns	
		2.7 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 8		tkCY2/2 - 8		tkCY2/2 - 8		ns	
		1.8 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 18		tkCY2/2 - 18		tkCY2/2 - 18		ns	
		1.6 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 66		tkCY2/2 - 66		tkCY2/2 - 66		ns	
Slp setup time (to SCKp↑)Note 1	tsIK2	2.7 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 20		1/fMCK + 30		1/fMCK + 30		ns	
		1.8 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 30		1/fMCK + 30		1/fMCK + 30		ns	
		1.6 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 40		1/fMCK + 40		1/fMCK + 40		ns	
Slp hold time (to SCKp↑)Note 1	tsIK2	1.8 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 31		1/fMCK + 31		1/fMCK + 31		ns	
		1.6 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 250		1/fMCK + 250		1/fMCK + 250		ns	

(Notes, Caution, and Remarks are listed on the next page.)

4. In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the external SCKp clock

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
Delay time from SCKp↓ to SOp output Note 2	tkSO2	C = 30 pF Note 3	2.7 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 44		2/fMCK + 110		2/fMCK + 110	ns
			2.4 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 75		2/fMCK + 110		2/fMCK + 110	ns
			1.8 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 110		2/fMCK + 110		2/fMCK + 110	ns
			1.6 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 220		2/fMCK + 220		2/fMCK + 220	ns

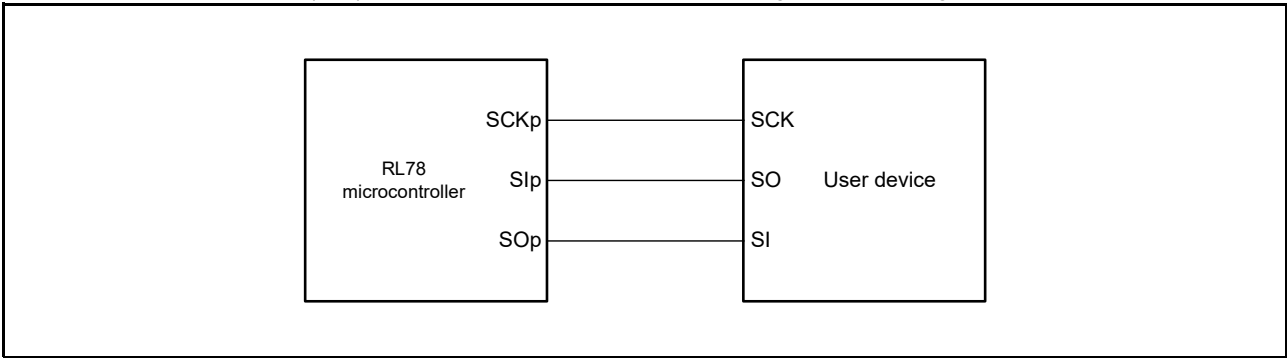
- Note 1.** The setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp ↓” and that for the Slp hold time becomes “from SCKp ↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 2.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 3.** C is the load capacitance of the SOp output line.
- Note 4.** The transfer rate in the SNOOZE mode is 1 Mbps maximum.

**Caution** Select the normal input buffer for the Slp and SCKp pins and normal output mode for the SOp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

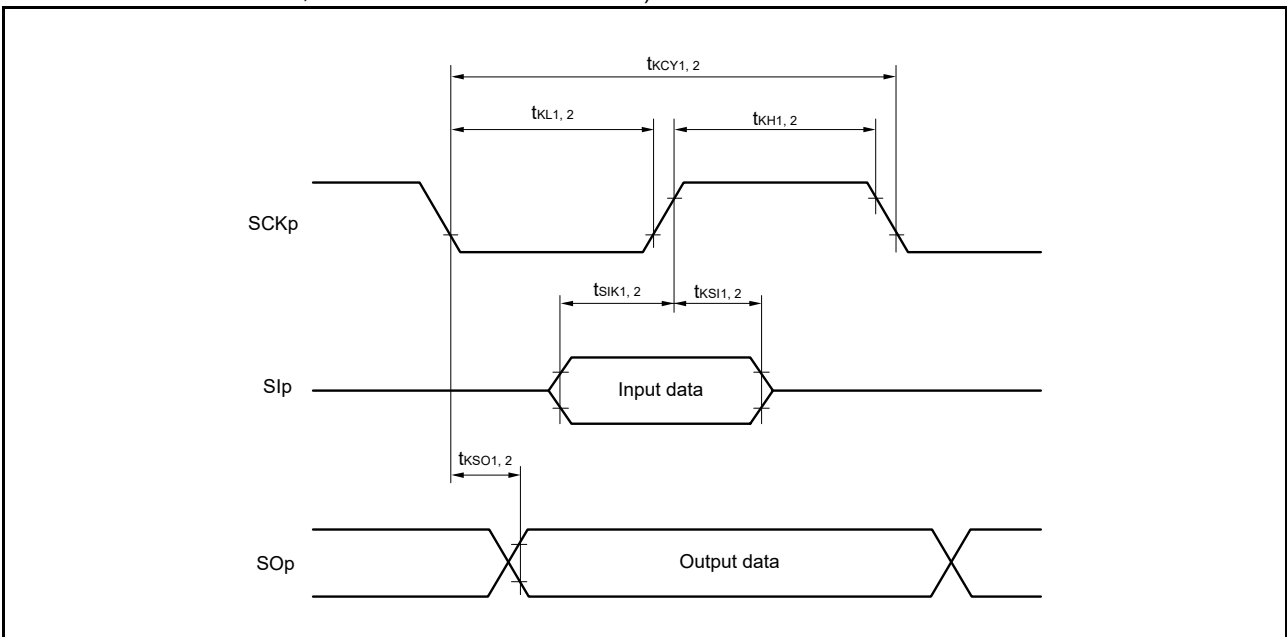
**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** fMCK: Serial array unit operating clock frequency  
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

Connection in simplified SPI (CSI) communications with devices operating at same voltage levels

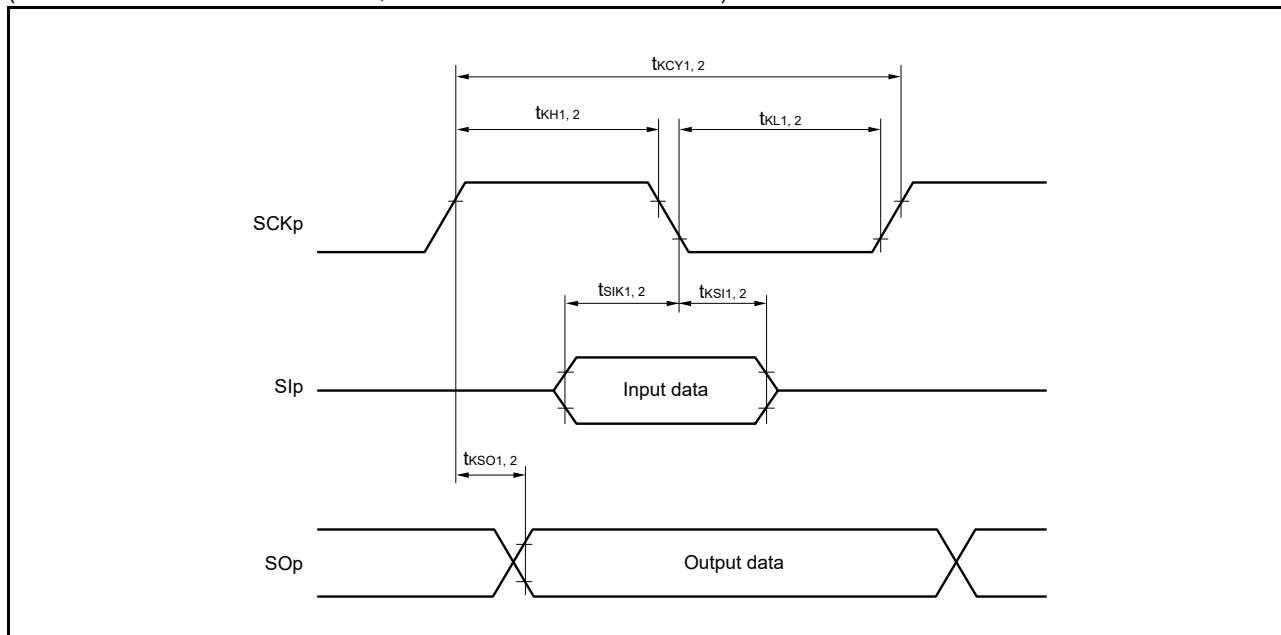


Timing of serial transfer in simplified SPI (CSI) communications with devices operating at same voltage levels (when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)





Timing of serial transfer in simplified SPI (CSI) communications with devices operating at same voltage levels  
 (when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



- Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21)
- Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

5. In simplified I<sup>2</sup>C communications with devices operating at same voltage levels

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(1/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	fSCL	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		1000 Note 1		400Note 1	kHz
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		400Note 1		400Note 1		400Note 1	kHz
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		300Note 1		300Note 1		300Note 1	kHz
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		250Note 1		250Note 1		250Note 1	kHz
Hold time when SCLr is low	tLOW	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns
Hold time when SCLr is high	tHIGH	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns
Data setup time (reception)	tSU:DAT	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 85 Note 2		1/fMCK + 85 Note 2		1/fMCK + 145 Note 2		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1/fMCK + 145 Note 2		1/fMCK + 145 Note 2		1/fMCK + 145 Note 2		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1/fMCK + 230 Note 2		1/fMCK + 230 Note 2		1/fMCK + 230 Note 2		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1/fMCK + 290 Note 2		1/fMCK + 290 Note 2		1/fMCK + 290 Note 2		ns

(Notes and Caution are listed on the next page, and Remarks are listed on page 84.)

5. In simplified I<sup>2</sup>C communications with devices operating at same voltage levels

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data hold time (transmission)	tHD:DAT	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	0	405	0	405	0	405	ns

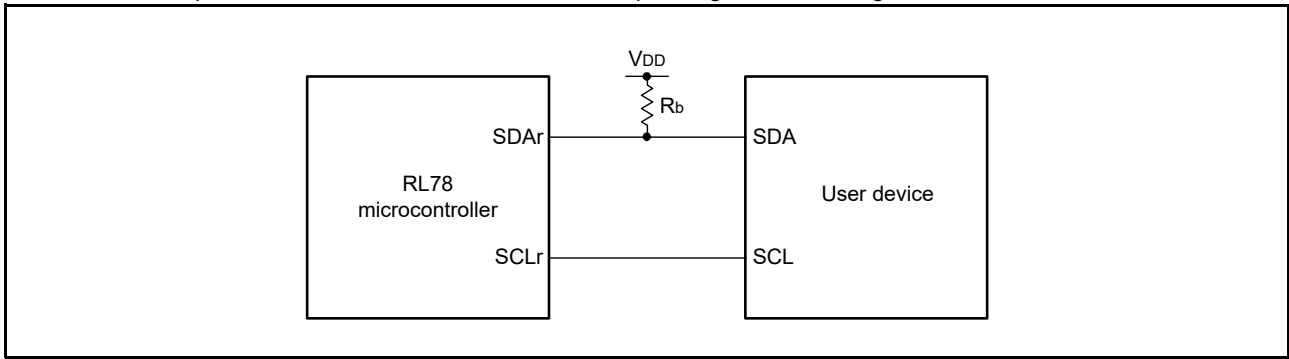
**Note 1.** The listed frequencies must be no greater than fMCK/4.

**Note 2.** Set the fMCK value that does not exceed the hold time when SCLr is low or high.

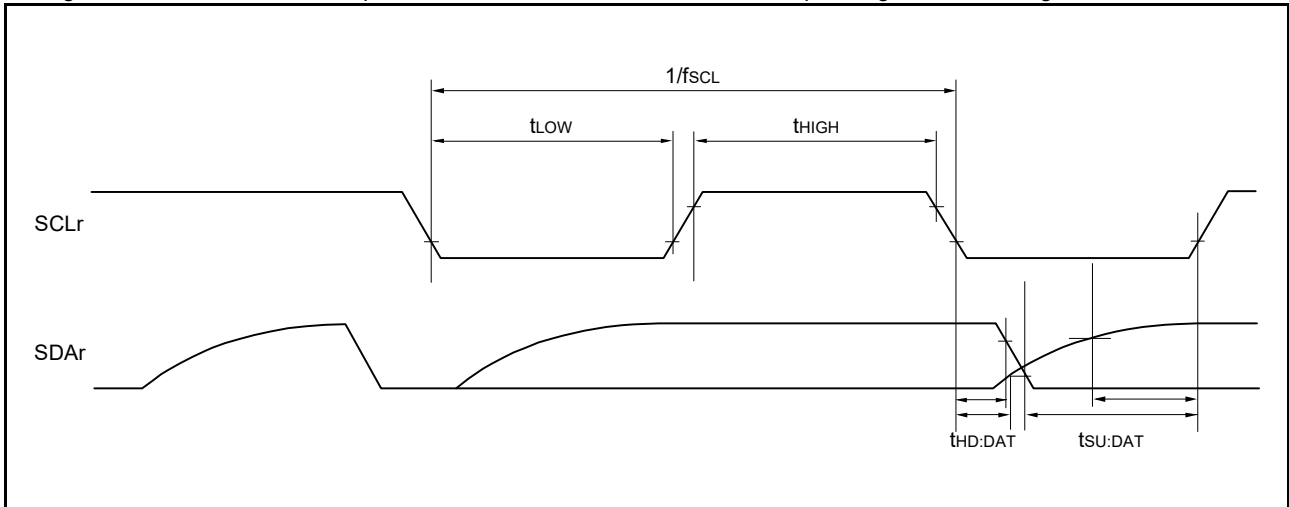
**Caution** Select the normal input buffer and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/ EVDD withstand voltage for 64-pin products) for the SDAr pin and the normal output mode for the SCLr pin by using the port input mode register g (PIMg) and the port output mode register h (POMh).

(Remarks are listed on the next page.)

Connection in simplified I<sup>2</sup>C communications with devices operating at same voltage levels



Timing of serial transfer in the simplified I<sup>2</sup>C communications with devices operating at same voltage levels



**Remark 1.** R<sub>b</sub>[Ω]: Communication line (SDAr) pull-up resistance, C<sub>b</sub>[F]: Communication line (SDAr, SCLr) load capacitance

**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1, 3, 5, 7), h: POM number (h = 0, 1, 3, 5, 7)

**Remark 3.** f<sub>MCK</sub>: Serial array unit operating clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

## 6. In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(1/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
Transfer rate		Reception	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK>Note 4		5.3		4		0.33	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK>Note 4		5.3		4		0.33	Mbps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V		fMCK/6 Notes 1, 2, 3		fMCK/6 Notes 1, 2		fMCK/6 Notes 1, 2	bps
			Theoretical value of the maximum transfer rate fMCK = fCLK>Note 4		5.3		4		0.33	Mbps

**Note 1.** Transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

**Note 2.** Use this rate with EVDD0 ≥ Vb.

**Note 3.** The following conditions are required for low-voltage interface when EVDD0 < VDD.

2.4 V ≤ EVDD0 < 2.7 V: 2.6 Mbps (max.)

1.8 V ≤ EVDD0 < 2.4 V: 1.3 Mbps (max.)

**Note 4.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 48 MHz (2.4 V ≤ VDD ≤ 5.5 V)

32 MHz (1.8 V ≤ VDD ≤ 5.5 V)

4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

LS (low-speed main) mode: 24 MHz (1.8 V ≤ VDD ≤ 5.5 V)

4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

LP (low-power main) mode: 2 MHz (1.6 V ≤ VDD ≤ 5.5 V)

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the TxDq pin by using the port input mode register g (PIMg) and the port output mode register g (POMg). For VIH and VIL, see the DC characteristics with the TTL input buffer selected.

**Remark 1.** Vb[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 3.** fMCK: Serial array unit operation clock frequency

To set this operating clock, use the CKSMn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

**Remark 4.** Communications by using UART2 with devices operating at different voltage levels are not possible when bit 1 (PIOR1) of the peripheral I/O redirection register 0 (PIOR0) is set to 1.

6. In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
Transfer rate		Transmission	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		Note 1		Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V		2.8Note 2		2.8Note 2		2.8Note 2	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		Note 3		Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V		1.2Note 4		1.2Note 4		1.2Note 4	Mbps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V		Notes 5, 6		Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

(Notes and Caution are listed on the next page.)

**Note 1.** The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when  $4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$ ,  $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 2.** This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

**Note 3.** The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when  $2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$ ,  $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 4.** This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**Note 5.** Use this rate with  $\text{EVDD0} \geq \text{Vb}$ .

**Note 6.** The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when  $1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$ ,  $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

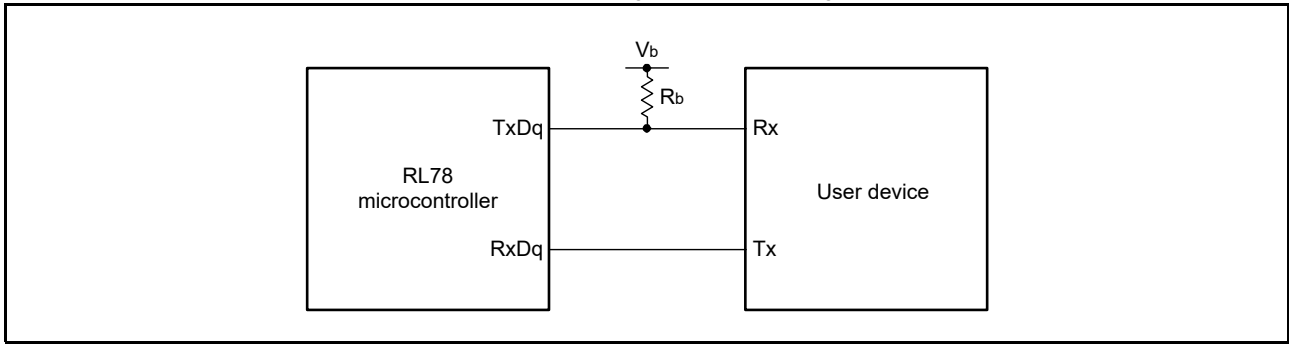
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

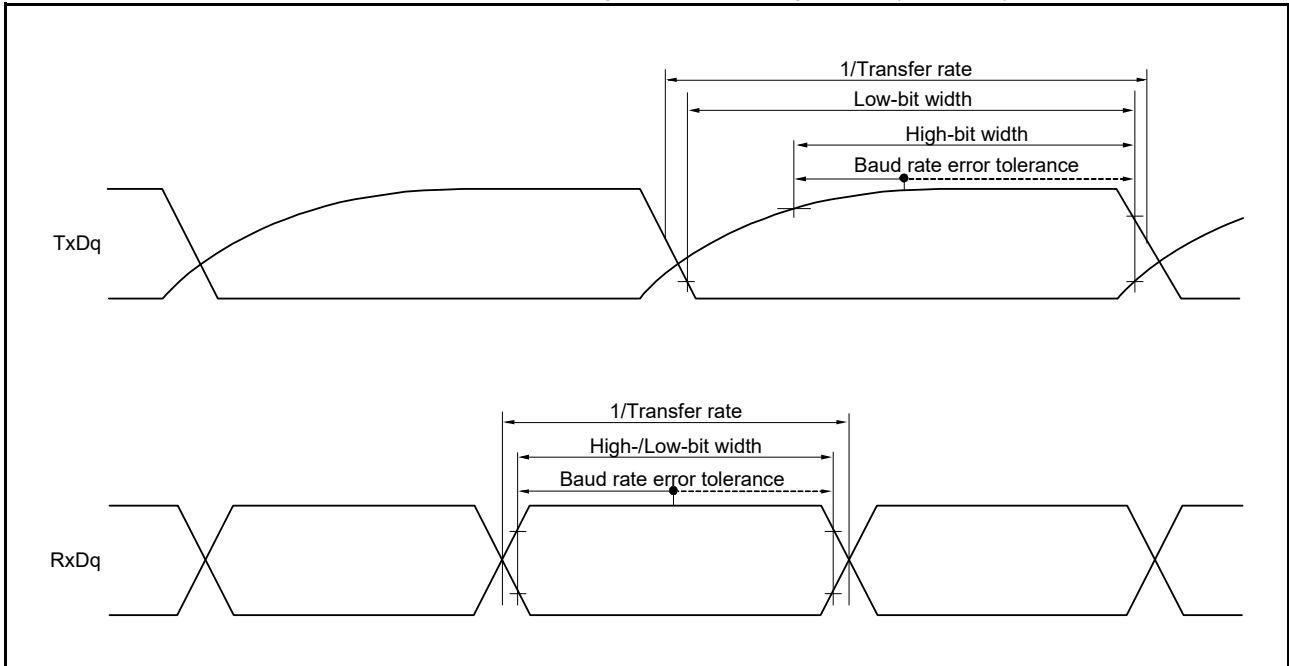
**Note 7.** This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the TxDq pin by using the port input mode register g (PIMg) and the port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with the TTL input buffer selected.

Connection in UART communications with devices operating at different voltage levels



Bit width in UART communications with devices operating at different voltage levels (reference)



- Remark 1.**  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  $C_b[F]$ : Communication line (TxDq) load capacitance,  $V_b[V]$ : Communication line voltage
- Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)
- Remark 3.**  $f_{MCK}$ : Serial array unit operating clock frequency  
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)
- Remark 4.** Communications by using UART2 with devices operating at different voltage levels are not possible when bit 1 (PIOR01) of the peripheral I/O redirection register 0 (PIOR0) is set to 1.



7. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

(TA = -40 to +105°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(1/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	tkCY1	tkCY1 ≥ 2/fCLK 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	200		200		2300		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	300		300		2300		ns
SCKp high-level width	tkH1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	tkCY1/2 - 120		tkCY1/2 - 120		tkCY1/2 - 120		ns
SCKp low-level width	tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	tkCY1/2 - 7		tkCY1/2 - 7		tkCY1/2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	tkCY1/2 - 10		tkCY1/2 - 10		tkCY1/2 - 50		ns
Slp setup time (to SCKp↑) <sup>Note 1</sup>	tsIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	58		58		479		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	121		121		479		ns
Slp hold time (from SCKp↑) <sup>Note 1</sup>	tsIH1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↓ to SOp output <sup>Note 1</sup>	tkSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ		60		60		60	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		130		130		130	ns

(Notes, Caution, and Remarks are listed on the next page.)

7. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

(TA = -40 to +105°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Slp setup time (to SCKp↓) <sup>Note 2</sup>	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	23		23		110		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	33		33		110		ns
Slp hold time (from SCKp↓) <sup>Note 2</sup>	tKS1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↑ to SOp output <sup>Note 2</sup>	tKS01	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ		10		10		10	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		10		10		10	ns

**Note 1.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1

**Note 2.** This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the SOp and SCKp pins by using the port input mode register g (PIMg) and the port output mode register g (POMg). For VIH and VIL, see the DC characteristics with the TTL input buffer selected.

**Remark 1.** Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

**Remark 3.** fMCK: Serial array unit operating clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00)

**Remark 4.** The listed values are only valid when the peripheral I/O redirect function of CSI00 is not in use.

8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(1/3)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	tkCY1	tkCY1 ≥ 4/fCLK 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	300		300		2300		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	500		500		2300		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note</sup> , Cb = 30 pF, Rb = 5.5 kΩ	1150		1150		2300		ns
SCKp high-level width	tkH1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	tkCY1/2 - 75		tkCY1/2 - 75		tkCY1/2 - 75		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	tkCY1/2 - 170		tkCY1/2 - 170		tkCY1/2 - 170		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note</sup> , Cb = 30 pF, Rb = 5.5 kΩ	tkCY1/2 - 458		tkCY1/2 - 458		tkCY1/2 - 458		ns
SCKp low-level width	tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	tkCY1/2 - 12		tkCY1/2 - 12		tkCY1/2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	tkCY1/2 - 18		tkCY1/2 - 18		tkCY1/2 - 50		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note</sup> , Cb = 30 pF, Rb = 5.5 kΩ	tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns

**Note** Use this setting with EVDD0 ≥ Vb.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the SOP and SCKp pins by using the port input mode register g (PIMg) and the port output mode register g (POMg). For VIH and VIL, see the DC characteristics with the TTL input buffer selected.

(Remarks are listed on page 94.)

8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(2/3)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Slp setup time (to SCKp↑) <sup>Note 1</sup>	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	81		81		479		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		177		479		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> , Cb = 30 pF, Rb = 5.5 kΩ	479		479		479		ns
Slp hold time (from SCKp↑) <sup>Note 1</sup>	tKS11	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> , Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output <sup>Note 1</sup>	tKSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> , Cb = 30 pF, Rb = 5.5 kΩ		483		483		483	ns

**Note 1.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Note 2.** Use this setting with EVDD0 ≥ Vb.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the SOp and SCKp pins by using the port input mode register g (PIMg) and the port output mode register g (POMg). For VIH and VIL, see the DC characteristics with the TTL input buffer selected.

(Remarks are listed on page 94.)

8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(3/3)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Slp setup time (to SCKp↓) <sup>Note 1</sup>	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	44		44		110		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		44		110		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> , Cb = 30 pF, Rb = 5.5 kΩ	110		110		110		ns
Slp hold time (from SCKp↓) <sup>Note 1</sup>	tKS11	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> , Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output <sup>Note 1</sup>	tKSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> , Cb = 30 pF, Rb = 5.5 kΩ		25		25		25	ns

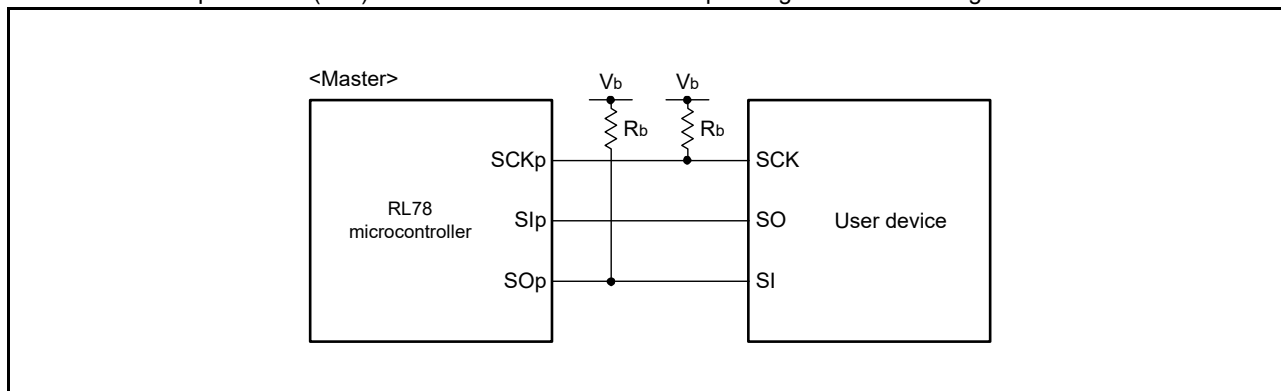
**Note 1.** This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** Use this setting with EVDD0 ≥ Vb.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the SOp and SCKp pins by using the port input mode register g (PIMg) and the port output mode register g (POMg). For VIH and VIL, see the DC characteristics with the TTL input buffer selected.

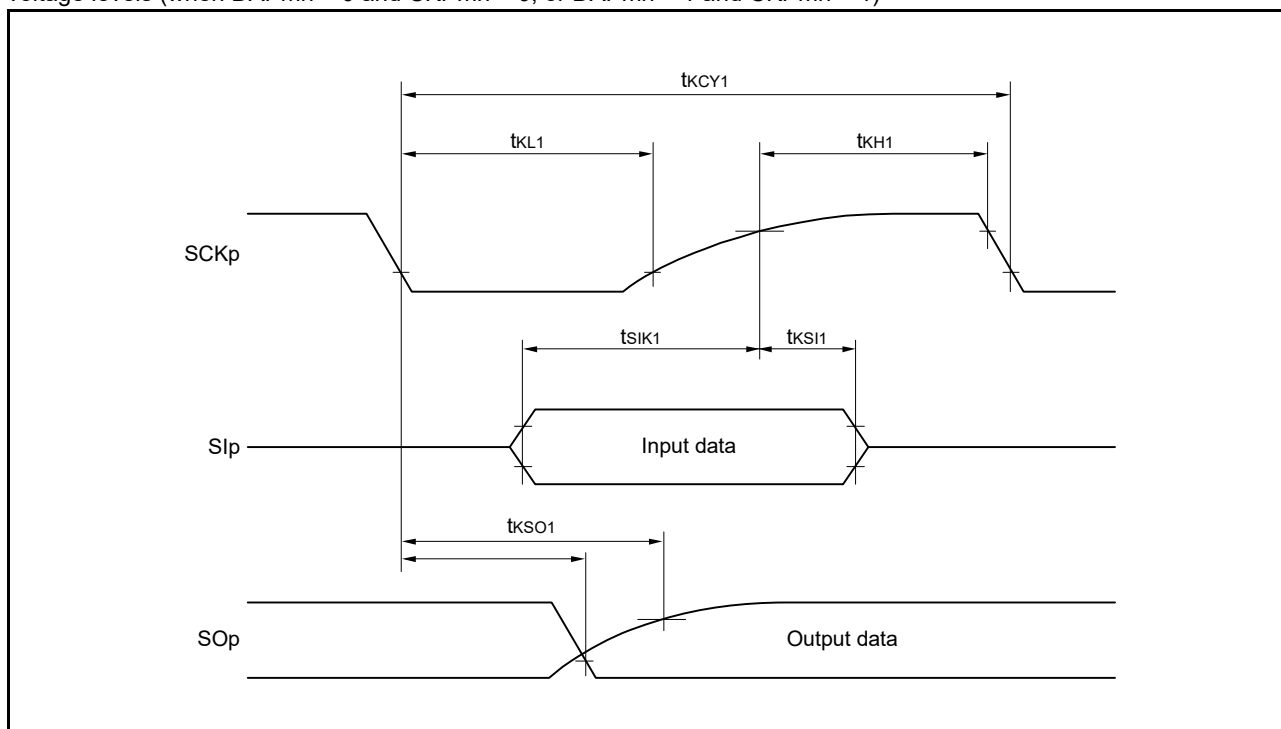
(Remarks are listed on the next page.)

Connection in simplified SPI (CSI) communications with devices operating at different voltage levels

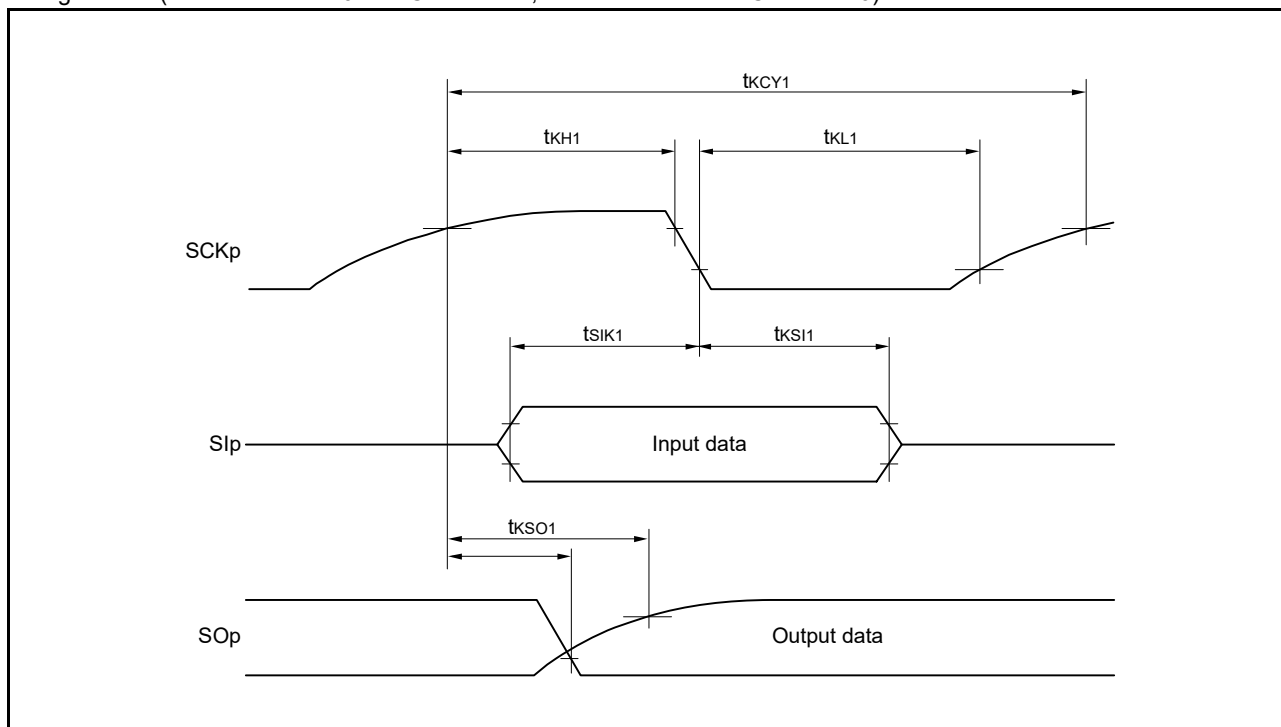


- Remark 1.**  $R_b[\Omega]$ : Communication line (SCKp, SOp) pull-up resistance,  $C_b[F]$ : Communication line (SCKp, SOp) load capacitance,  $V_b[V]$ : Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20), m: Unit number, n: Channel number (mn = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1, 3, 5, 7)
- Remark 3.** fMCK: Serial array unit operating clock frequency  
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00)
- Remark 4.** Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

Timing of serial transfer in simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Timing of serial transfer in simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



**Remark 1.** p: CSI number (p = 00, 01, 10, 20), m: Unit number, n: Channel number (mn = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

9. In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(1/2)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time Note 1	tkCY2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	24 MHz < fMCK	14/fMCK		—		—		ns
			20 MHz < fMCK ≤ 24 MHz	12/fMCK		12/fMCK		—		ns
			8 MHz < fMCK ≤ 20 MHz	10/fMCK		10/fMCK		—		ns
			4 MHz < fMCK ≤ 8 MHz	8/fMCK		8/fMCK		—		ns
			fMCK ≤ 4 MHz	6/fMCK		6/fMCK		10/fMCK		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	24 MHz < fMCK	20/fMCK		—		—		ns
			20 MHz < fMCK ≤ 24 MHz	16/fMCK		16/fMCK		—		ns
			16 MHz < fMCK ≤ 20 MHz	14/fMCK		14/fMCK		—		ns
			8 MHz < fMCK ≤ 16 MHz	12/fMCK		12/fMCK		—		ns
			4 MHz < fMCK ≤ 8 MHz	8/fMCK		8/fMCK		—		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2	24 MHz < fMCK	48/fMCK		—		—		ns
			20 MHz < fMCK ≤ 24 MHz	36/fMCK		36/fMCK		—		ns
			16 MHz < fMCK ≤ 20 MHz	32/fMCK		32/fMCK		—		ns
			8 MHz < fMCK ≤ 16 MHz	26/fMCK		26/fMCK		—		ns
			4 MHz < fMCK ≤ 8 MHz	16/fMCK		16/fMCK		—		ns
			fMCK ≤ 4 MHz	10/fMCK		10/fMCK		10/fMCK		ns

(Notes and Caution are listed on the next page, and Remarks are listed on page 98.)



9. In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(2/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp high-/low-level width	tkH2, tkL2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	tkCY2/2 - 12		tkCY2/2 - 12		tkCY2/2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	tkCY2/2 - 18		tkCY2/2 - 18		tkCY2/2 - 50		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup>	tkCY2/2 - 50		tkCY2/2 - 50		tkCY2/2 - 50		ns
Slp setup time (to SCKp↑) <sup>Note 3</sup>	tSIK2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	1/fMCK + 20		1/fMCK + 20		1/fMCK + 30		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	1/fMCK + 20		1/fMCK + 20		1/fMCK + 30		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup>	1/fMCK + 30		1/fMCK + 30		1/fMCK + 30		ns
Slp hold time (from SCKp↑) <sup>Note 3</sup>	tkSI2		1/fMCK + 31		1/fMCK + 31		1/fMCK + 31		ns
Delay time from SCKp↓ to SOp output <sup>Note 4</sup>	tkSO2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		2/fMCK + 120		2/fMCK + 120		2/fMCK + 573	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		2/fMCK + 214		2/fMCK + 214		2/fMCK + 573	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> , Cb = 30 pF, Rb = 5.5 kΩ		2/fMCK + 573		2/fMCK + 573		2/fMCK + 573	ns

**Note 1.** Transfer rate in the SNOOZE mode: 1 Mbps (max.)

**Note 2.** Use this setting with EVDD0 ≥ Vb.

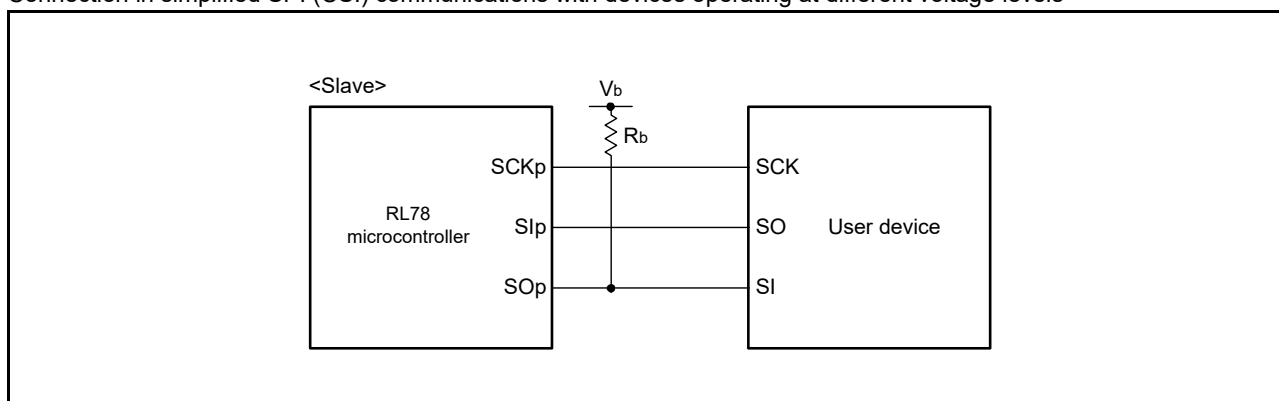
**Note 3.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” and Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp and SCKp pins and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the SOp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg). For VIH and VIL, see the DC characteristics with the TTL input buffer selected.

(Remarks are listed on the next page.)

## Connection in simplified SPI (CSI) communications with devices operating at different voltage levels



**Remark 1.**  $R_b[\Omega]$ : Communication line (SO<sub>p</sub>) pull-up resistance,  $C_b[F]$ : Communication line (SO<sub>p</sub>) load capacitance,  $V_b[V]$ : Communication line voltage

**Remark 2.** p: CSI number (p = 00, 01, 10, 20), m: Unit number, n: Channel number (mn = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1, 3, 5, 7)

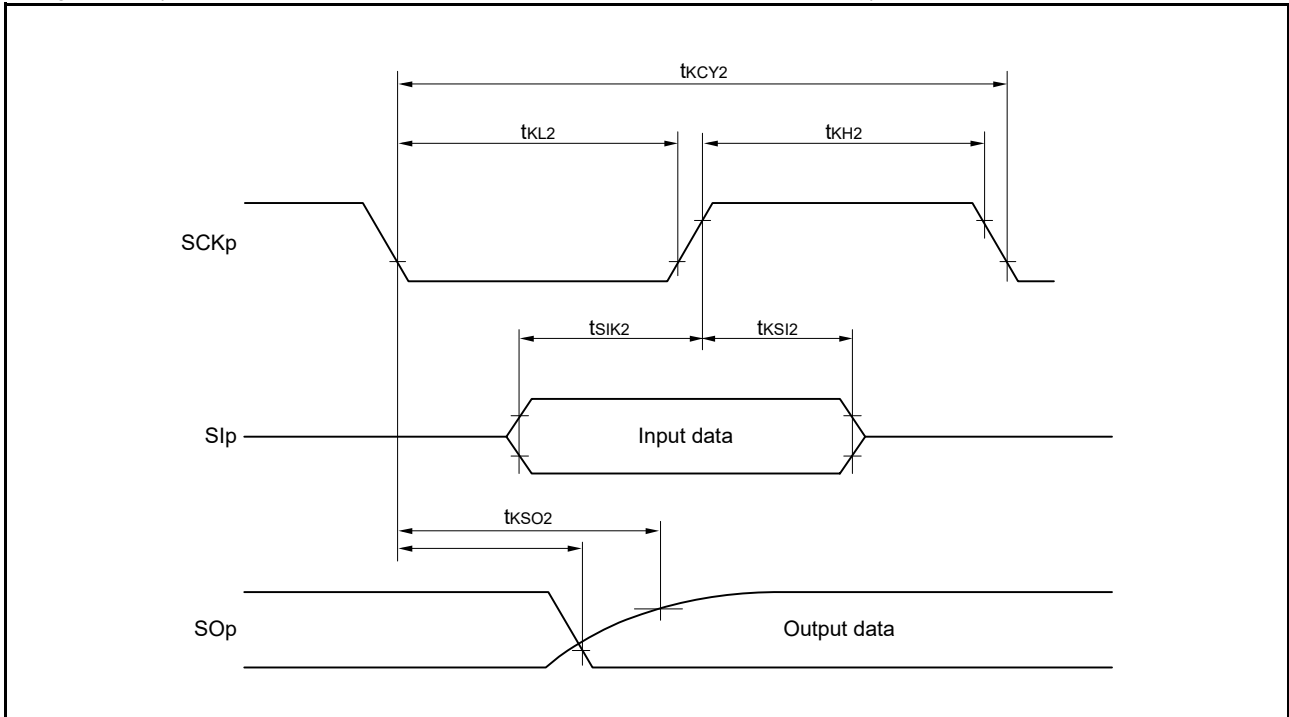
**Remark 3.** f<sub>MCK</sub>: Serial array unit operating clock frequency

To set this operating clock, use the CKS<sub>mn</sub> bit in the serial mode register mn (SMR<sub>mn</sub>).

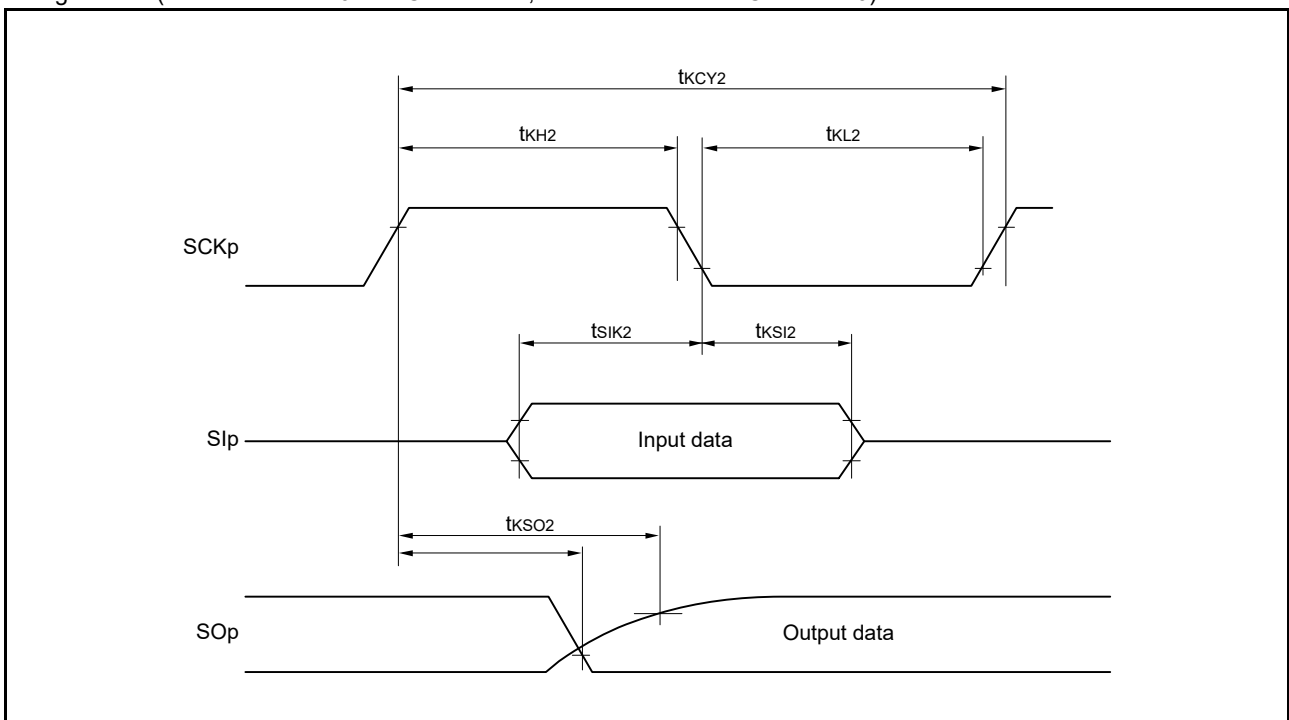
m: Unit number, n: Channel number (mn = 00, 01, 02, 10)

**Remark 4.** Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

Timing of serial transfer in simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Timing of serial transfer in simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



**Remark 1.** p: CSI number (p = 00, 01, 10, 20), m: Unit number, n: Channel number (mn = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

10. Simplified I<sup>2</sup>C communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V)

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(1/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	fSCL	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		1000 Note 1		300 Note 1	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		1000 Note 1		300 Note 1	kHz
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ		400 Note 1		400 Note 1		300 Note 1	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ		400 Note 1		400 Note 1		300 Note 1	kHz
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> , Cb = 100 pF, Rb = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr is low	tLOW	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	475		475		1550		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	475		475		1550		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> , Cb = 100 pF, Rb = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr is high	tHIGH	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	245		245		610		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	200		200		610		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	675		675		610		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	600		600		610		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> , Cb = 100 pF, Rb = 5.5 kΩ	610		610		610		ns

(Notes and Caution are listed on the next page, and Remarks are listed on page 102.)

10. Simplified I<sup>2</sup>C communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V)

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(2/2)

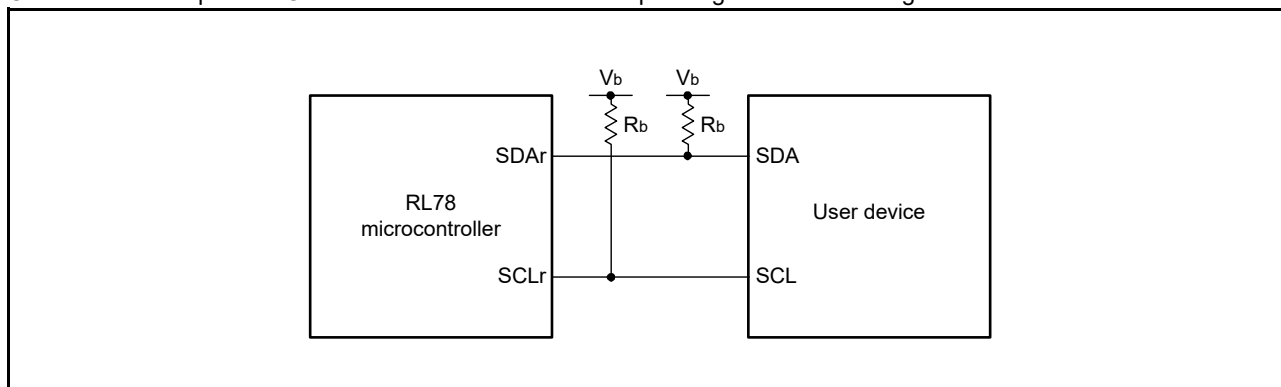
Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	tsu:DAT	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 135 Note 3		1/fMCK + 135 Note 3		1/fMCK + 190 Note 3		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 135 Note 3		1/fMCK + 135 Note 3		1/fMCK + 190 Note 3		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> , Cb = 100 pF, Rb = 5.5 kΩ	1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
Data hold time (transmission)	tHD:DAT	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> , Cb = 100 pF, Rb = 5.5 kΩ	0	405	0	405	0	405	ns

**Note 1.** The listed frequencies must be no greater than fMCK/4.**Note 2.** Use this setting with EVDD0 ≥ Vb.**Note 3.** Set the fMCK value that does not exceed the hold time when SCLr is low or high.

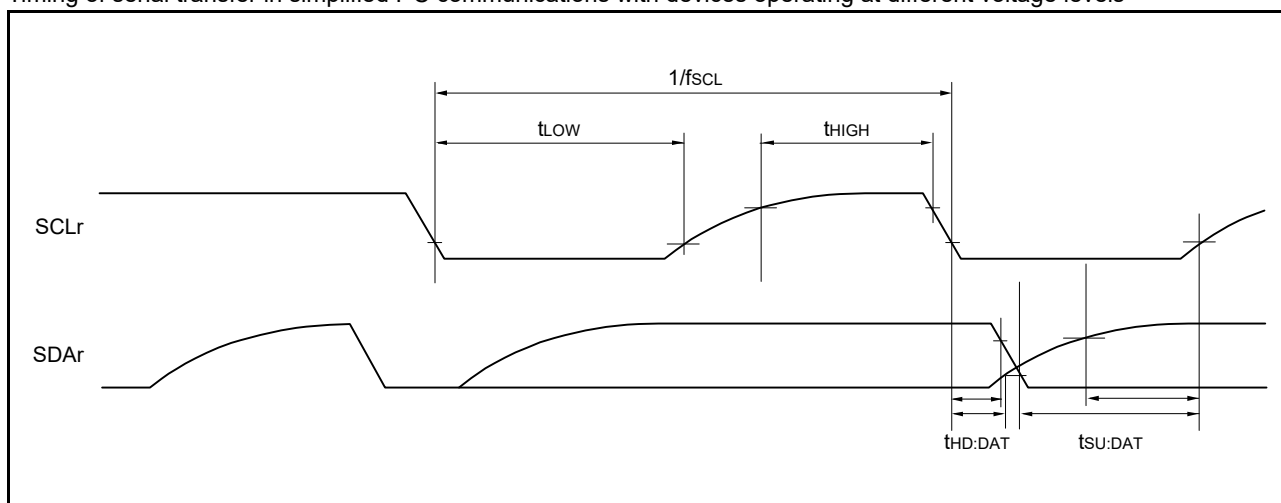
**Caution** Select the TTL input buffer and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the SDAr pin and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the SCLr pin by using the port input mode register g (PIMg) and the port output mode register g (POMg). For VIH and VIL, see the DC characteristics with the TTL input buffer selected.

(Remarks are listed on the next page.)

Connection in simplified I<sup>2</sup>C communications with devices operating at different voltage levels



Timing of serial transfer in simplified I<sup>2</sup>C communications with devices operating at different voltage levels



- Remark 1.** R<sub>b</sub>[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C<sub>b</sub>[F]: Communication line (SDAr, SCLr) load capacitance, V<sub>b</sub>[V]: Communication line voltage
- Remark 2.** r: IIC number (r = 00, 01, 10, 20), g: PIM and POM number (g = 0, 1, 3, 5, 7)
- Remark 3.** f<sub>MCK</sub>: Serial array unit operating clock frequency  
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00, 01, 02, 10)

## 2.5.2 Serial interface IICA

### 1. I<sup>2</sup>C standard mode

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	Standard mode: fCLK ≥ 1 MHz	0		100	kHz
Setup time of restart condition	tSU:STA		4.7			μs
Hold time <sup>Note 1</sup>	tHD:STA		4.0			μs
Hold time when SCLA0 is low	tLOW		4.7			μs
Hold time when SCLA0 is high	tHIGH		4.0			μs
Data setup time (reception)	tSU:DAT		250			ns
Data setup time (transmission) <sup>Note 2</sup>	tHD:DAT		0		3.45	μs
Setup time of stop condition	tSU:STO		4.0			μs
Path free time	tBUF		4.7			μs

**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.

**Caution** The listed values are applicable even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

**Remark** The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.  
Cb = 400 pF, Rb = 2.7 kΩ

2. I<sup>2</sup>C fast mode

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz 1.8 V ≤ EVDD0 ≤ 5.5 V	0		400	kHz
Setup time of restart condition	tSU:STA	1.8 V ≤ EVDD0 ≤ 5.5 V	0.6			μs
Hold time <sup>Note 1</sup>	tHD:STA	1.8 V ≤ EVDD0 ≤ 5.5 V	0.6			μs
Hold time when SCLA0 is low	tLOW	1.8 V ≤ EVDD0 ≤ 5.5 V	1.3			μs
Hold time when SCLA0 is high	tHIGH	1.8 V ≤ EVDD0 ≤ 5.5 V	0.6			μs
Data setup time (reception)	tSU:DAT	1.8 V ≤ EVDD0 ≤ 5.5 V	100			ns
Data hold time (transmission) <sup>Note 2</sup>	tHD:DAT	1.8 V ≤ EVDD0 ≤ 5.5 V	0		0.9	μs
Setup time of stop condition	tSU:STO	1.8 V ≤ EVDD0 ≤ 5.5 V	0.6			μs
Bus-free time	tBUF	1.8 V ≤ EVDD0 ≤ 5.5 V	1.3			μs

**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.

**Caution** The listed values are applicable even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

**Remark** The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.  
Cb = 320 pF, Rb = 1.1 kΩ



3. I<sup>2</sup>C fast mode plus

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	Fast mode plus: fCLK ≥ 10 MHz 2.7 V ≤ EVDD0 ≤ 5.5 V	0		1000	kHz
Setup time of restart condition	tSU:STA	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26			μs
Hold time <sup>Note 1</sup>	tHD:STA	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26			μs
Hold time when SCLA0 is low	tLOW	2.7 V ≤ EVDD0 ≤ 5.5 V	0.5			μs
Hold time when SCLA0 is high	tHIGH	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26			μs
Data setup time (reception)	tSU:DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	50			ns
Data hold time (transmission) <sup>Note 2</sup>	tHD:DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	0		0.45	μs
Setup time of stop condition	tSU:STO	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26			μs
Bus-free time	tBUF	2.7 V ≤ EVDD0 ≤ 5.5 V	0.5			μs

**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.

**Caution** The listed values are applicable even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

**Remark** The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.  
Cb = 120 pF, Rb = 1.1 kΩ

## 4. SMBus/PMBus™ mode (100 kHz Class)

(TA = -40 to +105°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	fCLK ≥ 1 MHz	10		100	kHz
Setup time of restart condition	tSU:STA		4.7			μs
Hold time <sup>Note 1</sup>	tHD:STA		4			μs
Hold time when SCLA0 is low	tLOW		4.7			μs
Hold time when SCLA0 is high	tHIGH		4			μs
Data setup time (reception)	tSU:DAT		250			ns
Data hold time (transmission) <sup>Note 2</sup>	tHD:DAT		0		3.45	μs
Setup time of stop condition	tSU:STO		4			μs
Clock/data falling time	tF				0.3	μs
Clock/data rising time	tR				1	μs
Bus-free time	tBUF		4.7			μs

**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.

**Caution** SMBus/PMBus™ communications are disabled when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1.

**Remark** The maximum value of communication line pull-up resistor (Rb) is as follows.  
Rb = 1.1 kΩ

5. SMBus/PMBus™ mode (400 kHz Class)

(TA = -40 to +105°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	fCLK ≥ 3.5 MHz	10		400	kHz
Setup time of restart condition	tSU:STA		0.6			μs
Hold time <sup>Note 1</sup>	tHD:STA		0.6			μs
Hold time when SCLA0 is low	tLOW		1.3			μs
Hold time when SCLA0 is high	tHIGH		0.6			μs
Data setup time (reception)	tSU:DAT		100			ns
Data hold time (transmission) <sup>Note 2</sup>	tHD:DAT		0		0.9	μs
Setup time of stop condition	tSU:STO		0.6			μs
Clock/data falling time	tF				0.3	μs
Clock/data rising time	tR				0.3	μs
Bus-free time	tBUF		1.3			μs

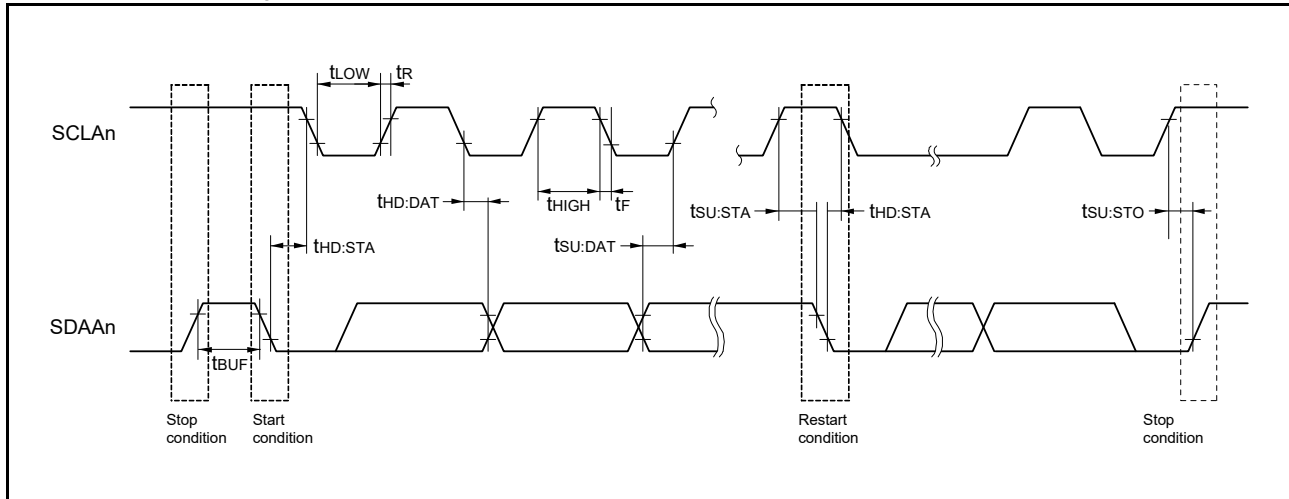
**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.

**Caution** SMBus/PMBus™ communications are disabled when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1.

**Remark** The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows. Cb = 400 pF, Rb = 1.1 kΩ

IICA serial transfer timing



**Remark** n = 0

## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

#### 1. Normal modes 1 and 2

(TA = -40 to +105°C, 2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, fCLK ≤ 32 MHz, reference voltage (+) = AVREFP (ADREFP[1:0] = 01B), reference voltage (-) = AVREFM (ADREFM = 1), target pins: ANI2 to ANI7, ANI16 to ANI30, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	fAD		1		32	MHz
Overall error <sup>Notes 1, 3, 4, 5</sup>	AINL	4.5 V ≤ AVREFP = VDD ≤ 5.5 V			±7.5	LSB
		2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±9.0	LSB
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±9.0	LSB
Conversion time <sup>Note 6</sup>	tCONV	4.5 V ≤ AVREFP = VDD ≤ 5.5 V	2			μs
		2.7 V ≤ AVREFP = VDD ≤ 5.5 V	2			μs
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V	2			μs
Zero-scale error <sup>Notes 1, 2, 3, 4, 5</sup>	EZS	4.5 V ≤ AVREFP = VDD ≤ 5.5 V			±0.17	%FSR
		2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
Full-scale error <sup>Notes 1, 2, 3, 4, 5</sup>	EFS	4.5 V ≤ AVREFP = VDD ≤ 5.5 V			±0.17	%FSR
		2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
Integral linearity error <sup>Notes 1, 4, 5</sup>	ILE	4.5 V ≤ AVREFP = VDD ≤ 5.5 V			±3.0	LSB
		2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±3.0	LSB
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±3.0	LSB
Differential linearity error <sup>Note 1</sup>	DLE	4.5 V ≤ AVREFP = VDD ≤ 5.5 V		±1.0		LSB
		2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±1.0		LSB
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V		±1.0		LSB
Analog input voltage	VAIN		0		AVREFP	V

**Note 1.** This value does not include the quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When pins ANI16 to ANI30 are selected as the conversion target, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

**Note 4.** The maximum values are as follows when VDD is selected for reference voltage (+) and VSS is selected for reference voltage (-).

Overall error: Add ±10 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.

Integral linearity error: Add ±4 LSB to the maximum value.

**Note 5.** When AVREFP < VDD, the maximum values are as follows.

Overall error: Add ±0.75 LSB × (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.

Zero-scale/full-scale error: Add ±0.018%FSR × (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.

Integral linearity error: Add ±0.2 LSB × (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.

**Note 6.** When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, the sampling time must be at least 5 μs. Accordingly, use normal mode 2 with the longer sampling time.

## 2. Normal modes 1 and 2 (advanced mode)

(TA = -40 to +105°C, 2.4 V ≤ AVREFF ≤ VDD ≤ 5.5 V, VSS = 0 V, fCLK ≤ 48 MHz, reference voltage (+) = AVREFF (ADREFP[1:0] = 01B), reference voltage (-) = AVREFM (ADREFM = 1), target pins: ANI2 to ANI7, ANI16 to ANI30, PGANote 1, S&HNote 1, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	fAD		1		48	MHz
Overall errorNotes 2, 4, 5, 6, 7, 9	AINL	4.5 V ≤ AVREFF = VDD ≤ 5.5 V			±7.5	LSB
		4.5 V ≤ AVREFF = VDD ≤ 5.5 V, and when the sample & hold circuit is in use (0.25 V ≤ VAIN ≤ VDD - 0.25 V)			±8.5	LSB
		2.7 V ≤ AVREFF = VDD ≤ 5.5 V			±9.0	LSB
		2.7 V ≤ AVREFF = VDD ≤ 5.5 V, and when the sample & hold circuit is in use (0.25 V ≤ VAIN ≤ VDD - 0.25 V)			±10.0	LSB
		2.4 V ≤ AVREFF = VDD ≤ 5.5 V			±9.0	LSB
Conversion timeNotes 7, 8	tCONV	4.5 V ≤ AVREFF = VDD ≤ 5.5 V	1			μs
		2.7 V ≤ AVREFF = VDD ≤ 5.5 V	1			μs
		2.4 V ≤ AVREFF = VDD ≤ 5.5 V	1.5			μs
Zero-scale error Notes 2, 3, 4, 5, 6, 7, 9	EZS	4.5 V ≤ AVREFF = VDD ≤ 5.5 V			±0.17	%FSR
		2.7 V ≤ AVREFF = VDD ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AVREFF = VDD ≤ 5.5 V			±0.21	%FSR
Full-scale error Notes 2, 3, 4, 5, 6, 7, 9	EFS	4.5 V ≤ AVREFF = VDD ≤ 5.5 V			±0.17	%FSR
		2.7 V ≤ AVREFF = VDD ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AVREFF = VDD ≤ 5.5 V			±0.21	%FSR
Integral linearity errorNotes 2, 5, 6	ILE	4.5 V ≤ AVREFF = VDD ≤ 5.5 V			±3.0	LSB
		2.7 V ≤ AVREFF = VDD ≤ 5.5 V			±3.0	LSB
		2.4 V ≤ AVREFF = VDD ≤ 5.5 V			±3.0	LSB
Differential linearity errorNote 2	DLE	4.5 V ≤ AVREFF = VDD ≤ 5.5 V		±1.0		LSB
		2.7 V ≤ AVREFF = VDD ≤ 5.5 V		±1.0		LSB
		2.4 V ≤ AVREFF = VDD ≤ 5.5 V		±1.0		LSB
Analog input voltage	VAIN		0		AVREFF	V

(Notes are listed on the next page.)

- Note 1.** If the sample & hold circuit or PGA is to be A/D converted, VDD must be at least 2.7 V.
- Note 2.** This value does not include the quantization error ( $\pm 1/2$  LSB).
- Note 3.** This value is indicated as a ratio (%FSR) to the full-scale value.
- Note 4.** When pins ANI16 to ANI30 are selected as the conversion target, the maximum values are as follows.  
Overall error: Add  $\pm 3$  LSB to the maximum value.  
Zero-scale/full-scale error: Add  $\pm 0.04\%$ FSR to the maximum value.
- Note 5.** The maximum values are as follows when VDD is selected for reference voltage (+) and VSS is selected for reference voltage (-).  
Overall error: Add  $\pm 10$  LSB to the maximum value.  
Zero-scale/full-scale error: Add  $\pm 0.25\%$ FSR to the maximum value.  
Integral linearity error: Add  $\pm 4$  LSB to the maximum value.
- Note 6.** When AVREFP < VDD, the maximum values are as follows.  
Overall error: Add  $\pm 0.75$  LSB  $\times$  (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.  
Zero-scale/full-scale error: Add  $\pm 0.018\%$ FSR  $\times$  (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.  
Integral linearity error: Add  $\pm 0.2$  LSB  $\times$  (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.
- Note 7.** Add the following values to the listed values in the cases below.
- 7 fAD when the conversion target includes low-speed conversion ANI (ANI16 to ANI30)
  - 12 fAD when the conversion target includes the PGA with the gain of  $\times 4$  to  $\times 16$ .
  - 43 fAD when the conversion target includes the PGA with the gain of  $\times 32$ .
- Note 8.** When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, the sampling time must be at least 5  $\mu$ s. Accordingly, use normal mode 2 with the longer sampling time.
- Note 9.** When the PGA is selected as the conversion target, the maximum values are as follows. For details, see **2.6.5 PGA characteristics**.  
Overall error: Add input offset voltage and amplification rate error of the PGA to the maximum value.  
Zero-scale error: Add input offset voltage of the PGA to the maximum value.  
Full-scale error: Add amplification rate error of the PGA to the maximum value.

## 3. Low-voltage modes 1 and 2

(TA = -40 to +105°C, 1.6 V ≤ AVREFF ≤ VDD ≤ 5.5 V, VSS = 0 V, fCLK ≤ 32 MHz,  
reference voltage (+) = AVREFF (ADREFP[1:0] = 01B), reference voltage (-) = AVREFM (ADREFM = 1),  
target pins: ANI2 to ANI7, ANI16 to ANI30, internal reference voltage<sup>Note 1</sup>, and temperature sensor output voltage<sup>Note 1</sup>)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	fAD		1		24	MHz
Overall error <sup>Notes 2, 4, 5, 6</sup>	AINL	2.7 V ≤ AVREFF = VDD ≤ 5.5 V			±9.0	LSB
		2.4 V ≤ AVREFF = VDD ≤ 5.5 V			±9.0	LSB
		1.8 V ≤ AVREFF = VDD ≤ 5.5 V			±11.5	LSB
		1.6 V ≤ AVREFF = VDD ≤ 5.5 V			±12.0	LSB
Conversion time <sup>Note 7</sup>	tCONV	2.7 V ≤ AVREFF = VDD ≤ 5.5 V	3.33			μs
		2.4 V ≤ AVREFF = VDD ≤ 5.5 V	5.00			μs
		1.8 V ≤ AVREFF = VDD ≤ 5.5 V	10.00			μs
		1.6 V ≤ AVREFF = VDD ≤ 5.5 V	20.00			μs
Zero-scale error <sup>Notes 2, 3, 4, 5, 6</sup>	Ezs	2.7 V ≤ AVREFF = VDD ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AVREFF = VDD ≤ 5.5 V			±0.21	%FSR
		1.8 V ≤ AVREFF = VDD ≤ 5.5 V			±0.27	%FSR
		1.6 V ≤ AVREFF = VDD ≤ 5.5 V			±0.28	%FSR
Full-scale error <sup>Notes 2, 3, 4, 5, 6</sup>	EFS	2.7 V ≤ AVREFF = VDD ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AVREFF = VDD ≤ 5.5 V			±0.21	%FSR
		1.8 V ≤ AVREFF = VDD ≤ 5.5 V			±0.27	%FSR
		1.6 V ≤ AVREFF = VDD ≤ 5.5 V			±0.28	%FSR
Integral linearity error <sup>Notes 2, 5, 6</sup>	ILE	2.7 V ≤ AVREFF = VDD ≤ 5.5 V			±4.0	LSB
		2.4 V ≤ AVREFF = VDD ≤ 5.5 V			±4.0	LSB
		1.8 V ≤ AVREFF = VDD ≤ 5.5 V			±4.5	LSB
		1.6 V ≤ AVREFF = VDD ≤ 5.5 V			±4.5	LSB
Differential linearity error <sup>Note 2</sup>	DLE	2.7 V ≤ AVREFF = VDD ≤ 5.5 V		±1.5		LSB
		2.4 V ≤ AVREFF = VDD ≤ 5.5 V		±1.5		LSB
		1.8 V ≤ AVREFF = VDD ≤ 5.5 V		±2.0		LSB
		1.6 V ≤ AVREFF = VDD ≤ 5.5 V		±2.0		LSB
Analog input voltage	VAIN		0		AVREFF	V

(Notes are listed on the next page.)

- Note 1.** If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VDD must be at least 1.8 V.
- Note 2.** This value does not include the quantization error ( $\pm 1/2$  LSB).
- Note 3.** This value is indicated as a ratio (%FSR) to the full-scale value.
- Note 4.** When pins ANI16 to ANI30 are selected as the conversion target, the maximum values are as follows.  
Overall error: Add  $\pm 3$  LSB to the maximum value.  
Zero-scale/full-scale error: Add  $\pm 0.04\%$ FSR to the maximum value.
- Note 5.** The maximum values are as follows when VDD is selected for reference voltage (+) and VSS is selected for reference voltage (-).  
Overall error: Add  $\pm 10$  LSB to the maximum value.  
Zero-scale/full-scale error: Add  $\pm 0.25\%$ FSR to the maximum value.  
Integral linearity error: Add  $\pm 4$  LSB to the maximum value.
- Note 6.** When  $AV_{REFP} < V_{DD}$ , the maximum values are as follows.  
Overall error: Add  $\pm 0.75$  LSB  $\times$  (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.  
Zero-scale/full-scale error: Add  $\pm 0.018\%$ FSR  $\times$  (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.  
Integral linearity error: Add  $\pm 0.2$  LSB  $\times$  (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.
- Note 7.** When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, the sampling time must be at least 5  $\mu$ s. Accordingly, use low-voltage mode 2 with the longer sampling time and the conversion clock (fAD) with a frequency of no more than 16 MHz.



## 4. Low-voltage modes 1 and 2 (advanced mode)

(TA = -40 to +105°C, 1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, fCLK ≤ 48 MHz, reference voltage (+) = AVREFP (ADREFP[1:0] = 01B), reference voltage (-) = AVREFM (ADREFM = 1), target pins: ANI2 to ANI7, ANI16 to ANI30, PGANote 1, S&HNote 1, internal reference voltageNote 2, and temperature sensor output voltageNote 2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	fAD		1		24	MHz
Overall errorNotes 3, 5, 6, 7, 8, 9	AINL	4.5 V ≤ AVREFP = VDD ≤ 5.5 V, and when the sample & hold circuit is in use (0.25 V ≤ VAIN ≤ VDD - 0.25 V)			±10.0	LSB
		2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±9.0	LSB
		2.7 V ≤ AVREFP = VDD ≤ 5.5 V, and when the sample & hold circuit is in use (0.25 V ≤ VAIN ≤ VDD - 0.25 V)			±10.0	LSB
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±9.0	LSB
		1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±11.5	LSB
		1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±12.0	LSB
Conversion timeNote 8	tCONV	2.7 V ≤ AVREFP = VDD ≤ 5.5 V	3.33			μs
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V	5.00			μs
		1.8 V ≤ AVREFP = VDD ≤ 5.5 V	10.00			μs
		1.6 V ≤ AVREFP = VDD ≤ 5.5 V	20.00			μs
Zero-scale error Notes 3, 4, 5, 6, 7, 8, 9	Ezs	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
		1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±0.27	%FSR
		1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±0.28	%FSR
Full-scale error Notes 3, 4, 5, 6, 7, 8, 9	EFS	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
		1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±0.27	%FSR
		1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±0.28	%FSR
Integral linearity errorNotes 3, 6, 7	ILE	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±4.0	LSB
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±4.0	LSB
		1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±4.5	LSB
		1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±4.5	LSB
Differential linearity errorNote 3	DLE	2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±1.5		LSB
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V		±1.5		LSB
		1.8 V ≤ AVREFP = VDD ≤ 5.5 V		±2.0		LSB
		1.6 V ≤ AVREFP = VDD ≤ 5.5 V		±2.0		LSB
Analog input voltage	VAIN		0		AVREFP	V

(Notes are listed on the next page.)

- Note 1.** If the sample & hold circuit or PGA is to be A/D converted, VDD must be at least 2.7 V.
- Note 2.** If the internal reference voltage or temperature sensor output voltage is to be A/D converted, VDD must be at least 1.8 V.
- Note 3.** This value does not include the quantization error ( $\pm 1/2$  LSB).
- Note 4.** This value is indicated as a ratio (%FSR) to the full-scale value.
- Note 5.** When pins AN16 to AN30 are selected as the conversion target, the maximum values are as follows.  
Overall error: Add  $\pm 3$  LSB to the maximum value.  
Zero-scale/full-scale error: Add  $\pm 0.04\%$ FSR to the maximum value.
- Note 6.** The maximum values are as follows when VDD is selected for reference voltage (+) and VSS is selected for reference voltage (-).  
Overall error: Add  $\pm 10$  LSB to the maximum value.  
Zero-scale/full-scale error: Add  $\pm 0.25\%$ FSR to the maximum value.  
Integral linearity error: Add  $\pm 4$  LSB to the maximum value.
- Note 7.** When  $AV_{REFP} < V_{DD}$ , the maximum values are as follows.  
Overall error: Add  $\pm 0.75$  LSB  $\times$  (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.  
Zero-scale/full-scale error: Add  $\pm 0.018\%$ FSR  $\times$  (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.  
Integral linearity error: Add  $\pm 0.2$  LSB  $\times$  (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.
- Note 8.** When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, the sampling time must be at least 5  $\mu$ s. Accordingly, use low-voltage mode 2 with the longer sampling time and the conversion clock (fAD) with a frequency of no more than 16 MHz.
- Note 9.** When the PGA is selected as the conversion target, the maximum values are as follows. For details, see **2.6.5 PGA characteristics**.  
Overall error: Add input offset voltage and amplification rate error of the PGA to the maximum value.  
Zero-scale error: Add input offset voltage of the PGA to the maximum value.  
Full-scale error: Add amplification rate error of the PGA to the maximum value.

## 5. When the internal reference voltage is selected as reference voltage (+)

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V, low-voltage modes 1 and 2, fCLK ≤ 32 MHz<sup>Note 1</sup>, fCLK ≤ 48 MHz<sup>Note 2</sup>, reference voltage (+) = internal reference voltage (ADREFP[1:0] = 10B), reference voltage (-) = AVREFM (ADREFM = 1))

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8			Bit
Conversion clock	fAD	1.6 V ≤ VDD ≤ 5.5 V	1		2	MHz
Zero-scale error <sup>Notes 3, 4, 6</sup>	EZS	1.6 V ≤ VDD ≤ 5.5 V			±0.6	%FSR
Integral linearity error <sup>Notes 3, 6</sup>	ILE	1.6 V ≤ VDD ≤ 5.5 V			±2.0	LSB
Differential linearity error <sup>Note 3</sup>	DLE	1.6 V ≤ VDD ≤ 5.5 V		±1.0		LSB
Analog input voltage	VAIN		0		VBGR Note 5	V

**Note 1.** This applies when the advanced mode is disabled.

**Note 2.** This applies when the advanced mode is enabled.

**Note 3.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 4.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 5.** Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

**Note 6.** When reference voltage (-) is selected as VSS, the maximum values are as follows.

Zero-scale error: Add  $\pm 0.35\%$ FSR to the maximum value.

Integral linearity error: Add  $\pm 0.5$  LSB to the maximum value.

### 2.6.2 Temperature sensor/internal reference voltage characteristics

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	VTMPS25	ADS register is set to 80H, TA = +25°C		1.05		V
Internal reference voltage	VBGR	ADS register is set to 81H	1.40	1.48	1.56	V
Temperature coefficient	FVTMPS	Temperature dependency of the temperature sensor voltage		-3.3		mV/°C
Operation stabilization wait time	tAMP		5			μs

### 2.6.3 D/A converter characteristics

(TA = -40 to +105°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES	DAC0, DAC1 (DACONF = 0)			10	Bit
		DAC1 (DACONF = 1), DAC2			8	Bit
Overall error	AINL	Rload = 8 MΩ			±2.5	LSB
Differential non-linearity error	ADNL				±1.0	LSB
Settling time	tSET	Cload = 20 pF when DAC0 is output			6	μs
		During full code conversion using CMP reference			3	μs
		During 1LSB code conversion using CMP reference			1	μs

**Caution** The voltage on the ANO0 to ANO2 pins must not exceed EVDD0.

### 2.6.4 Comparator characteristics

(TA = -40 to +105°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage range	IVREF	IVREF0 pin, IVREF1 pin input	0		EVDD0	V
	IVCMP	IVCMP0, IVCMP1, IVCMP2, IVCMP3 pin input	0		EVDD0	V
Output delay	td	Input amplitude ±100 mV		50	100	ns
Offset voltage	—			±5	±40	mV
Operation stabilization time <sup>Note</sup>	tCMP		1			μs
Input channel switching stabilization wait time	—		0.3			μs

**Note** The listed values indicate the time until the DC/AC characteristics of the comparator are satisfied following enabling of the comparator operation (CnENB = 1).

## 2.6.5 PGA characteristics

(TA = -40 to +105°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input offset voltage	VIOPGA					±10	mV
Input voltage range <sup>Note 1</sup>	VIPGA			0		0.9 × VDD/ amplification rate	V
Amplification rate error		×4, ×8				±1	%
		×16				±1.5	%
		×32				±2	%
Slew rate <sup>Note 1</sup>	SRRPGA	Rising Vin = VDD × 0.1/ amplification rate to VDD × 0.9/ amplification rate 10 to 90% of output amplitude	4.0 V ≤ VDD ≤ 5.5 V	Other than ×32	3.5		V/μs
			4.0 V ≤ VDD ≤ 5.5 V	×32	3		
			2.7 V ≤ VDD ≤ 4.0 V		0.5		
	SFPGA	Falling Vin = VDD × 0.1/ amplification rate to VDD × 0.9/ amplification rate 90 to 10% of output amplitude	4.0 V ≤ VDD ≤ 5.5 V	Other than ×32	3.5		
			4.0 V ≤ VDD ≤ 5.5 V	×32	3		
			2.7 V ≤ VDD ≤ 4.0 V		0.5		
Operation stabilization wait time <sup>Note 2</sup>	tPGA	×4, ×8				5	μs
		×16, ×32				10	μs

**Note 1.** A voltage of EVDD0 is supplied to the PGA10 to PGA13 pins.

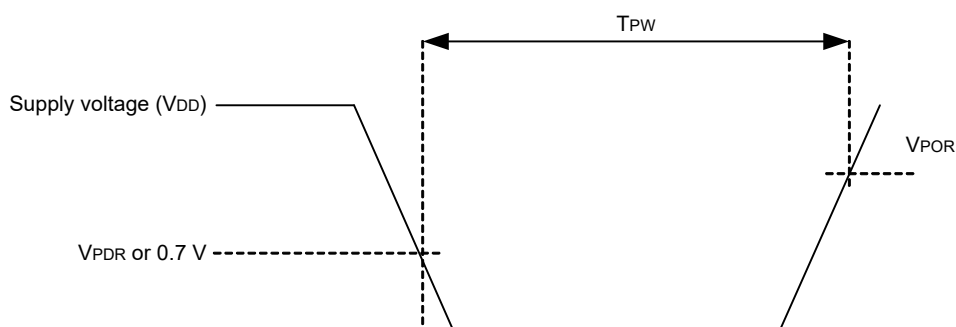
**Note 2.** The listed values indicate the time until the DC/AC characteristics of PGA operation are satisfied following enabling of the PGA operation (PGAEN = 1).

### 2.6.6 POR circuit characteristics

(TA = -40 to +105°C, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	V <sub>POR</sub> , V <sub>PDR</sub>		1.43	1.50	1.57	V
Minimum pulse width <sup>Note</sup>	TPW		300			μs

**Note** This width is the minimum time required for a POR reset when V<sub>DD</sub> falls below V<sub>PDR</sub>. This width is also the minimum time required for a POR reset from when V<sub>DD</sub> falls below 0.7 V to when V<sub>DD</sub> exceeds V<sub>POR</sub> in the STOP mode or while the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 2.6.7 LVD circuit characteristics

### 1. LVD detection voltage in the LVD0 reset mode and interrupt mode

(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit		
Detection voltage	Supply voltage level	VLVD00	The power supply voltage is rising.	3.84	3.96	4.08	V		
			The power supply voltage is falling.	3.76	3.88	4.00	V		
		VLVD01	The power supply voltage is rising.	2.88	2.97	3.06	V		
			The power supply voltage is falling.	2.82	2.91	3.00	V		
		VLVD02	The power supply voltage is rising.	2.59	2.67	2.75	V		
			The power supply voltage is falling.	2.54	2.62	2.70	V		
		VLVD03	The power supply voltage is rising.	2.31	2.38	2.45	V		
			The power supply voltage is falling.	2.26	2.33	2.40	V		
		VLVD04	The power supply voltage is rising.	1.84	1.90	1.95	V		
			The power supply voltage is falling.	1.80	1.86	1.91	V		
		VLVD05	The power supply voltage is rising.	1.64	1.69	1.74	V		
			The power supply voltage is falling.	1.60	1.65	1.70	V		
		Minimum pulse width		tLW		500			μs
		Detection delay time						500	μs

## 2. LVD detection voltage in the LVD1 reset mode and interrupt mode

(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Detection voltage	Supply voltage level	VLVD10	The power supply voltage is rising.	4.08	4.16	4.24	V
			The power supply voltage is falling.	4.00	4.08	4.16	V
		VLVD11	The power supply voltage is rising.	3.88	3.96	4.04	V
			The power supply voltage is falling.	3.80	3.88	3.96	V
		VLVD12	The power supply voltage is rising.	3.68	3.75	3.82	V
			The power supply voltage is falling.	3.60	3.67	3.74	V
		VLVD13	The power supply voltage is rising.	3.48	3.55	3.62	V
			The power supply voltage is falling.	3.40	3.47	3.54	V
		VLVD14	The power supply voltage is rising.	3.28	3.35	3.42	V
			The power supply voltage is falling.	3.20	3.27	3.34	V
		VLVD15	The power supply voltage is rising.	3.07	3.13	3.19	V
			The power supply voltage is falling.	3.00	3.06	3.12	V
		VLVD16	The power supply voltage is rising.	2.91	2.97	3.03	V
			The power supply voltage is falling.	2.85	2.91	2.97	V
		VLVD17	The power supply voltage is rising.	2.76	2.82	2.87	V
			The power supply voltage is falling.	2.70	2.76	2.81	V
		VLVD18	The power supply voltage is rising.	2.61	2.66	2.71	V
			The power supply voltage is falling.	2.55	2.60	2.65	V
		VLVD19	The power supply voltage is rising.	2.45	2.50	2.55	V
			The power supply voltage is falling.	2.40	2.45	2.50	V
		VLVD110	The power supply voltage is rising.	2.35	2.40	2.45	V
			The power supply voltage is falling.	2.30	2.35	2.40	V
		VLVD111	The power supply voltage is rising.	2.25	2.30	2.34	V
			The power supply voltage is falling.	2.20	2.25	2.29	V
		VLVD112	The power supply voltage is rising.	2.15	2.20	2.24	V
			The power supply voltage is falling.	2.10	2.15	2.19	V
		VLVD113	The power supply voltage is rising.	2.05	2.09	2.13	V
			The power supply voltage is falling.	2.00	2.04	2.08	V
		VLVD114	The power supply voltage is rising.	1.94	1.98	2.02	V
			The power supply voltage is falling.	1.90	1.94	1.98	V
		VLVD115 Note	The power supply voltage is rising.	1.84	1.88	1.91	V
			The power supply voltage is falling.	1.80	1.84	1.87	V
		VLVD116 Note	The power supply voltage is rising.	1.74	1.78	1.81	V
			The power supply voltage is falling.	1.70	1.74	1.77	V
VLVD117 Note	The power supply voltage is rising.	1.64	1.67	1.70	V		
	The power supply voltage is falling.	1.60	1.63	1.66	V		
Minimum pulse width	tLW		500			μs	
Detection delay					500	μs	

**Note** This setting can only be used when LVD0 is disabled.



### 2.6.8 Power supply voltage rising slope characteristics

(TA = -40 to +105°C, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power voltage rising slope	SVDD				54	V/ms

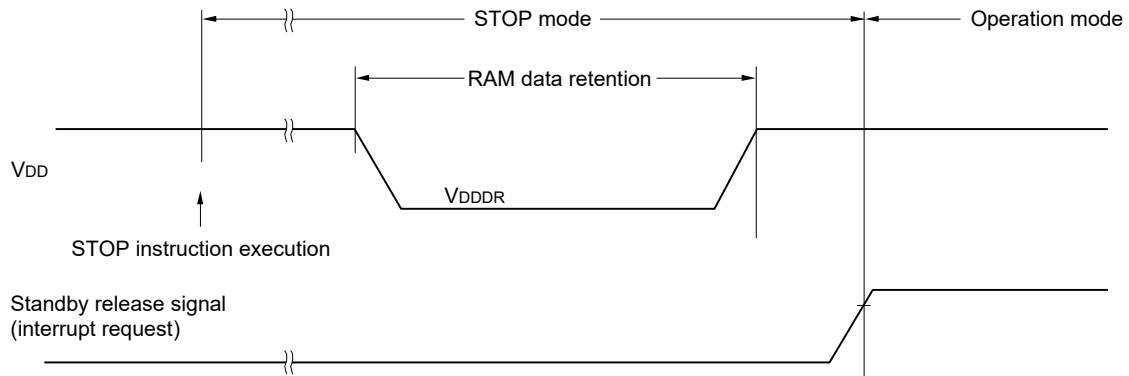
**Caution** Make sure to keep the internal reset state by the LVD0 circuit or an external reset until VDD reaches the operating voltage range shown in AC characteristics.

### 2.7 RAM Data Retention Characteristics

(TA = -40 to +105°C, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention power voltage	VDDDR		1.43 <sup>Note</sup>		5.5	V

**Note** This voltage depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.



### 2.8 Flash Memory Programming Characteristics

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
CPU/peripheral hardware clock frequency	fCLK		1		48	MHz	
Number of code flash rewrites <sup>Notes 1, 2, 3</sup>	Cerwr	Retained for 10 years TA = 85°C	10,000			Times	
		Retained for 20 years TA = 85°C	1,000				
Number of data flash rewrites <sup>Notes 1, 2, 3</sup>		Retained for 1 year TA = 25°C		1,000,000			
		Retained for 5 years TA = 85°C	100,000				
		Retained for 20 years TA = 85°C	10,000				

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**Note 2.** The listed numbers of times apply when using the flash memory programmer and the Renesas Electronics self-programming library.

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 1. Code flash memory

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	fCLK = 1 MHz			fCLK = 2 MHz, 3 MHz			4 MHz ≤ fCLK < 8 MHz			8 MHz ≤ fCLK < 32 MHz			fCLK = 32 MHz			fCLK = 48 MHz			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time	4 bytes	tP4	—	75.8	666.6	—	51.5	469.7	—	41.9	387.3	—	37.2	347.4	—	34.2	322.3	—	33.9	319.7	μs
Erase time	2 Kbytes	tE2K	—	10.4	312.2	—	7.7	258.5	—	6.4	231.8	—	5.8	218.4	—	5.6	214.4	—	5.6	213.9	ms
Blank checking time	4 bytes	tBC4	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	—	—	8.1	μs
	2 Kbytes	tBC2K	—	—	2618.9	—	—	1309.5	—	—	658.3	—	—	332.8	—	—	234.1	—	—	223.19	μs
Time taken to forcibly stop erasure		tSED	—	—	19.0	—	—	14.5	—	—	12.3	—	—	11.1	—	—	10.4	—	—	10.3	μs
Security setting time		tAWSSAS	—	18.2	526.4	—	14.4	469.3	—	12.6	441.1	—	11.6	427.1	—	11.3	422.6	—	11.3	422.1	ms
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	μs

**Caution** The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

## 2. Data flash memory

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	fCLK = 1 MHz			fCLK = 2 MHz, 3 MHz			4 MHz ≤ fCLK < 8 MHz			8 MHz ≤ fCLK < 32 MHz			fCLK = 32 MHz			fCLK = 48 MHz			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time	1 byte	tP4	—	75.8	666.6	—	51.51	469.7	—	41.9	387.34	—	37.24	347.4	—	34.2	322.3	—	33.92	319.7	μs
Erase time	256 bytes	tE2K	—	7.8	259.2	—	6.4	232.0	—	5.8	218.5	—	5.5	211.8	—	5.4	209.7	—	5.3	209.5	ms
Blank checking time	1 byte	tBC4	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	—	—	8.1	μs
	256 bytes	tBC2K	—	—	1326.1	—	—	663.1	—	—	335.1	—	—	171.2	—	—	121.0	—	—	115.5	μs
Time taken to forcibly stop erasure		tSED	—	—	19.0	—	—	14.5	—	—	12.3	—	—	11.1	—	—	10.4	—	—	10.3	μs
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	μs
Time until reading starts following setting DFLEN to 1		—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	ns

**Caution** The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

### 2.9 Dedicated Flash Memory Programmer Communication (UART)

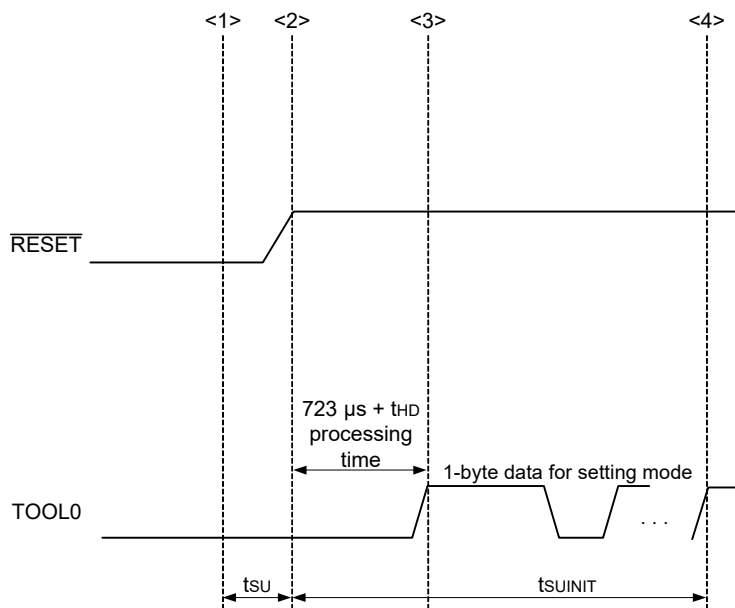
(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

### 2.10 Timing of Entry to Flash Memory Programming Modes

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Time to complete the communication for the initial setting after the external reset is released	tsuINIT	POR and LVD reset must be released before the external reset is released			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	tsu	POR and LVD reset must be released before the external reset is released	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (the processing time of the firmware to control the flash memory is not included)	tHD	POR and LVD reset must be released before the external reset is released	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released. Note that the POR and LVD reset must be released before the external reset is released.
- <3> The TOOL0 pin is set to the high level.
- <4> The baud rate setting is complete upon UART reception.

**Remark** tsuINIT: The time during which the communications for the initial setting must be completed within 100 ms after the external reset is released.

tsu: Time to release the external reset after the TOOL0 pin is set to the low level

tHD: Time to hold the TOOL0 pin at the low level after the external reset is released. It does not include the processing time of the firmware to control the flash memory.

### 3. Electrical Characteristics (TA = -40 to +125°C)

This section describes the electrical characteristics of the following type of products.

- 4C: Industrial applications, TA = -40 to +125°C  
R7F101Gxx4Cxx

**Caution 1.** RL78 microcontrollers have on-chip debugging functionality for use in the development and evaluation of user systems. Do not use on-chip debugging with products designated as part of mass production, because using this function may cause the guaranteed number of times the flash memory is rewritten to be exceeded, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when on-chip debugging is used with products designated as part of mass production.

**Caution 2.** For products that do not have an EVDD0 or EVSS0 pin, read EVDD0 as VDD, and EVSS0 as VSS.

**Caution 3.** The present pins differ depending on the products. For details, see 2.1 Functions of Port Pins through 2.2.1 Functions for each product in the RL78/G24 User's Manual.

**Remark** If you use a product under the condition TA = -40 to +105°C, see 2. Electrical Characteristics (TA = -40 to +105°C).

### 3.1 Absolute Maximum Ratings

(1/2)

Item	Symbols	Conditions	Ratings	Unit
Supply voltage	VDD		-0.5 to +6.5	V
	EVDD0		-0.5 to +6.5	V
	EVSS0		-0.5 to +0.3	V
REGC pin input voltage	VIREGC	REGC	-0.3 to +2.1 and -0.3 to VDD + 0.3 <sup>Note 1</sup>	V
Input voltage	Vi1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P140, P141, P146, P147	-0.3 to EVDD0 + 0.3 and -0.3 to VDD + 0.3 <sup>Note 2</sup>	V
	Vi2	P60, P61 (N-ch open drain)	-0.3 to +6.5	V
	Vi3	P20 to P27, P121 to P124, P137, EXCLK, EXCLKS, RESET	-0.3 to VDD + 0.3 <sup>Note 2</sup>	V
Output voltage	Vo1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147	-0.3 to EVDD0 + 0.3 and -0.3 to VDD + 0.3 <sup>Note 2</sup>	V
	Vo2	P20 to P27, P121, P122	-0.3 to VDD + 0.3 <sup>Note 2</sup>	V
Analog input voltage	VAI1	ANI16 to ANI30	-0.3 to EVDD0 + 0.3 and -0.3 to AVREFP + 0.3 <b>Notes 2, 3</b>	V
	VAI2	ANI0 to ANI7	-0.3 to VDD + 0.3 and -0.3 to AVREFP + 0.3 <b>Notes 2, 3</b>	V

**Note 1.** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). The listed value is the absolute maximum rating of the REGC pin. Do not apply a specific voltage to this pin.

**Note 2.** This voltage must be no higher than 6.5 V.

**Note 3.** The voltage on a pin in use for A/D conversion must not exceed AVREFP + 0.3.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark 1.** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

**Remark 2.** AVREFP refers to the positive reference voltage of the A/D converter.

**Remark 3.** The reference voltage is Vss.

(2/2)

Item	Symbols	Conditions		Ratings	Unit
High-level output current	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P62, P63, P70 to P77, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P121, P122	-5	mA
		Total of all pins		-20	mA
Low-level output current	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77, P146, P147	100	mA
	IOL2	Per pin	P20 to P27, P121, P122	10	mA
		Total of all pins		20	mA
	Ambient operating temperature	TA	In normal operation mode		-40 to +125
In flash memory programming mode			-40 to +125	°C	
Storage temperature	Tstg			-65 to +150	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

## 3.2 Characteristics of the Oscillators

### 3.2.1 Characteristics of the X1 and XT1 oscillators

(TA = -40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time <sup>Note</sup>	Ceramic resonator/ crystal resonator		0.05		1	μs
XT1 clock oscillation frequency (f <sub>XT</sub> ) <sup>Note</sup>	Crystal resonator			32.768		kHz

**Note** The listed time and frequency indicate permissible ranges of the oscillators. For actual applications, request the resonator manufacturer for evaluation of the resonators on the oscillator circuit mounted on a board so you can use appropriate values. Refer to **3.4 AC Characteristics** for instruction execution time.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Sufficiently evaluate the oscillation stabilization time with the resonator to be used, and then specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS).



### 3.2.2 Characteristics of the on-chip oscillators

(TA = -40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f <sub>ih</sub>			1		48	MHz
High-speed on-chip oscillator clock frequency accuracy <sup>Note 1</sup>		HIPREC = 1	+105 to +125°C	-1.5		+1.5	%
			+85 to +105°C	-1.5		+1.5	%
			-20 to +85°C	-1.0		+1.0	%
			-40 to -20°C	-1.5		+1.5	%
		HIPREC = 0 <sup>Note 4</sup>	-15		0	%	
High-speed on-chip oscillator clock correction resolution					0.05		%
Middle-speed on-chip oscillator clock frequency <sup>Note 2</sup>	f <sub>im</sub>			1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy <sup>Note 1</sup>				-12		+12	%
Middle-speed on-chip oscillator clock correction resolution					0.15		%
Middle-speed on-chip oscillator frequency temperature coefficient						±0.17 <sup>Note 3</sup>	%/°C
Low-speed on-chip oscillator clock frequency <sup>Note 2</sup>	f <sub>il</sub>				32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy <sup>Note 1</sup>				-15		+15	%
Low-speed on-chip oscillator clock correction resolution					0.3		%
Low-speed on-chip oscillator frequency temperature coefficient						±0.21 <sup>Note 3</sup>	%/°C

**Note 1.** The accuracy values were obtained in testing of this product.

**Note 2.** The listed values only indicate the characteristics of the oscillators. Refer to **3.4 AC Characteristics** for instruction execution time.

**Note 3.** These values were obtained in the evaluation.

**Note 4.** This condition applies when the setting of the FRQSEL3 bit is 1.

### 3.2.3 Characteristics of the PLL oscillator

(TA = -40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
PLL input frequency	f <sub>PLLIN</sub>	High-speed system clock (f <sub>MX</sub> ) or high-speed on-chip oscillator clock (f <sub>IH</sub> )		8		MHz
PLL output frequency	f <sub>PLL</sub>	f <sub>PLLIN</sub> × 12		96		MHz
		f <sub>PLLIN</sub> × 8		64		MHz
Lock-up wait time		Wait time after PLL output is enabled until the output frequency is stabilized	50			μs
Interval wait time		Wait time after PLL stop until PLL operation is set again	4			μs
Setting wait time		Required wait time after the PLL input clock is stabilized and the PLL setting is determined until startup settings are made	1			μs

### 3.3 DC Characteristics

#### 3.3.1 Pin characteristics

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Allowable high-level output current <sup>Note 1</sup>	IOH1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70-P77, P120, P130, P140, P141, P146, P147	2.7 V ≤ EVDD0 ≤ 5.5 V			-10.0 <b>Note 2</b>	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (when duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EVDD0 ≤ 5.5 V			-24.0	mA
			2.7 V ≤ EVDD0 < 4.0 V			-10.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P62, P63, P70 to P77, P146, P147 (when duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EVDD0 ≤ 5.5 V			-42.0	mA
			2.7 V ≤ EVDD0 < 4.0 V			-17.0	mA
	Total of all pins (when duty ≤ 70% <sup>Note 3</sup> )	2.7 V ≤ EVDD0 ≤ 5.5 V			-54.0	mA	
	IOH2	Per pin for P20 to P27, P121, P122	4.0 V ≤ VDD ≤ 5.5 V			-3.0 <b>Note 2</b>	mA
			2.7 V ≤ VDD < 4.0 V			-1.0 <b>Note 2</b>	mA
		Total of all pins (when duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ VDD ≤ 5.5 V			-14	mA
			2.7 V ≤ VDD < 4.0 V			-8	mA

**Note 1.** Device operation is guaranteed at the listed currents even if current is flowing from the EVDD0 or VDD pin to an output pin.

**Note 2.** The combination of these and other pins must not exceed the total current value.

**Note 3.** The listed output current values apply when the duty cycle is no greater than 70%.

Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle (%).

- Total output current from all pins =  $(I_{OH} \times 0.7)/(n \times 0.01)$

Example when  $I_{OH} = -10.0$  mA,  $n = 80\%$

Total output current from all pins =  $(-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7$  mA

Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. No current higher than the absolute maximum rating must not flow into a single pin.

**Caution** The following pins do not output high-level signals in the N-ch open-drain mode.

**P00, P02 to P04, P10 to P15, P17, P30, P50, P51, P55, and P71 to P74**

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(2/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Allowable low-level output current <sup>Note 1</sup>	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147			17.0 <b>Note 2</b>	mA
		Per pin for P60, P61	2.7 V ≤ EVDD0 < 5.5 V		15.0 <b>Note 2</b>	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (when duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EVDD0 ≤ 5.5 V		34.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		15.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P55, P60 to P63, P70 to P77, P146, P147 (when duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EVDD0 ≤ 5.5 V		34.0	mA
	2.7 V ≤ EVDD0 < 4.0 V			15.0	mA	
	Total of all pins (when duty ≤ 70% <sup>Note 3</sup> )			68.0	mA	
	IOL2	Per pin for P20 to P27, P121, P122	4.0 V ≤ VDD ≤ 5.5 V		8.5 <b>Note 2</b>	mA
			2.7 V ≤ VDD < 4.0 V		1.5 <b>Note 2</b>	mA
		Total of all pins (when duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ VDD ≤ 5.5 V		14.0	mA
2.7 V ≤ VDD < 4.0 V				14.0	mA	

**Note 1.** Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the EVSS0 or VSS pin.

**Note 2.** The combination of these and other pins must not exceed the total current value.

**Note 3.** The listed output current values apply when the duty cycle is no greater than 70%.

Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle (%).

- Total output current from all pins = (I<sub>OH</sub> × 0.7)/(n × 0.01)

Example when I<sub>OH</sub> = -10.0 mA, n = 80%

$$\text{Total output current from all pins} = (-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7 \text{ mA}$$

Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. No current higher than the absolute maximum rating must not flow into a single pin.

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(3/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input voltage, high	V <sub>IH1</sub>	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer	0.8 EVDD0		EVDD0	V
	V <sub>IH2</sub>	P01, P03, P04, P10, P11, P14 to P17, P30, P50, P55, P73	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2		EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0		EVDD0	V
			TTL input buffer 2.7 V ≤ EVDD0 < 3.3 V	1.5		EVDD0	V
	V <sub>IH3</sub>	P20 to P27		0.7 VDD		VDD	V
	V <sub>IH4</sub>	P60, P61	I/O port mode	0.7 EVDD0		6.0	V
	V <sub>IH5</sub>	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 VDD		VDD	V
V <sub>IH6</sub>	P60, P61	SMBus input mode	1.35		EVDD0	V	
Input voltage, low	V <sub>IL1</sub>	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P140, P141, P146, P147	Normal input buffer	0		0.2 EVDD0	V
	V <sub>IL2</sub>	P01, P03, P04, P10, P11, P14 to P17, P30, P50, P55, P73	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0		0.5	V
			TTL input buffer 2.7 V ≤ EVDD0 < 3.3 V	0		0.32	V
	V <sub>IL3</sub>	P20 to P27		0		0.3 VDD	V
	V <sub>IL4</sub>	P60, P61	I/O port mode	0		0.3 EVDD0	V
	V <sub>IL5</sub>	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 VDD	V
V <sub>IL6</sub>	P60, P61	SMBus input mode			0.8	V	

**Caution** The maximum value of V<sub>IH</sub> of pins P00, P02 to P04, P10 to P15, P17, P30, P50, P51, P55, and P71 to P74 is EVDD0, even in the N-ch open-drain mode.

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(4/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Output voltage, high	VOH1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EVDD0 ≤ 5.5 V, I <sub>OH1</sub> = -10.0 mA	EVDD0			V
			4.0 V ≤ EVDD0 ≤ 5.5 V, I <sub>OH1</sub> = -3.0 mA	EVDD0			V
			2.7 V ≤ EVDD0 ≤ 5.5 V, I <sub>OH1</sub> = -2.0 mA	EVDD0			V
	VOH2	P20 to P27, P121, P122	4.0 V ≤ VDD ≤ 5.5 V, I <sub>OH2</sub> = -3.0 mA	VDD			V
			2.7 V ≤ VDD < 4.0 V, I <sub>OH2</sub> = -1.0 mA	VDD			V

**Caution** Pins P00, P02 to P04, P10 to P15, P17, P30, P50, P51, P55, P71 to P74 do not output high-level signals in the N-ch open-drain mode.

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(5/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Output voltage, low	VOL1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147	4.0 V ≤ EVDD0 ≤ 5.5 V, I <sub>OL1</sub> = 17.0 mA			1.3	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, I <sub>OL1</sub> = 8.5 mA			0.7	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, I <sub>OL1</sub> = 3.0 mA			0.6	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, I <sub>OL1</sub> = 1.5 mA			0.4	V
	VOL2	P20 to P27, P121, P122	4.0 V ≤ VDD ≤ 5.5 V, I <sub>OL2</sub> = 6.0 mA			0.7	V
			2.7 V ≤ VDD < 4.0 V, I <sub>OL2</sub> = 1.5 mA			0.5	V
	VOL3	P60, P61	4.0 V ≤ EVDD0 ≤ 5.5 V, I <sub>OL3</sub> = 7.0 mA			2.0	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, I <sub>OL3</sub> = 5.0 mA			0.4	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, I <sub>OL3</sub> = 3.0 mA			0.4	V

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	
Output current <sup>Note</sup>	CCDIOL	P10, P11, P16, P17, P60 to P63	CCSm = 01H	4.0 V ≤ EVDD0 ≤ 5.5 V	1.0	1.8	2.6	mA
				2.7 V ≤ EVDD0 < 4.0 V	0.8	1.5	2.3	mA
			CCSm = 02H	4.0 V ≤ EVDD0 ≤ 5.5 V	3.0	4.9	6.5	mA
				3.0 V ≤ EVDD0 < 4.0 V	2.7	4.3	5.9	mA
			CCSm = 03H	4.0 V ≤ EVDD0 ≤ 5.5 V	6.6	10.0	13.2	mA
				3.3 V ≤ EVDD0 < 4.0 V	6.0	9.1	12.1	mA
	P60, P61	CCSm = 04H	4.0 V ≤ EVDD0 ≤ 5.5 V	10.2	15.0	19.8	mA	
			3.3 V ≤ EVDD0 < 4.0 V	9.4	13.8	18.2	mA	

**Note** The listed currents apply when the output current control function is enabled.

(TA = -40 to +125°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

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Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input leakage current, high	ILIH1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P60 to P63, P70 to P77, P120, P140, P141, P146, P147	Vi = EVDD0			1	μA
	ILIH2	P20 to P27, P137, $\overline{\text{RESET}}$	Vi = VDD			1	μA
	ILIH3	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	Vi = VDD			1	μA
Input leakage current, low	ILIL1	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120, P130, P140, P141, P146, P147	Vi = EVSS0			1	μA
	ILIL2	P20 to P27, P137, $\overline{\text{RESET}}$	Vi = VSS			1	μA
	ILIL3	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	Vi = VSS			1	μA
On-chip pull-up resistance	RU	P00 to P06, P10 to P17, P30, P31, P40 to P43, P50 to P55, P62, P63, P70 to P77, P120 to P122, P140, P141, P146, P147	Vi = EVSS0, input port	10	20	100	kΩ

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

## 3.3.2 Supply current characteristics

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/5)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f <sub>PLL</sub> = 96 MHz f <sub>CLK</sub> = 48 MHz (MCM0 = 0)Note 2	Normal operation	VDD = 5.0 V	5.5	19.7	mA
						VDD = 2.7 V	5.5	19.7	
				f <sub>PLL</sub> = 96 MHz f <sub>CLK</sub> = 48 MHz (MCM = 1)Note 4	Normal operation	VDD = 5.0 V	5.3	19.4	mA
						VDD = 2.7 V	5.3	19.4	
				f <sub>IH</sub> = 48 MHzNote 2	Normal operation	VDD = 5.0 V	4.6	13.3	mA
						VDD = 2.7 V	4.6	13.3	
				f <sub>PLL</sub> = 64 MHz f <sub>CLK</sub> = 32 MHz (MCM0 = 0)Note 2	Normal operation	VDD = 5.0 V	3.9	13.6	mA
						VDD = 2.7 V	3.9	13.5	
				f <sub>PLL</sub> = 64 MHz f <sub>CLK</sub> = 32 MHz (MCM = 1)Note 4	Normal operation	VDD = 5.0 V	3.7	13.3	mA
						VDD = 2.7 V	3.7	13.3	
				f <sub>IH</sub> = 32 MHzNote 2	Basic operation	VDD = 5.0 V	1.6	—	mA
						VDD = 2.7 V	1.6	—	
			Normal operation		VDD = 5.0 V	3.3	9.3	mA	
					VDD = 2.7 V	3.3	9.3		
			LS (low-speed main) mode	f <sub>IH</sub> = 24 MHzNote 2	Normal operation	VDD = 5.0 V	2.5	7.1	mA
						VDD = 2.7 V	2.5	7.1	
				f <sub>IH</sub> = 16 MHzNote 2	Normal operation	VDD = 5.0 V	1.8	5.1	mA
						VDD = 2.7 V	1.8	5.1	
				f <sub>IM</sub> = 4 MHzNote 3	Normal operation	VDD = 5.0 V	0.5	1.6	mA
						VDD = 2.7 V	0.5	1.6	
			LP (low-power main) mode	f <sub>IM</sub> = 2 MHzNote 3	Normal operation	VDD = 5.0 V	0.2	968	μA
						VDD = 2.7 V	0.2	968	
				f <sub>IM</sub> = 1 MHzNote 3	Normal operation	VDD = 5.0 V	0.1	701	μA
						VDD = 2.7 V	0.1	701	
HS (high-speed main) mode	f <sub>MX</sub> = 20 MHzNote 4, Square wave input	Normal operation	VDD = 5.0 V	2.0	5.9	mA			
			VDD = 2.7 V	2.0	5.9				
LS (low-speed main) mode	f <sub>MX</sub> = 20 MHzNote 4, Square wave input	Normal operation	VDD = 5.0 V	1.9	5.8	mA			
			VDD = 2.7 V	1.9	5.8				
	f <sub>MX</sub> = 20 MHzNote 4, Resonator connection	Normal operation	VDD = 5.0 V	2.1	6.0	mA			
			VDD = 2.7 V	2.1	6.0				
	f <sub>MX</sub> = 10 MHzNote 4, Square wave input	Normal operation	VDD = 5.0 V	1.0	3.2	mA			
			VDD = 2.7 V	1.0	3.2				
	f <sub>MX</sub> = 10 MHzNote 4, Resonator connection	Normal operation	VDD = 5.0 V	1.1	3.4	mA			
			VDD = 2.7 V	1.1	3.4				
	f <sub>MX</sub> = 8 MHzNote 4, Square wave input	Normal operation	VDD = 5.0 V	0.8	2.7	mA			
			VDD = 2.7 V	0.8	2.6				

(Notes and Remarks are listed on the next page.)



(TA = -40 to +125°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(2/5)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	LS (low-speed main) mode	fMX = 8 MHz <sup>Note 4</sup> , Resonator connection	Normal operation	VDD = 5.0 V	0.9	2.8	mA
						VDD = 2.7 V	0.9	2.8	

**Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The currents in the Typ. column do not include the peripheral operating current when the CPU is placed in the HS (high-speed main), LS (low-speed main), or LV (low-voltage main) mode. The currents in the Max. column include the peripheral operating current, but do not include those of the FAA, A/D converter, sample & hold circuit, D/A converter, PGA, comparator, TRNG, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing when the data flash memory is being rewritten.

**Note 2.** The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

**Note 3.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

**Note 4.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

**Remark 1.** f<sub>ih</sub>: High-speed on-chip oscillator clock frequency

**Remark 2.** f<sub>im</sub>: Middle-speed on-chip oscillator clock frequency

**Remark 3.** f<sub>mx</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 4.** f<sub>pll</sub>: PLL clock frequency (up to 96 MHz)

**Remark 5.** f<sub>clk</sub>: CPU/peripheral hardware clock frequency

**Remark 6.** The typical value for the ambient operating temperature (TA) is 25°C unless otherwise specified.

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(3/5)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit	
Supply current Note 1	IDD1	Operating mode	Subsystem clock operation mode	fsUB = 32.768 kHz <sup>Note 2</sup> , Low-speed on-chip oscillator operation	Normal operation	TA = -40°C		3.9	16.8	μA
						TA = +25°C		4.7	17.4	
						TA = +50°C		6.3	30.9	
						TA = +70°C		9.7	52.3	
						TA = +85°C		15.3	83.2	
						TA = +105°C		30.6	177.3	
						TA = +125°C		61.3	324.1	
				fsUB = 32.768 kHz <sup>Note 3</sup> , Square wave input	Normal operation	TA = -40°C		3.5	16.3	μA
						TA = +25°C		4.9	22.0	
						TA = +50°C		5.9	31.7	
						TA = +70°C		9.2	53.9	
						TA = +85°C		14.7	81.8	
		fsUB = 32.768 kHz <sup>Note 3</sup> , Resonator connection	Normal operation	TA = -40°C		3.6	13.4	μA		
				TA = +25°C		4.3	14.1			
				TA = +50°C		5.8	27.2			
				TA = +70°C		9.2	50.0			
				TA = +85°C		14.9	79.7			
				TA = +105°C		30.0	174.3			
TA = +125°C		59.5	319.4							

**Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The currents in the Typ. and Max. columns do not include the peripheral operating current when the CPU is operating with the sub-system clock.

**Note 2.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

**Note 3.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 11B). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

**Remark 1.** fil: Low-speed on-chip oscillator clock frequency

**Remark 2.** fsUB: Subsystem clock frequency (XT1 clock oscillation frequency)

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(4/5)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit	
Supply current <sup>Note 1</sup>	IDD2 <sup>Note 2</sup>	HALT mode	HS (high-speed main) mode	f <sub>PLL</sub> = 96 MHz f <sub>CLK</sub> = 48 MHz (MCM0 = 0) <sup>Note 2</sup>	VDD = 5.0 V		1.57	14.37	mA	
					VDD = 2.7 V		1.57	14.37		
				f <sub>PLL</sub> = 96 MHz f <sub>CLK</sub> = 48 MHz (MCM = 1) <sup>Note 4</sup>	VDD = 5.0 V		1.39	14.13	mA	
					VDD = 2.7 V		1.39	14.13		
				f <sub>IH</sub> = 48 MHz <sup>Note 2</sup>	VDD = 5.0 V		0.73	8.06	mA	
					VDD = 2.7 V		0.73	8.06		
				f <sub>PLL</sub> = 64 MHz f <sub>CLK</sub> = 32 MHz (MCM0 = 0) <sup>Note 2</sup>	VDD = 5.0 V		1.19	9.90	mA	
					VDD = 2.7 V		1.18	9.90		
				f <sub>PLL</sub> = 64 MHz f <sub>CLK</sub> = 32 MHz (MCM = 1) <sup>Note 4</sup>	VDD = 5.0 V		1.01	9.66	mA	
					VDD = 2.7 V		1.00	9.66		
				f <sub>IH</sub> = 32 MHz <sup>Note 3</sup>	VDD = 5.0 V		0.62	5.68	mA	
					VDD = 2.7 V		0.61	5.68		
				LS (low-speed main) mode	f <sub>IH</sub> = 24 MHz <sup>Note 3</sup>	VDD = 5.0 V		0.51	4.42	mA
						VDD = 2.7 V		0.50	4.42	
			f <sub>IH</sub> = 16 MHz <sup>Note 3</sup>		VDD = 5.0 V		0.48	3.27	mA	
					VDD = 2.7 V		0.48	3.27		
			f <sub>IM</sub> = 4 MHz <sup>Note 4</sup>		VDD = 5.0 V		0.10	1.09	mA	
					VDD = 2.7 V		0.10	1.09		
			LP (low-power main) mode	f <sub>IM</sub> = 2 MHz <sup>Note 4</sup>	VDD = 5.0 V		0.04	731	μA	
					VDD = 2.7 V		0.04	731		
				f <sub>IM</sub> = 1 MHz <sup>Note 4</sup>	VDD = 5.0 V		0.03	583	μA	
					VDD = 2.7 V		0.03	583		
			HS (high-speed main) mode	f <sub>MX</sub> = 20 MHz <sup>Note 5</sup> , Square wave input	VDD = 5.0 V		0.25	3.52	mA	
					VDD = 2.7 V		0.23	3.50		
			LS (low-speed main) mode	f <sub>MX</sub> = 20 MHz <sup>Note 5</sup> , Square wave input	VDD = 5.0 V		0.26	3.53	mA	
					VDD = 2.7 V		0.23	3.50		
				f <sub>MX</sub> = 20 MHz <sup>Note 5</sup> , Resonator connection	VDD = 5.0 V		0.44	3.78	mA	
					VDD = 2.7 V		0.44	3.77		
f <sub>MX</sub> = 10 MHz <sup>Note 5</sup> , Square wave input	VDD = 5.0 V			0.16	2.00	mA				
	VDD = 2.7 V			0.14	1.99					
f <sub>MX</sub> = 10 MHz <sup>Note 5</sup> , Resonator connection	VDD = 5.0 V			0.30	2.20	mA				
	VDD = 2.7 V			0.30	2.19					
f <sub>MX</sub> = 8 MHz <sup>Note 5</sup> , Square wave input	VDD = 5.0 V			0.14	1.70	mA				
	VDD = 2.7 V			0.12	1.68					
f <sub>MX</sub> = 8 MHz <sup>Note 5</sup> , Resonator connection	VDD = 5.0 V		0.23	1.83	mA					
	VDD = 2.7 V		0.23	1.82						

(Notes and Remarks are listed on the next page.)

- Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The currents in the Typ. column do not include the peripheral operating current when the CPU is placed in the HS (high-speed main), LS (low-speed main), or LV (low-voltage main) mode. The currents in the Max. column include the peripheral operating current, but do not include those flowing into the FAA, A/D converter, sample & hold circuit, D/A converter, PGA, comparator, TRNG, LVD circuit, I/O port, and on-chip pull-up-/pull-down resistors, and those flowing when the data flash memory is being rewritten. The currents in the Max. column include that of the RTC when the CPU is placed in the HALT mode.
- Note 2.** The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.
- Note 3.** The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
- Note 4.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.
- Note 5.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
- Remark 1.** f<sub>H</sub>: High-speed on-chip oscillator clock frequency
- Remark 2.** f<sub>M</sub>: Middle-speed on-chip oscillator clock frequency
- Remark 3.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 4.** f<sub>PLL</sub>: PLL clock frequency (up to 96 MHz)
- Remark 5.** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency
- Remark 6.** The typical value for the ambient operating temperature (TA) is 25°C unless otherwise specified.

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(5/5)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	Subsystem clock operation mode	fSUB = 32.768 kHz Note 3, Low-speed on-chip oscillator operation	TA = -40°C		0.97	12.34	μA
					TA = +25°C		1.55	12.63	
					TA = +50°C		2.80	25.52	
					TA = +70°C		5.54	45.91	
					TA = +85°C		10.41	75.72	
					TA = +105°C		23.12	165.90	
					TA = +125°C		49.38	305.79	
				fSUB = 32.768 kHz, Square wave input Note 4	TA = -40°C		0.27	11.36	μA
					TA = +25°C		1.48	16.75	
					TA = +50°C		2.19	26.07	
					TA = +70°C		4.93	47.35	
					TA = +85°C		9.37	73.72	
					TA = +105°C		22.71	168.74	
				fSUB = 32.768 kHz, Resonator connection Note 5	TA = -40°C		0.40	8.83	μA
	TA = +25°C		0.94		9.53				
	TA = +50°C		2.16		22.41				
	TA = +70°C		4.91		43.76				
	TA = +85°C		9.71		72.66				
	TA = +105°C		22.43		163.33				
	IDD3	STOP mode	Realtime clock stopped Note 6	TA = -40°C		0.16	10.00	μA	
				TA = +25°C		0.63	10.00		
TA = +50°C					1.80	20.00			
TA = +70°C					4.30	40.00			
TA = +85°C					9.30	70.00			
TA = +105°C					22.00	160.00			
TA = +125°C					50.00	300.00			
128Hz realtime clock operation Note 7				TA = -40°C		0.24	11.00	μA	
				TA = +25°C		0.71	11.00		
				TA = +50°C		1.95	22.00		
				TA = +70°C		4.60	45.00		
				TA = +85°C		9.50	80.00		
				TA = +105°C		23.00	170.00		
		TA = +125°C		52.00	320.00				

(Notes and Remarks are listed on the next page.)

- Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The currents in the Typ. and Max. columns do not include the peripheral operating current when the CPU is operating with the sub-system clock, or when the CPU is placed in the STOP mode, but include that of the RTC when in the HALT mode.
- Note 2.** The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.
- Note 3.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped, including the current flowing into the RTC. They do not include the currents flowing into the 32-bit interval timer and watchdog timer.
- Note 4.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, including the current flowing into the RTC. They do not include the currents flowing into the 32-bit interval timer and watchdog timer.
- Note 5.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and when RTCLPC is set to 1 and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 11B), including the current flowing into the RTC. They do not include the currents flowing into the 32-bit interval timer and watchdog timer.
- Note 6.** The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. They do not include the currents flowing into the RTC, 32-bit interval timer and watchdog timer. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.
- Note 7.** The listed currents apply when the low-speed on-chip oscillator is stopped, and when RTCLPC is set to 1 and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 11B), including the current flowing into the RTC. They do not include the currents flowing into the 32-bit interval timer and watchdog timer.

**Remark 1.** f<sub>L</sub>: Low-speed on-chip oscillator clock frequency

**Remark 2.** f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)

## Peripheral Functions (Common to all products)

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	IFIH Note 1	HIPREC = 0			380	—	μA
		HIPREC = 1			240	—	μA
Middle-speed on-chip oscillator operating current	IFIM Note 1				20	—	μA
Low-speed on-chip oscillator operating current	IFIL Note 1				0.3	—	μA
RTC operating current	IRTC Notes 1, 2, 3	fRTCCLK = 32.768 kHz			0.005	—	μA
		fRTCCLK = 128 Hz			0.002	—	μA
32-bit interval timer operating current	IIT Notes 1, 2, 4				0.04	—	μA
Watchdog timer operating current	IWDT Notes 1, 2, 5	fil = 32.768 kHz (typ.)			0.32	—	μA
A/D converter operating current	IADC Notes 1, 6	Conversion at maximum speed	Normal mode, AVREFP = VDD = 5.0 V		0.95	1.6	mA
			Low-voltage mode, AVREFP = VDD = 3.0 V		0.54	0.81	mA
AVREFP current	IADREF Note 7	AVREFP = 5.0 V			60	—	μA
A/D converter internal reference voltage current	IADREF Note 1				114	—	μA
Temperature sensor operating current	ITMPS Note 1				110	—	μA
D/A converter operating current	IDAC Notes 1, 8	Per channel	10-bit DAC, VDD = 5.0 V		223	—	μA
			8-bit DAC, VDD = 5.0 V		120	—	μA
Comparator operating current	ICMP Notes 1, 9	Per channel			100	—	μA
PGA operating current	IPGA Notes 1, 10				460	—	μA
Sample & hold operating current	ISH Notes 1, 11	Per channel			800	—	μA
LVD operating current	ILVD0 Notes 1, 12				0.03	—	μA
	ILVD1 Notes 1, 12				0.03	—	μA
FAA operating current	IFAA Notes 1, 13	fCLK = 48 MHz			11.0	—	mA
		fCLK = 32 MHz			7.3	—	mA
True random number generator operating current	ITRNG				1.6	—	mA
SMBus operating current	ISMBUS				250	—	μA
Self-programming operating current	IFSP Notes 1, 14	-40 to +105°C			2.5	12.2	mA
Data flash rewrite operating current	IBGO Notes 1, 15				2.5	12.2	mA

&lt;R&gt;

(Notes and Remarks are listed on the next page.)

(TA = -40 to +125°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(2/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
SNOOZE operating current	ISNOZ <sup>Note 1</sup>	ADC to be in use	The ADC is shifting to the SNOOZE mode. <sup>Note 16</sup>		0.7	1.2	mA
			The ADC is operating in the low-voltage mode, AVREFF = VDD = 3.0 V		1.2	2.0	
		Simplified SPI (CSI)/UART to be in use			0.7	1.07	
Low-speed peripheral clock supply current	ISXP <sup>Notes 1, 17</sup>	RTCLPC = 0			0.27	—	μA
Output current control operating current	ICCD <sup>Notes 1, 18</sup>	The setting of the CCDE register is not 00H.			100	—	μA
		ICCDP <sup>Notes 19, 20</sup>	Per single controlled current drive port	Low-level output current setting: Hi-Z		30	—
	Low-level output current setting: 2 to 15 mA				210	—	μA

**Note 1.** This current flows into VDD.

**Note 2.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.

**Note 3.** This current only flows to the realtime clock (RTC). It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and IRTC when the realtime clock is operating in the operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be included in the supply current. IDD2 in the subsystem clock operation mode includes the operating current of the realtime clock.

**Note 4.** This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and IIT when the 32-bit interval timer is operating or in the HALT mode.

**Note 5.** This current only flows to the watchdog timer. It includes the operating current of the low-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3, and IWDT when the watchdog timer is operating.

**Note 6.** This current only flows to the A/D converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and IADC when the A/D converter is operating or in the HALT mode.

**Note 7.** This current flows into AVREFF.

**Note 8.** This current only flows to the D/A converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and IDAC when the D/A converter is operating.

**Note 9.** This current only flows to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3, and ICMP when the comparator circuit is operating.

**Note 10.** This current only flows to the PGA circuit. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and IPGA when the PGA circuit is operating.

**Note 11.** This current only flows to the sample & hold circuit. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and ISH when the sample & hold circuit is operating.

**Note 12.** This current only flows to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3, and ILVD when the LVD circuit is operating.

**Note 13.** This current only flows to the FAA circuit. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2, and IFAA when the FAA circuit is operating.

**Note 14.** This current only flows during self-programming.

**Note 15.** This current only flows while the data flash memory is being rewritten.

**Note 16.** For shift time to the SNOOZE mode, see **20.9 SNOOZE Mode Function** in the RL78/G24 User's Manual.

**Note 17.** This current is added to the supply current in the STOP mode when the setting of RTCLPC is 0 with the subsystem clock X (fsx) oscillating, or in the HALT mode when the setting of RTCLPC is 0 with the subsystem clock X (fsx) selected as the CPU clock.

**Note 18.** This current is added to the supply current when the controlled current drive port is set.

**Note 19.** This current does not include the current flowing into the I/O ports.

**Note 20.** This current flows into EVDD0 and EVDD1.

**Remark 1.** fIL: Low-speed on-chip oscillator clock frequency

**Remark 2.** fsx: Subsystem clock X frequency

**Remark 3.** fCLK: CPU/peripheral hardware clock frequency

**Remark 4.** The typical value for the ambient operating temperature is 25°C.



## 3.4 AC Characteristics

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Instruction cycle	TCY	Main system clock (fMAIN) operation	HS (high-speed main) mode (Prefetch ON)	0.02083		1	μs
			HS (high-speed main) mode (Prefetch OFF)	0.03125		1	μs
			LS (low-speed main) mode	0.04167		1	μs
			LP (low-power main) mode	0.5		1	μs
		Subsystem clock (fSUB) operation		26.041	30.5	31.3	μs
		Self-programming mode	HS (high-speed main) mode	0.03125		1	μs
LS (low-speed main) mode	0.04167			1	μs		
External system clock frequency	fEX			1.0		20.0	MHz
	fEXS			32		38.4	kHz
External system clock input high-level width, low-level width	tEXH, tEXL			24			ns
	tEXHS, tEXLS			13.7			μs
Ti00 to Ti03 input high-level width, low-level width	tTIH, tTIL			1/fMCK + 10			ns
Timer RJ input cycle	tC	TRJIO		100			ns
Timer RJ input high-level width, low-level width	tTJIH, tTJIL	TRJIO		40			ns
Timer RD2 input high-level width, low-level width	tTDIH, tTDIL	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/fCLK			ns
Timer RD2 forcible shut-off signal input low-level width	tTDSIL	P137/INTP0	2 MHz ≤ fCLK ≤ 48 MHz	1			μs
			fCLK ≤ 2 MHz	1/fCLK + 1			μs
Timer RG2 input high-level width, low-level width	tTGIH, tTGIL	TRGIOA, TRGIOB, TRGIDZ, TRGTRG		2.5/fCLK			ns
TO00 to TO03 TKBO00, TKBO01, TKBO10, TKBO11, TKBO20, TKBO21, TRJIO0, TRJIO1, TRGIOA, TRGIOB, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 output frequency	fTO	HS (high-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
			LS (low-speed main) mode	2.7 V ≤ EVDD0 < 4.0 V			8
		LP (low-power main) mode					2
PCLBUZ0, PCLBUZ1 output frequency	fPCL	HS (high-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
			LS (low-speed main) mode	2.7 V ≤ EVDD0 < 4.0 V			8
		LP (low-power main) mode					2
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0, INTP20, INTP21	2.7 V ≤ VDD ≤ 5.5 V	1			μs
		INTP1 to INTP11	2.7 V ≤ EVDD0 ≤ 5.5 V	1			μs
Key interrupt input high-level width, low-level width	tKRH, tKRL	KR0 to KR7	2.7 V ≤ EVDD0 ≤ 5.5 V	250			ns

(Remark is listed on the next page.)

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

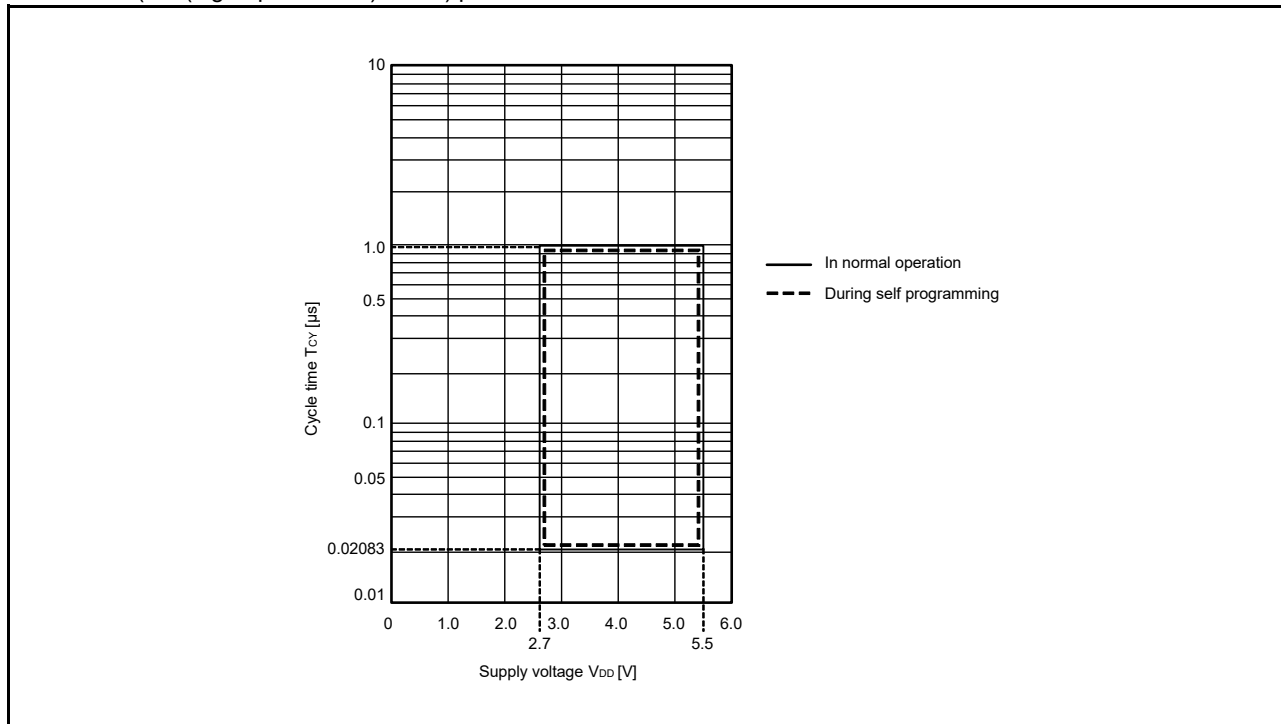
(2/2)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
$\overline{\text{RESET}}$ low-level width	tRSL		10			μs

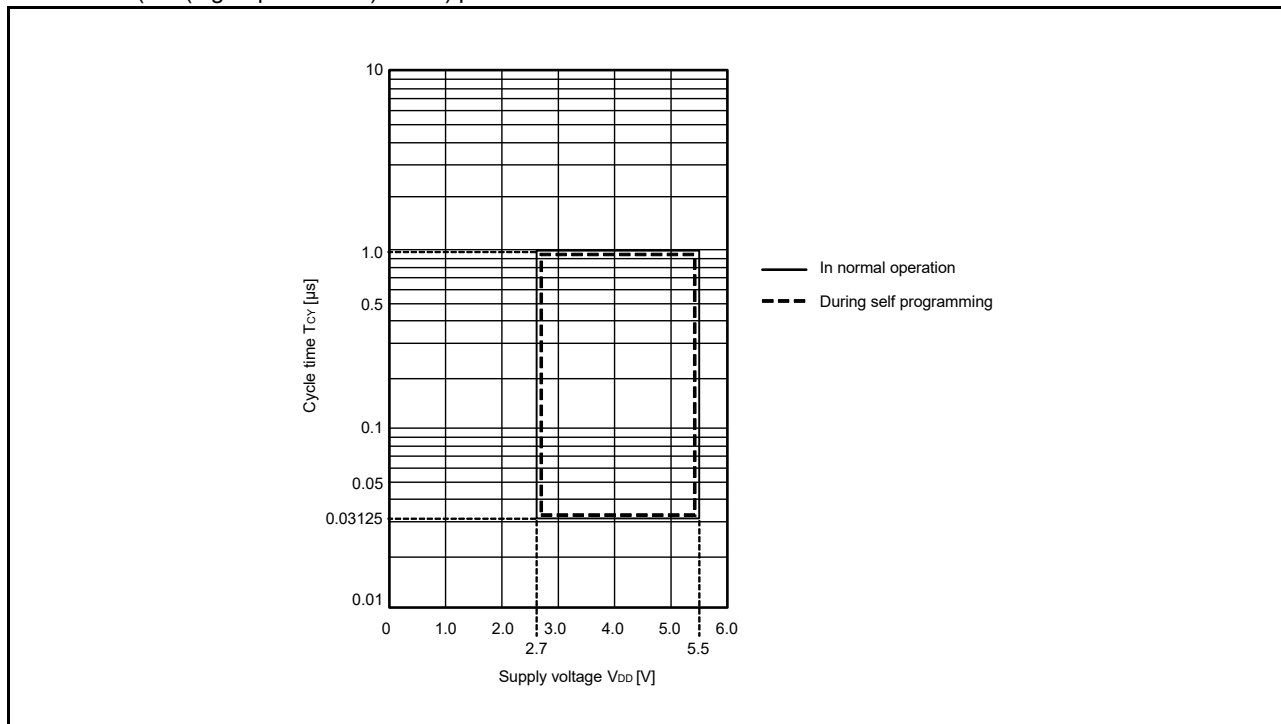
**Remark** fMCK: Timer array unit operating clock frequency  
 To set this operating clock, use the CKSmn0 and CKSmn1 bits of the timer mode register mn (TMRmn).  
 m: Unit number (m = 0), n: Channel number (n = 0 to 3)

Minimum Instruction Execution Time during Main System Clock Operation

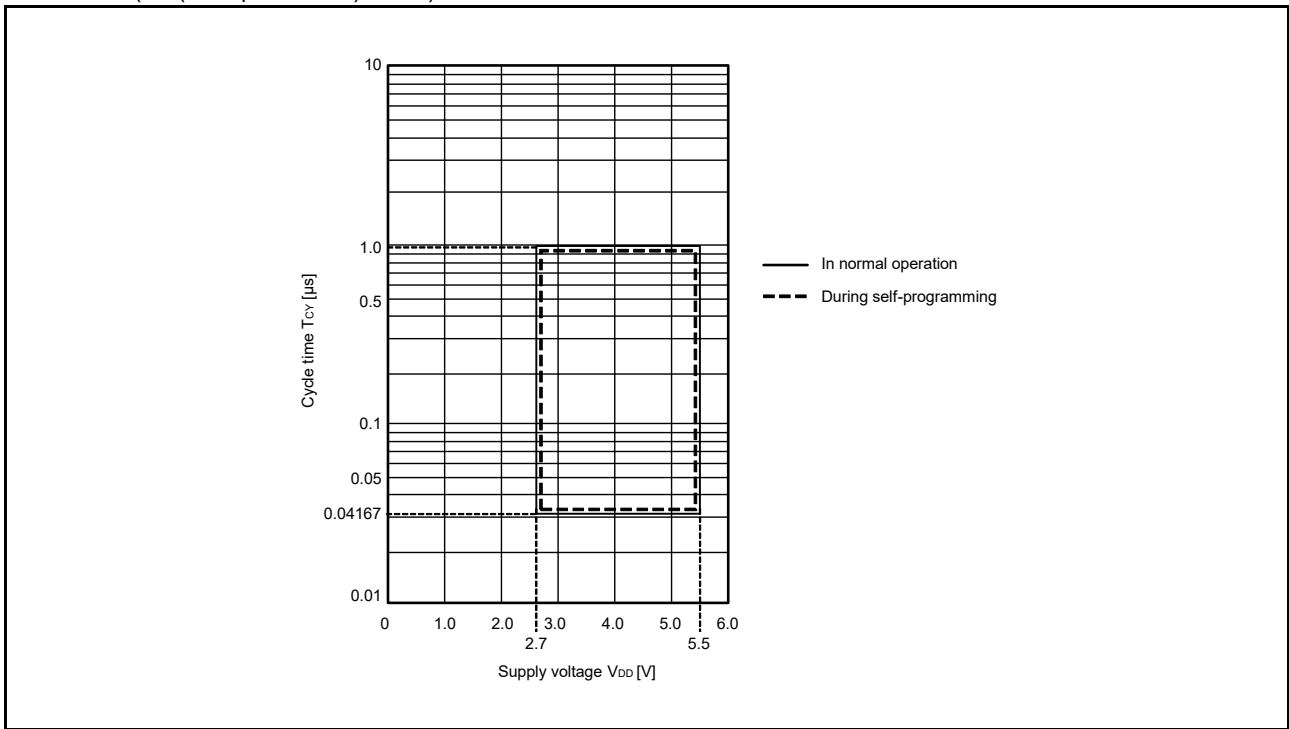
TCY vs VDD (HS (high-speed main) mode) prefetch ON



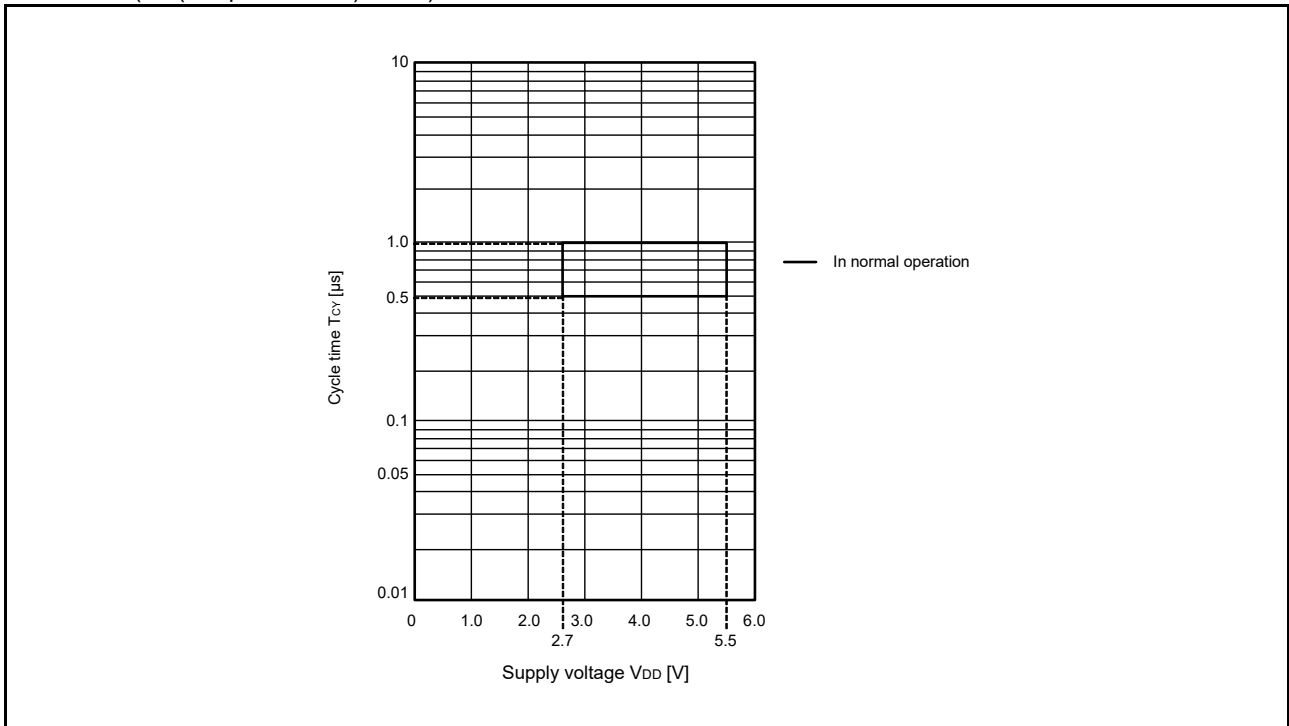
TCY vs VDD (HS (high-speed main) mode) prefetch OFF



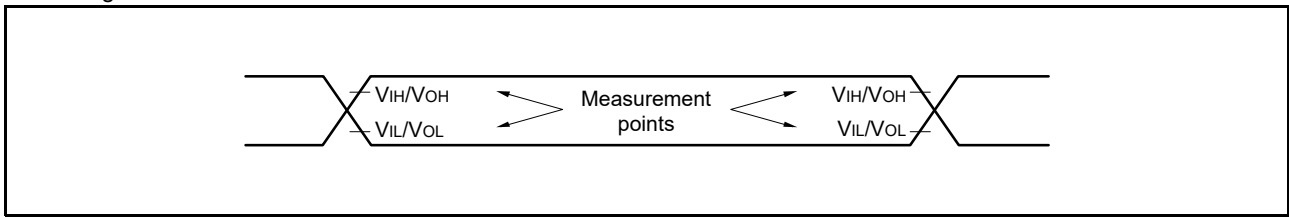
TCY vs VDD (LS (low-speed main) mode)



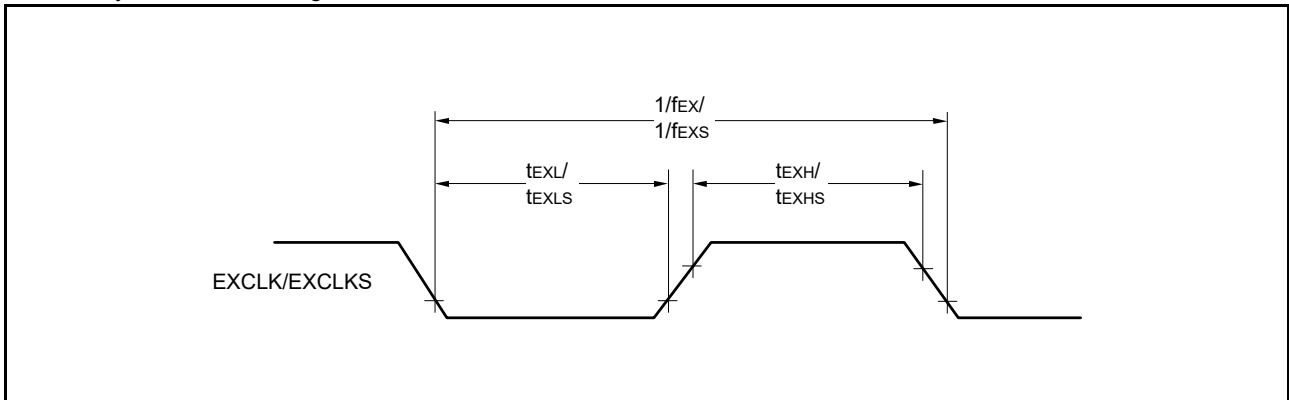
TCY vs VDD (LP (low-power main) mode)



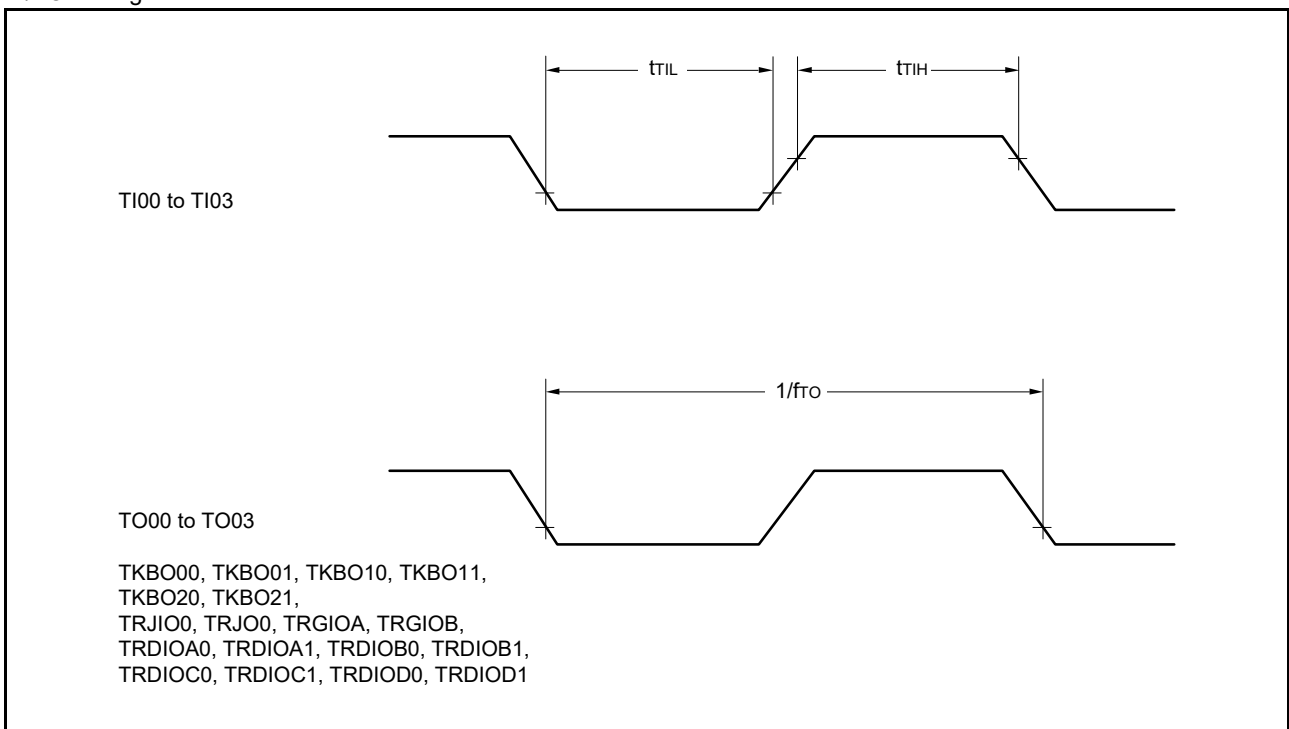
AC Timing Measurement Points



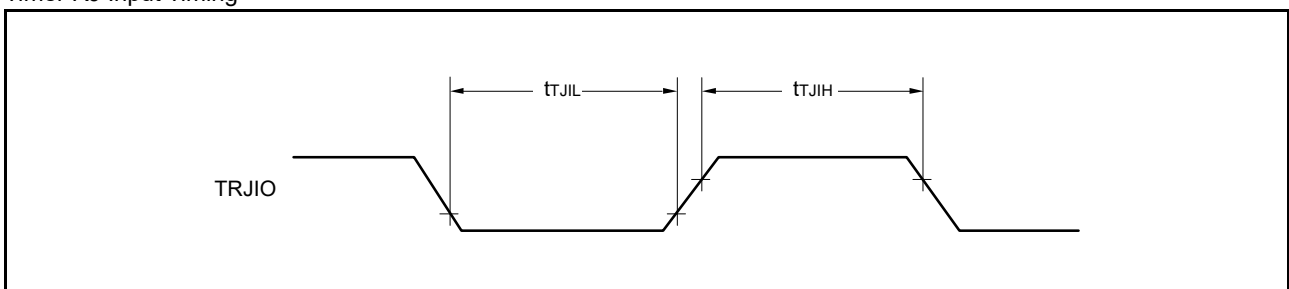
External System Clock Timing



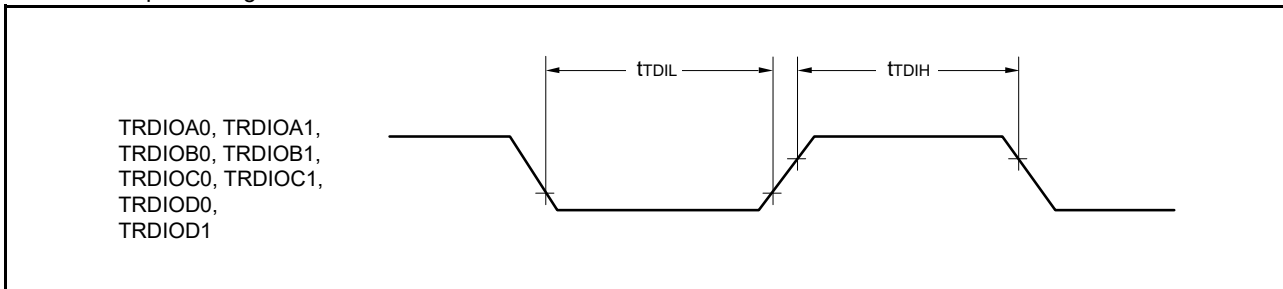
TI/TO Timing



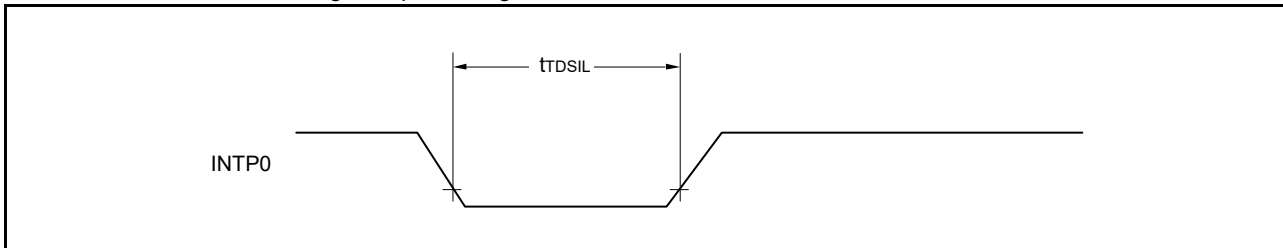
Timer RJ Input Timing



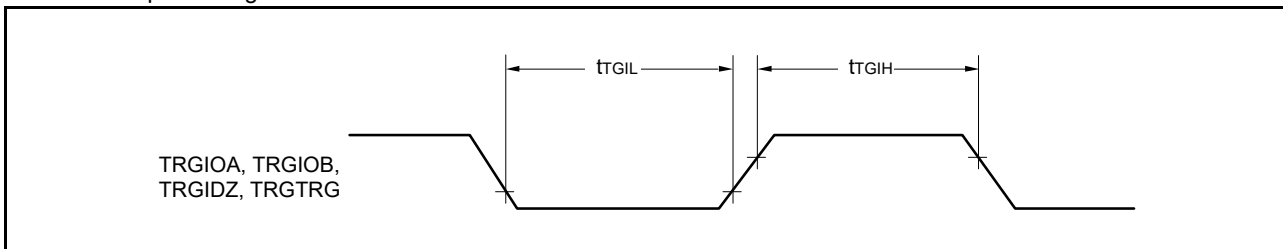
Timer RD2 Input Timing



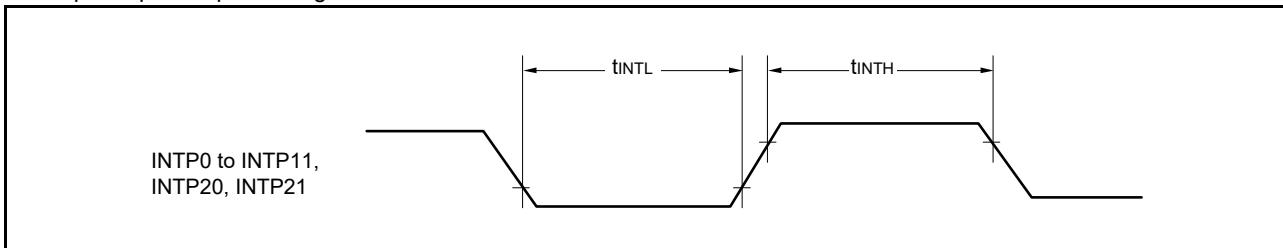
Timer RD2 Forcible Shut-off Signal Input Timing



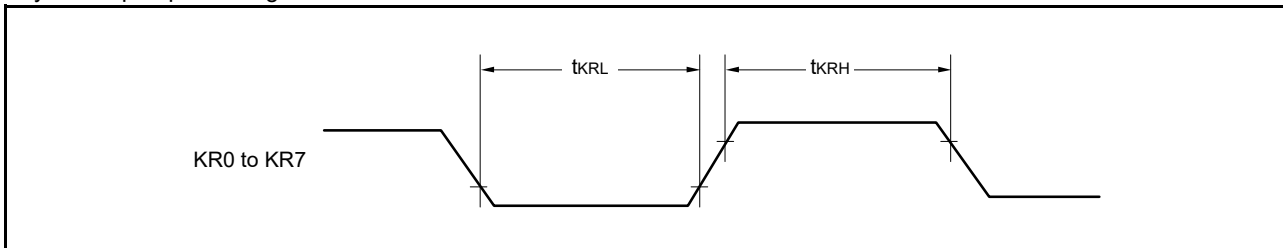
Timer RG2 Input Timing



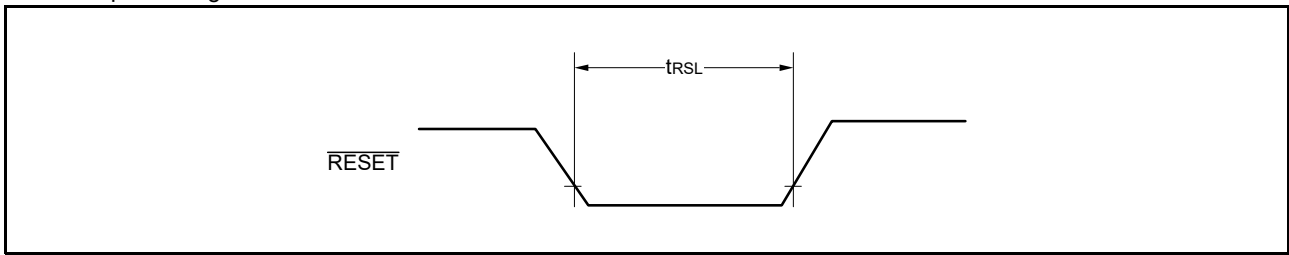
Interrupt Request Input Timing



Key Interrupt Input Timing

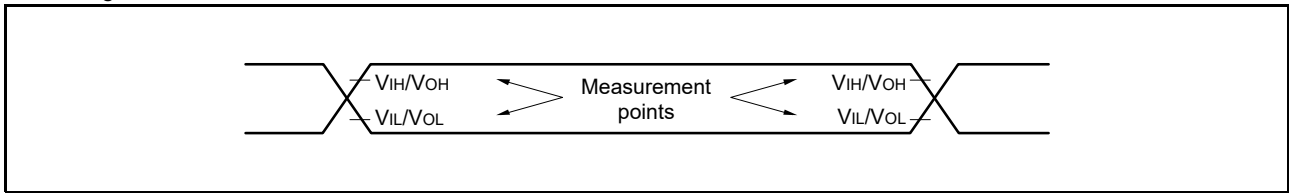


$\overline{\text{RESET}}$  Input Timing



### 3.5 Characteristics of the Peripheral Functions

#### AC Timing Measurement Points



#### 3.5.1 Serial array unit

1. In UART communications with devices operating at same voltage levels

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate Note 1		2.7 V ≤ EVDD0 ≤ 5.5 V		fMCK/6		fMCK/6		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK>Note 2		5.3		4		0.33	Mbps

**Note 1.** The transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

**Note 2.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are as follows.

HS (high-speed main) mode: 48 MHz (2.7 V ≤ VDD ≤ 5.5 V)

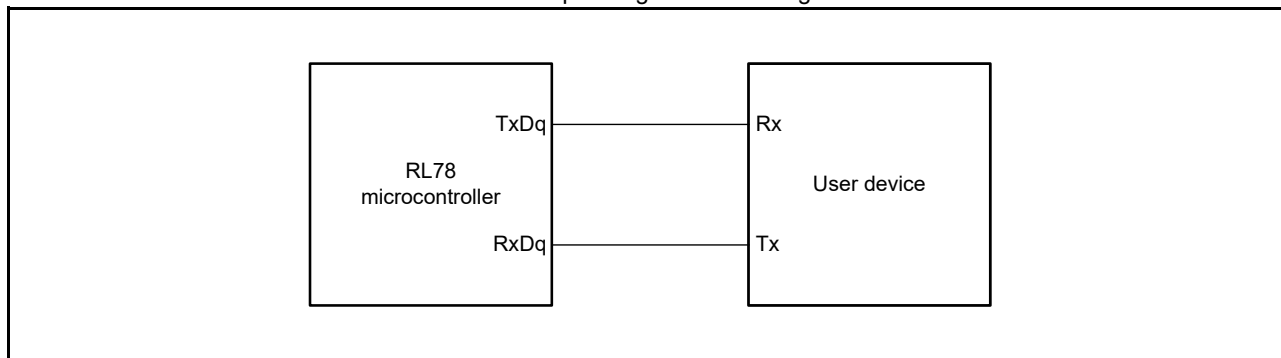
LS (low-speed main) mode: 24 MHz (2.7 V ≤ VDD ≤ 5.5 V)

LP (low-power main) mode: 2 MHz (2.7 V ≤ VDD ≤ 5.5 V)

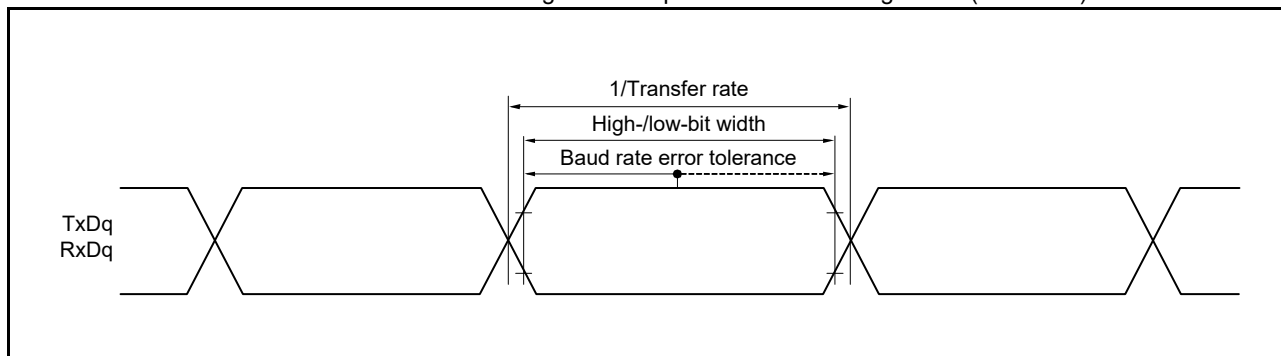
**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).



Connection in UART communications with devices operating at same voltage levels



Bit width in UART communications when interfacing devices operate at same voltage level (reference)



**Remark 1.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** fMCK: Serial array unit operation clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

2. In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	tKCY1	tKCY1 ≥ 4/fCLK 2.7 V ≤ EVDD0 ≤ 5.5 V	125		166		2000		ns
SCKp high-/low-level width	tKH1, tKL1	4.0 V ≤ EVDD0 ≤ 5.5 V	tKCY1/2 - 12		tKCY1/2 - 21		tKCY1/2 - 50		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	tKCY1/2 - 18		tKCY1/2 - 25		tKCY1/2 - 50		ns
Slp setup time (to SCKp↑) <sup>Note 1</sup>	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V	44		54		110		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	44		54		110		ns
Slp hold time (from SCKp↑) <b>Note 1</b>	tKSI1	2.7 V ≤ EVDD0 ≤ 5.5 V	19		19		19		ns
Delay time from SCKp↓ to SOp output <sup>Note 2</sup>	tKSO1	2.7 V ≤ EVDD0 ≤ 5.5 V C = 30 pF <sup>Note 3</sup>		25		25		25	ns

**Note 1.** The setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp↓” and that for the Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and normal output mode for the SOp and SCKp pins by using the port input mode register g (PIMg) and the port output mode register g (POMg).

**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** fMCK: Serial array unit operating clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

3. In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the external SCKp clock

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

Item	Symbol	Conditions		HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time Note 4	tkCY2	4.0 V ≤ EVDD0 ≤ 5.5 V	20 MHz < fMCK	8/fMCK		8/fMCK		—		ns
			fMCK ≤ 20 MHz	6/fMCK		6/fMCK		6/fMCK		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	16 MHz < fMCK	8/fMCK		8/fMCK		—		ns
			fMCK ≤ 16 MHz	6/fMCK		6/fMCK		6/fMCK		ns
SCKp high-/ low-level width	tkH2, tkL2	4.0 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 – 7		tkCY2/2 – 7		tkCY2/2 – 7		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 – 8		tkCY2/2 – 8		tkCY2/2 – 8		ns
Slp setup time (to SCKp↑)Note 1	tSIK2	2.7 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 20		1/fMCK + 30		1/fMCK + 30		ns
Slp hold time (to SCKp↑)Note 1	tSIK2	2.7 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 31		1/fMCK + 31		1/fMCK + 31		ns
Delay time from SCKp↓ to SOP output Note 2	tkSO2	C = 30 pFNote 3	2.7 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 44		2/fMCK + 110		2/fMCK + 110	ns

**Note 1.** The setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp ↓” and that for the Slp hold time becomes “from SCKp ↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOP output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** C is the load capacitance of the SOP output line.

**Note 4.** The transfer rate in the SNOOZE mode is 1 Mbps maximum.

**Caution** Select the normal input buffer for the Slp and SCKp pins and normal output mode for the SOP pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

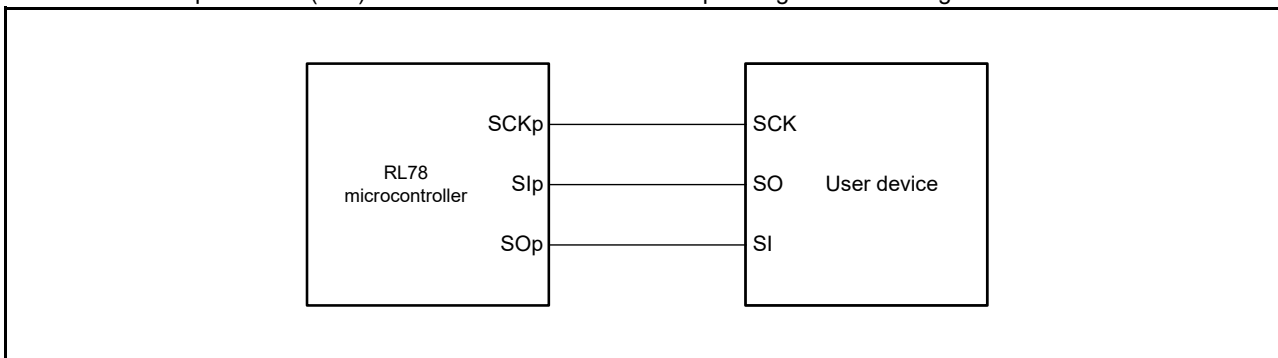
**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** fMCK: Serial array unit operating clock frequency

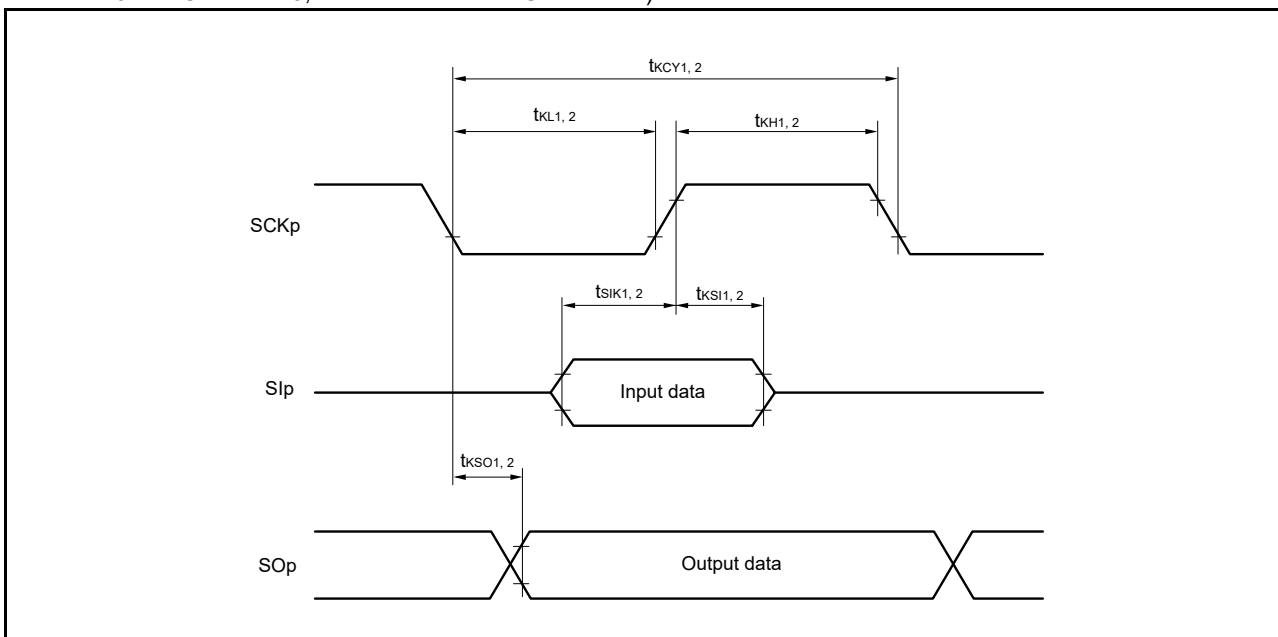
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

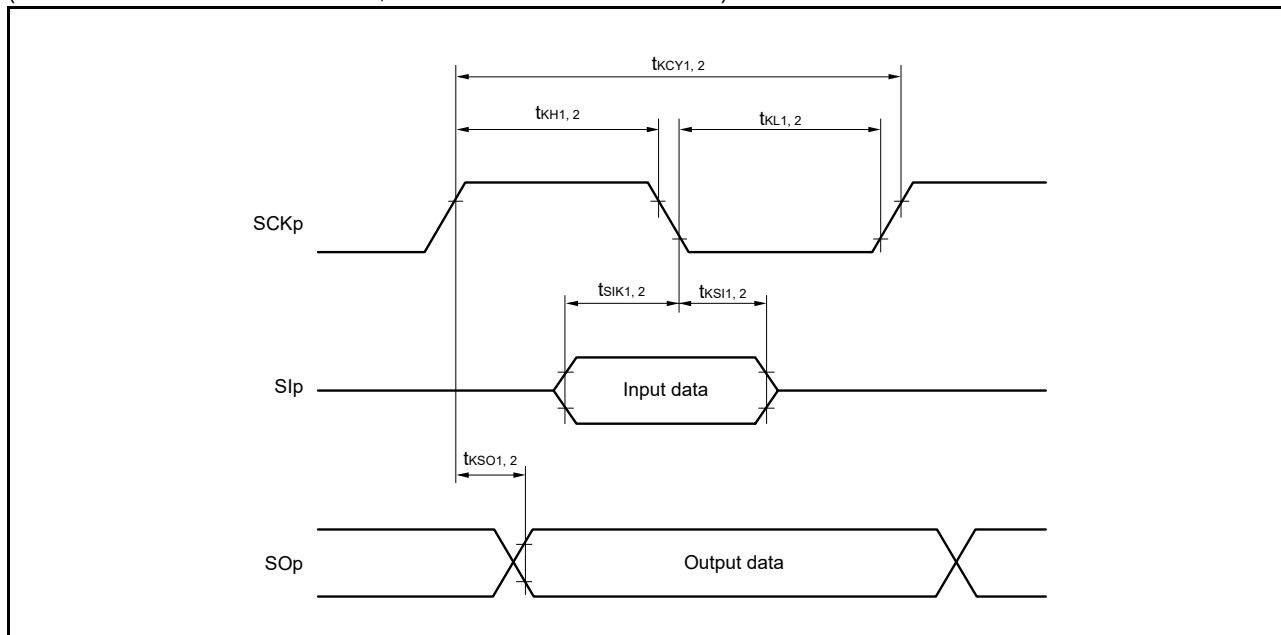
Connection in simplified SPI (CSI) communications with devices operating at same voltage levels



Timing of serial transfer in simplified SPI (CSI) communications with devices operating at same voltage levels (when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Timing of serial transfer in simplified SPI (CSI) communications with devices operating at same voltage levels  
 (when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21)

**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

4. In simplified I<sup>2</sup>C communications with devices operating at same voltage levels

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

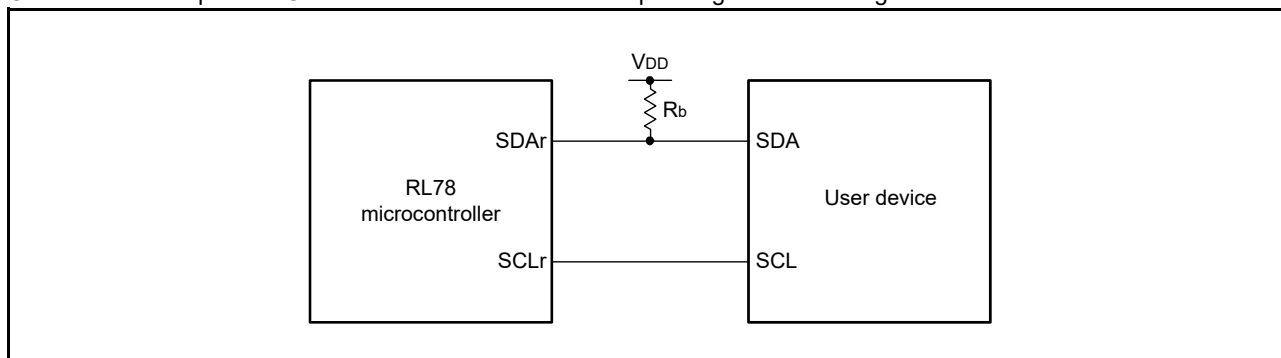
Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	fSCL	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		1000 Note 1		400 Note 1	kHz
Hold time when SCLr is low	tLOW	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		475		1150		ns
Hold time when SCLr is high	tHIGH	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		475		1150		ns
Data setup time (reception)	tSU:DAT	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 85 Note 2		1/fMCK + 85 Note 2		1/fMCK + 145 Note 2		ns
Data hold time (transmission)	tHD:DAT	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns

**Note 1.** The listed frequencies must be no greater than fMCK/4.**Note 2.** Set the fMCK value that does not exceed the hold time when SCLr is low or high.

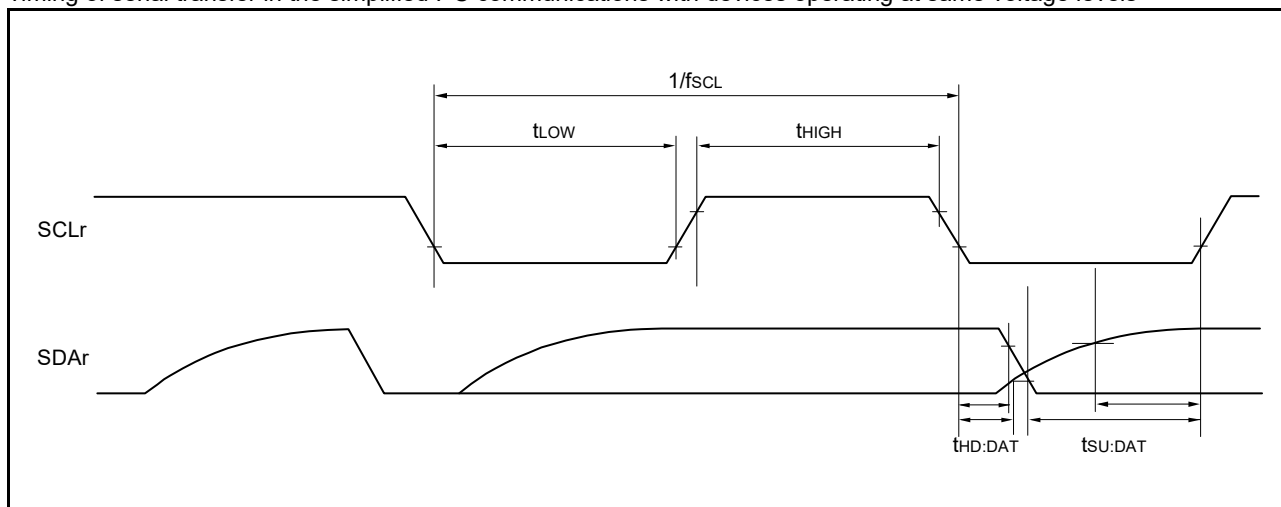
**Caution** Select the normal input buffer and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/ EVDD withstand voltage for 64-pin products) mode for the SDAr pin and the normal output mode for the SCLr pin by using the port input mode register g (PIMg) and the port output mode register h (POMh).

(Remarks are listed on the next page.)

Connection in simplified I<sup>2</sup>C communications with devices operating at same voltage levels



Timing of serial transfer in the simplified I<sup>2</sup>C communications with devices operating at same voltage levels



**Remark 1.** R<sub>b</sub>[Ω]: Communication line (SDAr) pull-up resistance, C<sub>b</sub>[F]: Communication line (SDAr, SCLr) load capacitance

**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1, 3, 5, 7), h: POM number (h = 0, 1, 3, 5, 7)

**Remark 3.** f<sub>MCK</sub>: Serial array unit operating clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11

5. In UART communications with devices operating at different voltage levels (2.5 V, 3 V)

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit		
			Min.	Max.	Min.	Max.	Min.	Max.			
Transfer rate		Reception	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1	bps	
			Theoretical value of the maximum transfer rate fMCK = fCLK <sup>Note 2</sup>		5.3		4		0.33	Mbps	
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		fMCK/6 Note 1		fMCK/6 Note 1		fMCK/6 Note 1	bps	
				Theoretical value of the maximum transfer rate fMCK = fCLK <sup>Note 2</sup>		5.3		4		0.33	Mbps
		Trans- mission	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		Note 3		Note 3		Note 3	bps	
				Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V		2.8 <sup>Note 4</sup>		2.8 <sup>Note 4</sup>		2.8 <sup>Note 4</sup>	Mbps
				2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		Note 5		Note 5		Note 5	bps
					Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V		1.2 <sup>Note 6</sup>		1.2 <sup>Note 6</sup>		1.2 <sup>Note 6</sup>

(Notes, Caution, and Remarks are listed on the next page.)



**Note 1.** Transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

**Note 2.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 48 MHz (2.7 V ≤ VDD ≤ 5.5 V)

LS (low-speed main) mode: 24 MHz (2.7 V ≤ VDD ≤ 5.5 V)

LP (low-power main) mode: 2 MHz (2.7 V ≤ VDD ≤ 5.5 V)

**Note 3.** The smaller maximum transfer rate derived by using fmCK/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 4.** This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**Note 5.** The smaller maximum transfer rate derived by using fmCK/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 6.** This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the TxDq pin by using the port input mode register g (PIMg) and the port output mode register g (POMg). For VIH and VIL, see the DC characteristics with the TTL input buffer selected.

**Remark 1.** Vb[V]: Communication line voltage

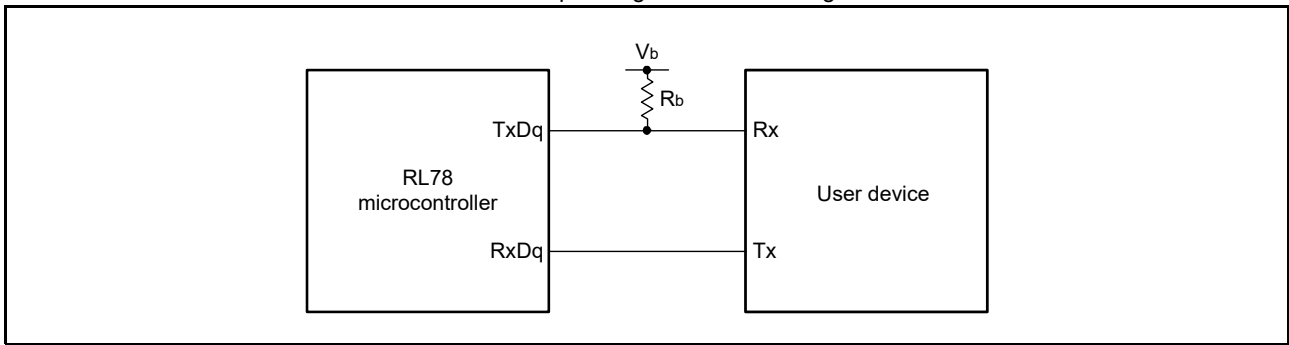
**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 3.** fmCK: Serial array unit operation clock frequency

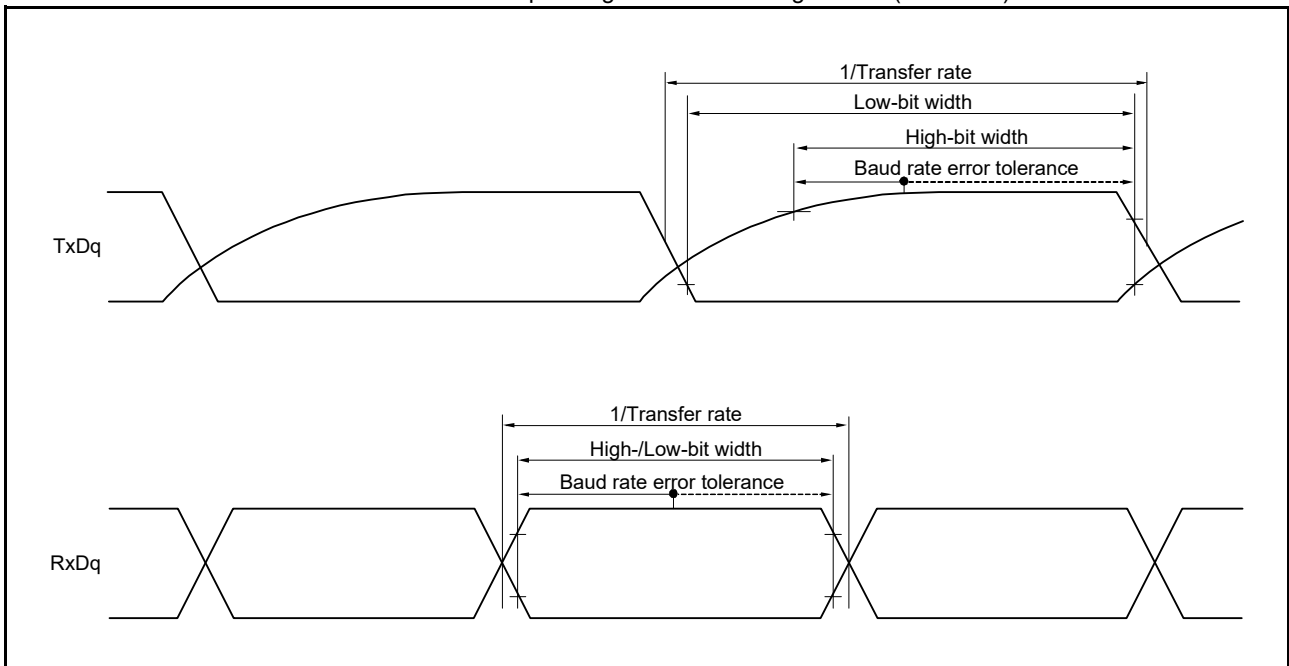
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10, 11).

**Remark 4.** Communications by using UART2 with devices operating at different voltage levels are not possible when bit 1 (PIOR01) of the peripheral I/O redirection register 0 (PIOR0) is set to 1.

Connection in UART communications with devices operating at different voltage levels



Bit width in UART communications with devices operating at different voltage levels (reference)



**Remark 1.**  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  $C_b[F]$ : Communication line (TxDq) load capacitance,  $V_b[V]$ : Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 3.**  $f_{MCK}$ : Serial array unit operating clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

**Remark 4.** Communications by using UART2 with devices operating at different voltage levels are not possible when bit 1 (PIOR01) of the peripheral I/O redirection register 0 (PIOR0) is set to 1.

6. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock

(TA = -40 to +125°C, 1.8 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(1/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	tkCY1	tkCY1 ≥ 4/fCLK 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	300		300		2300		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	500		500		2300		ns
SCKp high-level width	tkH1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	tkCY1/2 - 75		tkCY1/2 - 75		tkCY1/2 - 75		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	tkCY1/2 - 170		tkCY1/2 - 170		tkCY1/2 - 170		ns
SCKp low-level width	tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	tkCY1/2 - 12		tkCY1/2 - 12		tkCY1/2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	tkCY1/2 - 18		tkCY1/2 - 18		tkCY1/2 - 50		ns
Slp setup time (to SCKp↑) <sup>Note</sup>	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	81		81		479		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		177		479		ns
Slp hold time (from SCKp↑) <sup>Note</sup>	tKS11	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOP output <sup>Note</sup>	tkSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195		195	ns

(Note and Caution are listed on the next page, and Remarks are listed on page 165.)

6. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(2/2)

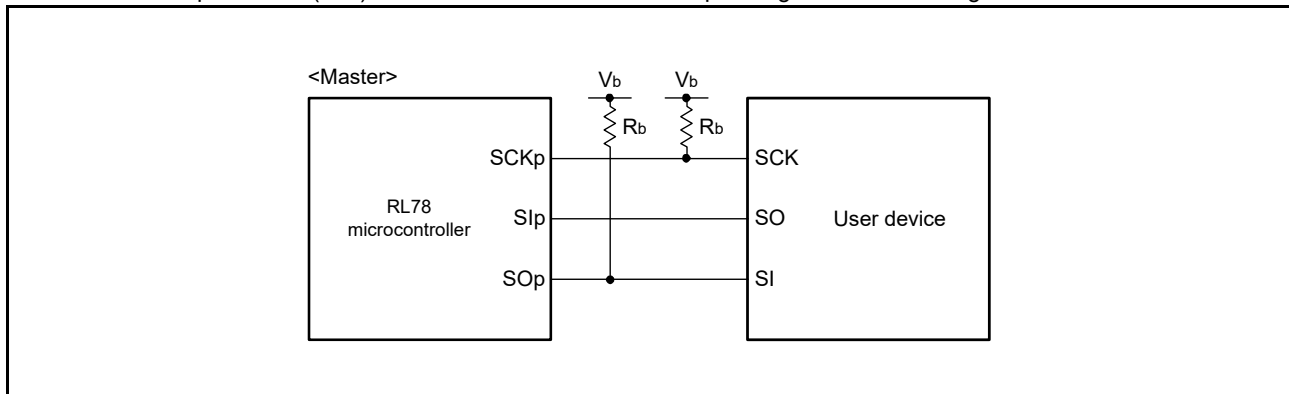
Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Slp setup time (to SCKp↓) <sup>Note</sup>	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	44		44		110		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		44		110		ns
Slp hold time (from SCKp↓) <sup>Note</sup>	tKS1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output <sup>Note</sup>	tKSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25		25	ns

**Note** This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the SOp and SCKp pins by using the port input mode register g (PIMg) and the port output mode register g (POMg). For VIH and VIL, see the DC characteristics with the TTL input buffer selected.

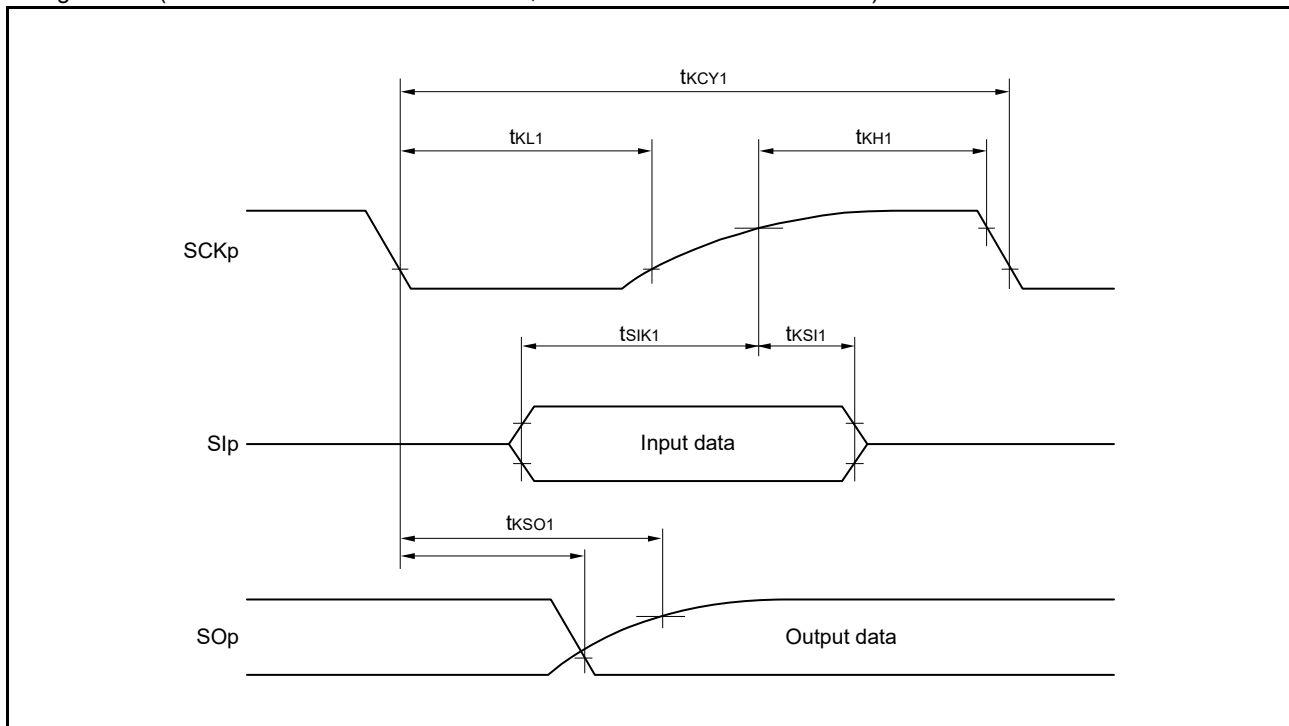
(Remarks are listed on the next page.)

Connection in simplified SPI (CSI) communications with devices operating at different voltage levels

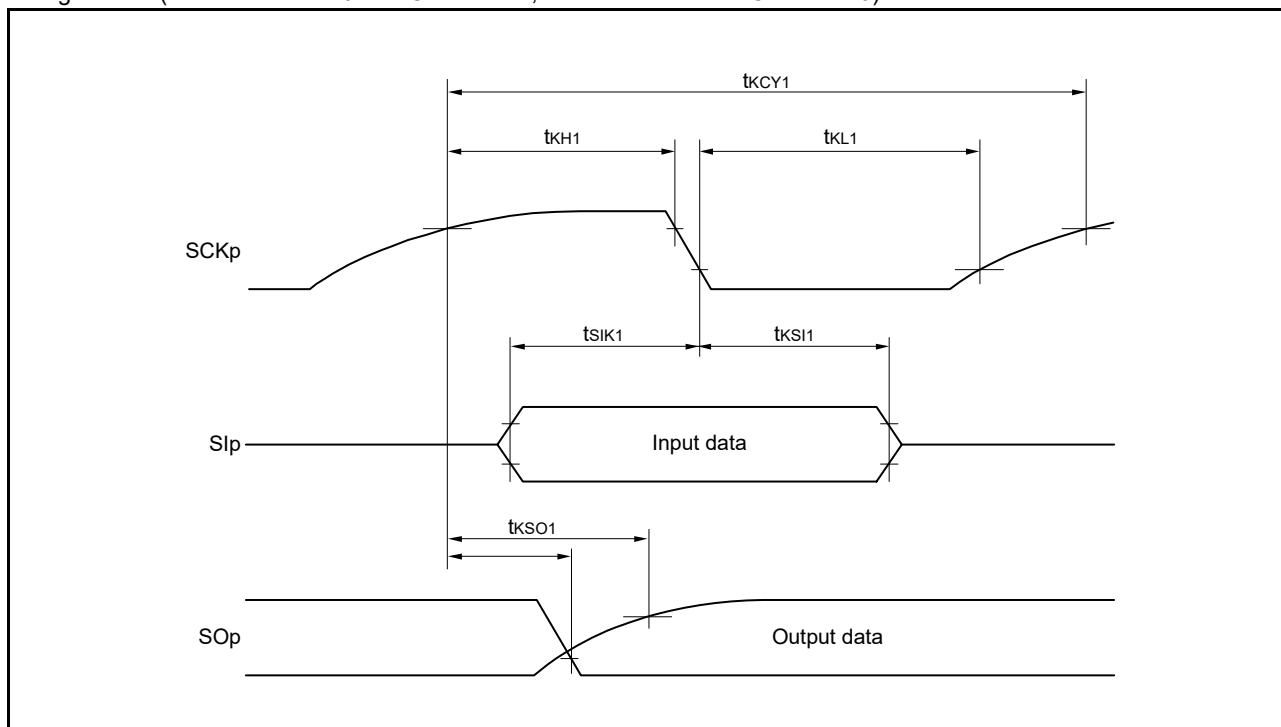


- Remark 1.**  $R_b[\Omega]$ : Communication line (SCKp, SOp) pull-up resistance,  $C_b[F]$ : Communication line (SCKp, SOp) load capacitance,  $V_b[V]$ : Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20), m: Unit number, n: Channel number (mn = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1, 3, 5, 7)
- Remark 3.** fMCK: Serial array unit operating clock frequency  
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00)
- Remark 4.** Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

Timing of serial transfer in simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Timing of serial transfer in simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



**Remark 1.** p: CSI number (p = 00, 01, 10, 20), m: Unit number, n: Channel number (mn = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

7. In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (2.5 V or 3 V) with the external SCKp clock

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time Note 1	tkCY2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	24 MHz < fMCK	14/fMCK		—		—		ns
			20 MHz < fMCK ≤ 24 MHz	12/fMCK		12/fMCK		—		ns
			8 MHz < fMCK ≤ 20 MHz	10/fMCK		10/fMCK		—		ns
			4 MHz < fMCK ≤ 8 MHz	8/fMCK		8/fMCK		—		ns
			fMCK ≤ 4 MHz	6/fMCK		6/fMCK		10/fMCK		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	24 MHz < fMCK	20/fMCK		—		—		ns
			20 MHz < fMCK ≤ 24 MHz	16/fMCK		16/fMCK		—		ns
			16 MHz < fMCK ≤ 20 MHz	14/fMCK		14/fMCK		—		ns
			8 MHz < fMCK ≤ 16 MHz	12/fMCK		12/fMCK		—		ns
			4 MHz < fMCK ≤ 8 MHz	8/fMCK		8/fMCK		—		ns
fMCK ≤ 4 MHz	6/fMCK		6/fMCK		10/fMCK		ns			
SCKp high-/low-level width	tkH2, tkL2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	tkCY2/2 - 12		tkCY2/2 - 12		tkCY2/2 - 50		ns	
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	tkCY2/2 - 18		tkCY2/2 - 18		tkCY2/2 - 50		ns	
Slp setup time (to SCKp↑) Note 2	tsIK2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	1/fMCK + 20		1/fMCK + 20		1/fMCK + 30		ns	
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	1/fMCK + 20		1/fMCK + 20		1/fMCK + 30		ns	
Slp hold time (from SCKp↑) Note 2	tkSI2		1/fMCK + 31		1/fMCK + 31		1/fMCK + 31		ns	
Delay time from SCKp↓ to SOp output Note 3	tkSO2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		2/fMCK + 120		2/fMCK + 120		2/fMCK + 573	ns	
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		2/fMCK + 214		2/fMCK + 214		2/fMCK + 573	ns	

**Note 1.** Transfer rate in the SNOOZE mode: 1 Mbps (max.)

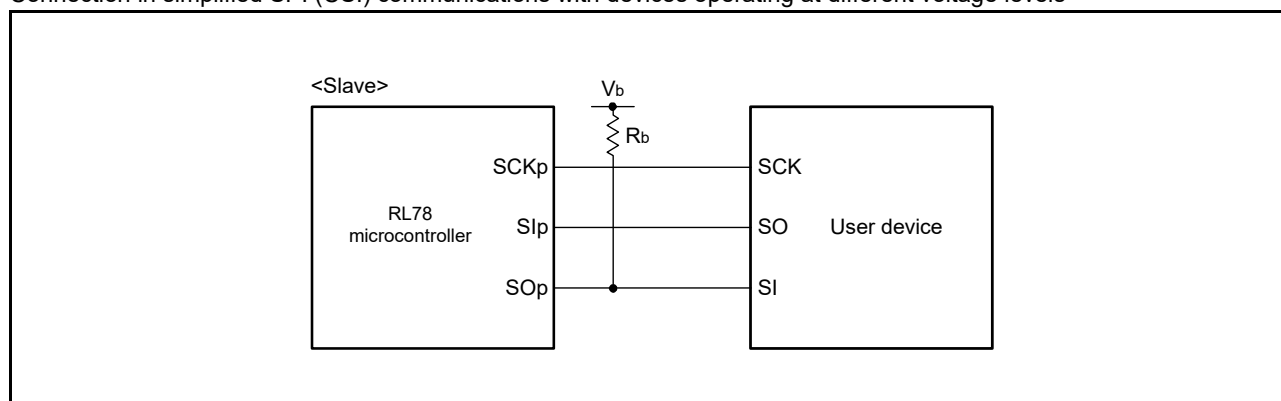
**Note 2.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” and Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp and SCKp pins and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the SOp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg). For VIH and VIL, see the DC characteristics with the TTL input buffer selected.

(Remarks are listed on the next page.)

## Connection in simplified SPI (CSI) communications with devices operating at different voltage levels



**Remark 1.**  $R_b[\Omega]$ : Communication line (SO<sub>p</sub>) pull-up resistance,  $C_b[F]$ : Communication line (SO<sub>p</sub>) load capacitance,  $V_b[V]$ : Communication line voltage

**Remark 2.** p: CSI number (p = 00, 01, 10, 20), m: Unit number, n: Channel number (mn = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 3.** f<sub>MCK</sub>: Serial array unit operating clock frequency

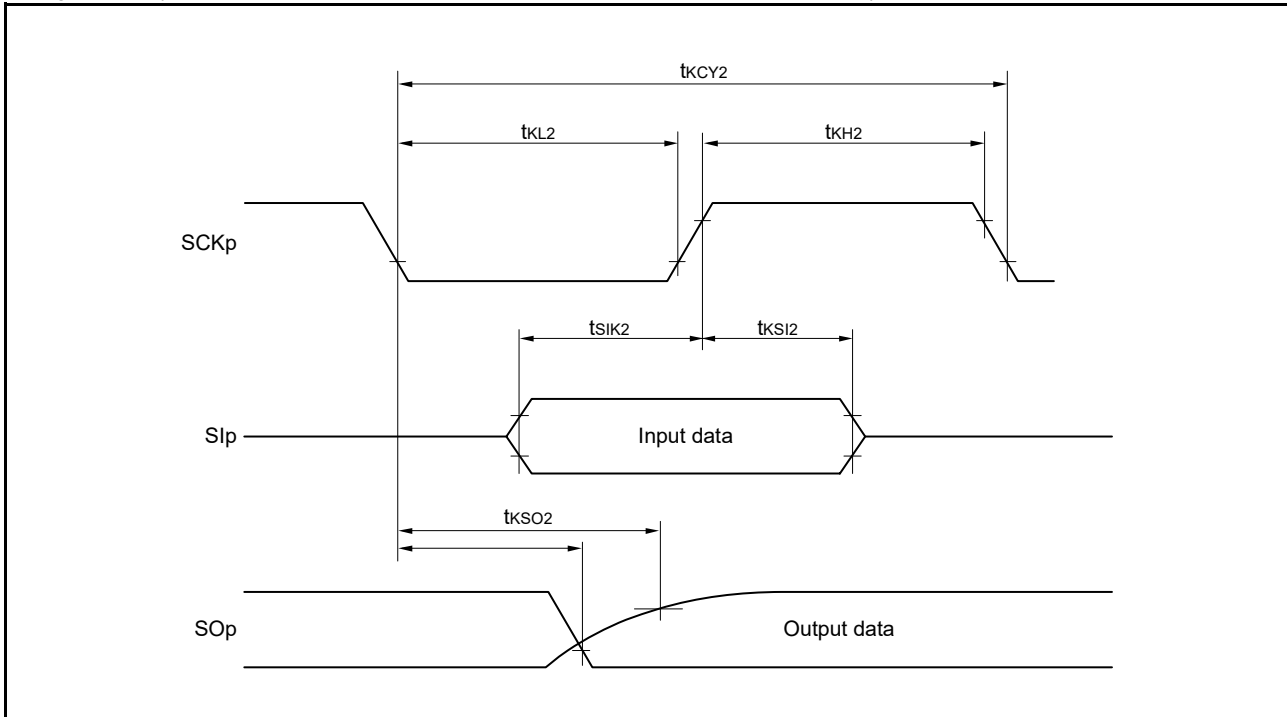
To set this operating clock, use the CKS<sub>mn</sub> bit in the serial mode register mn (SMR<sub>mn</sub>).

m: Unit number, n: Channel number (mn = 00, 01, 02, 10)

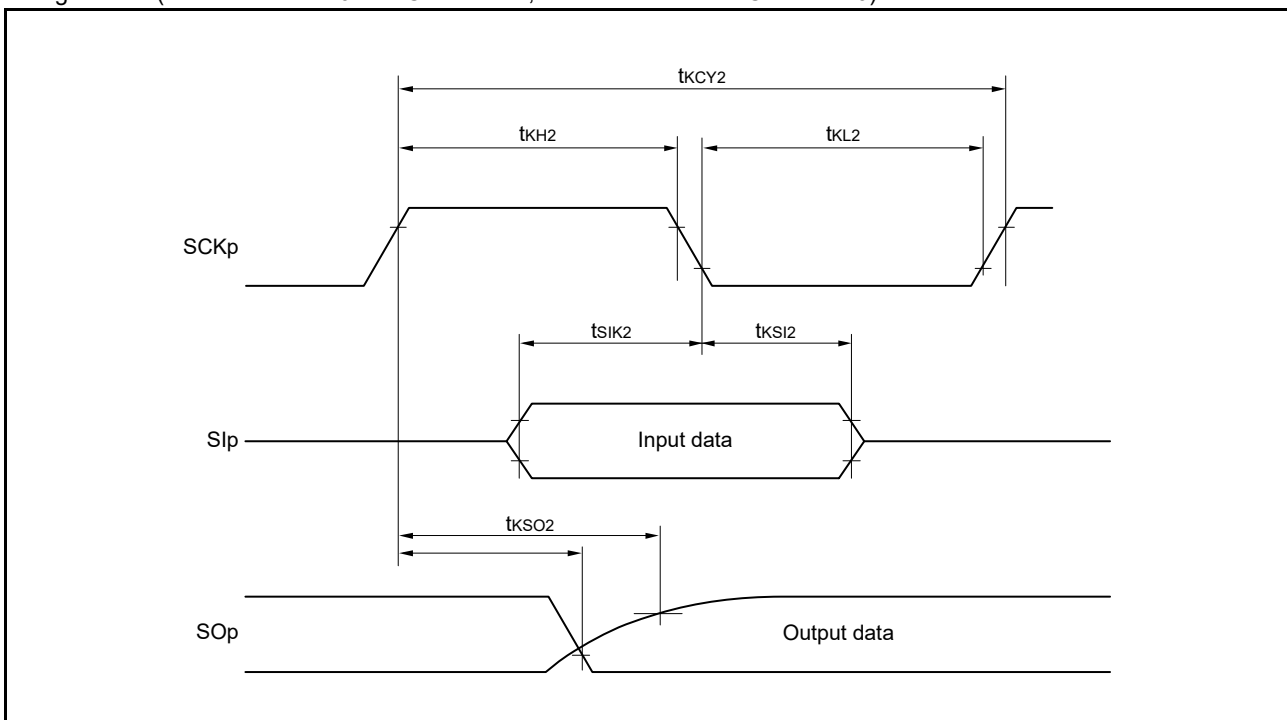
**Remark 4.** Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.



Timing of serial transfer in simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1)



Timing of serial transfer in simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0)



**Remark 1.** p: CSI number (p = 00, 01, 10, 20), m: Unit number, n: Channel number (mn = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1, 3, 5, 7)

**Remark 2.** Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

8. Simplified I<sup>2</sup>C communications with devices operating at different voltage levels (2.5 V or 3 V)

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(1/2)

Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	fSCL	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		1000 Note 1		300 Note 1	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		1000 Note 1		300 Note 1	kHz
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ		400 Note 1		400 Note 1		300 Note 1	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ		400 Note 1		400 Note 1		300 Note 1	kHz
Hold time when SCLr is low	tLOW	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	475		475		1550		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	475		475		1550		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1150		1550		1550		ns
Hold time when SCLr is high	tHIGH	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	245		245		610		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	200		200		610		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	675		675		610		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	600		600		610		ns

(Notes and Caution are listed on the next page, and Remarks are listed on page 172.)

8. Simplified I<sup>2</sup>C communications with devices operating at different voltage levels (2.5 V or 3 V)

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V, fMCK ≤ 32 MHz)

(2/2)

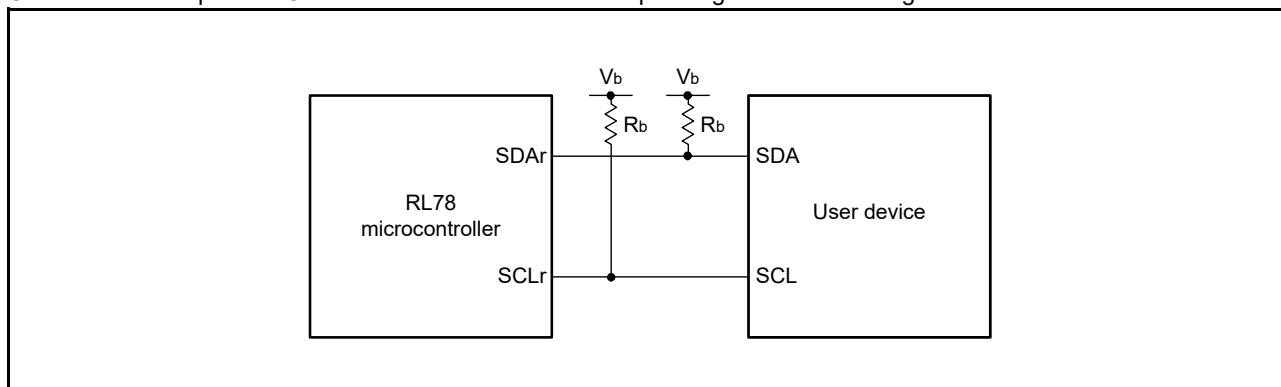
Item	Symbol	Conditions	HS (High-speed Main) Mode		LS (Low-speed Main) Mode		LP (Low-power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	tSU:DAT	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 135 Note 2		1/fMCK + 135 Note 2		1/fMCK + 190 Note 2		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 135 Note 2		1/fMCK + 135 Note 2		1/fMCK + 190 Note 2		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	1/fMCK + 190 Note 2		1/fMCK + 190 Note 2		1/fMCK + 190 Note 2		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1/fMCK + 190 Note 2		1/fMCK + 190 Note 2		1/fMCK + 190 Note 2		ns
Data hold time (transmission)	tHD:DAT	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	0	355	0	355	0	355	ns

**Note 1.** The listed frequencies must be no greater than fMCK/4.**Note 2.** Set the fMCK value that does not exceed the hold time when SCLr is low or high.

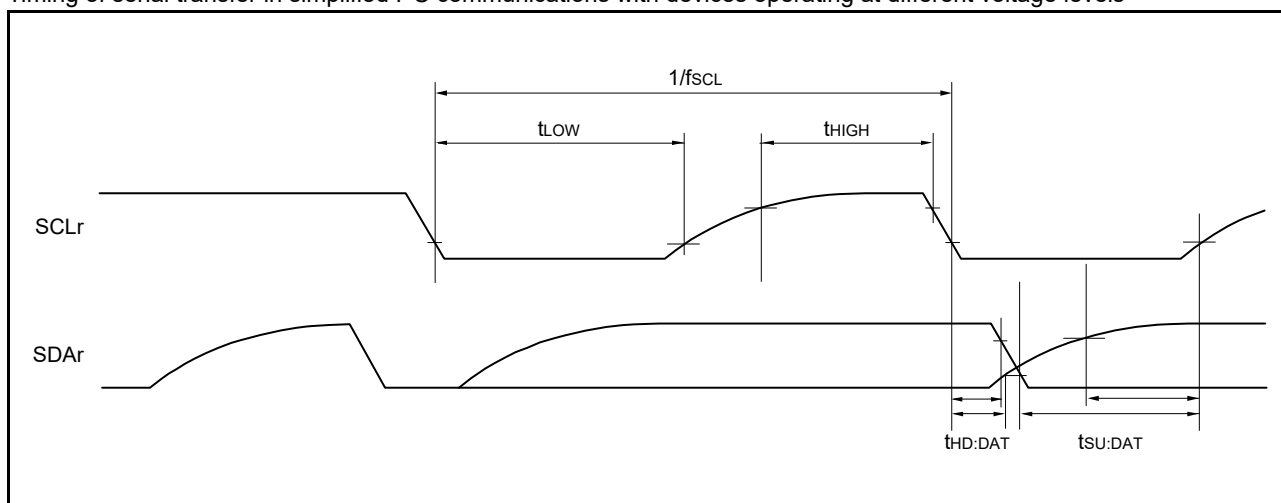
**Caution** Select the TTL input buffer and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the SDAr pin and the N-ch open drain output (VDD withstand voltage for 20- to 52-pin products/EVDD withstand voltage for 64-pin products) for the SCLr pin by using the port input mode register g (PIMg) and the port output mode register g (POMg). For VIH and VIL, see the DC characteristics with the TTL input buffer selected.

(Remarks are listed on the next page.)

Connection in simplified I<sup>2</sup>C communications with devices operating at different voltage levels



Timing of serial transfer in simplified I<sup>2</sup>C communications with devices operating at different voltage levels



- Remark 1.**  $R_b[\Omega]$ : Communication line (SDAr, SCLr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance,  $V_b[V]$ : Communication line voltage
- Remark 2.** r: IIC number (r = 00, 01, 10, 20), g: PIM and POM number (g = 0, 1, 3, 5, 7)
- Remark 3.**  $f_{MCK}$ : Serial array unit operating clock frequency  
To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00, 01, 02, 10)

### 3.5.2 Serial interface IICA

#### 1. I<sup>2</sup>C standard mode

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	Standard mode: fCLK ≥ 1 MHz	0		100	kHz
Setup time of restart condition	tSU:STA		4.7			μs
Hold time <sup>Note 1</sup>	tHD:STA		4.0			μs
Hold time when SCLA0 is low	tLOW		4.7			μs
Hold time when SCLA0 is high	tHIGH		4.0			μs
Data setup time (reception)	tSU:DAT		250			ns
Data setup time (transmission) <sup>Note 2</sup>	tHD:DAT		0		3.45	μs
Setup time of stop condition	tSU:STO		4.0			μs
Path free time	tBUF		4.7			μs

**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.

**Caution** The listed values are applicable even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

**Remark** The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.  
Cb = 400 pF, Rb = 2.7 kΩ

2. I<sup>2</sup>C fast mode

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz	0		400	kHz
Setup time of restart condition	tSU:STA		0.6			μs
Hold time <sup>Note 1</sup>	tHD:STA		0.6			μs
Hold time when SCLA0 is low	tLOW		1.3			μs
Hold time when SCLA0 is high	tHIGH		0.6			μs
Data setup time (reception)	tSU:DAT		100			ns
Data hold time (transmission) <sup>Note 2</sup>	tHD:DAT		0		0.9	μs
Setup time of stop condition	tSU:STO		0.6			μs
Bus-free time	tBUF		1.3			μs

**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.

**Caution** The listed values are applicable even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

**Remark** The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.  
Cb = 320 pF, Rb = 1.1 kΩ

3. I<sup>2</sup>C fast mode plus

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	Fast mode plus: fCLK ≥ 10 MHz	0		1000	kHz
Setup time of restart condition	tSU:STA		0.26			μs
Hold time <sup>Note 1</sup>	tHD:STA		0.26			μs
Hold time when SCLA0 is low	tLOW		0.5			μs
Hold time when SCLA0 is high	tHIGH		0.26			μs
Data setup time (reception)	tSU:DAT		50			ns
Data hold time (transmission) <sup>Note 2</sup>	tHD:DAT		0		0.45	μs
Setup time of stop condition	tSU:STO		0.26			μs
Bus-free time	tBUF		0.5			μs

**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.

**Caution** The listed values are applicable even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

**Remark** The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.  
Cb = 120 pF, Rb = 1.1 kΩ

## 4. SMBus/PMBus™ mode (100 kHz Class)

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	fCLK ≥ 1 MHz	10		100	kHz
Setup time of restart condition	tSU:STA		4.7			μs
Hold time <sup>Note 1</sup>	tHD:STA		4			μs
Hold time when SCLA0 is low	tLOW		4.7			μs
Hold time when SCLA0 is high	tHIGH		4			μs
Data setup time (reception)	tSU:DAT		250			ns
Data hold time (transmission) <sup>Note 2</sup>	tHD:DAT		0		3.45	μs
Setup time of stop condition	tSU:STO		4			μs
Clock/data falling time	tF				0.3	μs
Clock/data rising time	tR				1	μs
Bus-free time	tBUF		4.7			μs

**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.

**Caution** SMBus/PMBus™ communications are disabled when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1.

**Remark** The maximum value of communication line pull-up resistor (Rb) is as follows.  
Rb = 1.1 kΩ



5. SMBus/PMBus™ mode (400 kHz Class)

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	fCLK ≥ 3.5 MHz	10		400	kHz
Setup time of restart condition	tSU:STA		0.6			μs
Hold time <sup>Note 1</sup>	tHD:STA		0.6			μs
Hold time when SCLA0 is low	tLOW		1.3			μs
Hold time when SCLA0 is high	tHIGH		0.6			μs
Data setup time (reception)	tSU:DAT		100			ns
Data hold time (transmission) <sup>Note 2</sup>	tHD:DAT		0		0.9	μs
Setup time of stop condition	tSU:STO		0.6			μs
Clock/data falling time	tF				0.3	μs
Clock/data rising time	tR				0.3	μs
Bus-free time	tBUF		1.3			μs

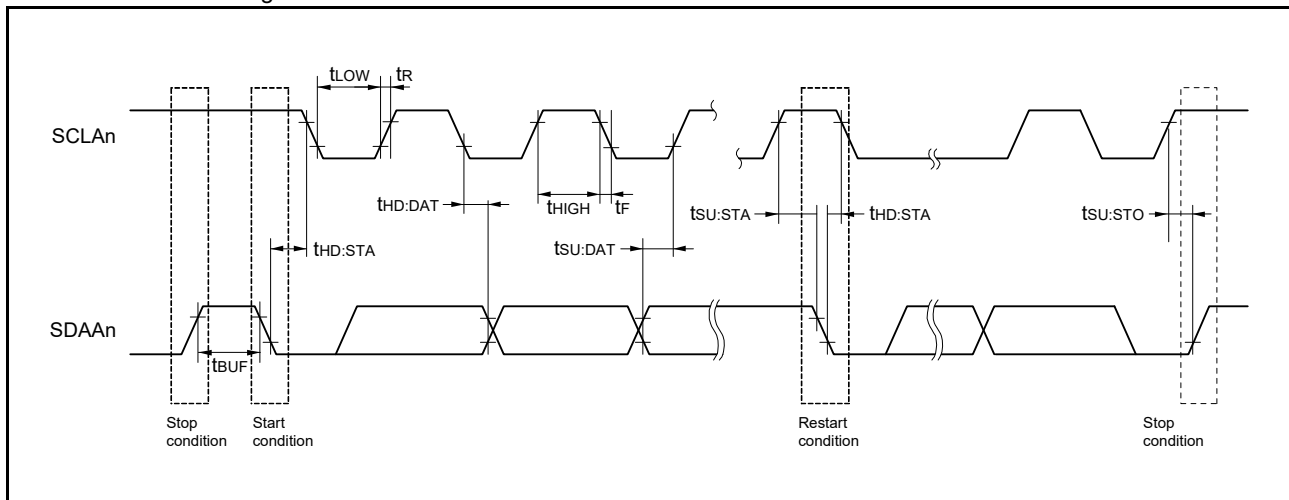
**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching is inserted on reception of an acknowledgment (ACK) signal.

**Caution** SMBus/PMBus™ communications are disabled when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1.

**Remark** The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows. Cb = 400 pF, Rb = 1.1 kΩ

IICA serial transfer timing



**Remark** n = 0

## 3.6 Analog Characteristics

### 3.6.1 A/D converter characteristics

#### 1. Normal modes 1 and 2

(TA = -40 to +125°C,  $2.7\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $f_{CLK} \leq 32\text{ MHz}$ , reference voltage (+) =  $AV_{REFP}$  ( $ADREFP[1:0] = 01B$ ), reference voltage (-) =  $AV_{REFM}$  ( $ADREFM = 1$ ), target pins: ANI2 to ANI7, ANI16 to ANI30, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	fAD		1		32	MHz
Overall error <sup>Notes 1, 3, 4, 5</sup>	AINL	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±7.5	LSB
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±9.0	LSB
Conversion time <sup>Note 6</sup>	tCONV	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$	2			μs
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$	2			μs
Zero-scale error <sup>Notes 1, 2, 3, 4, 5</sup>	Ezs	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.17	%FSR
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.21	%FSR
Full-scale error <sup>Notes 1, 2, 3, 4, 5</sup>	EFS	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.17	%FSR
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.21	%FSR
Integral linearity error <sup>Notes 1, 4, 5</sup>	ILE	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±3.0	LSB
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±3.0	LSB
Differential linearity error <sup>Note 1</sup>	DLE	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±1.0		LSB
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±1.0		LSB
Analog input voltage	VAIN		0		$AV_{REFP}$	V

**Note 1.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When pins ANI16 to ANI30 are selected as the conversion target, the maximum values are as follows.

Overall error: Add  $\pm 3$  LSB to the maximum value.

Zero-scale/full-scale error: Add  $\pm 0.04\%$ FSR to the maximum value.

**Note 4.** The maximum values are as follows when  $V_{DD}$  is selected for reference voltage (+) and  $V_{SS}$  is selected for reference voltage (-).

Overall error: Add  $\pm 10$  LSB to the maximum value.

Zero-scale/full-scale error: Add  $\pm 0.25\%$ FSR to the maximum value.

Integral linearity error: Add  $\pm 4$  LSB to the maximum value.

**Note 5.** When  $AV_{REFP} < V_{DD}$ , the maximum values are as follows.

Overall error/zero-scale/full-scale error: Add  $\pm 0.75\text{ LSB} \times (V_{DD}\text{ voltage (V)} - AV_{REFP}\text{ voltage (V)})$  to the maximum value.

Integral linearity error: Add  $\pm 0.2\text{ LSB} \times (V_{DD}\text{ voltage (V)} - AV_{REFP}\text{ voltage (V)})$  to the maximum value.

**Note 6.** When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, the sampling time must be at least 5 μs. Accordingly, use normal mode 2 with the longer sampling time.

## 2. Normal modes 1 and 2 (advanced mode)

(TA = –40 to +125°C,  $2.7\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $f_{CLK} \leq 48\text{ MHz}$ , reference voltage (+) =  $AV_{REFP}$  ( $ADREFP[1:0] = 01B$ ), reference voltage (–) =  $AV_{REFM}$  ( $ADREFM = 1$ ), target pins: ANI2 to ANI7, ANI16 to ANI30, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	fAD		1		48	MHz
Overall error <sup>Notes 1, 3, 4, 5, 6, 7</sup>	AINL	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±7.5	LSB
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±9.0	LSB
Conversion time <sup>Notes 7, 8</sup>	tCONV	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$	1			μs
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$	1			μs
Zero-scale error <sup>Notes 1, 2, 3, 4, 5, 6, 7</sup>	Ezs	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.17	%FSR
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.21	%FSR
Full-scale error <sup>Notes 1, 2, 3, 4, 5, 6, 7</sup>	EFS	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.17	%FSR
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.21	%FSR
Integral linearity error <sup>Notes 1, 4, 5</sup>	ILE	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±3.0	LSB
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±3.0	LSB
Differential linearity error <sup>Note 1</sup>	DLE	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±1.0		LSB
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±1.0		LSB
Analog input voltage	VAIN		0		$AV_{REFP}$	V

**Note 1.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When pins ANI16 to ANI30 are selected as the conversion target, the maximum values are as follows.

Overall error: Add  $\pm 3$  LSB to the maximum value.

Zero-scale/full-scale error: Add  $\pm 0.04\%$ FSR to the maximum value.

**Note 4.** The maximum values are as follows when  $V_{DD}$  is selected for reference voltage (+) and  $V_{SS}$  is selected for reference voltage (–).

Overall error: Add  $\pm 10$  LSB to the maximum value.

Zero-scale/full-scale error: Add  $\pm 0.25\%$ FSR to the maximum value.

Integral linearity error: Add  $\pm 4$  LSB to the maximum value.

**Note 5.** When  $AV_{REFP} < V_{DD}$ , the maximum values are as follows.

Overall error/zero-scale/full-scale error: Add  $\pm 0.75\text{ LSB} \times (V_{DD}\text{ voltage (V)} - AV_{REFP}\text{ voltage (V)})$  to the maximum value.

Integral linearity error: Add  $\pm 0.2\text{ LSB} \times (V_{DD}\text{ voltage (V)} - AV_{REFP}\text{ voltage (V)})$  to the maximum value.

**Note 6.** When the sample & hold circuit is selected as the conversion target, the maximum values are as follows.

Overall error: Add  $\pm 1$  LSB to the maximum value.

Zero-scale/full-scale error: Add  $\pm 0.03\%$ FSR to the maximum value.

**Note 7.** Add the following values to the listed values in the cases below.

- 7 fAD when the conversion target includes low-speed conversion ANI (ANI16 to ANI30)
- 12 fAD when the conversion target includes the PGA with the gain of  $\times 4$  to  $\times 16$ .
- 43 fAD when the conversion target includes the PGA with the gain of  $\times 32$ .

**Note 8.** When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, the sampling time must be at least 5 μs. Accordingly, use normal mode 2 with the longer sampling time.

## 3. Low-voltage modes 1 and 2

(TA = -40 to +125°C,  $2.7\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $f_{CLK} \leq 32\text{ MHz}$ ,  
reference voltage (+) =  $AV_{REFP}$  ( $ADREFP[1:0] = 01B$ ), reference voltage (-) =  $AV_{REFM}$  ( $ADREFM = 1$ ),  
target pins: ANI2 to ANI7, ANI16 to ANI30, PGA, S&H, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	fAD		1		24	MHz
Overall error <sup>Notes 1, 3, 4, 5</sup>	AINL	$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±9.0	LSB
Conversion time <sup>Note 6</sup>	tCONV	$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$	3.33			µs
Zero-scale error <sup>Notes 1, 2, 3, 4, 5</sup>	EZS	$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.21	%FSR
Full-scale error <sup>Notes 1, 2, 3, 4, 5</sup>	EFS	$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.21	%FSR
Integral linearity error <sup>Notes 1, 4, 5</sup>	ILE	$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±4.0	LSB
Differential linearity error <sup>Note 1</sup>	DLE	$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±1.5		LSB
Analog input voltage	VAIN		0		$AV_{REFP}$	V

**Note 1.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When pins ANI16 to ANI30 are selected as the conversion target, the maximum values are as follows.

Overall error: Add  $\pm 3$  LSB to the maximum value.

Zero-scale/full-scale error: Add  $\pm 0.04\%$ FSR to the maximum value.

**Note 4.** The maximum values are as follows when  $V_{DD}$  is selected for reference voltage (+) and  $V_{SS}$  is selected for reference voltage (-).

Overall error: Add  $\pm 10$  LSB to the maximum value.

Zero-scale/full-scale error: Add  $\pm 0.25\%$ FSR to the maximum value.

Integral linearity error: Add  $\pm 4$  LSB to the maximum value.

**Note 5.** When  $AV_{REFP} < V_{DD}$ , the maximum values are as follows.

Overall error/zero-scale/full-scale error: Add  $\pm 0.75\text{ LSB} \times (V_{DD}\text{ voltage (V)} - AV_{REFP}\text{ voltage (V)})$  to the maximum value.

Integral linearity error: Add  $\pm 0.2\text{ LSB} \times (V_{DD}\text{ voltage (V)} - AV_{REFP}\text{ voltage (V)})$  to the maximum value.

**Note 6.** When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, the sampling time must be at least  $5\text{ }\mu\text{s}$ . Accordingly, use low-voltage mode 2 with the longer sampling time and the conversion clock (fAD) with a frequency of no more than 16 MHz.

## 4. Low-voltage modes 1 and 2 (advanced mode)

(TA = -40 to +125°C, 2.7 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, fCLK ≤ 48 MHz,  
reference voltage (+) = AVREFP (ADREFP[1:0] = 01B), reference voltage (-) = AVREFM (ADREFM = 1),  
target pins: ANI2 to ANI7, ANI16 to ANI30, PGA, S&H, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	fAD		1		24	MHz
Overall error <sup>Notes 1, 3, 4, 5, 6</sup>	AINL	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±9.0	LSB
Conversion time <sup>Note 7</sup>	tCONV	2.7 V ≤ AVREFP = VDD ≤ 5.5 V	3.63			μs
Zero-scale error <sup>Notes 1, 2, 3, 4, 5, 6</sup>	EZS	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
Full-scale error <sup>Notes 1, 2, 3, 4, 5, 6</sup>	EFS	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
Integral linearity error <sup>Notes 1, 4, 5</sup>	ILE	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±4.0	LSB
Differential linearity error <sup>Note 1</sup>	DLE	2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±1.5		LSB
Analog input voltage	VAIN		0		AVREFP	V

**Note 1.** This value does not include the quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When pins ANI16 to ANI30 are selected as the conversion target, the maximum values are as follows.

Overall error: Add ±3 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.04%FSR to the maximum value.

**Note 4.** The maximum values are as follows when VDD is selected for reference voltage (+) and VSS is selected for reference voltage (-).

Overall error: Add ±10 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.25%FSR to the maximum value.

Integral linearity error: Add ±4 LSB to the maximum value.

**Note 5.** When AVREFP < VDD, the maximum values are as follows.

Overall error/zero-scale/full-scale error: Add ±0.75 LSB × (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.

Integral linearity error: Add ±0.2 LSB × (VDD voltage (V) – AVREFP voltage (V)) to the maximum value.

**Note 6.** When the sample & hold circuit is selected as the conversion target, the maximum values are as follows.

Overall error: Add ±1 LSB to the maximum value.

Zero-scale/full-scale error: Add ±0.03%FSR to the maximum value.

**Note 7.** When the internal reference voltage or the temperature sensor output voltage is selected as the conversion target, the sampling time must be at least 5 μs. Accordingly, use low-voltage mode 2 with the longer sampling time and the conversion clock (fAD) with a frequency of no more than 16 MHz.

## 5. When the internal reference voltage is selected as reference voltage (+)

(TA = -40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V, low-voltage modes 1 and 2, fCLK ≤ 32 MHz<sup>Note 1</sup>, fCLK ≤ 48 MHz<sup>Note 2</sup>, reference voltage (+) = internal reference voltage (ADREFP[1:0] = 10B), reference voltage (-) = AVREFM (ADREFM = 1))

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8			Bit
Conversion clock	fAD		1		2	MHz
Zero-scale error <sup>Notes 3, 4, 6</sup>	EZS				±0.6	%FSR
Integral linearity error <sup>Notes 3, 6</sup>	ILE				±2.0	LSB
Differential linearity error <sup>Note 3</sup>	DLE			±1.0		LSB
Analog input voltage	VAIN		0		VBGR Note 5	V

**Note 1.** This applies when the advanced mode is disabled.

**Note 2.** This applies when the advanced mode is enabled.

**Note 3.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 4.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 5.** Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

**Note 6.** When reference voltage (-) is selected as VSS, the maximum values are as follows.

Zero-scale error: Add  $\pm 0.35\%$ FSR to the maximum value.

Integral linearity error: Add  $\pm 0.5$  LSB to the maximum value.

### 3.6.2 Temperature sensor/internal reference voltage characteristics

(TA = -40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	VTMPS25	ADS register is set to 80H, TA = +25°C		1.05		V
Internal reference voltage	VBGR	ADS register is set to 81H	1.40	1.48	1.56	V
Temperature coefficient	FVTMPS	Temperature dependency of the temperature sensor voltage		-3.3		mV/°C
Operation stabilization wait time	tAMP		5			μs

### 3.6.3 D/A converter characteristics

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES	DAC0, DAC1 (DACONF = 0)			10	Bit
		DAC1 (DACONF = 1), DAC2			8	Bit
Overall error	AINL	Rload = 8 MΩ			±2.5	LSB
Differential non-linearity error	ADNL				±1.0	LSB
Settling time	tSET	Clod = 20 pF when DAC0 is output			6	μs
		During full code conversion using CMP reference			3	μs
		During 1LSB code conversion using CMP reference			1	μs

**Caution** The voltage on the ANO0 to ANO2 pins must not exceed EVDD0.

### 3.6.4 Comparator characteristics

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage range	IVREF	IVREF0 pin, IVREF1 pin input	0		EVDD0	V
	IVCMP	IVCMP0, IVCMP1, IVCMP2, IVCMP3 pin input	0		EVDD0	V
Output delay	td	Input amplitude ±100 mV		50	100	ns
Offset voltage	—			±5	±40	mV
Operation stabilization time <sup>Note</sup>	tCMP		1			μs
Input channel switching stabilization wait time	—		0.3			μs

**Note** The listed values indicate the time until the DC/AC characteristics of the comparator are satisfied following enabling of the comparator operation (CnENB = 1).

## 3.6.5 PGA characteristics

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input offset voltage	VIOPGA					±10	mV
Input voltage range <sup>Note 1</sup>	VIPGA			0		0.9 × VDD/ amplification rate	V
Amplification rate error		×4, ×8				±1	%
		×16				±1.5	%
		×32				±2	%
Slew rate <sup>Note 1</sup>	SRRPGA	Rising Vin = VDD × 0.1/ amplification rate to VDD × 0.9/ amplification rate 10 to 90% of output amplitude	4.0 V ≤ VDD ≤ 5.5 V	Other than ×32	3.5		V/μs
			4.0 V ≤ VDD ≤ 5.5 V	×32	3		
			2.7 V ≤ VDD ≤ 4.0 V		0.5		
	SFPGA	Falling Vin = VDD × 0.1/ amplification rate to VDD × 0.9/ amplification rate 90 to 10% of output amplitude	4.0 V ≤ VDD ≤ 5.5 V	Other than ×32	3.5		
			4.0 V ≤ VDD ≤ 5.5 V	×32	3		
			2.7 V ≤ VDD ≤ 4.0 V		0.5		
Operation stabilization wait time <sup>Note 2</sup>	tPGA	×4, ×8				5	μs
		×16, ×32				10	μs

**Note 1.** A voltage of EVDD0 is supplied to the PGA10 to PGA13 pins.

**Note 2.** The listed values indicate the time until the DC/AC characteristics of PGA operation are satisfied following enabling of the PGA operation (PGAEN = 1).

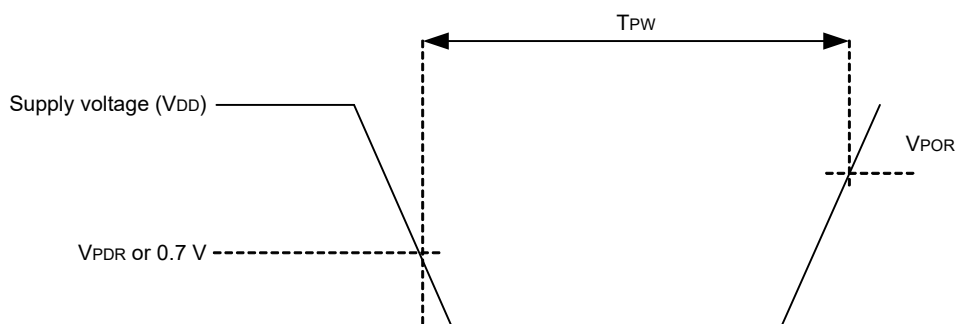


### 3.6.6 POR circuit characteristics

(TA = -40 to +125°C, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	V <sub>POR</sub> , V <sub>PDR</sub>		1.43	1.50	1.57	V
Minimum pulse width <sup>Note</sup>	TPW		300			μs

**Note** This width is the minimum time required for a POR reset when V<sub>DD</sub> falls below V<sub>PDR</sub>. This width is also the minimum time required for a POR reset from when V<sub>DD</sub> falls below 0.7 V to when V<sub>DD</sub> exceeds V<sub>POR</sub> in the STOP mode or while the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



### 3.6.7 LVD circuit characteristics

#### 1. LVD detection voltage in the LVD0 reset mode and interrupt mode

(TA = -40 to +125°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	Supply voltage level	VLVD00	The power supply voltage is rising.	3.84	3.96	4.08	V
			The power supply voltage is falling.	3.76	3.88	4.00	V
		VLVD01	The power supply voltage is rising.	2.88	2.97	3.06	V
			The power supply voltage is falling.	2.82	2.91	3.00	V
Minimum pulse width		tlw		500			μs
Detection delay time						500	μs

#### 2. LVD detection voltage in the LVD1 reset mode and interrupt mode

(TA = -40 to +125°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	Supply voltage level	VLVD10	The power supply voltage is rising.	4.08	4.16	4.24	V
			The power supply voltage is falling.	4.00	4.08	4.16	V
		VLVD11	The power supply voltage is rising.	3.88	3.96	4.04	V
			The power supply voltage is falling.	3.80	3.88	3.96	V
		VLVD12	The power supply voltage is rising.	3.68	3.75	3.82	V
			The power supply voltage is falling.	3.60	3.67	3.74	V
		VLVD13	The power supply voltage is rising.	3.48	3.55	3.62	V
			The power supply voltage is falling.	3.40	3.47	3.54	V
		VLVD14	The power supply voltage is rising.	3.28	3.35	3.42	V
			The power supply voltage is falling.	3.20	3.27	3.34	V
		VLVD15	The power supply voltage is rising.	3.07	3.13	3.19	V
			The power supply voltage is falling.	3.00	3.06	3.12	V
		VLVD16	The power supply voltage is rising.	2.91	2.97	3.03	V
			The power supply voltage is falling.	2.85	2.91	2.97	V
		VLVD17	The power supply voltage is rising.	2.76	2.82	2.87	V
			The power supply voltage is falling.	2.70	2.76	2.81	V
Minimum pulse width		tlw		500			μs
Detection delay						500	μs

### 3.6.8 Power supply voltage rising slope characteristics

(TA = -40 to +125°C, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power voltage rising slope	SVDD				54	V/ms

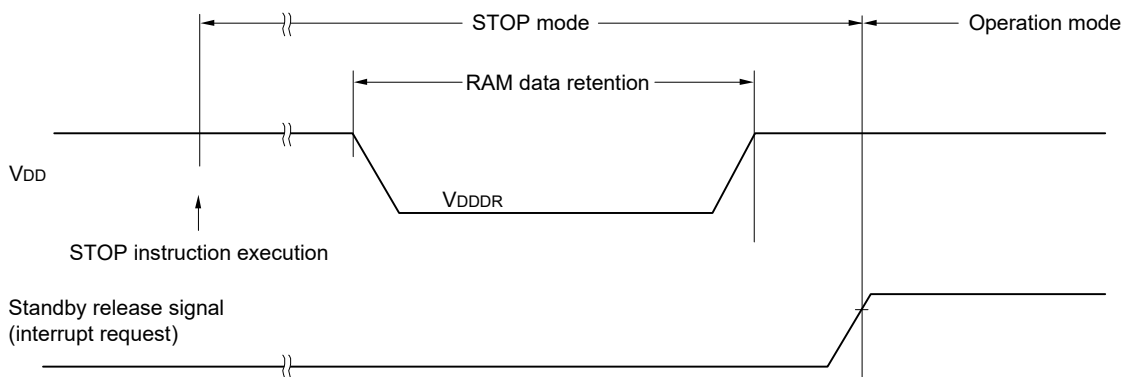
**Caution** Make sure to keep the internal reset state by the LVD0 circuit or an external reset until VDD reaches the operating voltage range shown in AC characteristics.

### 3.7 RAM Data Retention Characteristics

(TA = -40 to +125°C, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention power voltage	VDDDR		1.43 <sup>Note</sup>		5.5	V

**Note** This voltage depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.



### 3.8 Flash Memory Programming Characteristics

(TA = -40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CPU/peripheral hardware clock frequency	fCLK		1		48	MHz
Number of code flash rewrites <sup>Notes 1, 2, 3</sup>	Cerwr	Retained for 10 years TA = 85°C	10,000			Times
		Retained for 20 years TA = 85°C	1,000			
Number of data flash rewrites <sup>Notes 1, 2, 3</sup>	Cerwr	Retained for 1 year TA = 25°C		1,000,000		
		Retained for 5 years TA = 85°C	100,000			
		Retained for 20 years TA = 85°C	10,000			

- Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
- Note 2.** The listed numbers of times apply when using the flash memory programmer and the Renesas Electronics self-programming library.
- Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 1. Code flash memory

(TA = -40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	fCLK = 1 MHz			fCLK = 2 MHz, 3 MHz			4 MHz ≤ fCLK < 8 MHz			8 MHz ≤ fCLK < 32 MHz			fCLK = 32 MHz			fCLK = 48 MHz			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time	4 bytes	tP4	—	75.8	666.6	—	51.5	469.7	—	41.9	387.3	—	37.2	347.4	—	34.2	322.3	—	33.9	319.7	μs
Erase time	2 Kbytes	tE2K	—	10.4	312.2	—	7.7	258.5	—	6.4	231.8	—	5.8	218.4	—	5.6	214.4	—	5.6	213.9	ms
Blank checking time	4 bytes	tBC4	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	—	—	8.1	μs
	2 Kbytes	tBC2K	—	—	2618.9	—	—	1309.5	—	—	658.3	—	—	332.8	—	—	234.1	—	—	223.19	μs
Time taken to forcibly stop erasure		tSED	—	—	19.0	—	—	14.5	—	—	12.3	—	—	11.1	—	—	10.4	—	—	10.3	μs
Security setting time		tAWSSAS	—	18.2	526.4	—	14.4	469.3	—	12.6	441.1	—	11.6	427.1	—	11.3	422.6	—	11.3	422.1	ms
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	μs

**Caution** The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

## 2. Data flash memory

(TA = -40 to +125°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	fCLK = 1 MHz			fCLK = 2 MHz, 3 MHz			4 MHz ≤ fCLK < 8 MHz			8 MHz ≤ fCLK < 32 MHz			fCLK = 32 MHz			fCLK = 48 MHz			Unit	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time	1 byte	tP4	—	75.8	666.6	—	51.51	469.7	—	41.9	387.34	—	37.24	347.4	—	34.2	322.3	—	33.92	319.7	μs
Erase time	256 bytes	tE2K	—	7.8	259.2	—	6.4	232.0	—	5.8	218.5	—	5.5	211.8	—	5.4	209.7	—	5.3	209.5	ms
Blank checking time	1 byte	tBC4	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	—	—	8.1	μs
	256 bytes	tBC2K	—	—	1326.1	—	—	663.1	—	—	335.1	—	—	171.2	—	—	121.0	—	—	115.5	μs
Time taken to forcibly stop erasure		tSED	—	—	19.0	—	—	14.5	—	—	12.3	—	—	11.1	—	—	10.4	—	—	10.3	μs
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	μs
Time until reading starts following setting DFLEN to 1		—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	ns

**Caution** The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

### 3.9 Dedicated Flash Memory Programmer Communication (UART)

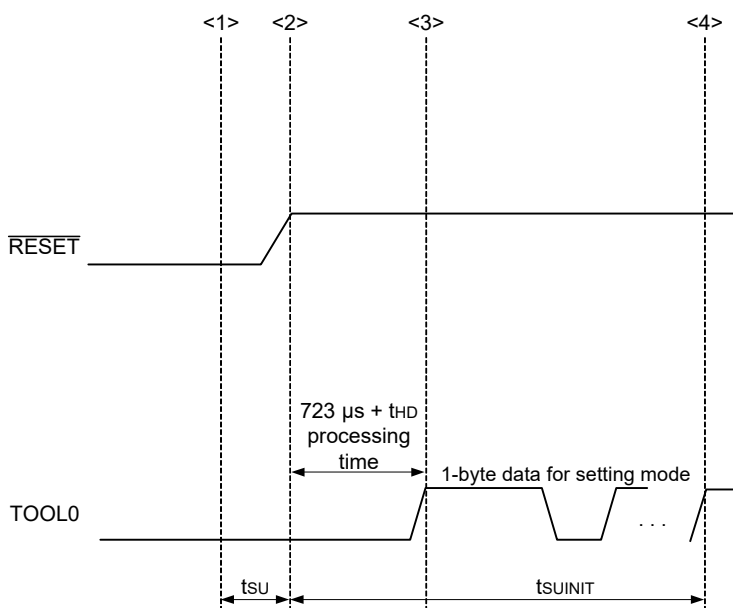
(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

### 3.10 Timing of Entry to Flash Memory Programming Modes

(TA = -40 to +125°C, 2.7 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Time to complete the communication for the initial setting after the external reset is released	tsuINIT	POR and LVD reset must be released before the external reset is released			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	tsu	POR and LVD reset must be released before the external reset is released	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (the processing time of the firmware to control the flash memory is not included)	tHD	POR and LVD reset must be released before the external reset is released	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released. Note that the POR and LVD reset must be released before the external reset is released.
- <3> The TOOL0 pin is set to the high level.
- <4> The baud rate setting is complete upon UART reception.

**Remark** tsuINIT: The time during which the communications for the initial setting must be completed within 100 ms after the external reset is released.

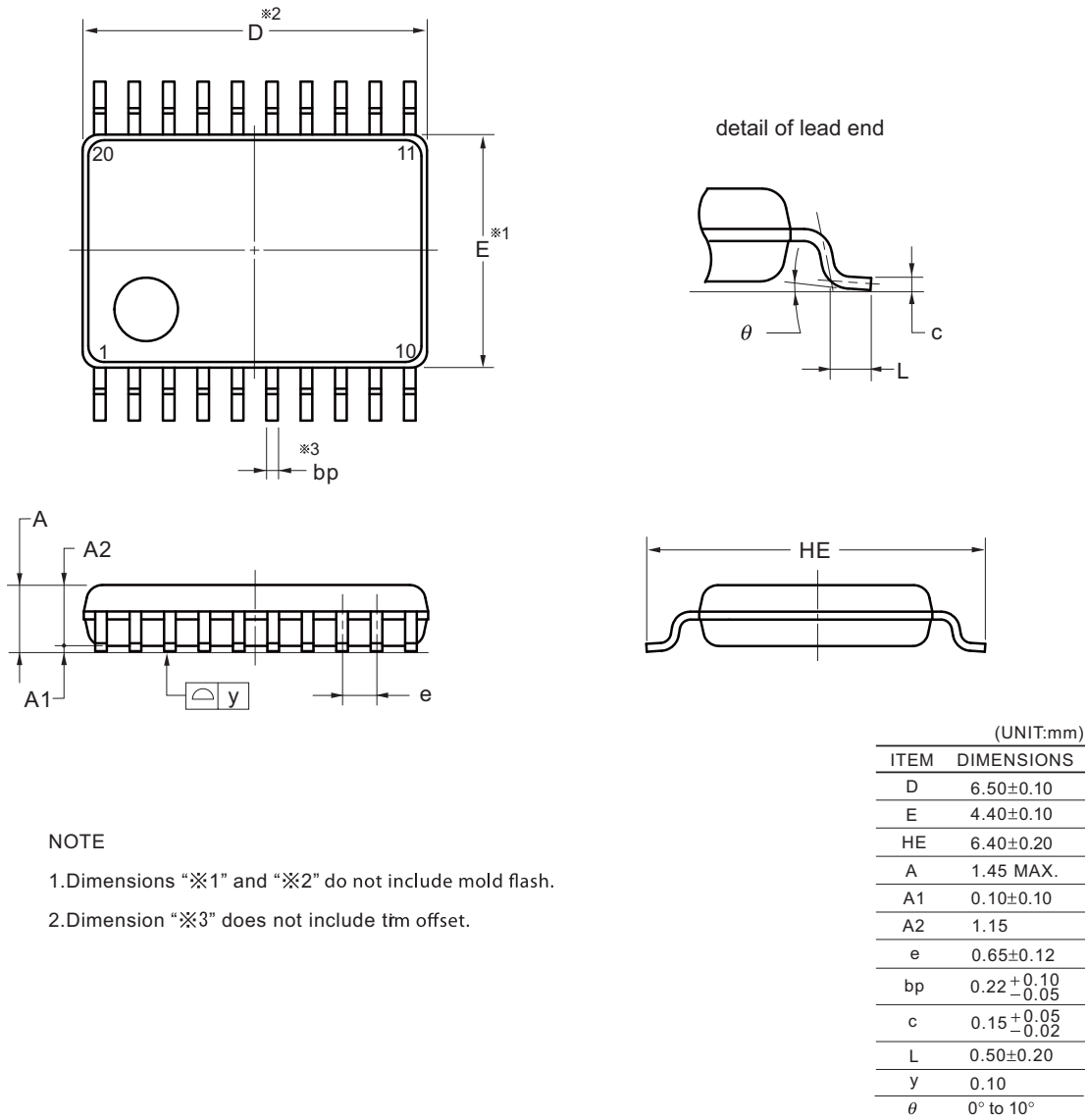
tsu: Time to release the external reset after the TOOL0 pin is set to the low level

tHD: Time to hold the TOOL0 pin at the low level after the external reset is released. It does not include the processing time of the firmware to control the flash memory.

## 4. Package Drawings

### 4.1 20-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	P20MA-65-NAA-1	0.1



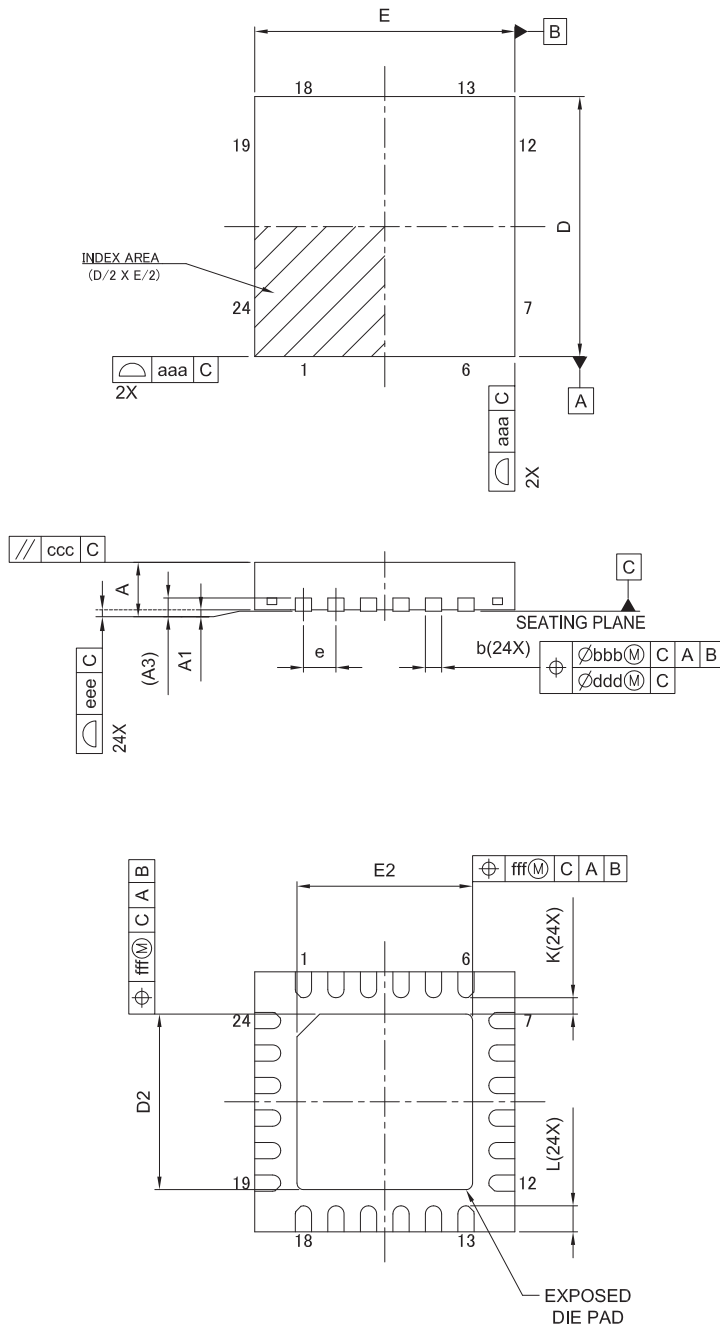
**NOTE**

1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include tfm offset.

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4.2 24-pin Products

JEITA Package Code	RENESAS Code	MASS (Typ.) [g]
P-HWFQFN24-4 × 4-0.50	PWQN0024KG-A	0.04



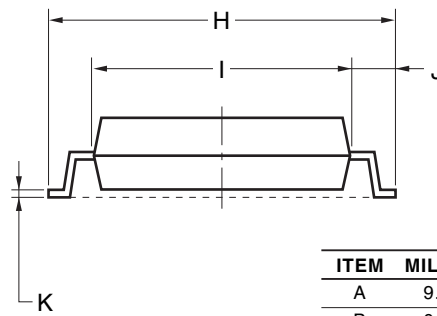
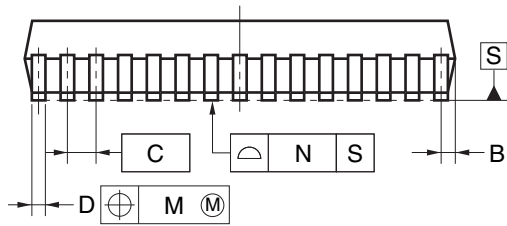
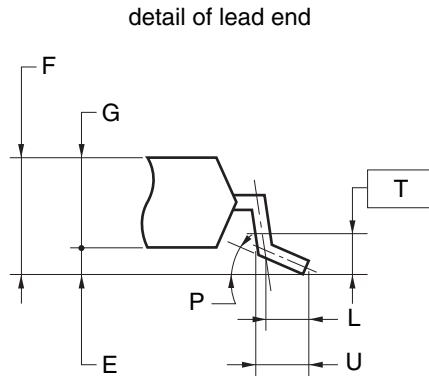
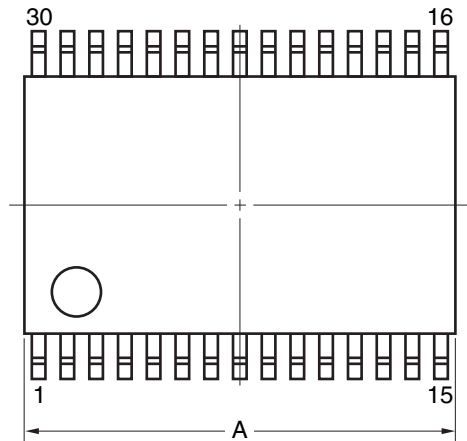
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A <sub>1</sub>	0.00	0.02	0.05
A <sub>3</sub>	0.203 REF.		
b	0.18	0.25	0.30
D	4.00 BSC		
E	4.00 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
K	0.20	—	—
D <sub>2</sub>	2.65	2.70	2.75
E <sub>2</sub>	2.65	2.70	2.75
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		





4.4 30-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



**NOTE**

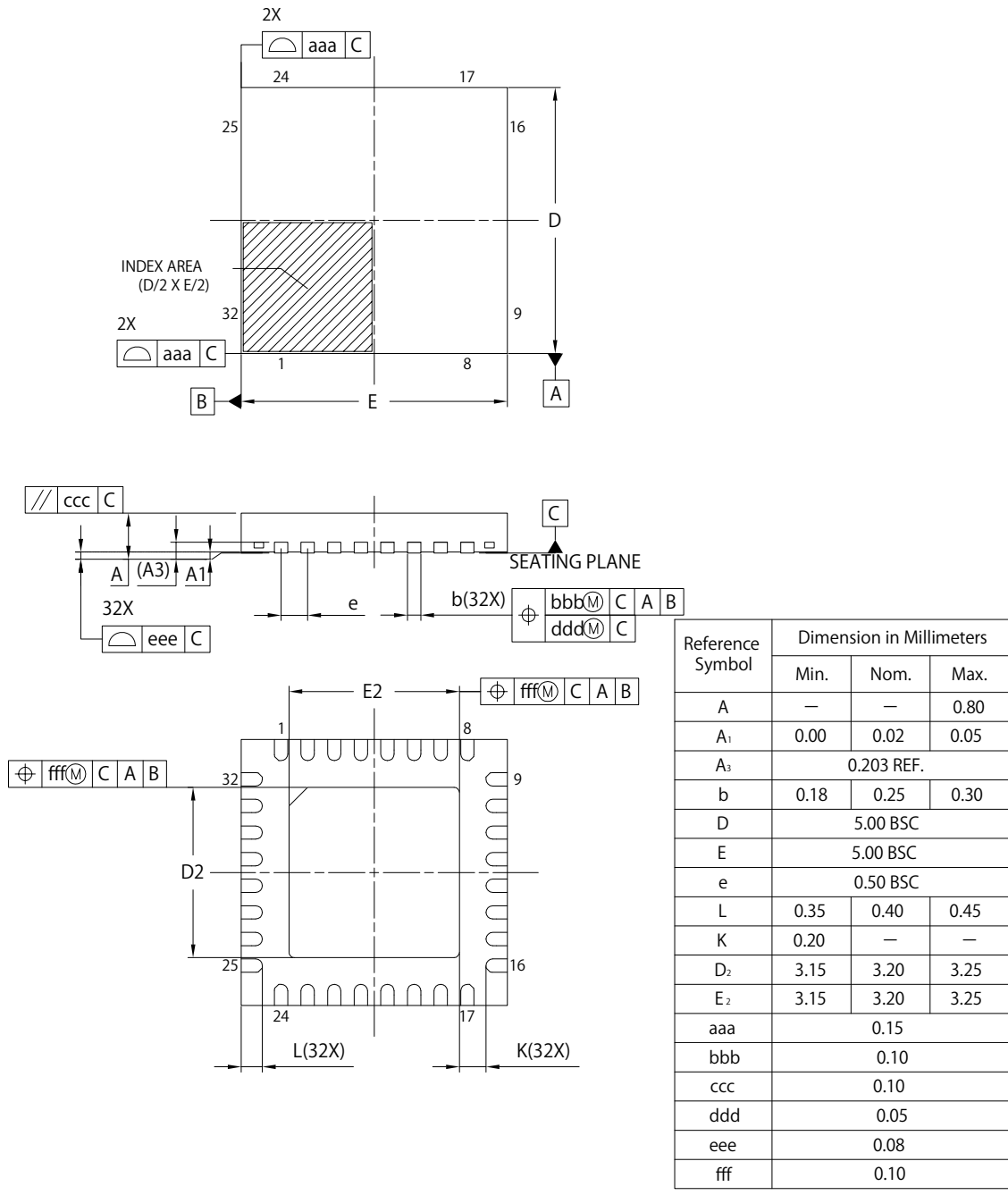
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° <sup>+5°</sup> <sub>-3°</sub>
T	0.25
U	0.6±0.15

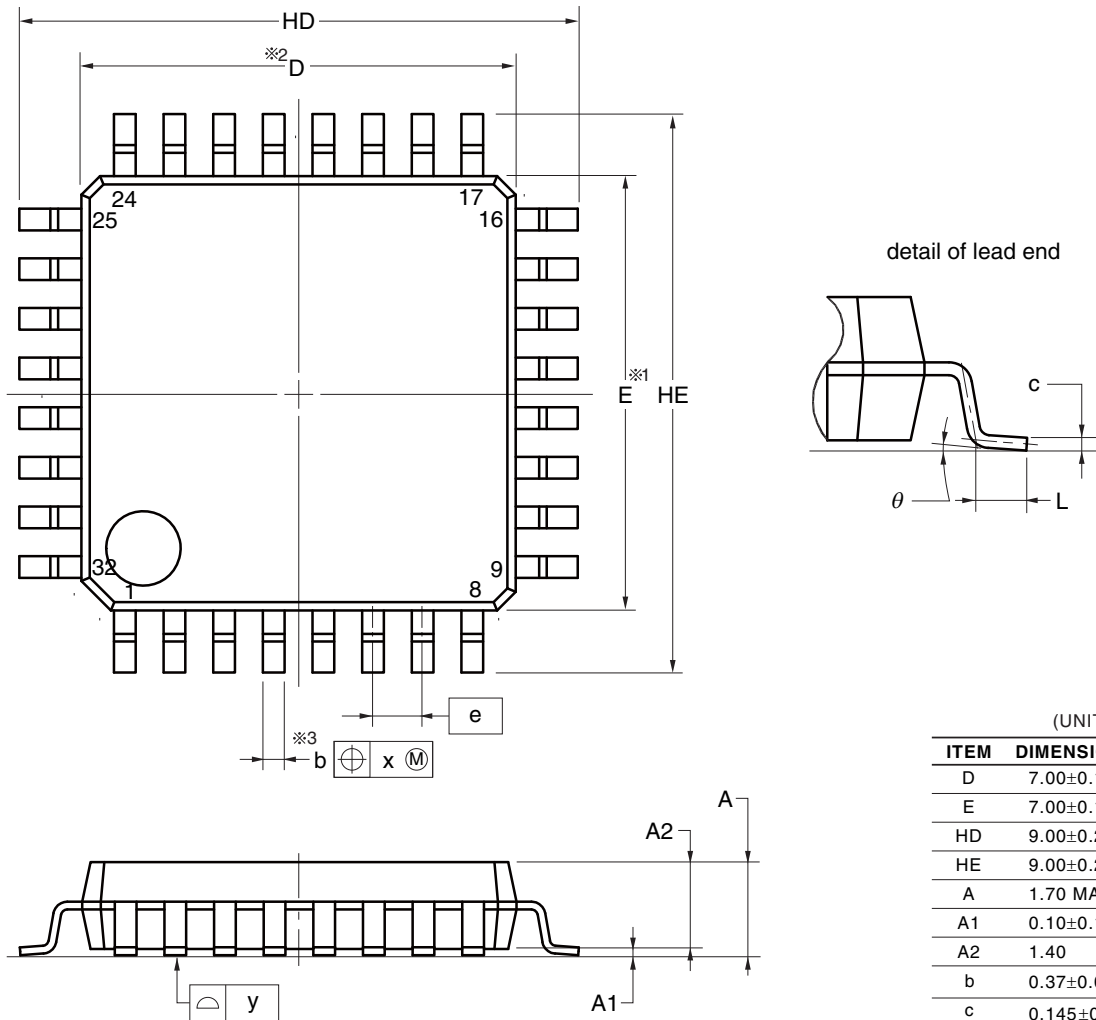
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4.5 32-pin Products

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
$\theta$	0° to 8°
e	0.80
x	0.20
y	0.10

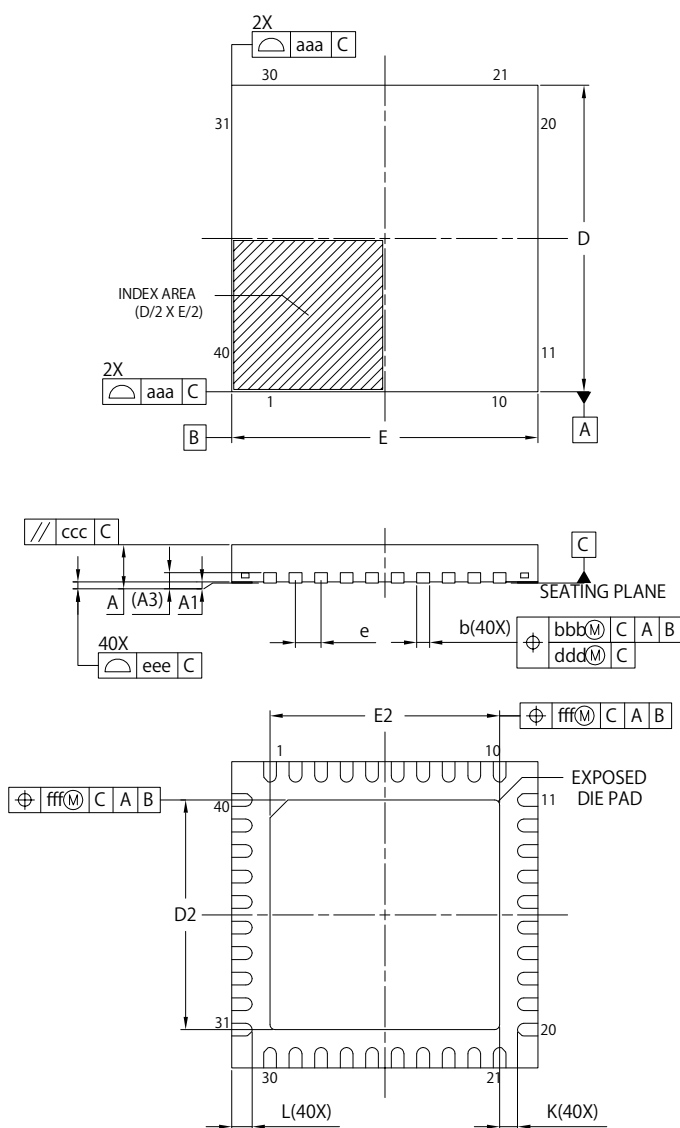
**NOTE**

1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include trim offset.

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4.6 40-pin Products

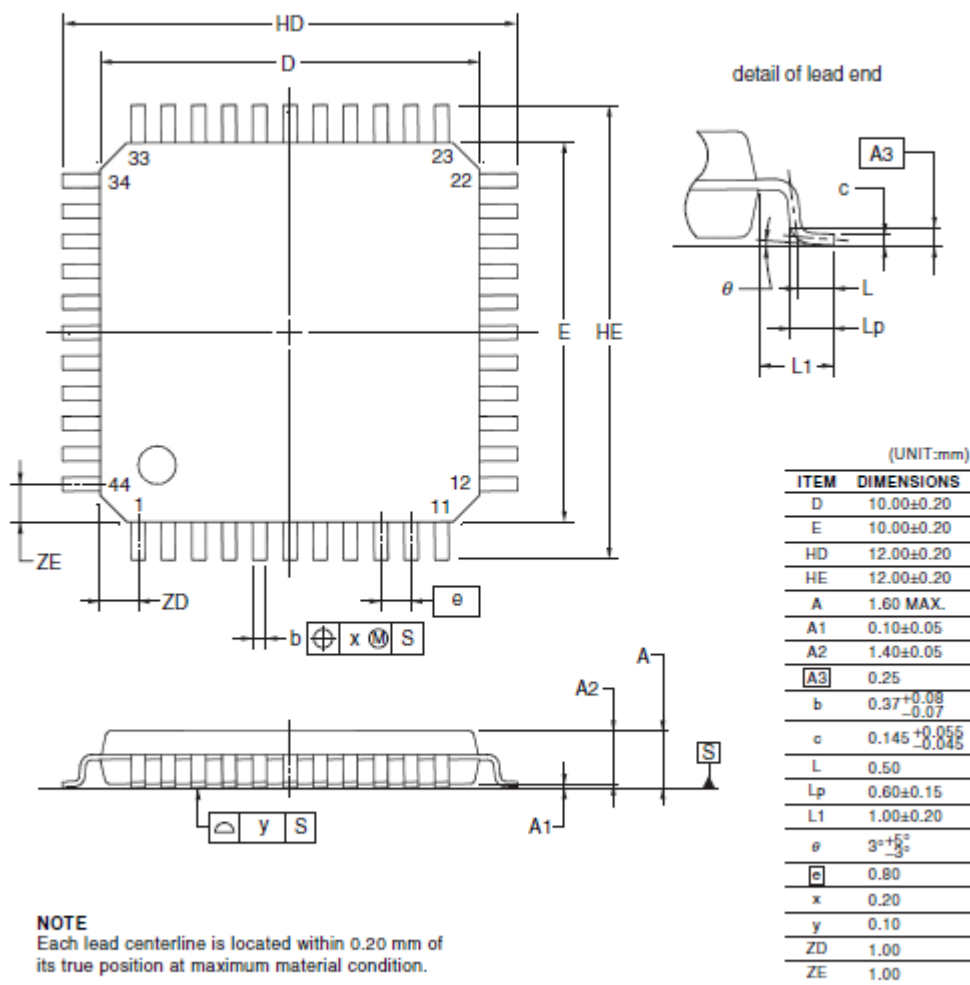
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN040-6x6-0.50	PWQN0040KD-A	0.08



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A <sub>1</sub>	0.00	0.02	0.05
A <sub>3</sub>	0.203 REF.		
b	0.18	0.25	0.30
D	6.00 BSC		
E	6.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
D <sub>2</sub>	4.45	4.50	4.55
E <sub>2</sub>	4.45	4.50	4.55
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

4.7 44-pin Products

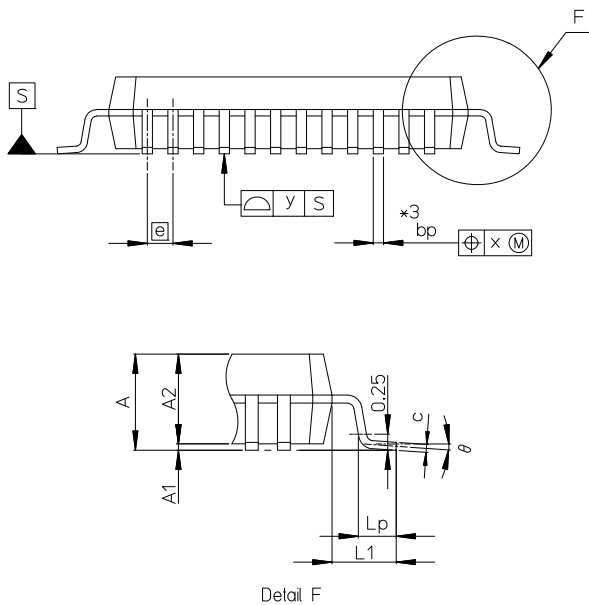
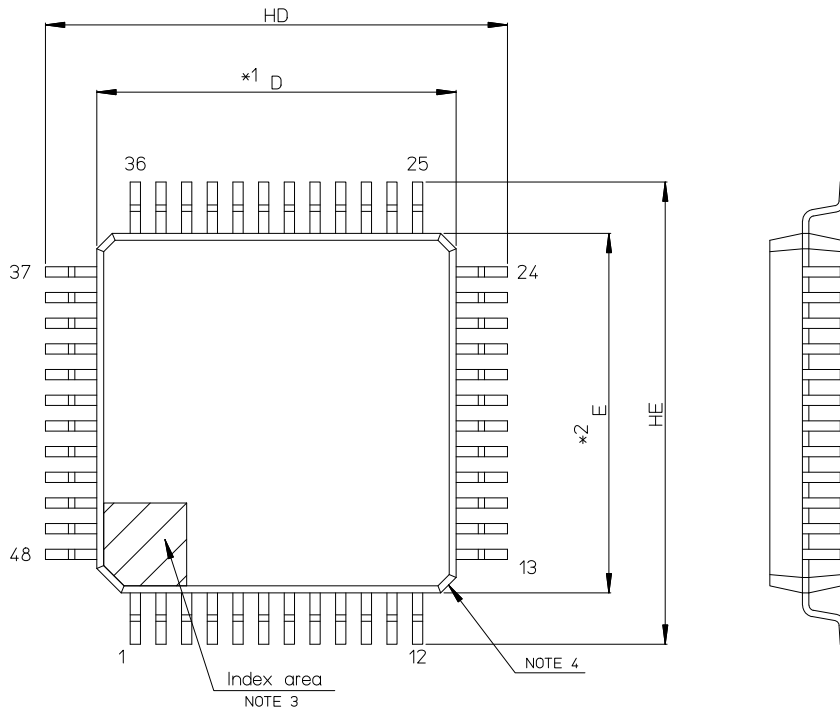
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



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4.8 48-pin Products

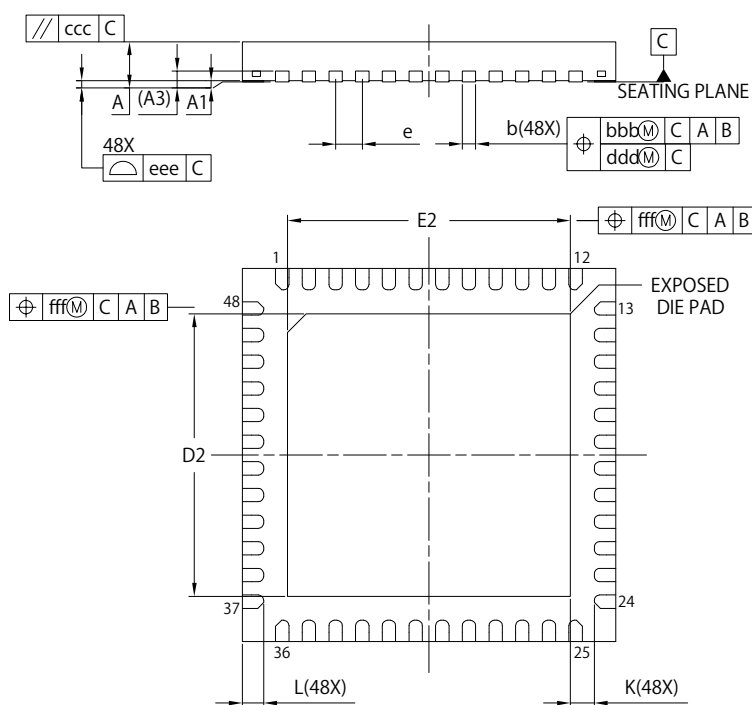
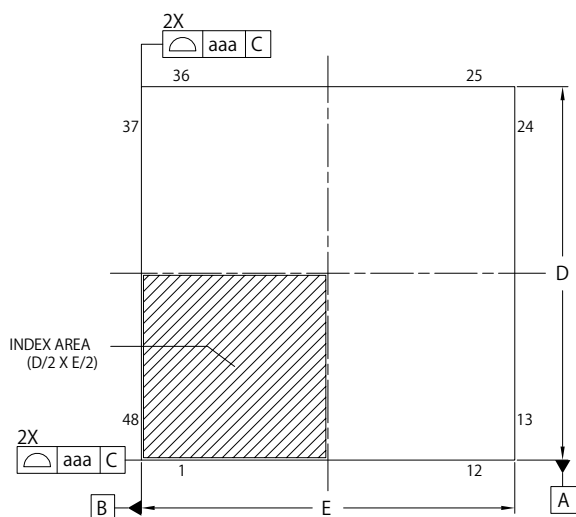
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2g



- NOTE)
1. DIMENSIONS \*1\* AND \*2\* DO NOT INCLUDE MOLD FLASH.
  2. DIMENSION \*3\* DOES NOT INCLUDE TRIM OFFSET.
  3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
  4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	—	1.4	—
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	—	—	1.7
A1	0.05	—	0.15
bp	0.17	0.20	0.27
c	0.09	—	0.20
$\theta$	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Lp	0.45	0.6	0.75
L1	—	1.0	—

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g

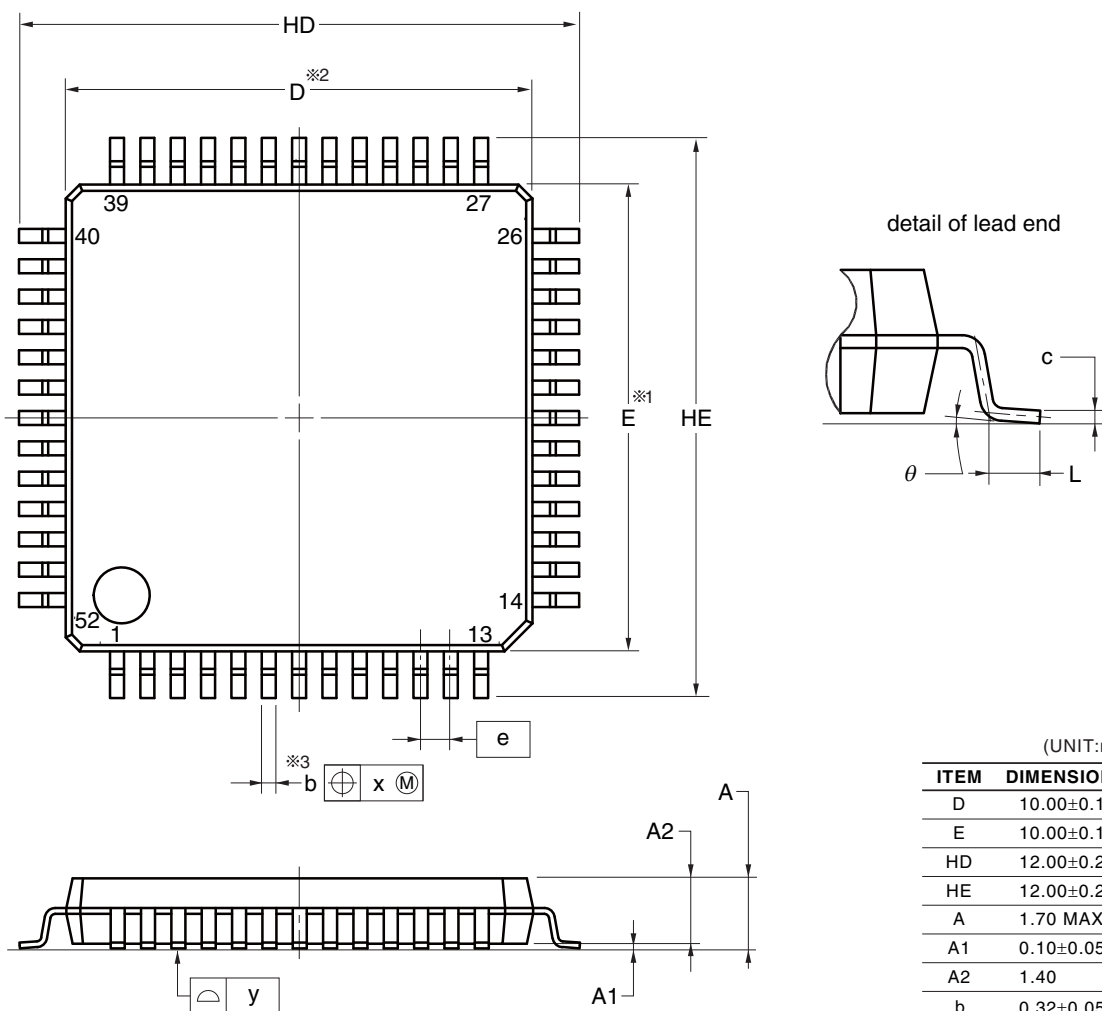


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A <sub>1</sub>	0.00	0.02	0.05
A <sub>3</sub>	0.203 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
D <sub>2</sub>	5.25	5.30	5.35
E <sub>2</sub>	5.25	5.30	5.35
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		



4.9 52-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
HD	12.00±0.20
HE	12.00±0.20
A	1.70 MAX.
A1	0.10±0.05
A2	1.40
b	0.32±0.05
c	0.145±0.055
L	0.50±0.15
$\theta$	0° to 8°
e	0.65
x	0.13
y	0.10

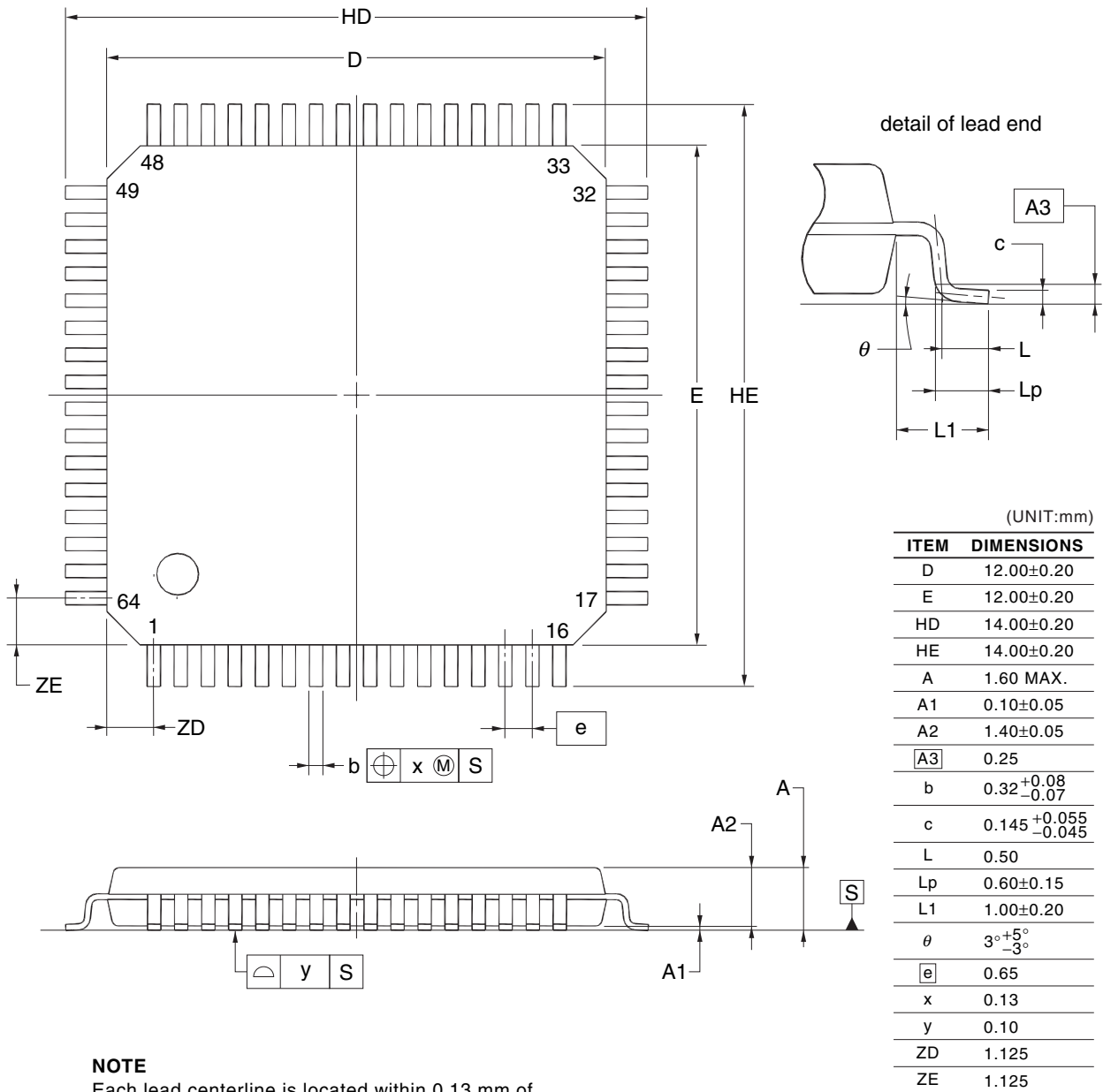
**NOTE**

1. Dimensions “※1” and “※2” do not include mold flash.
2. Dimension “※3” does not include trim offset.

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4.10 64-pin Products

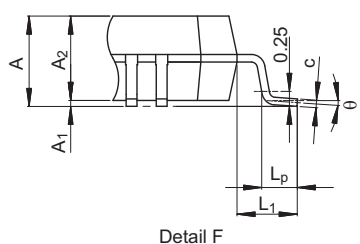
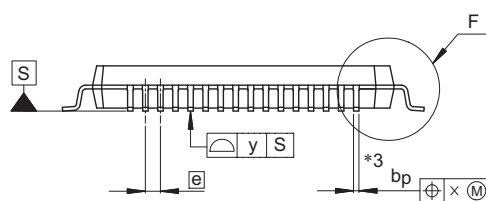
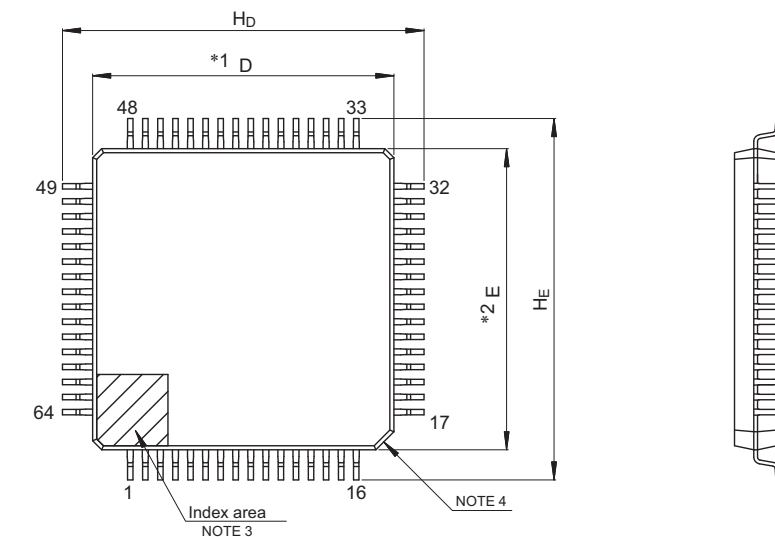
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51



**NOTE**  
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

<b>JEITA Package Code</b>	<b>RENESAS Code</b>	<b>Previous Code</b>	<b>MASS (Typ) [g]</b>
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm



NOTE)

1. DIMENSIONS "\*\*1" AND "\*\*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "\*\*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A <sub>2</sub>	—	1.4	—
H <sub>D</sub>	11.8	12.0	12.2
H <sub>E</sub>	11.8	12.0	12.2
A	—	—	1.7
A <sub>1</sub>	0.05	—	0.15
b <sub>p</sub>	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L <sub>p</sub>	0.45	0.6	0.75
L <sub>1</sub>	—	1.0	—

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REVISION HISTORY	RL78/G24 Datasheet
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Rev.	Date	Description	
		Page	Summary
1.00	May 10, 2023	—	First edition issued
1.10	Nov 1, 2023	p.5	Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G24 was modified.
		p.6	Table 1 - 1 List of Ordering Part Numbers was modified.
		p.65	2.3.2 Supply current characteristics was modified.
		p.108	2.6.1 A/D converter characteristics: 1. Normal modes 1 and 2 was modified.
		p.143	3.3.2 Supply current characteristics was modified.

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# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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