RX671 Group
Renesas MCUs

R01DS0373EJ0120
Rev.1.20
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120-MHz 32-bit RX MCU, on-chip double-precision FPU, 707 CoreMark,
up to 2-MB flash memory (supporting the dual bank function), 384-KB SRAM,
various communications interfaces, including SD host interface, Quad SPI, and CAN, Capacitive touch sensing unit,
12-bit A/D converter, RTC, Encryption function, Serial sound interface, Remote control signal receiver

Features

■ 32-bit RXv3 CPU core
- Maximum operating frequency: 120 MHz
  Capable of 707 CoreMark in operation at 120 MHz
- Double-precision 64-bit IEEE-754 floating point
- A collective register bank save function is available.
- Supports the memory protection unit (MPU)
- JTAG and FINE (one-line) debugging interfaces

■ Low-power design and architecture
- Operation from a single 2.7- to 3.6-V supply
- Battery supply of backup power allows continued operations of the RTC and the backup registers.
- Four low-power modes

■ On-chip code flash memory
- Supports versions with up to 2 Mbytes of ROM
- No wait cycles at up to 60 MHz or when the ROM cache is hit, one-wait state at up to 120 MHz
- User code is programmable by on-board or off-board programming.
- Programming/erasing as background operations (BGOs)
- A dual-bank structure allows exchanging the start-up bank.

■ On-chip data flash memory
- 8 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM
- 384 Kbytes of SRAM (no wait states)
- 4 Kbytes of standby RAM (backup on deep software standby)

■ External address space
- Buses for full-speed data transfer (maximum operating frequency of 60 MHz)
- 8 CS areas
- 8- or 16-bit bus space is selectable per area
- Independent SDRAM area (128 Mbytes)

■ Data transfer
- DMACAb: 8 channels
- DTCb: 1 channel
- EXDMACa: 2 channels

■ Reset and supply management
- Power-on reset (POR)
- Low voltage detection (LVD) with voltage settings
- Backup domain low power detection

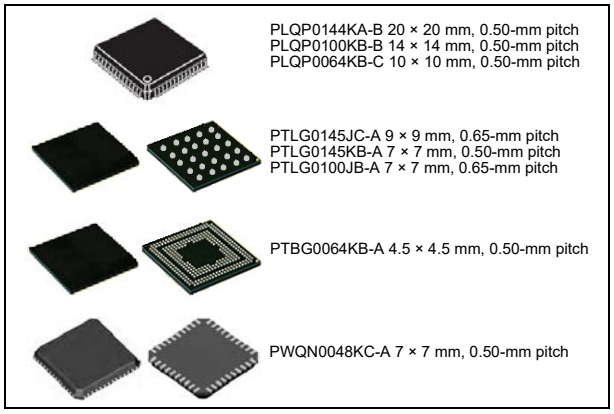
■ Clock functions
- External crystal resonator or internal PLL for operation at 8 to 24 MHz
- A sub-clock oscillator connectable to a 32.768-kHz crystal resonator
- Internal 240-kHz LOCO and HOCO selectable from 16, 18, and 20 MHz
- 120-kHz clock for the IWDTa

■ Real-time clock
- Adjustment functions (30 seconds, leap year, and error)
- Real-time clock counting and binary counting modes are selectable
- Time capture in response to an event-signal input

■ Independent watchdog timer
- Operates with the 120-kHz clock frequency generated by the dedicated low-speed oscillator

■ Useful functions for IEC60730 compliance
- Oscillation-stoppage detection, frequency measurement, CRCA, IWDTa, self-diagnostic function for the A/D converter, etc.
- Register write protection function that protects important registers against overwriting

■ Remote control signal receiver



■ Various communications interfaces
- PHY layer (up to 2 channels) for host/function or OTG controller (1 channel) with full-speed USB 2.0 transfer
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (up to 2 channels)
- SCIk and SCIh with multiple functionalities (up to 13 channels)
  Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I^2C, and extended serial mode.
- SCIm with 16-byte transmission and reception FIFOs (up to 2 channels)
- Up to two RSCIs with Manchester encoding and HBS functionality
- The I^2C bus interfaces RIIC and RIICHS for transfer at up to 3.4 Mbps (up to 3 channels), and the RIICHS also supports high-speed mode.
- Single I/O RSPId (3 channels), single I/O RSPIA (1 channel), and quad QSPIX (1 channel). The QSPIX supports fetching from serial flash memory.
- SD host interface (1 channel) with a 1- or 4-bit SD bus for use with SD memory or SDIO
- Serial sound interface supporting various audio data formats, including I^2S

■ Up to 25 extended-function timers
- 16-bit TPUa, MTU3a
- 8-bit TMRb (4 channels), 16-bit CMT (4 channels), 32-bit CMTW (2 channels)

■ 12-bit A/D converter
- Two 12-bit units (8 channels for unit 0; 12 channels for unit 1)
- Self diagnosis, detection of analog input disconnection

■ Temperature sensor for measuring temperature within the chip

■ Capacitive touch sensing unit
- Self-capacitance method: A single pin configures a single key, supporting up to 17 keys
- Mutual capacitance method: Matrix configuration with 17 pins, supporting up to 64 keys

■ Encryption function
- Trusted Secure IP (TSIP)
  AES128/192/256, TDES, ARC4, RSA, ECC,
  True-random number generator (TRNG), SHA1, SHA224, SHA256, MD5, GHASH, Prevention of the illicit copying of keys

■ Up to 114 pins for general I/O ports
- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Operating temp. range
- D-version: –40°C to +85°C
- G-version: –40°C to +105°C

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 give a comparison of the functions of products in different packages.
Table 1.1 is an outline of maximum specifications, and the peripheral modules and the number of channels of the modules differ depending on the number of pins on the package. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/10)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per state (cycle of the system clock) • Address space: 4-Gbyte linear • Register set of the CPU General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers • 113 instructions Instructions installed as standard: 111 Basic instructions: 77 Single-precision floating-point operation instructions: 11 DSP instructions: 23 Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
	FPU	• Single precision (32-bit) floating point • Data types and floating-point exceptions in conformance with the IEEE754 standard
	Double-precision floating point coprocessor	• Double-precision floating-point register set Double-precision floating-point data registers: 16, each with 64-bit width Double-precision floating-point control registers: Four, each with 32-bit width • Double-precision floating-point processing instructions: 21 • Notifying the interrupt controller of double-precision floating-point exceptions
	Register bank save function	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks
Memory	Code flash memory	• Capacity: 1 Mbyte/1.5 Mbytes/2 Mbytes • ROM cache: 8 Kbytes • 60 MHz ≤ No-wait cycle access 120 MHz ≤ 1-wait cycle access • Instructions hitting the ROM cache or operand = 120 MHz: No-wait access • On-board programming: Four types • Off-board programming (parallel programmer mode) • Instructions are executable only for the program stored in the TM target area by using the Trusted Memory (TM) function and protection against data reading is realized. • A dual-bank structure allows programming during reading or exchanging the start-up areas
	Data flash memory	• Capacity: 8 Kbytes • Programming/erasing: 100,000 times
	Unique ID	• 16-byte unique ID for the device
	RAM	• Capacity: 384 Kbytes • 120 MHz, no-wait access
	Standby RAM	• Capacity: 4 Kbytes • Operation synchronized with PCLKB: Up to 60 MHz, two-cycle access

Table 1.1 Outline of Specifications (2/10)

Classification	Module/Function	Description
Operating modes		• Operating modes by the mode-setting pins at the time of release from the reset state Single-chip mode Boot mode (for the SCI interface) Boot mode (for the USB interface) Boot mode (for the FINE interface) • Selection of operating mode by register setting Single-chip mode On-chip ROM disabled extended mode On-chip ROM enabled extended mode • Endian selectable
Clock	Clock generation circuit	• Main clock oscillator, sub clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • The peripheral module clocks can be set to frequencies above that of the system clock. • Main-clock oscillation stoppage detection • Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 120 MHz QSPIX runs in synchronization with ICLK at Up to 120 MHz. Peripheral modules of MTU, RSPI, SCIm, RSPIA, RSCI, and RIICHS run in synchronization with PCLKA, which operates at up to 120 MHz. Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz ADCLK in the S12AD (unit 0) runs in synchronization with PCLKC: Up to 60 MHz ADCLK in the S12AD (unit 1) runs in synchronization with PCLKD: Up to 60 MHz Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 60 MHz • Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit • External clock input frequency: 30 MHz (max) • Clock output function
Reset		Nine types of reset • RES# pin reset: Generated when the RES# pin is driven low. • Power-on reset: Generated when the RES# pin is driven high and VCC = AVCC0 = AVCC1 rises. • Voltage-monitoring 0 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 1 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Voltage-monitoring 2 reset: Generated when VCC = AVCC0 = AVCC1 falls. • Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby. • Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. • Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. • Software reset: Generated by register setting.
Power-on reset		If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC = AVCC0 = AVCC1 has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.
Voltage detection circuit (LVDA)		Monitors the voltage being input to the VCC = AVCC0 = AVCC1 pins and generates an internal reset or interrupt. • Voltage detection circuit 0 Capable of generating an internal reset The option-setting memory can be used to select enabling or disabling of the reset. Voltage detection level: Selectable from three different levels (2.94 V, 2.87 V, 2.80 V) • Voltage detection circuits 1 and 2 Voltage detection level: Selectable from three different levels (2.99 V, 2.92 V, 2.85 V) Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) Capable of generating an internal reset • Two types of timing are selectable for release from reset An internal interrupt can be requested. • Detection of voltage rising above and falling below thresholds is selectable. • Maskable or non-maskable interrupt is selectable Voltage detection monitoring Event linking

Table 1.1 Outline of Specifications (3/10)

Classification	Module/Function	Description
Low power consumption	Low power consumption function	• Module stop function • Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode
	Battery backup function	• When the voltage on the VCC pin drops, power can be supplied to the backup power area from the VBATT pin. • Backup power area: Sub-clock oscillator Realtime clock Backup register Tamper detection • Detection of low voltage in the backup power area
Interrupt	Interrupt controller (ICUE)	• Peripheral function interrupts: 256 sources • External interrupts: 16 (pins IRQ0 to IRQ15) • Software interrupts: 2 sources • Non-maskable interrupts: 8 sources • Sixteen levels specifiable for the order of priority • Method of interrupt source selection: The interrupt vectors consist of 256 vectors (128 sources are fixed. The remaining 133 vectors are selected from among the other 128 sources.)
External bus extension		• The external address space can be divided into eight areas (CS0 to CS7), each with independent control of access settings. Capacity of each area: 16 Mbytes (CS0 to CS7) A chip-select signal (CS0# to CS7#) can be output for each area. Each area is specifiable as an 8-, or 16-bit bus space. The data arrangement in each area is selectable as little or big endian (only for data). • SDRAM interface connectable • Bus format: Separate bus, multiplex bus • Wait control • Write buffer facility
DMA	DMA controller (DMACAb)	• 8 channels • Three transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Software trigger, external interrupts, and interrupt requests from peripheral functions • Transfer space: 4 Gbytes (0000 0000h to FFFF FFFFh excluding reserved areas)
	EXDMA controller (EXDMACa)	• 2 channels Four transfer modes: Normal transfer, repeat transfer, block transfer, and cluster transfer • Single-address transfer enabled with the EDACKn signal • Request sources: Software trigger, external DMA requests (EDREQn), and interrupt requests from peripheral functions
	Data transfer controller (DTCb)	• Three transfer modes: Normal transfer, repeat transfer, and block transfer • Request sources: External interrupts and interrupt requests from peripheral functions • Sequence transfer

Table 1.1 Outline of Specifications (4/10)

Classification	Module/Function	Description
I/O ports	Programmable I/O ports	• I/O ports for the 145-pin TFLGA (0.65-mm pitch) I/O pins: 111 Input pin: 1 Pull-up resistors: 111 Open-drain outputs: 111 5-V tolerance: 20 • I/O ports for the 145-pin TFLGA (0.50-mm pitch) and 144-pin LFQFP I/O pins: 113 Input pin: 1 Pull-up resistors: 113 Open-drain outputs: 113 5-V tolerance: 20 • I/O ports for the 100-pin TFLGA and 100-pin LFQFP I/O pins: 80 Input pin: 1 Pull-up resistors: 80 Open-drain outputs: 80 5-V tolerance: 18 • I/O ports for the 64-pin TFBGA I/O pins: 43 Input pin: 1 Pull-up resistors: 43 Open-drain outputs: 43 5-V tolerance: 8 • I/O ports for the 64-pin LFQFP I/O pins: 44 Input pin: 1 Pull-up resistors: 44 Open-drain outputs: 44 5-V tolerance: 8 • I/O ports for the 48-pin HWQFN I/O pins: 33 Input pin: 1 Pull-up resistors: 33 Open-drain outputs: 33 5-V tolerance: 6
Event link controller (ELC)		• Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions. • 99 internal event signals can be freely combined for interlinked operation with connected functions. • Event signals from peripheral modules can be used to change the states of output pins (of ports B and E). • Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules.
Timers	16-bit timer pulse unit (TPUa)	• (16 bits × 6 channels) × 1 unit • Maximum of 16 pulse-input/output possible • Select from among seven or eight counter-input clock signals for each channel • Input capture/output compare function • Output of PWM waveforms in up to 15 phases in PWM mode • Support for buffered operation, phase-counting mode (two phase encoder input) and cascade-connected operation (32 bits × 2 channels) depending on the channel. • PPG output trigger can be generated • Capable of generating conversion start triggers for the A/D converters • Digital filtering of signals from the input capture pins • Event linking by the ELC
	8-bit timers (TMRb)	• (8 bits × 2 channels) × 2 units • Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal • Capable of output of pulse trains with desired duty cycles or of PWM signals • The 2 channels of each unit can be cascaded to create a 16-bit timer • Generation of triggers for A/D converter conversion • Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 • Capable of generating operating clock for the remote control signal receiver (REMC) • Event linking by the ELC

Table 1.1 Outline of Specifications (5/10)

Classification	Module/Function	Description
Timers	Compare match timer (CMT)	• (16 bits × 2 channels) × 2 units • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Event linking by the ELC
	Compare match timer W (CMTW)	• (32 bits × 1 channel) × 2 units • Compare-match, input-capture input, and output-comparison output are available. • Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) • Interrupt requests can be output in response to compare-match, input-capture, and output-comparison events. • Event linking by the ELC
	Watchdog timer (WDTA)	• 14 bits × 1 channel • Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Counter-input clock: IWDT-dedicated on-chip oscillator • Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 • Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). • Event linking by the ELC
	Multifunction timer pulse unit (MTU3a)	• 9 channels (16 bits × 8 channels, 32 bits × 1 channel) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 14 counter-input clock signals for each channel (PCLKA/1, PCLKA/2, PCLKA/4, PCLKA/8, PCLKA/16, PCLK/A32, PCLKA/64, PCLKA/256, PCLKA/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) 14 of the signals are available for channel 0, 11 are available for channels 1, 3, 4, 6 to 8, 12 are available for channel 2, and 10 are available for channel 5. • Input capture function • 39 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • 43 interrupt sources • Automatic transfer of register data • Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffer configuration • Reset synchronous PWM mode Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion • A/D converter start triggers can be skipped • Digital filter function for signals on the input capture and external counter clock pins • PPG output trigger can be generated • Event linking by the ELC
	Port output enable 3 (POE3a)	• Control of the high-impedance state of the MTU waveform output pins • 5 pins for input from signal sources: POE0#, POE4#, POE8#, POE10#, POE11# • Initiation on detection of short-circuited outputs (detection of simultaneous PWM output to the active level) • Initiation by oscillation-stoppage detection or software • Additional programming of output control target pins is enabled

Table 1.1 Outline of Specifications (6/10)

Classification	Module/Function	Description
Timers	Programmable pulse generator (PPG)	• (4 bits × 4 groups) × 2 units • Pulse output with the MTU or TPU output as a trigger • Maximum of 32 pulse-output possible
	Realtime clock (RTCd)*1	• Clock sources: Main clock, sub clock • Selection of the 32-bit binary count in time count/second unit possible • Clock and calendar functions • Interrupt sources: Alarm interrupt, periodic interrupt, and carry interrupt • Battery backup operation • Time capture function (up to 3 pins) • Event linking by the ELC
Communication function	USB 2.0 FS host/ function module (USBb)	• Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS • Up to two ports • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Both self-powered mode and bus-powered mode are supported • OTG (On the Go) operation is possible (low-speed is not supported) • Incorporates 2 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required
	Serial communications interfaces (SCIk, SCIm, SCIh)	• 13 channels (SCIk: 10 channels + SCIh: 1 channel + SCIm: 2 channels) • SCIk, SCIh, SCIm Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 9-bit transfer mode Bit rate modulation Double-speed mode • SCIk, SCIh Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Event linking by the ELC (only on channel 5) • SCIh Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format • SCIm Data can be transmitted or received in sequence by the 16-byte FIFO buffers of the transmission and reception unit • SCIk, SCIm Data match detection Adjustment of the timing of sampling of the RXD signals

Table 1.1 Outline of Specifications (7/10)

Classification	Module/Function	Description
Communication function	Serial communications interfaces (RSCI)	• 2 channels (RSCI10, RSCI11) • Serial communications modes: Asynchronous, clock synchronous, and smart-card interface • Multi-processor function • On-chip baud rate generator allows selection of the desired bit rate • Choice of LSB-first or MSB-first transfer • Start-bit detection: Level or edge detection is selectable. • Simple I^2C • Simple SPI • 9-bit transfer mode • Bit rate modulation • Double-speed mode • Event linking by the ELC (only RSCI10) • Supports the serial communications protocol, which contains the start frame and information frame • Supports the LIN format • Data can be transmitted or received in sequence by the 32-byte FIFO buffers of the transmission and reception unit • Manchester encoding is supported. • HBS (home bus system) support mode • Data match detection • Adjustment of the timing of sampling of the RXD signals
	I^2C bus interface (RIICa)	• 3 channels (only channel 0 can be used in fast-mode plus) Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 1 Mbps (channel 0) • Event linking by the ELC
	High-speed I^2C bus interface (RIICHS)	• 1 channel Communication formats I^2C bus format/SMBus format Supports the multi-master Max. transfer rate: 3.4 Mbps • Event linking by the ELC
	CAN module (CAN)	• 2 channels • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes per channel
	Serial peripheral interface (RSPId)	• 3 channels • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Transmit/receive data can be swapped in byte units • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC

Table 1.1 Outline of Specifications (8/10)

Classification	Module/Function	Description
Communication function	Serial peripheral interface (RSPIA)	• 1 channel • RSPI transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, or to 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) Transit/receive data can be swapped in byte units • Buffered structure The transmission and reception sections have 4-stage and 32-bit-wide FIFO buffers for the sequential transmission and reception of data. • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC • Communications protocol: RSPIA supports the Texas Instruments Synchronous Serial Protocol (TI SSP).
	Quad-SPI memory interface (QSPIX)	• 1 channel • This interface can handle fetching from serial flash memory that has an SPI-compatible interface. • It supports extended SPI, dual-SPI, and quad-SPI protocols. • Address width is selectable from among 8, 16, 24, and 32 bits.
	Remote control signal receiver (REMCa)	• 1 channel • Four pattern matching (header, data 0, data 1, and special data detection) • 8-byte receive buffer per unit • The operating clock can be selected from among the PCLK, sub-clock, and TMR.
Serial sound interface (SSIE)		• 1 channel • Full-duplex transmission • Various types of serial audio formatting are supported. • Master and slave operations are supported. • The bit-clock frequency is selectable from among 13 frequencies (1/1, 1/2, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64, 1/96, or 1/128). • Data formats with 8, 16, 18, 20, 22, 24, and 32 bits are supported. • 32-stage FIFO buffers for transmission and reception • Stopping or not stopping the SSILRCK signal on stopping of data transmission is selectable.
SD host interface (SDHI)		• 1 channel • Transfer speed: Supports high-speed mode (25 MB/s) and default speed mode (12.5 MB/s) • One interface for SD memory and I/O cards (supporting 1- and 4-bit SD buses) • SD specifications Part 1: Physical Layer Specification Ver. 3.01 compliant (DDR not supported) Part E1: SDIO Specification Ver. 3.00 • Error checking: CRC7 for commands and CRC16 for data • Interrupt requests: Card access interrupt, SDIO access interrupt, card detection interrupt, SD buffer access interrupt • DMA transfer requests: SD_BUF write and SD_BUF read • Support for card detection and write protection

Table 1.1 Outline of Specifications (9/10)

Classification	Module/Function	Description
12-bit A/D converter (S12ADFa)		• 12 bits × 2 units (unit 0: 8 channels; unit 1: 12 channels) • 12-bit resolution (switchable between 8, 10, and 12 bits) • Conversion time 0.48 µs per channel (for 12-bit conversion) 0.45 µs per channel (for 10-bit conversion) 0.42 µs per channel (for 8-bit conversion) • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group priority control (only for 3 group scan mode) • Sample-and-hold function Common sample-and-hold circuit included • Sampling variable Sampling time can be set up for each channel. • Digital comparison Method: Comparison to detect voltages above or below thresholds and window comparison Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion • Self-diagnostic function The self-diagnostic function internally generates three analog input voltages (unit 0: VREFL0, VREFH0 × 1/2, VREFH0; unit 1: AVSS1, AVCC1 × 1/2, AVCC1) • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Three ways to start A/D conversion Software trigger, timer (MTU, TMR, TPU) trigger, external trigger • Event linking by the ELC
Temperature sensor		• 1 channel • Relative precision: ± 1°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 1).
Capacitive touch sensing unit (CTSUa)		• Detection pin: 17 channels
Safety	Memory protection unit (MPU)	• Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An access exception occurs when the detected access is not in the permitted area.
	Trusted Memory (TM) Function	• Programs in the TM target area in the code flash memory are protected against reading • Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled.
	Register write protection function	• Protects important registers from being overwritten for in case a program runs out of control.
	CRC calculator (CRCA)	• Generation of CRC codes for 8-/32-bit data 8-bit data Selectable from the following three polynomials $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ 32-bit data Selectable from the following two polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable
	Main clock oscillation stop detection	• Main clock oscillation stop detection: Available
	Clock frequency accuracy measurement circuit (CAC)	• Monitors the clock output from the main clock oscillator, sub-clock oscillator, low- and high-speed on-chip oscillators, IWDT-dedicated on-chip oscillator, and PCLKB, and generates interrupts when the setting range is exceeded.
	Data operation circuit (DOCA)	• This handles the comparison, addition, subtraction, comparison in terms of which is larger or smaller, or window comparison of 32-bit values.

Table 1.1 Outline of Specifications (10/10)

Classification	Module/Function	Description
Encryption function	Trusted Secure IP (TSIP)*2	• Access management circuit • Encryption engine Common key encryption: AES (compliant with NIST FIPS PUB 197), TDES, ARC4 Public key encryption: RSA, ECC Hash functions: SHA1, SHA224, SHA256, MD5, GHASH • Other features TRNG (true-random number generator) Prevention from illicit copying of a key
Operating frequency		Up to 120 MHz
Power supply voltage		VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0 ≤ AVCC0, V_{BATT} = 1.62*3 to 3.6 V
Operating temperature		D-version: –40 to +85°C G-version: –40 to +105°C
Package		145-pin TFLGA (PTLG0145JC-A) 145-pin TFLGA (PTLG0145KB-A) 144-pin LFQFP (PLQP0144KA-B) 100-pin TFLGA (PTLG0100JB-A) 100-pin LFQFP (PLQP0100KB-B) 64-pin TFBGA (PTBG0064KB-A) 64-pin LFQFP (PLQP0064KB-C) 48-pin HWQFN (PWQN0048KC-A)
Debugging interface		JTAG and FINE interfaces

Note 1. When the realtime clock is not used, initialize the registers in the time clock according to description in section 31.6.8, Initialization Procedure When the Realtime Clock is Not to be Used in the User's Manual: Hardware.
Note 2. The product part number differs according to whether or not the MCU includes the encryption function.
Note 3. The low CL crystal unit cannot be used when the V_{BATT} voltage is less than 2.0 V.

Table 1.2 Comparison of Functions for Different Packages (1/2)

Functions	Products	RX671				
	Package	145-pin TFLGA (0.65-mm pitch)	145-pin TFLGA (0.50-mm pitch) 144-pin LFQFP	100-pin TFLGA 100-pin LFQFP	64-pin TFBGA 64-pin LFQFP	48-pin HWQFN
Code Flash Memory	Code Flash Memory Capacity	1 Mbyte/1.5 Mbytes/2 Mbytes				
	Dual bank function	Available				
	BGO function	Available				
Data Flash Memory		8 Kbytes				
RAM		384 Kbytes				
Standby RAM		4 Kbytes				
External bus	External bus width	16/8 bits			Not available	
	SDRAM area controller	Available		Not available		
DMA	DMA controller	Ch. 0 to 7				
	Data transfer controller	Available				
	EXDMA controller	Ch. 0 and 1			Not available	
Timers	16-bit timer pulse unit	Ch. 0 to 5				
	Multi-function timer pulse unit 3	Ch. 0 to 8				
	Port output enable 3	Available				
	Programmable pulse generator	Ch. 0 and 1			Not available	
	8-bit timers	Ch. 0 to 3				
	Compare match timer	Ch. 0 to 3				
	Compare match timer W	Ch. 0 and 1				
	Realtime clock	Available				Not available
	Watchdog timer	Available				
	Independent watchdog timer	Available				
Communication function	USB 2.0 FS host/function module	Ch. 0 and 1	Ch. 0		Ch. 0*1	Not available
	Serial communications interfaces (SCIk)	Ch. 0 to 9		Ch. 0 to 3, 5, 6, 8 and 9	Ch. 1 to 3, 5, 8 and 9	
	Serial communications interfaces (SCIm)	Ch. 10 and 11				
	Serial communications interfaces (SCIh)	Ch. 12				
	Serial communications interfaces (RSCI)	Ch. 10 and 11				
	I²C bus interfaces (RIIC)	Ch. 0 to 2				Ch. 0 and 2
	Hi-speed I²C bus interfaces (RIICHS)	Ch. 0				
	Serial peripheral interface (RSPI)	Ch. 0 to 2			Ch. 0 and 1	
	Serial peripheral interface (RSPIA)	Ch. 0				
	CAN module	Ch. 0 and 1			Not available	
	Quad-SPI memory interface (QSPIX)	Ch. 0				
	SD host interface (SDHI)	Available				
	Serial sound interface (SSIE)	Ch. 0				
	Remote control signal receiver (REMC)	Ch. 0				
Capacitive touch sensing unit (CTSU)		17 channels + 1 channel (TSCAP)			8 channels + 1 channel (TSCAP)	6 channels + 1 channel (TSCAP)
12-bit A/D converter		Unit 0: 8 channels Unit 1: 12 channels		Unit 0: 8 channels Unit 1: 8 channels	Unit 0: 4 channels Unit 1: 6 channels	Unit 0: 4 channels Unit 1: 4 channels
Temperature sensor		Available				
CRC calculator		Available				
Data operation circuit (DOC)		Available				

Table 1.2 Comparison of Functions for Different Packages (2/2)

Functions	Products	RX671				
	Package	145-pin TFLGA (0.65-mm pitch)	145-pin TFLGA (0.50-mm pitch) 144-pin LFQFP	100-pin TFLGA 100-pin LFQFP	64-pin TFBGA 64-pin LFQFP	48-pin HWQFN
Clock frequency accuracy measurement circuit (CAC)		Available				
Trusted Secure IP		Available/Not available				
Event link controller (ELC)		Available				
Battery backup function		Available				Not available
Backup register		Available				
Off-board programming (parallel programmer mode)		Available			Not available	

Note 1. Only supports the function controller.

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/3)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	Operating temperature (°C)
RX671 (D-version)	R5F5671EHDFB	PLQP0144KA-B	2 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671EDDFB	PLQP0144KA-B	2 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671CHDFB	PLQP0144KA-B	1.5 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671CDDFB	PLQP0144KA-B	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F56719HDFB	PLQP0144KA-B	1 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F56719DDFB	PLQP0144KA-B	1 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671EHDFP	PLQP0100KB-B	2 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671EDDFP	PLQP0100KB-B	2 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671CHDFP	PLQP0100KB-B	1.5 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671CDDFP	PLQP0100KB-B	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F56719HDFP	PLQP0100KB-B	1 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F56719DDFP	PLQP0100KB-B	1 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671EHDFM	PLQP0064KB-C	2 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671EDDFM	PLQP0064KB-C	2 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671CHDFM	PLQP0064KB-C	1.5 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671CDDFM	PLQP0064KB-C	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F56719HDFM	PLQP0064KB-C	1 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F56719DDFM	PLQP0064KB-C	1 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671EHDNE	PWQN0048KC-A	2 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671EDDNE	PWQN0048KC-A	2 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671CHDNE	PWQN0048KC-A	1.5 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671CDDNE	PWQN0048KC-A	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F56719HDNE	PWQN0048KC-A	1 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F56719DDNE	PWQN0048KC-A	1 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671EHDBP	PTBG0064KB-A	2 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671EDDBP	PTBG0064KB-A	2 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671CHDBP	PTBG0064KB-A	1.5 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671CDDBP	PTBG0064KB-A	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F56719HDBP	PTBG0064KB-A	1 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F56719DDBP	PTBG0064KB-A	1 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671EHDLE	PTLG0145JC-A	2 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671EDDLE	PTLG0145JC-A	2 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671CHDLE	PTLG0145JC-A	1.5 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671CDDLE	PTLG0145JC-A	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F56719HDLE	PTLG0145JC-A	1 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F56719DDLE	PTLG0145JC-A	1 M	384 K	8 K	120 MHz	Not available	–40 to +85

Table 1.3 List of Products (2/3)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	Operating temperature (°C)
RX671 (D-version)	R5F5671EHDLK	PTLG0145KB-A	2 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671EDDLK	PTLG0145KB-A	2 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671CHDLK	PTLG0145KB-A	1.5 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671CDDLK	PTLG0145KB-A	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F56719HDLK	PTLG0145KB-A	1 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F56719DDLK	PTLG0145KB-A	1 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671EHDLJ	PTLG0100JB-A	2 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671EDDLJ	PTLG0100JB-A	2 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F5671CHDLJ	PTLG0100JB-A	1.5 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F5671CDDLJ	PTLG0100JB-A	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +85
	R5F56719HDLJ	PTLG0100JB-A	1 M	384 K	8 K	120 MHz	Available	–40 to +85
	R5F56719DDLJ	PTLG0100JB-A	1 M	384 K	8 K	120 MHz	Not available	–40 to +85
RX671 (G-version)	R5F5671EHGFB	PLQP0144KA-B	2 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671EDGFB	PLQP0144KA-B	2 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671CHGFB	PLQP0144KA-B	1.5 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671CDGFB	PLQP0144KA-B	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F56719HGFB	PLQP0144KA-B	1 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F56719DGFB	PLQP0144KA-B	1 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671EHGFP	PLQP0100KB-B	2 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671EDGFP	PLQP0100KB-B	2 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671CHGFP	PLQP0100KB-B	1.5 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671CDGFP	PLQP0100KB-B	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F56719HGFP	PLQP0100KB-B	1 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F56719DGFP	PLQP0100KB-B	1 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671EHGFM	PLQP0064KB-C	2 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671EDGFM	PLQP0064KB-C	2 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671CHGFM	PLQP0064KB-C	1.5 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671CDGFM	PLQP0064KB-C	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F56719HGFM	PLQP0064KB-C	1 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F56719DGFM	PLQP0064KB-C	1 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671EHGNE	PWQN0048KC-A	2 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671EDGNE	PWQN0048KC-A	2 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671CHGNE	PWQN0048KC-A	1.5 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671CDGNE	PWQN0048KC-A	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F56719HGNE	PWQN0048KC-A	1 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F56719DGNE	PWQN0048KC-A	1 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671EHGBP	PTBG0064KB-A	2 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671EDGBP	PTBG0064KB-A	2 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671CHGBP	PTBG0064KB-A	1.5 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671CDGBP	PTBG0064KB-A	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +105

Table 1.3 List of Products (3/3)

Group	Part No.	Package	Code Flash Memory Capacity (byte(s))	RAM Capacity (byte(s))	Data Flash Memory Capacity (byte(s))	Operating Frequency (Max.)	Encryption Module	Operating temperature (°C)
RX671 (G-version)	R5F56719HGBP	PTBG0064KB-A	1 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F56719DGBP	PTBG0064KB-A	1 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671EHGLE	PTLG0145JC-A	2 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671EDGLE	PTLG0145JC-A	2 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671CHGLE	PTLG0145JC-A	1.5 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671CDGLE	PTLG0145JC-A	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F56719HGLE	PTLG0145JC-A	1 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F56719DGLE	PTLG0145JC-A	1 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671EHGLK	PTLG0145KB-A	2 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671EDGLK	PTLG0145KB-A	2 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671CHGLK	PTLG0145KB-A	1.5 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671CDGLK	PTLG0145KB-A	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F56719HGLK	PTLG0145KB-A	1 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F56719DGLK	PTLG0145KB-A	1 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671EHGLJ	PTLG0100JB-A	2 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671EDGLJ	PTLG0100JB-A	2 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F5671CHGLJ	PTLG0100JB-A	1.5 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F5671CDGLJ	PTLG0100JB-A	1.5 M	384 K	8 K	120 MHz	Not available	–40 to +105
	R5F56719HGLJ	PTLG0100JB-A	1 M	384 K	8 K	120 MHz	Available	–40 to +105
	R5F56719DGLJ	PTLG0100JB-A	1 M	384 K	8 K	120 MHz	Not available	–40 to +105

Note: Visit the Renesas Electronics Web site to check and obtain the ordering part numbers.

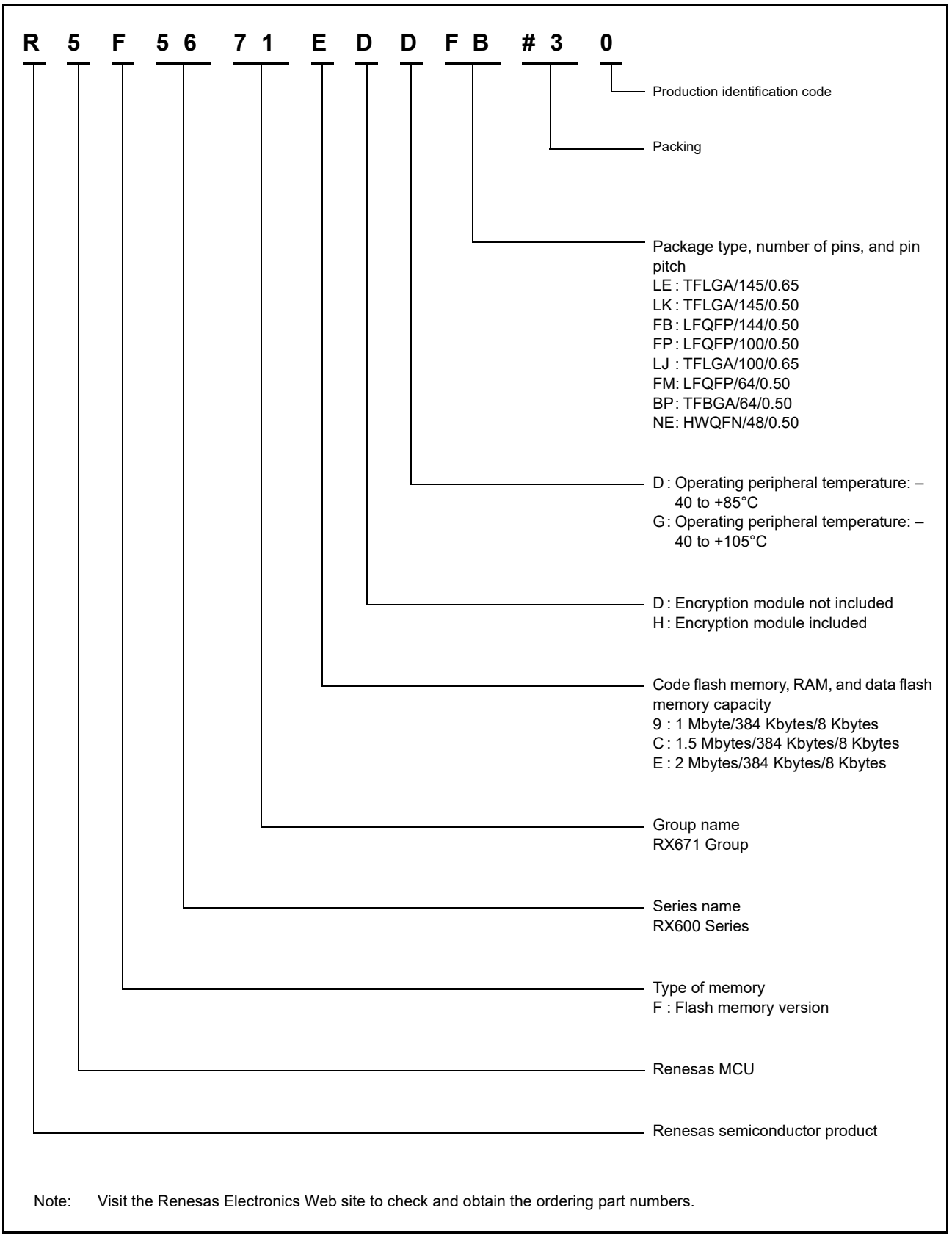
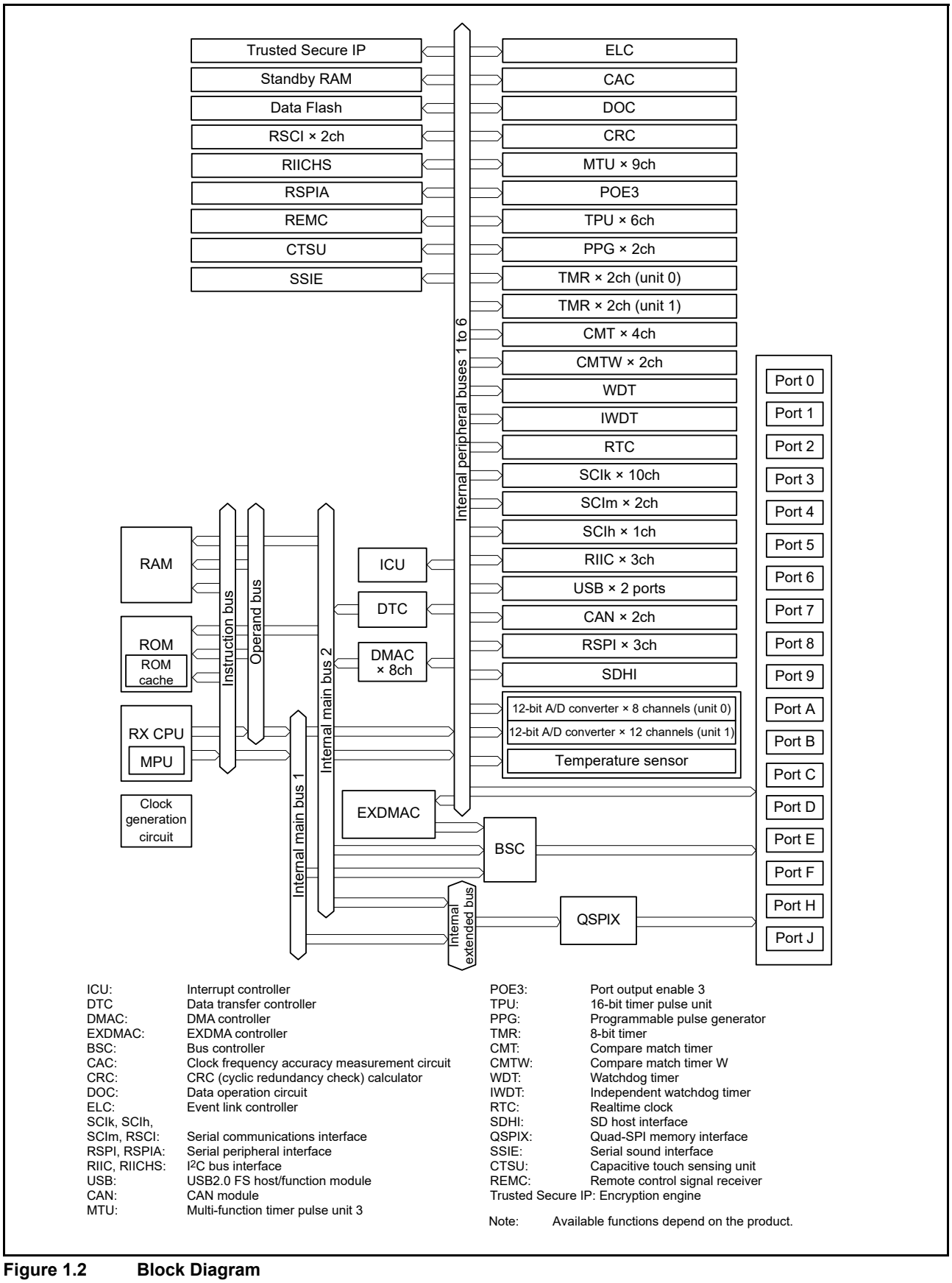


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.



ICU: Interrupt controller
DTC Data transfer controller
DMAC: DMA controller
EXDMAC: EXDMA controller
BSC: Bus controller
CAC: Clock frequency accuracy measurement circuit
CRC: CRC (cyclic redundancy check) calculator
DOC: Data operation circuit
ELC: Event link controller
SCIk, SCIh, SCIm, RSCI: Serial communications interface
RSPI, RSPIA: Serial peripheral interface
RIIC, RIICHS: I²C bus interface
USB: USB2.0 FS host/function module
CAN: CAN module
MTU: Multi-function timer pulse unit 3
POE3: Port output enable 3
TPU: 16-bit timer pulse unit
PPG: Programmable pulse generator
TMR: 8-bit timer
CMT: Compare match timer
CMTW: Compare match timer W
WDT: Watchdog timer
IWDT: Independent watchdog timer
RTC: Realtime clock
SDHI: SD host interface
QSPIX: Quad-SPI memory interface
SSIE: Serial sound interface
CTSU: Capacitive touch sensing unit
REMC: Remote control signal receiver
Trusted Secure IP: Encryption engine

Note: Available functions depend on the product.

Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/8)

Classifications	Pin Name	I/O	Description
Digital power supply	VCC	Input	Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VCL	Input	Connect this pin to VSS via a 0.22-μF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	BCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	XCOUT	Output	Input/output pins for the sub clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCIN	Input	
	CLKOUT	Output	Clock output pin.
	EXCIN	Input	External clock input pin for the RTC, battery backup, and REMC
Clock frequency accuracy measurement	CACREF	Input	Reference clock input pin for the clock frequency accuracy measurement circuit
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation.
	UB	Input	USB boot mode enable pin
	UPSEL	Input	Selects the power supply method in USB boot mode. The low level selects self-powered mode and the high level selects bus-powered mode.
System control	RES#	Input	Reset signal input pin. This LSI enters the reset state when this signal goes low.
	EMLE	Input	Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low.
	BSCANP	Input	Boundary scan enable pin. Boundary scan is enabled when this pin goes high. When not used, it should be driven low.
On-chip emulator	FINED	I/O	Fine interface pin
	TRST#	Input	On-chip emulator or boundary scan pins. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator.
	TMS	Input	
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TRCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TRSYNC TRSYNC1	Output	These pins indicate that output from the TRDATA0 to TRDATA7 pins is valid.
	TRDATA0 TRDATA1 TRDATA2 TRDATA3 TRDATA4 TRDATA5 TRDATA6 TRDATA7	Output	These pins output the trace information.

Table 1.4 Pin Functions (2/8)

Classifications	Pin Name	I/O	Description
Address bus	A0 to A23	Output	Output pins for the address
Data bus	D0 to D15	I/O	Input and output pins for the bidirectional data bus
Multiplexed bus	A0/D0 to A15/D15	I/O	Address/data multiplexed bus
Bus control	RD#	Output	Strobe signal which indicates that reading from the external bus interface space is in progress
	WR#	Output	Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode
	WR0#, WR1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode
	BC0#, BC1#	Output	Strobe signals which indicate that either group of data bus pins (D7 to D0 and D15 to D8) is valid in access to the external bus interface space, in 1-write strobe mode
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT#	Input	Input pin for wait request signals in access to the external space
	CS0# to CS7#	Output	Select signals for CS areas
SDRAM interface	CKE	Output	SDRAM clock enable signal
	SDCS#	Output	SDRAM chip select signal
	RAS#	Output	SDRAM row address strobe signal
	CAS#	Output	SDRAM column address strove signal
	WE#	Output	SDRAM write enable pin
	DQM0, DQM1	Output	SDRAM I/O data mask enable signals
EXDMA controller	EDREQ0, EDREQ1	Input	External DMA transfer request pins
	EDACK0, EDACK1	Output	Single address transfer acknowledge signals
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15, IRQ0-DS to IRQ15-DS	Input	Maskable interrupt request pins
Multi-function timer pulse unit 3	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/dead time compensation input pins
	MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D	I/O	The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins
	MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D	I/O	The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins
	MTIOC8A, MTIOC8B, MTIOC8C, MTIOC8D	I/O	The TGRA8 to TGRD8 input capture input/output compare output/PWM output pins
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Port output enable 3	POE0#, POE4#, POE8#, POE10#, POE11#	Input	Input pins for request signals to place the MTU in the high impedance state

Table 1.4 Pin Functions (3/8)

Classifications	Pin Name	I/O	Description
16-bit timer pulse unit	TIOCA0, TIOCB0, TIOCC0, TIOCD0	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins
	TIOCA1, TIOCB1	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins
	TIOCA2, TIOCB2	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins
	TIOCA3, TIOCB3, TIOCC3, TIOCD3	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins
	TIOCA4, TIOCB4	I/O	The TGRA4 and TGRB4 input capture input/output compare output/PWM output pins
	TIOCA5, TIOCB5	I/O	The TGRA5 and TGRB5 input capture input/output compare output/PWM output pins
	TCLKA, TCLKB, TCLKC, TCLKD	Input	Input pins for external clock signals or for phase counting mode clock signals
Programmable pulse generator	PO0 to PO31	Output	Output pins for the pulse signals
8-bit timer	TMO0 to TMO3	Output	Compare match output pins
	TMCI0 to TMCI3	Input	Input pins for external clocks to be input to the counter
	TMRI0 to TMRI3	Input	Input pins for the counter reset
Compare match timer W	TIC0 to TIC3	Input	Input pins for CMTW
	TOC0 to TOC3	Output	Output pins for CMTW
Serial communications interface (SCIk)	• Asynchronous mode/clock synchronous mode		
	SCK0 to SCK9	I/O	Input/output pins for the clock
	RXD0 to RXD9	Input	Input pins for received data
	TXD0 to TXD9	Output	Output pins for transmitted data
	CTS0# to CTS9#	Input	Input pins for controlling the start of transmission and reception
	RTS0# to RTS9#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL0 to SSCL9	I/O	Input/output pins for the I^2C clock
	SSDA0 to SSDA9	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK0 to SCK9	I/O	Input/output pins for the clock
	SMISO0 to SMISO9	I/O	Input/output pins for slave transmission of data
	SMOSI0 to SMOSI9	I/O	Input/output pins for master transmission of data
	SS0# to SS9#	Input	Chip-select input pins

Table 1.4 Pin Functions (4/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock
	RXD12	Input	Input pin for received data
	TXD12	Output	Output pin for transmitted data
	CTS12#	Input	Input pin for controlling the start of transmission and reception
	RTS12#	Output	Output pin for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock
	SSDA12	I/O	Input/output pin for the I^2C data
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock
	SMISO12	I/O	Input/output pin for slave transmission of data
	SMOSI12	I/O	Input/output pin for master transmission of data
	SS12#	Input	Chip-select input pin
	• Extended serial mode		
	RXDX12	Input	Input pin for received data
	TXDX12	Output	Output pin for transmitted data
	SIOX12	I/O	Input/output pin for received or transmitted data
Serial communications interface (SCIm)	• Asynchronous mode/clock synchronous mode		
	SCK10, SCK11	I/O	Input/output pins for the clock
	RXD10, RXD11	Input	Input pins for received data
	TXD10, TXD11	Output	Output pins for transmitted data
	CTS10#, CTS11#	Input	Input pins for controlling the start of transmission and reception
	RTS10#, RTS11#	Output	Output pins for controlling the start of transmission and reception
	• Simple I^2C mode		
	SSCL10, SSCL11	I/O	Input/output pins for the I^2C clock
	SSDA10, SSDA11	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK10, SCK11	I/O	Input/output pins for the clock
	SMISO10, SMISO11	I/O	Input/output pins for slave transmission of data
	SMOSI10, SMOSI11	I/O	Input/output pins for master transmission of data
	SS10#, SS11#	Input	Chip-select input pins

Table 1.4 Pin Functions (5/8)

Classifications	Pin Name	I/O	Description
Serial communications interface (RSCI)	• Asynchronous mode/clock synchronous mode		
	SCK010, SCK011	I/O	Input/output pins for the clock
	RXD010, RXD011	Input	Input pins for received data
	TXD010, TXD011	Output	Output pins for transmitted data
	CTS010#, CTS011#	Input	Input pins for controlling the start of transmission and reception
	RTS010#, RTS011#	Output	Output pins for controlling the start of transmission and reception
	DE010, DE011	Output	DriveEnable output pins
	• Simple I^2C mode		
	SSCL010, SSCL011	I/O	Input/output pins for the I^2C clock
	SSDA010, SSDA011	I/O	Input/output pins for the I^2C data
	• Simple SPI mode		
	SCK010, SCK011	I/O	Input/output pins for the clock
	SMISO010, SMISO011	I/O	Input/output pins for slave transmission of data
	SMOSI010, SMOSI011	I/O	Input/output pins for master transmission of data
	SS010#, SS011#	Input	Chip-select input pins
	• HBS support mode		
	RXD010, RXD011	Input	Input pin for received data
	TXD010, TXD011, TXDA011, TXDB011	Output	Output pins for transmitted data
I^2C bus interface	SCL0[FM+], SCL1, SCL2, SCL2-DS	I/O	Input/output pins for clocks. Bus can be directly driven by the N-channel open drain
	SDA0[FM+], SDA1, SDA2, SDA2-DS	I/O	Input/output pins for data. Bus can be directly driven by the N-channel open drain
Hi-speed I^2C bus interface (RIICHS)	SCLHS0[FM+/HS]	I/O	Input/output pin for clocks. Bus can be directly driven by the N-channel open drain
	SDAHS0[FM+/HS]	I/O	Input/output pin for data. Bus can be directly driven by the N-channel open drain
USB 2.0 host/function module	VCC_USB	Input	Power supply pin
	VSS_USB	Input	Ground pin
	USB0_DP, USB1_DP	I/O	Input or output USB transceiver D+ data.
	USB0_DM, USB1_DM	I/O	Input or output USB transceiver D- data.
	USB0_EXICEN, USB1_EXICEN	Output	Connect to the OTG power IC.
	USB0_ID, USB1_ID	Input	Connect to the OTG power IC.
	USB0_VBUSEN, USB1_VBUSEN	Output	USB VBUS power enable pins
	USB0_OVRCURA/ USB0_OVRCURB, USB1_OVRCURA/ USB1_OVRCURB	Input	USB overcurrent pins
	USB0_VBUS, USB1_VBUS	Input	USB cable connection/disconnection detection input pins
CAN module	CRX0, CRX1, CRX1-DS	Input	Input pins
	CTX0, CTX1	Output	Output pins

Table 1.4 Pin Functions (6/8)

Classifications	Pin Name	I/O	Description
Serial peripheral interface	RSPCKA-A/RSPCKA-B/ RSPCKB-A/RSPCKB-B/ RSPCKC-A/RSPCKC-B	I/O	Clock input/output pins
	MOSIA-A/MOSIA-B/ MOSIB-A/MOSIB-B/ MOSIC-A/MOSIC-B	I/O	Input or output data output from the master
	MISOA-A/MISOA-B/ MISOB-A/MISOB-B/ MISOC-A/MISOC-B	I/O	Input or output data output from the slave
	SSLA0-A/SSLA0-B/ SSLB0-A/SSLB0-B/ SSLC0-A	I/O	Input or output pins for slave selection
	SSLA1-A/SSLA1-B/ SSLB1-A/SSLB1-B/ SSLC1-A, SSLA2-A/SSLA2-B/ SSLB2-A/SSLB2-B/ SSLC2-A, SSLA3-A/SSLA3-B/ SSLB3-A/SSLB3-B/ SSLC3-A	Output	Output pins for slave selection
Serial peripheral interface (RSPIA)	RSPCK0-A/RSPCK0-B	I/O	Clock input/output pins
	MOSI0-A/MOSI0-B	I/O	Input or output data output from the master
	MISO0-A/MISO0-B	I/O	Input or output data output from the slave
	SSL00-A/SSL00-B	I/O	Input or output pins for slave selection
	SSL01-A/SSL01-B, SSL02-A/SSL02-B, SSL03-A/SSL03-B	Output	Output pins for slave selection
Quad-SPI memory interface	QSPCLK-A/QSPCLK-B	Output	Clock output pins
	QSSL-A/QSSL-B	Output	Output pins for slave selection
	QIO0-A/QIO0-B, QIO1-A/QIO1-B, QIO2-A/QIO2-B, QIO3-A/QIO3-B	I/O	Data input/output pins
Serial sound interface	SSIBCK0	I/O	SSIE serial bit-clock pin
	SSILRCK0	I/O	LR clock
	SSITXD0	Output	Serial data output pin
	SSIRXD0	Input	Serial data input pin
	AUDIO_CLK	Input	External clock pin for audio (input for an oversampling clock)
SD host interface	SDHI_CLK-A/SDHI_CLK-B/ SDHI_CLK-C	Output	SD clock output pins
	SDHI_CMD-A/SDHI_CMD-B/ SDHI_CMD-C	I/O	SD command output, response input signal pins
	SDHI_D3-A/SDHI_D3-B/ SDHI_D3-C to SDHI_D0-A/ SDHI_D0-B/SDHI_D0-C	I/O	SD data bus pins
	SDHI_CD	Input	SD card detection pin
	SDHI_WP	Input	SD write-protect signal
Realtime clock	RTCOUT	Output	Output pin for 1-Hz/64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
Battery backup	TAMPI0 to TAMPI2	Input	Input pins for detecting tampering
Remote control signal receiver (REMC)	PMC0-DS	Input	Input pin for external pulse signal

Table 1.4 Pin Functions (7/8)

Classifications	Pin Name	I/O	Description
12-bit A/D converter	AN000 to AN007, AN100 to AN111	Input	Input pins for the analog signals to be processed by the A/D converter
	ADTRG0#, ADTRG1#	Input	Input pins for the external trigger signals that start the A/D conversion
	ANEX0	Output	Extended analog output pin
	ANEX1	Input	Extended analog input pin
Capacitive touch sensing unit (CTSU)	TS0 to TS16	I/O	Electrostatic capacitance measurement pins (touch pins).
	TSCAP	—	Connect to the VSS via a decoupling capacitor (10 nF) for stabilizing the internal voltage. The capacitor should be placed close to the pin.
Analog power supply	AVCC0*1	Input	Analog voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	AVSS0*1	Input	Analog ground pin for the 12-bit A/D converter (unit 0). Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC0 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter (unit 0). Connect this pin to VCC if the 12-bit A/D converter is not to be used.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter (unit 0). Connect this pin to VSS if the 12-bit A/D converter is not to be used.
	AVCC1*1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1). This pin also supplies the analog voltage to the temperature sensor. Connect this pin to a branch from the VCC power supply. Connect the pin to AVSS1 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.
	AVSS1*1	Input	Analog voltage supply and reference voltage supply pin for the 12-bit A/D converter (unit 1). This pin also supplies the analog ground voltage to the temperature sensor. Connect this pin to a branch from the VSS ground power supply. Connect the pin to AVCC1 via a 0.1-µF multilayer ceramic capacitor. The capacitor should be placed close to the pin.

Table 1.4 Pin Functions (8/8)

Classifications	Pin Name	I/O	Description
I/O ports	P00 to P03, P05, P07	I/O	6-bit input/output pins
	P12 to P17	I/O	6-bit input/output pins
	P20 to P27	I/O	8-bit input/output pins
	P30 to P37	I/O	8-bit input/output pins (P35: input pin)
	P40 to P47	I/O	8-bit input/output pins
	P50 to P56	I/O	7-bit input/output pins
	P60 to P67	I/O	8-bit input/output pins
	P70 to P77	I/O	8-bit input/output pins
	P80 to P83, P86, P87	I/O	6-bit input/output pins
	P90 to P93	I/O	4-bit input/output pins
	PA0 to PA7	I/O	8-bit input/output pins
	PB0 to PB7	I/O	8-bit input/output pins
	PC0 to PC7	I/O	8-bit input/output pins
	PD0 to PD7	I/O	8-bit input/output pins
	PE0 to PE7	I/O	8-bit input/output pins
	PF5	I/O	1-bit input/output pins
	PH1, PH2	I/O	2-bit input/output pins
	PJ3, PJ5	I/O	2-bit input/output pins

Note: Note the following regarding pin names. For details, see section 1.6, List of Pin and Pin Functions.
- When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group.
  All RSPI, RSPIA, QSPIX, SDHI AC timings are measured in combination with the pins in the same group.
- When the pin functions have “-DS” appended to their names, they can also be used as triggers for release from deep software standby.
- RIIC and RIICHS pin functions that have [FM+] appended to their names support fast-mode plus.

Note 1. When neither the 12-bit A/D converter nor temperature sensor is to be used, connect the AVCC0 and AVCC1 pins to VCC, and the AVSS0 and AVSS1 pins to VSS.

1.5 Pin Assignments

1.5.1 145-Pin TFLGA (0.65-mm Pitch)

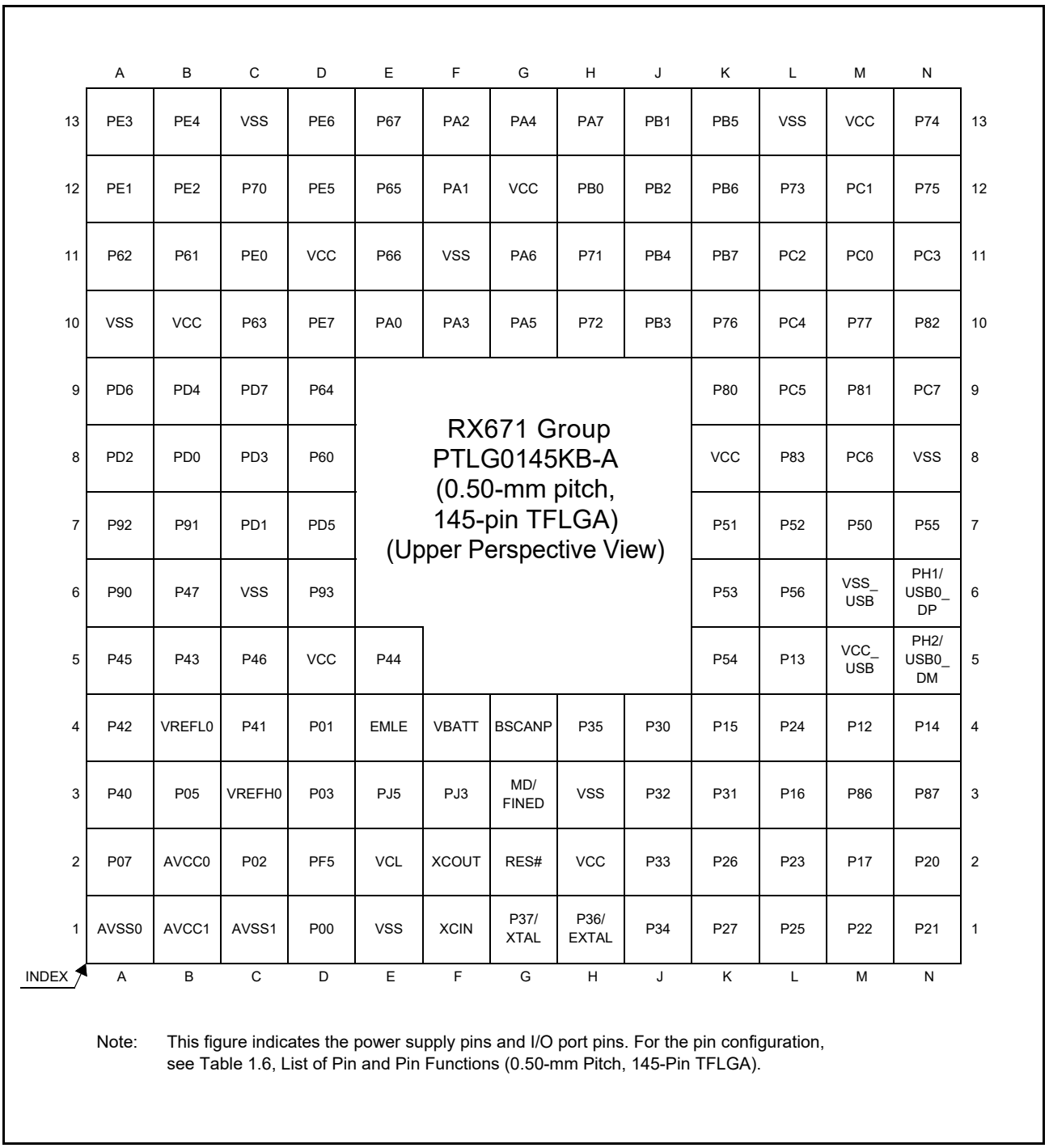
	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	PE3	PE4	VSS	PE6	P67	PA2	USB1_ DP	USB1_ DM	PB1	PB5	VSS	VCC	P74	13
12	PE1	PE2	P70	PE5	P65	PA1	VSS_ USB	VCC_ USB	PB2	PB6	P73	PC1	P75	12
11	P62	P61	PE0	VCC	P66	PA4	PA6	PA7	PB4	PB7	PC2	PC0	PC3	11
10	VSS	VCC	P63	PE7	PA0	PA3	PA5	PB0	PB3	P76	PC4	P77	P82	10
9	PD6	PD4	PD7	P64						P80	PC5	P81	PC7	9
8	PD2	PD0	PD3	P60						VCC	P83	PC6	VSS	8
7	P92	P91	PD1	PD5						P51	P52	P50	P55	7
6	P90	P47	VSS	P93						P53	P56	VSS_ USB	PH1/ USB0_ DP	6
5	P45	P43	P46	VCC	P44					P54	P13	VCC_ USB	PH2/ USB0_ DM	5
4	P42	VREFL0	P41	P01	EMLE	VBATT	BSCANP	P35	P30	P15	P24	P12	P14	4
3	P40	P05	VREFH0	P03	PJ5	PJ3	MD/ FINED	VSS	P32	P31	P16	P86	P87	3
2	P07	AVCC0	P02	PF5	VCL	XCOUT	RES#	VCC	P33	P26	P23	P17	P20	2
1	AVSS0	AVCC1	AVSS1	P00	VSS	XCIN	P37/ XTAL	P36/ EXTAL	P34	P27	P25	P22	P21	1
INDEX	A	B	C	D	E	F	G	H	J	K	L	M	N	

RX671 Group
PTLG0145JC-A
(0.65-mm pitch,
145-pin TFLGA)
(Upper Perspective View)

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.5, List of Pin and Pin Functions (0.65-mm Pitch, 145-Pin TFLGA).

Figure 1.3 Pin Assignment (0.65-mm Pitch, 145-Pin TFLGA)

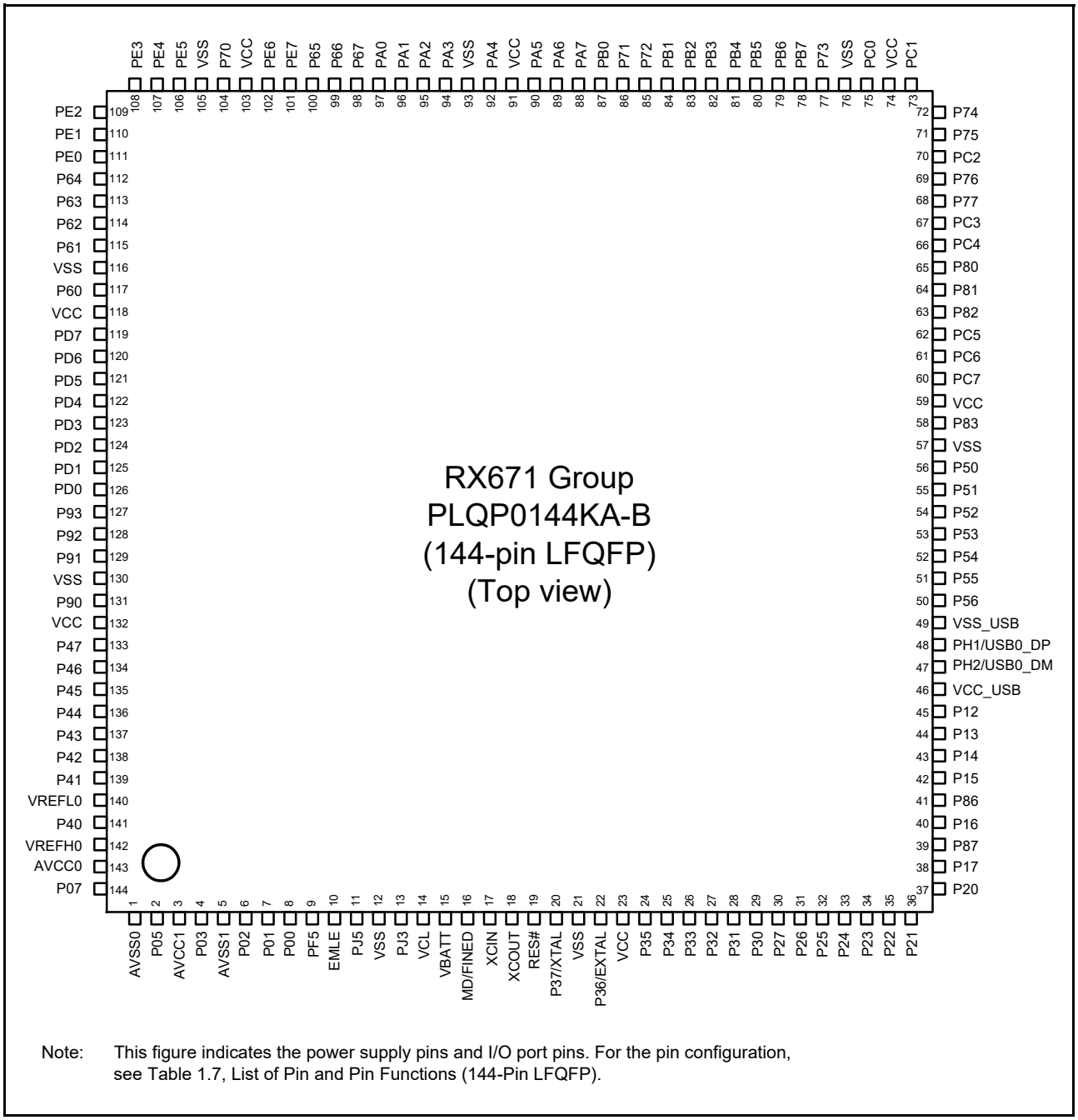
1.5.2 145-Pin TFLGA (0.50-mm Pitch)



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.6, List of Pin and Pin Functions (0.50-mm Pitch, 145-Pin TFLGA).

Figure 1.4 Pin Assignment (0.50-mm Pitch, 145-Pin TFLGA)

1.5.3 144-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.7, List of Pin and Pin Functions (144-Pin LFQFP).

Figure 1.5 Pin Assignment (144-Pin LFQFP)

1.5.4 100-Pin TFLGA

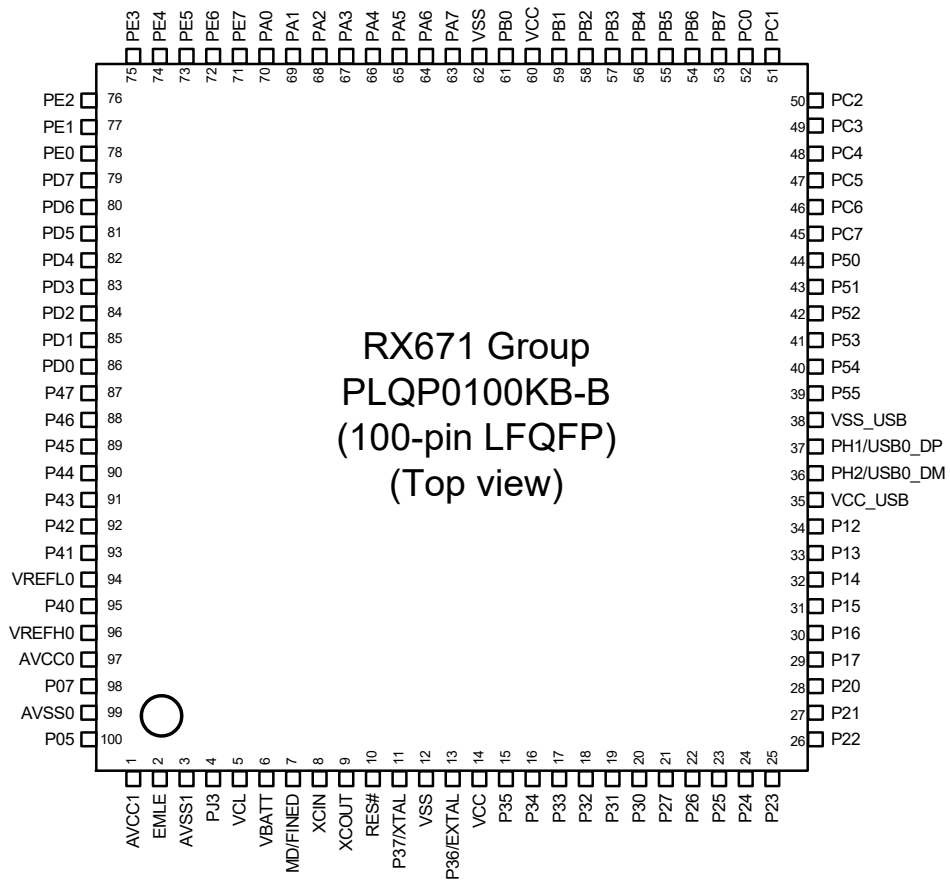
RX671 Group
PTLG0100JB-A (100-pin TFLGA)
(Upper Perspective View)

	A	B	C	D	E	F	G	H	J	K	
10	PE2	PE3	PE4	PA0	PA3	VSS	VCC	PB7	PC1	PC2	10
9	PE1	PD7	PE5	PA1	PA5	PA7	PB1	PB6	PC0	PC3	9
8	PE0	PD6	PD5	PE7	PA4	PB0	PB4	PC6	PC4	PC5	8
7	PD4	PD3	PD2	PE6	PA6	PB2	PB5	PC7	P50	P51	7
6	PD0	PD1	P47	P46	PA2	PB3	P52	P54	VCC_ USB	PH1/ USB0_ DP	6
5	P43	P44	P42	P45	P41	P12	P53	P55	VSS_ USB	PH2/ USB0_ DM	5
4	VREFL0	P40	VREFH0	VBATT	P34	P32	P27	P15	P13	P14	4
3	P07	AVCC0	PJ3	MD/ FINED	RES#	P35	P30	P16	P17	P20	3
2	AVCC1	AVSS0	AVSS1	XCOUT	VSS	VCC	P31	P25	P21	P22	2
1	P05	EMLE	VCL	XCIN	P37/ XTAL	P36/ EXTAL	P33	P26	P24	P23	1
INDEX	A	B	C	D	E	F	G	H	J	K	

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.8, List of Pin and Pin Functions (100-Pin TFLGA).

Figure 1.6 Pin Assignment (100-Pin TFLGA)

1.5.5 100-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.9, List of Pin and Pin Functions (100-Pin LFQFP).

Figure 1.7 Pin Assignment (100-Pin LFQFP)

1.5.6 64-Pin TFBGA

RX671 Group
PTBG0064KB-A (64-pin TFBGA)
(Upper Perspective View)

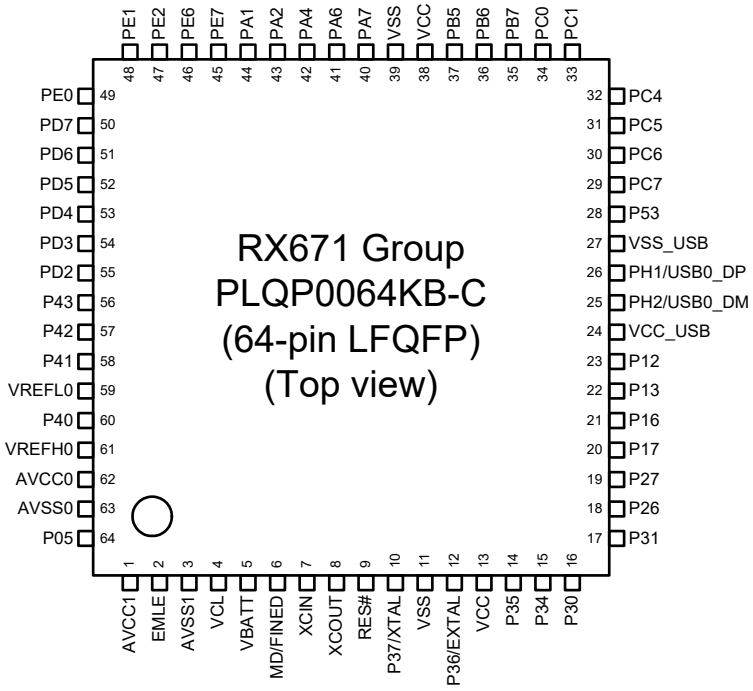
	A	B	C	D	E	F	G	H	
8	PE2	PE6	PE7	PA4	VSS	PB5	PC0	PC1	8
7	PE0	PE1	PA1	PA2	VCC	PB6	PC5	PC4	7
6	PD7	PD6	PD5	PA6	PA7	PB7	PC7	PC6	6
5	PD2	PD3	PD4	P43	BSCANP	P53	VSS_USB	PH1/ USB0_DP	5
4	VREFL0	P42	P41	P40	P13	P12	VCC_USB	PH2/ USB0_DM	4
3	VREFH0	AVCC0	MD/FINED	RES#	P34	P35	P30	P16	3
2	AVSS0	AVSS1	VBATT	XCOUT	VSS	VCC	P31	P17	2
1	AVCC1	EMLE	VCL	XCIN	P37/ XTAL	P36/ EXTAL	P27	P26	1
	A	B	C	D	E	F	G	H	

INDEX

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.10, List of Pin and Pin Functions (64-Pin TFBGA).

Figure 1.8 Pin Assignment (64-Pin TFBGA)

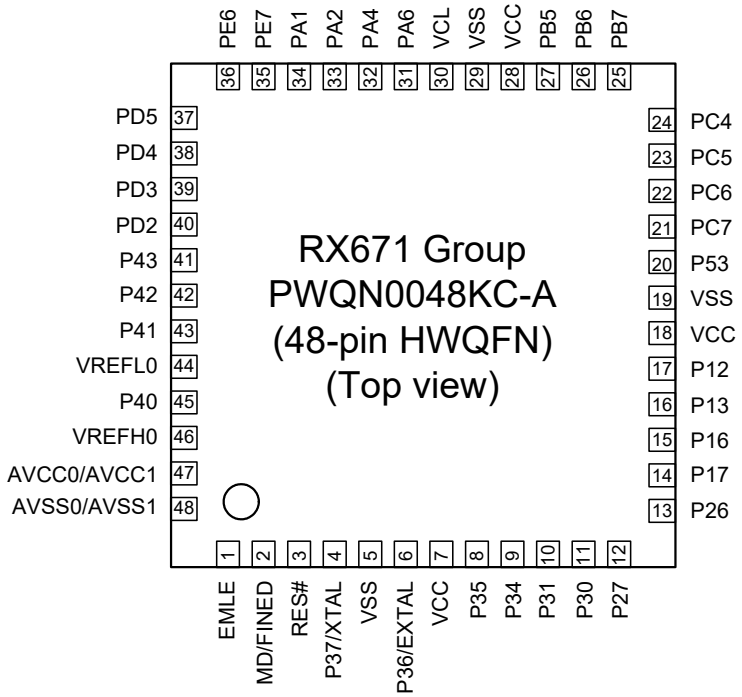
1.5.7 64-Pin LFQFP



Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.11, List of Pin and Pin Functions (64-Pin LFQFP).

Figure 1.9 Pin Assignment (64-Pin LFQFP)

1.5.8 48-Pin HWQFN



Note: It is recommended to connect the exposed die pad to VSS.

Note: This figure indicates the power supply pins and I/O port pins. For the pin configuration, see Table 1.12, List of Pin and Pin Functions (48-Pin HWQFN).

Figure 1.10 Pin Assignment (48-Pin HWQFN)

1.6 List of Pin and Pin Functions

1.6.1 145-Pin TFLGA (0.65-mm Pitch)

Table 1.5 List of Pin and Pin Functions (0.65-mm Pitch, 145-Pin TFLGA) (1/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.65-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
A1	AVSS0								
A2		P07					IRQ15	ADTRG0#	
A3		P40					IRQ8-DS	AN000	
A4		P42					IRQ10-DS	AN002	
A5		P45					IRQ13-DS	AN005	
A6		P90	A16		TXD7/SMOSI7/ SSDA7		IRQ0	AN108	
A7		P92	A18	POE4#	RXD7/SMISO7/ SSCL7		IRQ10		
A8		PD2	D2[A2/D2]	MTIOC4D/ TIC2	CRX0/MISOC-A	SDHI_D2-B/ QIO2-B	IRQ2	AN105	
A9		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	SDHI_D0-B/ QIO0-B	IRQ6	AN101	
A10	VSS								
A11		P62	CS2#/ RAS#/ D1[A1/D1]				IRQ2		
A12		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	TXD12/SMOSI12/ SSDA12/ TXDX12/SIOX12/ SSLB2-B		IRQ9	ANEX1	
A13		PE3	D11[A11/ D11]/ D3[A3/D3]	MTIOC4B/ PO26/POE8#/ TOC3	CTS12#/RTS12#/ SS12#		IRQ11		
B1	AVCC1								
B2	AVCC0								
B3		P05					IRQ13		
B4	VREFL0								
B5		P43					IRQ11-DS	AN003	
B6		P47					IRQ15-DS	AN007	
B7		P91	A17		SCK7		IRQ9		
B8		PD0	D0[A0/D0]	POE4#			IRQ0	AN107	
B9		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	SDHI_CMD-B/ QSSL-B	IRQ4	AN103	
B10	VCC								
B11		P61	CS1#/ SDCS#/ D0[A0/D0]				IRQ1		
B12		PE2	D10[A10/ D10]/ D2[A2/D2]	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3-B		IRQ7-DS		

Table 1.5 List of Pin and Pin Functions (0.65-mm Pitch, 145-Pin TFLGA) (2/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.65-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
B13		PE4	D12[A12/D12]/D4[A4/D4]	MTIOC4D/MTIOC1A/PO28	SSLB0-B		IRQ12		
C1	AVSS1								
C2		P02		TMCI1	SCK6		IRQ10	AN109	
C3	VREFH0								
C4		P41					IRQ9-DS	AN001	
C5		P46					IRQ14-DS	AN006	
C6	VSS								
C7		PD1	D1[A1/D1]	MTIOC4B/POE0#	CTX0/MOSIC-A		IRQ1	AN106	
C8		PD3	D3[A3/D3]	MTIOC8D/POE8#/TOC2	RSPCKC-A	SDHI_D3-B/QIO3-B	IRQ3	AN104	
C9		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3-A	SDHI_D1-B/QIO1-B	IRQ7	AN100	
C10		P63	CS3#/CAS#/D2[A2/D2]				IRQ3		
C11		PE0	D8[A8/D8]/D0[A0/D0]	MTIOC3D	SCK12/SSLB1-B		IRQ8	ANEX0	
C12		P70	SDCLK				IRQ0		
C13	VSS								
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6		IRQ8	AN111	
D2		PF5					IRQ4		
D3		P03					IRQ11		
D4		P01		TMCI0	RXD6/SMISO6/SSCL6		IRQ9	AN110	
D5	VCC								
D6		P93	A19	POE0#	CTS7#/RTS7#/SS7#		IRQ11		
D7		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/POE10#	SSLC1-A	SDHI_CLK-B/QSPCLK-B	IRQ5	AN102	
D8		P60	CS0#				IRQ0		
D9		P64	CS4#/WE#/D3[A3/D3]				IRQ4		
D10		PE7	D15[A15/D15]/D7[A7/D7]	MTIOC6A/TOC1	MISOB-B	SDHI_WP/SDHI_D1-B/QIO1-B	IRQ7		
D11	VCC								
D12		PE5	D13[A13/D13]/D5[A5/D5]	MTIOC4C/MTIOC2B	RSPCKB-B		IRQ5		
D13		PE6	D14[A14/D14]/D6[A6/D6]	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/SDHI_D0-B/QIO0-B	IRQ6		
E1	VSS								
E2	VCL								

Table 1.5 List of Pin and Pin Functions (0.65-mm Pitch, 145-Pin TFLGA) (3/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.65-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
E3		PJ5		POE8#	CTS2#/RTS2#/ SS2#		IRQ13		
E4	EMLE								
E5		P44					IRQ12-DS	AN004	
E10		PA0	A0/BC0#	MTIOC4A/ MTIOC6D/ TIOCA0/ CACREF/ PO16	SSLA1-B/ SSL01-B		IRQ0		
E11		P66	CS6#/ DQM0	MTIOC7D			IRQ14		
E12		P65	CS5#/CKE				IRQ13		
E13		P67	CS7#/ DQM1	MTIOC7C			IRQ15		
F1	XCIN								
F2	XCOUT								
F3	EXCIN	PJ3	EDACK1	MTIOC3C	CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#		IRQ11		
F4	VBATT								
F10		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	RXD5/SMISO5/ SSCL5		IRQ6-DS		
F11		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ SSL00-B/TXD12/ SMOSI12/ SSDA12/ TXDX12/SIOX12		IRQ5-DS		
F12		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	SCK5/SSLA2-B/ SSL02-B/SCK12	SDHI_CD	IRQ11		
F13		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B/ SSL03-B/RXD12/ SMISO12/ SSCL12/RXDX12	SDHI_WP	IRQ10		
G1	XTAL	P37							
G2	RES#								
G3	MD/FINED								
G4	BSCANP								
G10		PA5	A5	MTIOC6B/ TIOCB1/PO21	RSPCKA-B/ RSPCK0-B		IRQ5		
G11		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	CTS5#/RTS5#/ SS5#/MOSIA-B/ MOSI0-B/ CTS12#/RTS12#/ SS12#		IRQ14		
G12	VSS_USB								
G13					USB1_DP				

Table 1.5 List of Pin and Pin Functions (0.65-mm Pitch, 145-Pin TFLGA) (4/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.65-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
H1	EXTAL	P36							
H2	VCC								
H3	VSS								
H4	UPSEL	P35					NMI		
H10		PB0	A8	MTIC5W/ TIOCA3/PO24	RXD4/RXD6/ SMISO4/ SMISO6/SSCL4/ SSCL6		IRQ12		
H11		PA7	A7	TIOCB2/PO23	MISOA-B/ MISO0-B		IRQ7		
H12	VCC_USB								
H13					USB1_DM				
J1	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE10#	SCK6/SCK0		IRQ4		TS0
J2		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0		IRQ3-DS		TS1
J3		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCOUT/ RTCIC2/ POE0#/ POE10#	TXD6/TXD0/ SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN		IRQ2-DS		TAMPI2
J4	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS		TAMPI0
J10		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/ TMO0/PO27/ POE11#	SCK4/SCK6/ PMC0-DS		IRQ3		
J11		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#/ SS011#/ CTS011#/ RTS011#/DE011		IRQ4		
J12		PB2	A10	TIOCC3/ TCLKC/PO26	CTS4#/RTS4#/ CTS6#/RTS6#/ SS4#/SS6#		IRQ2		
J13		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	TXD4/TXD6/ SMOSI4/ SMOSI6/SSDA4/ SSDA6		IRQ4-DS		
K1	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB-A		IRQ7		TS2

Table 1.5 List of Pin and Pin Functions (0.65-mm Pitch, 145-Pin TFLGA) (5/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.65-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
K2	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ MOSIB-A		IRQ6		TS3
K3	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A		IRQ1-DS		TAMPI1
K4		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/ TMCI2/PO13	RXD1/SCK3/ SMISO1/SSCL1/ CRX1-DS		IRQ5		TS10
K5	TRDATA2	P54	ALE/ D1[A1/D1]/ EDACK0	MTIOC4B/ TMCI1	CTS2#/RTS2#/ SS2#/CTX1/ MOSIC-B		IRQ4		
K6		P53*1	BCLK		SSIRXD0/ PMC0-DS		IRQ3		TS12
K7		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A		IRQ1		
K8	VCC								
K9	TRDATA0	P80	EDREQ0	MTIOC3B/ PO26	SCK10/RTS10#/ SCK010/ RTS010#/DE010/ USB1_EXICEN	SDHI_WP/ QIO2-A	IRQ8		
K10	TRDATA6	P76	CS6#	PO22	SMISO11/ SSCL11/RXD11/ SMISO011/ SSCL011/ RXD011	SDHI_CMD-A/ QSSL-A	IRQ14		
K11		PB7	A15	MTIOC3B/ TIOCB5/PO31	TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11/ SMOSI011/ SSDA011/ TXD011		IRQ15		
K12		PB6	A14	MTIOC3D/ TIOCA5/PO30	RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11/ SMISO011/ SSCL011/ RXD011		IRQ6		
K13		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	SCK9/SCK11/ SCK011		IRQ13		
L1		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD	IRQ5	ADTRG0#	TS4/ CLKOUT
L2		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/ RTS0#/SMOSI3/ SS0#/SSDA3/ SSIBCK0	SDHI_D1-C	IRQ3		TS6

Table 1.5 List of Pin and Pin Functions (0.65-mm Pitch, 145-Pin TFLGA) (6/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.65-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
L3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/ SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#	
L4		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP	IRQ12		TS5
L5		P13		MTIOC0B/ TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]/ SDAHS0[FM+/ HS]		IRQ3	ADTRG1#	
L6		P56	EDACK1	MTIOC3C/ TIOCA1	SCK7/ RSPCKC-B		IRQ6		
L7		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A		IRQ2		
L8	TRCLK	P83	EDACK1	MTIOC4C	SS10#/CTS10#/ SCK10/SS010#/ CTS010#/ SCK010		IRQ3		
L9		PC5	D3[A3/D3]/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	SCK8/SCK10/ RSPCKA-A/ SSIBCK0/ SCK010/ RSPCK0-A		IRQ5		TS14
L10		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/ SSLA0-A/ AUDIO_CLK/ SS010#/ CTS010#/ RTS010#/DE010/ SSL00-A	SDHI_D1-A/ QIO1-A	IRQ12		TSCAP
L11		PC2	A18	MTIOC4B/ TCLKA/PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ TXDB011/ SSL03-A	SDHI_D3-A	IRQ10		
L12	TRDATA4	P73	CS3#	PO16	USB1_VBUS/ USB1_VBUSEN/ USB1_OVRCURB		IRQ8		
L13	VSS								
M1		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_CLK	SDHI_D0-C	IRQ15		TS7

Table 1.5 List of Pin and Pin Functions (0.65-mm Pitch, 145-Pin TFLGA) (7/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.65-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
M2		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/ TMO1/PO15/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/ SSITXD0	SDHI_D3-C	IRQ7	ADTRG1#	
M3		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10/ SMISO010/ SSCL010/ RXD010		IRQ14		
M4		P12		MTIC5U/ TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]/ SCLHS0[FM+/ HS]		IRQ2		
M5	VCC_USB								
M6	VSS_USB								
M7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A		IRQ0		
M8		PC6	D2[A2/D2]/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/TIC0/ PO30	RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A/ SSILRCK0/ SMISO010/ SSCL010/ RXD010/ MOSI0-A		IRQ13		TS13
M9	TRDATA1	P81	EDACK0	MTIOC3D/ PO27	SMISO10/ SSCL10/RXD10/ SMISO010/ SSCL010/ RXD010/ USB1_OVRCURB	SDHI_CD/ QIO3-A	IRQ9		
M10	TRDATA7	P77	CS7#	PO23	SMOSI11/ SSDA11/TXD11/ SMOSI011/ SSDA011/ TXD011/ USB1_ID	SDHI_CLK-A/ QSPCLK-A	IRQ7		
M11		PC0	A16	MTIOC3C/ TCLKC/PO17	CTS5#/RTS5#/ SS5#/SSLA1-A/ RXD011/ SMISO011/ SSCL011/ SSL01-A		IRQ14		TS16
M12		PC1	A17	MTIOC3A/ TCLKD/PO18	SCK5/SSLA2-A/ TXD011/ SMOSI011/ SSDA011/ TXDA011/ SSL02-A		IRQ12		TS15
M13	VCC								

Table 1.5 List of Pin and Pin Functions (0.65-mm Pitch, 145-Pin TFLGA) (8/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.65-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
N1		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/ SSILRCK0	SDHI_CLK-C	IRQ9		TS8
N2		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID/ SSIRXD0	SDHI_CMD-C	IRQ8		TS9
N3		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10/ SMOSI010/ SSDA010/ TXD010	SDHI_D2-C	IRQ15		
N4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/ TMRI2/PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA		IRQ4		TS11
N5		PH2		TMRI0	USB0_DM		IRQ1		
N6		PH1		TMO0	USB0_DP		IRQ0		
N7	TRDATA3	P55	D0[A0/D0]/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	TXD7/SMOSI7/ SSDA7/CRX1/ MISOC-B		IRQ10		
N8	VSS								
N9	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/TOC0/ PO31/ CACREF	TXD8/SMOSI8/ SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A/ SSITXD0/ SMOSI010/ SSDA010/ TXD010/ MISO0-A		IRQ14		
N10	TRSYNC	P82	EDREQ1	MTIOC4A/ PO28	SMOSI10/ SSDA10/TXD10/ SMOSI010/ SSDA010/ TXD010/ USB1_VBUSEN		IRQ2		
N11		PC3	A19	MTIOC4D/ TCLKB/PO24	TXD5/SMOSI5/ SSDA5/ PMC0-DS	SDHI_D0-A/ QIO0-A	IRQ11		
N12	TRSYNC1	P75	CS5#	PO20	SCK11/RTS11#/ SCK011/ RTS011#/DE011/ USB1_OVRCURA	SDHI_D2-A	IRQ13		
N13	TRDATA5	P74	A20/CS4#	PO19	SS11#/CTS11#/ SS011#/ CTS011#/ USB1_VBUSEN		IRQ12		

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

1.6.2 145-Pin TFLGA (0.50-mm Pitch)

Table 1.6 List of Pin and Pin Functions (0.50-mm Pitch, 145-Pin TFLGA) (1/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.50-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
A1	AVSS0								
A2		P07					IRQ15	ADTRG0#	
A3		P40					IRQ8-DS	AN000	
A4		P42					IRQ10-DS	AN002	
A5		P45					IRQ13-DS	AN005	
A6		P90	A16		TXD7/SMOSI7/ SSDA7		IRQ0	AN108	
A7		P92	A18	POE4#	RXD7/SMISO7/ SSCL7		IRQ10		
A8		PD2	D2[A2/D2]	MTIOC4D/ TIC2	CRX0/MISOC-A	SDHI_D2-B/ QIO2-B	IRQ2	AN105	
A9		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	SDHI_D0-B/ QIO0-B	IRQ6	AN101	
A10	VSS								
A11		P62	CS2#/ RAS#/ D1[A1/D1]				IRQ2		
A12		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	TXD12/SMOSI12/ SSDA12/ TXDX12/SIOX12/ SSLB2-B		IRQ9	ANEX1	
A13		PE3	D11[A11/ D11]/ D3[A3/D3]	MTIOC4B/ PO26/POE8#/ TOC3	CTS12#/RTS12#/ SS12#		IRQ11		
B1	AVCC1								
B2	AVCC0								
B3		P05					IRQ13		
B4	VREFL0								
B5		P43					IRQ11-DS	AN003	
B6		P47					IRQ15-DS	AN007	
B7		P91	A17		SCK7		IRQ9		
B8		PD0	D0[A0/D0]	POE4#			IRQ0	AN107	
B9		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	SDHI_CMD-B/ QSSL-B	IRQ4	AN103	
B10	VCC								
B11		P61	CS1#/ SDCS#/ D0[A0/D0]				IRQ1		
B12		PE2	D10[A10/ D10]/ D2[A2/D2]	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3-B		IRQ7-DS		

Table 1.6 List of Pin and Pin Functions (0.50-mm Pitch, 145-Pin TFLGA) (2/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.50-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
B13		PE4	D12[A12/D12]/D4[A4/D4]	MTIOC4D/MTIOC1A/PO28	SSLB0-B		IRQ12		
C1	AVSS1								
C2		P02		TMCI1	SCK6		IRQ10	AN109	
C3	VREFH0								
C4		P41					IRQ9-DS	AN001	
C5		P46					IRQ14-DS	AN006	
C6	VSS								
C7		PD1	D1[A1/D1]	MTIOC4B/POE0#	CTX0/MOSIC-A		IRQ1	AN106	
C8		PD3	D3[A3/D3]	MTIOC8D/POE8#/TOC2	RSPCKC-A	SDHI_D3-B/QIO3-B	IRQ3	AN104	
C9		PD7	D7[A7/D7]	MTIC5U/POE0#	SSLC3-A	SDHI_D1-B/QIO1-B	IRQ7	AN100	
C10		P63	CS3#/CAS#/D2[A2/D2]				IRQ3		
C11		PE0	D8[A8/D8]/D0[A0/D0]	MTIOC3D	SCK12/SSLB1-B		IRQ8	ANEX0	
C12		P70	SDCLK				IRQ0		
C13	VSS								
D1		P00		TMRI0	TXD6/SMOSI6/SSDA6		IRQ8	AN111	
D2		PF5					IRQ4		
D3		P03					IRQ11		
D4		P01		TMCI0	RXD6/SMISO6/SSCL6		IRQ9	AN110	
D5	VCC								
D6		P93	A19	POE0#	CTS7#/RTS7#/SS7#		IRQ11		
D7		PD5	D5[A5/D5]	MTIC5W/MTIOC8C/POE10#	SSLC1-A	SDHI_CLK-B/QSPCLK-B	IRQ5	AN102	
D8		P60	CS0#				IRQ0		
D9		P64	CS4#/WE#/D3[A3/D3]				IRQ4		
D10		PE7	D15[A15/D15]/D7[A7/D7]	MTIOC6A/TOC1	MISOB-B	SDHI_WP/SDHI_D1-B/QIO1-B	IRQ7		
D11	VCC								
D12		PE5	D13[A13/D13]/D5[A5/D5]	MTIOC4C/MTIOC2B	RSPCKB-B		IRQ5		
D13		PE6	D14[A14/D14]/D6[A6/D6]	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/SDHI_D0-B/QIO0-B	IRQ6		
E1	VSS								
E2	VCL								

Table 1.6 List of Pin and Pin Functions (0.50-mm Pitch, 145-Pin TFLGA) (3/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.50-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
E3		PJ5		POE8#	CTS2#/RTS2#/SS2#		IRQ13		
E4	EMLE								
E5		P44					IRQ12-DS	AN004	
E10		PA0	A0/BC0#	MTIOC4A/MTIOC6D/TIOCA0/CACREF/PO16	SSLA1-B/SSL01-B		IRQ0		
E11		P66	CS6#/DQM0	MTIOC7D			IRQ14		
E12		P65	CS5#/CKE				IRQ13		
E13		P67	CS7#/DQM1	MTIOC7C			IRQ15		
F1	XCIN								
F2	XCOUT								
F3	EXCIN	PJ3	EDACK1	MTIOC3C	CTS6#/RTS6#/CTS0#/RTS0#/SS6#/SS0#		IRQ11		
F4	VBATT								
F10		PA3	A3	MTIOC0D/MTCLKD/TIOCD0/TCLKB/PO19	RXD5/SMISO5/SSCL5		IRQ6-DS		
F11	VSS								
F12		PA1	A1	MTIOC0B/MTCLKC/MTIOC7B/TIOCB0/PO17	SCK5/SSLA2-B/SSL02-B/SCK12	SDHI_CD	IRQ11		
F13		PA2	A2	MTIOC7A/PO18	RXD5/SMISO5/SSCL5/SSLA3-B/SSL03-B/RXD12/SMISO12/SSCL12/RXDX12	SDHI_WP	IRQ10		
G1	XTAL	P37							
G2	RES#								
G3	MD/FINED								
G4	BSCANP								
G10		PA5	A5	MTIOC6B/TIOCB1/PO21	RSPCKA-B/RSPCK0-B		IRQ5		
G11		PA6	A6	MTIC5V/MTCLKB/TIOCA2/TMCI3/PO22/POE10#	CTS5#/RTS5#/SS5#/MOSIA-B/MOSI0-B/CTS12#/RTS12#/SS12#		IRQ14		
G12	VCC								
G13		PA4	A4	MTIC5U/MTCLKA/TIOCA1/TMRI0/PO20	TXD5/SMOSI5/SSDA5/SSLA0-B/SSL00-B/TXD12/SMOSI12/SSDA12/TXDX12/SIOX12		IRQ5-DS		

Table 1.6 List of Pin and Pin Functions (0.50-mm Pitch, 145-Pin TFLGA) (4/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.50-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
H1	EXTAL	P36							
H2	VCC								
H3	VSS								
H4	UPSEL	P35					NMI		
H10		P72	A19/CS2#				IRQ10		
H11		P71	A18/CS1#				IRQ1		
H12		PB0	A8	MTIC5W/ TIOCA3/PO24	RXD4/RXD6/ SMISO4/ SMISO6/SSCL4/ SSCL6		IRQ12		
H13		PA7	A7	TIOCB2/PO23	MISOA-B/ MISO0-B		IRQ7		
J1	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE10#	SCK6/SCK0		IRQ4		TS0
J2		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0		IRQ3-DS		TS1
J3		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCOUT/ RTCIC2/ POE0#/ POE10#	TXD6/TXD0/ SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN		IRQ2-DS		TAMPI2
J4	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS		TAMPI0
J10		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/ TMO0/PO27/ POE11#	SCK4/SCK6/ PMC0-DS		IRQ3		
J11		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#/ SS011#/ CTS011#/ RTS011#/DE011		IRQ4		
J12		PB2	A10	TIOCC3/ TCLKC/PO26	CTS4#/RTS4#/ CTS6#/RTS6#/ SS4#/SS6#		IRQ2		
J13		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	TXD4/TXD6/ SMOSI4/ SMOSI6/SSDA4/ SSDA6		IRQ4-DS		
K1	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB-A		IRQ7		TS2

Table 1.6 List of Pin and Pin Functions (0.50-mm Pitch, 145-Pin TFLGA) (5/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.50-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
K2	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ MOSIB-A		IRQ6		TS3
K3	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A		IRQ1-DS		TAMPI1
K4		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/ TMCI2/PO13	RXD1/SCK3/ SMISO1/SSCL1/ CRX1-DS		IRQ5		TS10
K5	TRDATA2	P54	ALE/ D1[A1/D1]/ EDACK0	MTIOC4B/ TMCI1	CTS2#/RTS2#/ SS2#/CTX1/ MOSIC-B		IRQ4		
K6		P53*1	BCLK		SSIRXD0/ PMC0-DS		IRQ3		TS12
K7		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A		IRQ1		
K8	VCC								
K9	TRDATA0	P80	EDREQ0	MTIOC3B/ PO26	SCK10/RTS10#/ SCK010/ RTS010#/DE010	SDHI_WP/ QIO2-A	IRQ8		
K10	TRDATA6	P76	CS6#	PO22	SMISO11/ SSCL11/RXD11/ SMISO011/ SSCL011/ RXD011	SDHI_CMD-A/ QSSL-A	IRQ14		
K11		PB7	A15	MTIOC3B/ TIOCB5/PO31	TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11/ SMOSI011/ SSDA011/ TXD011		IRQ15		
K12		PB6	A14	MTIOC3D/ TIOCA5/PO30	RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11/ SMISO011/ SSCL011/ RXD011		IRQ6		
K13		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	SCK9/SCK11/ SCK011		IRQ13		
L1		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD	IRQ5	ADTRG0#	TS4/ CLKOUT
L2		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/ RTS0#/SMOSI3/ SS0#/SSDA3/ SSIBCK0	SDHI_D1-C	IRQ3		TS6

Table 1.6 List of Pin and Pin Functions (0.50-mm Pitch, 145-Pin TFLGA) (6/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.50-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
L3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/ SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#	
L4		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP	IRQ12		TS5
L5		P13		MTIOC0B/ TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]/ SDAHS0[FM+/ HS]		IRQ3	ADTRG1#	
L6		P56	EDACK1	MTIOC3C/ TIOCA1	SCK7/ RSPCKC-B		IRQ6		
L7		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A		IRQ2		
L8	TRCLK	P83	EDACK1	MTIOC4C	SS10#/CTS10#/ SCK10/SS010#/ CTS010#/ SCK010		IRQ3		
L9		PC5	D3[A3/D3]/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	SCK8/SCK10/ RSPCKA-A/ SSIBCK0/ SCK010/ RSPCK0-A		IRQ5		TS14
L10		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/ SSLA0-A/ AUDIO_CLK/ SS010#/ CTS010#/ RTS010#/DE010/ SSL00-A	SDHI_D1-A/ QIO1-A	IRQ12		TSCAP
L11		PC2	A18	MTIOC4B/ TCLKA/PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ TXDB011/ SSL03-A	SDHI_D3-A	IRQ10		
L12	TRDATA4	P73	CS3#	PO16			IRQ8		
L13	VSS								
M1		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_CLK	SDHI_D0-C	IRQ15		TS7
M2		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/ TMO1/PO15/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/ SSITXD0	SDHI_D3-C	IRQ7	ADTRG1#	

Table 1.6 List of Pin and Pin Functions (0.50-mm Pitch, 145-Pin TFLGA) (7/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.50-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
M3		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10/ SMISO010/ SSCL010/ RXD010		IRQ14		
M4		P12		MTIC5U/ TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]/ SCLHS0[FM+/ HS]		IRQ2		
M5	VCC_USB								
M6	VSS_USB								
M7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A		IRQ0		
M8		PC6	D2[A2/D2]/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/TIC0/ PO30	RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A/ SSILRCK0/ SMISO010/ SSCL010/ RXD010/ MOSI0-A		IRQ13		TS13
M9	TRDATA1	P81	EDACK0	MTIOC3D/ PO27	SMISO10/ SSCL10/RXD10/ SMISO010/ SSCL010/ RXD010	SDHI_CD/ QIO3-A	IRQ9		
M10	TRDATA7	P77	CS7#	PO23	SMOSI11/ SSDA11/TXD11/ SMOSI011/ SSDA011/ TXD011	SDHI_CLK-A/ QSPCLK-A	IRQ7		
M11		PC0	A16	MTIOC3C/ TCLKC/PO17	CTS5#/RTS5#/ SS5#/SSLA1-A/ RXD011/ SMISO011/ SSCL011/ SSL01-A		IRQ14		TS16
M12		PC1	A17	MTIOC3A/ TCLKD/PO18	SCK5/SSLA2-A/ TXD011/ SMOSI011/ SSDA011/ TXDA011/ SSL02-A		IRQ12		TS15
M13	VCC								
N1		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/ SSILRCK0	SDHI_CLK-C	IRQ9		TS8
N2		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID/ SSIRXD0	SDHI_CMD-C	IRQ8		TS9

Table 1.6 List of Pin and Pin Functions (0.50-mm Pitch, 145-Pin TFLGA) (8/8)

Pin No.				Timer	Communication				
145-Pin TFLGA (0.50-mm pitch)	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
N3		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10/ SMOSI010/ SSDA010/ TXD010	SDHI_D2-C	IRQ15		
N4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/ TMRI2/PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA		IRQ4		TS11
N5		PH2		TMRI0	USB0_DM		IRQ1		
N6		PH1		TMO0	USB0_DP		IRQ0		
N7	TRDATA3	P55	D0[A0/D0]/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	TXD7/SMOSI7/ SSDA7/CRX1/ MISOC-B		IRQ10		
N8	VSS								
N9	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/TOC0/ PO31/ CACREF	TXD8/SMOSI8/ SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A/ SSITXD0/ SMOSI010/ SSDA010/ TXD010/ MISO0-A		IRQ14		
N10	TRSYNC	P82	EDREQ1	MTIOC4A/ PO28	SMOSI10/ SSDA10/TXD10/ SMOSI010/ SSDA010/ TXD010		IRQ2		
N11		PC3	A19	MTIOC4D/ TCLKB/PO24	TXD5/SMOSI5/ SSDA5/ PMC0-DS	SDHI_D0-A/ QIO0-A	IRQ11		
N12	TRSYNC1	P75	CS5#	PO20	SCK11/RTS11#/ SCK011/ RTS011#/DE011	SDHI_D2-A	IRQ13		
N13	TRDATA5	P74	A20/CS4#	PO19	SS11#/CTS11#/ SS011#/CTS011#		IRQ12		

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

1.6.3 144-Pin LFQFP

Table 1.7 List of Pin and Pin Functions (144-Pin LFQFP) (1/8)

Pin No.				Timer	Communication				
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
1	AVSS0								
2		P05					IRQ13		
3	AVCC1								
4		P03					IRQ11		
5	AVSS1								
6		P02		TMCI1	SCK6		IRQ10	AN109	
7		P01		TMCI0	RXD6/SMISO6/ SSCL6		IRQ9	AN110	
8		P00		TMRI0	TXD6/SMOSI6/ SSDA6		IRQ8	AN111	
9		PF5					IRQ4		
10	EMLE								
11		PJ5		POE8#	CTS2#/RTS2#/ SS2#		IRQ13		
12	VSS								
13	EXCIN	PJ3	EDACK1	MTIOC3C	CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#		IRQ11		
14	VCL								
15	VBATT								
16	MD/FINED								
17	XCIN								
18	XCOUT								
19	RES#								
20	XTAL	P37							
21	VSS								
22	EXTAL	P36							
23	VCC								
24	UPSEL	P35					NMI		
25	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE10#	SCK6/SCK0		IRQ4		TS0
26		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0		IRQ3-DS		TS1
27		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCOUT/ RTCIC2/ POE0#/ POE10#	TXD6/TXD0/ SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN		IRQ2-DS		TAMPI2

Table 1.7 List of Pin and Pin Functions (144-Pin LFQFP) (2/8)

Pin No.				Timer	Communication				
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
28	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A		IRQ1-DS		TAMPI1
29	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS		TAMPI0
30	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB-A		IRQ7		TS2
31	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ MOSIB-A		IRQ6		TS3
32		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD	IRQ5	ADTRG0#	TS4/ CLKOUT
33		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP	IRQ12		TS5
34		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/ RTS0#/SMOSI3/ SS0#/SSDA3/ SSIBCK0	SDHI_D1-C	IRQ3		TS6
35		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_CLK	SDHI_D0-C	IRQ15		TS7
36		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/ SSILRCK0	SDHI_CLK-C	IRQ9		TS8
37		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID/ SSIRXD0	SDHI_CMD-C	IRQ8		TS9
38		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/ TMO1/PO15/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/ SSITXD0	SDHI_D3-C	IRQ7	ADTRG1#	
39		P87		MTIOC4C/ TIOCA2	SMOSI10/ SSDA10/TXD10/ SMOSI010/ SSDA010/ TXD010	SDHI_D2-C	IRQ15		
40		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/ SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#	

Table 1.7 List of Pin and Pin Functions (144-Pin LFQFP) (3/8)

Pin No.				Timer	Communication				
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
41		P86		MTIOC4D/ TIOCA0	SMISO10/ SSCL10/RXD10/ SMISO010/ SSCL010/ RXD010		IRQ14		
42		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/ TMCI2/PO13	RXD1/SCK3/ SMISO1/SSCL1/ CRX1-DS		IRQ5		TS10
43		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/ TMRI2/PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA		IRQ4		TS11
44		P13		MTIOC0B/ TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]/ SDAHS0[FM+/ HS]		IRQ3	ADTRG1#	
45		P12		MTIC5U/ TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]/ SCLHS0[FM+/ HS]		IRQ2		
46	VCC_USB								
47		PH2		TMRI0	USB0_DM		IRQ1		
48		PH1		TMO0	USB0_DP		IRQ0		
49	VSS_USB								
50		P56	EDACK1	MTIOC3C/ TIOCA1	SCK7/ RSPCKC-B		IRQ6		
51	TRDATA3	P55	D0[A0/D0]/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	TXD7/SMOSI7/ SSDA7/CRX1/ MISOC-B		IRQ10		
52	TRDATA2	P54	ALE/ D1[A1/D1]/ EDACK0	MTIOC4B/ TMCI1	CTS2#/RTS2#/ SS2#/CTX1/ MOSIC-B		IRQ4		
53		P53*1	BCLK		SSIRXD0/ PMC0-DS		IRQ3		TS12
54		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A		IRQ2		
55		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A		IRQ1		
56		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A		IRQ0		
57	VSS								
58	TRCLK	P83	EDACK1	MTIOC4C	SS10#/CTS10#/ SCK10/SS010#/ CTS010#/ SCK010		IRQ3		
59	VCC								

Table 1.7 List of Pin and Pin Functions (144-Pin LFQFP) (4/8)

Pin No.				Timer	Communication				
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
60	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/TOC0/ PO31/ CACREF	TXD8/SMOSI8/ SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A/ SSITXD0/ SMOSI010/ SSDA010/ TXD010/ MISO0-A		IRQ14		
61		PC6	D2[A2/D2]/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/TIC0/ PO30	RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A/ SSILRCK0/ SMISO010/ SSCL010/ RXD010/ MOSI0-A		IRQ13		TS13
62		PC5	D3[A3/D3]/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	SCK8/SCK10/ RSPCKA-A/ SSIBCK0/ SCK010/ RSPCK0-A		IRQ5		TS14
63	TRSYNC	P82	EDREQ1	MTIOC4A/ PO28	SMOSI10/ SSDA10/TXD10/ SMOSI010/ SSDA010/ TXD010		IRQ2		
64	TRDATA1	P81	EDACK0	MTIOC3D/ PO27	SMISO10/ SSCL10/RXD10/ SMISO010/ SSCL010/ RXD010	SDHI_CD/ QIO3-A	IRQ9		
65	TRDATA0	P80	EDREQ0	MTIOC3B/ PO26	SCK10/RTS10#/ SCK010/ RTS010#/DE010	SDHI_WP/ QIO2-A	IRQ8		
66		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/ SSLA0-A/ AUDIO_CLK/ SS010#/ CTS010#/ RTS010#/DE010/ SSL00-A	SDHI_D1-A/ QIO1-A	IRQ12		TSCAP
67		PC3	A19	MTIOC4D/ TCLKB/PO24	TXD5/SMOSI5/ SSDA5/ PMC0-DS	SDHI_D0-A/ QIO0-A	IRQ11		
68	TRDATA7	P77	CS7#	PO23	SMOSI11/ SSDA11/TXD11/ SMOSI011/ SSDA011/ TXD011	SDHI_CLK-A/ QSPCLK-A	IRQ7		

Table 1.7 List of Pin and Pin Functions (144-Pin LFQFP) (5/8)

Pin No.				Timer	Communication				
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
69	TRDATA6	P76	CS6#	PO22	SMISO11/ SSCL11/RXD11/ SMISO011/ SSCL011/ RXD011	SDHI_CMD-A/ QSSL-A	IRQ14		
70		PC2	A18	MTIOC4B/ TCLKA/PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ TXDB011/ SSL03-A	SDHI_D3-A	IRQ10		
71	TRSYNC1	P75	CS5#	PO20	SCK11/RTS11#/ SCK011/ RTS011#/DE011	SDHI_D2-A	IRQ13		
72	TRDATA5	P74	A20/CS4#	PO19	SS11#/CTS11#/ SS011#/CTS011#		IRQ12		
73		PC1	A17	MTIOC3A/ TCLKD/PO18	SCK5/SSLA2-A/ TXD011/ SMOSI011/ SSDA011/ TXDA011/ SSL02-A		IRQ12		TS15
74	VCC								
75		PC0	A16	MTIOC3C/ TCLKC/PO17	CTS5#/RTS5#/ SS5#/SSLA1-A/ RXD011/ SMISO011/ SSCL011/ SSL01-A		IRQ14		TS16
76	VSS								
77	TRDATA4	P73	CS3#	PO16			IRQ8		
78		PB7	A15	MTIOC3B/ TIOCB5/PO31	TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11/ SMOSI011/ SSDA011/ TXD011		IRQ15		
79		PB6	A14	MTIOC3D/ TIOCA5/PO30	RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11/ SMISO011/ SSCL011/ RXD011		IRQ6		
80		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	SCK9/SCK11/ SCK011		IRQ13		
81		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#/ SS011#/ CTS011#/ RTS011#/DE011		IRQ4		

Table 1.7 List of Pin and Pin Functions (144-Pin LFQFP) (6/8)

Pin No.				Timer	Communication				
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
82		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/ TMO0/PO27/ POE11#	SCK4/SCK6/ PMC0-DS		IRQ3		
83		PB2	A10	TIOCC3/ TCLKC/PO26	CTS4#/RTS4#/ CTS6#/RTS6#/ SS4#/SS6#		IRQ2		
84		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	TXD4/TXD6/ SMOSI4/ SMOSI6/SSDA4/ SSDA6		IRQ4-DS		
85		P72	A19/CS2#				IRQ10		
86		P71	A18/CS1#				IRQ1		
87		PB0	A8	MTIC5W/ TIOCA3/PO24	RXD4/RXD6/ SMISO4/ SMISO6/SSCL4/ SSCL6		IRQ12		
88		PA7	A7	TIOCB2/PO23	MISOA-B/ MISO0-B		IRQ7		
89		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	CTS5#/RTS5#/ SS5#/MOSIA-B/ MOSI0-B/ CTS12#/RTS12#/ SS12#		IRQ14		
90		PA5	A5	MTIOC6B/ TIOCB1/PO21	RSPCKA-B/ RSPCK0-B		IRQ5		
91	VCC								
92		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ SSL00-B/TXD12/ SMOSI12/ SSDA12/ TXDX12/SIOX12		IRQ5-DS		
93	VSS								
94		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	RXD5/SMISO5/ SSCL5		IRQ6-DS		
95		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B/ SSL03-B/RXD12/ SMISO12/ SSCL12/RXDX12	SDHI_WP	IRQ10		
96		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	SCK5/SSLA2-B/ SSL02-B/SCK12	SDHI_CD	IRQ11		
97		PA0	A0/BC0#	MTIOC4A/ MTIOC6D/ TIOCA0/ CACREF/ PO16	SSLA1-B/ SSL01-B		IRQ0		

Table 1.7 List of Pin and Pin Functions (144-Pin LFQFP) (7/8)

Pin No.				Timer	Communication				
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
98		P67	CS7#/ DQM1	MTIOC7C			IRQ15		
99		P66	CS6#/ DQM0	MTIOC7D			IRQ14		
100		P65	CS5#/CKE				IRQ13		
101		PE7	D15[A15/ D15]/ D7[A7/D7]	MTIOC6A/ TOC1	MISOB-B	SDHI_WP/ SDHI_D1-B/ QIO1-B	IRQ7		
102		PE6	D14[A14/ D14]/ D6[A6/D6]	MTIOC6C/ TIC1	MOSIB-B	SDHI_CD/ SDHI_D0-B/ QIO0-B	IRQ6		
103	VCC								
104		P70	SDCLK				IRQ0		
105	VSS								
106		PE5	D13[A13/ D13]/ D5[A5/D5]	MTIOC4C/ MTIOC2B	RSPCKB-B		IRQ5		
107		PE4	D12[A12/ D12]/ D4[A4/D4]	MTIOC4D/ MTIOC1A/ PO28	SSLB0-B		IRQ12		
108		PE3	D11[A11/ D11]/ D3[A3/D3]	MTIOC4B/ PO26/POE8#/ TOC3	CTS12#/RTS12#/ SS12#		IRQ11		
109		PE2	D10[A10/ D10]/ D2[A2/D2]	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3-B		IRQ7-DS		
110		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	TXD12/SMOSI12/ SSDA12/ TXDX12/SIOX12/ SSLB2-B		IRQ9	ANEX1	
111		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	SCK12/SSLB1-B		IRQ8	ANEX0	
112		P64	CS4#/WE#/ D3[A3/D3]				IRQ4		
113		P63	CS3#/ CAS#/ D2[A2/D2]				IRQ3		
114		P62	CS2#/ RAS#/ D1[A1/D1]				IRQ2		
115		P61	CS1#/ SDCS#/ D0[A0/D0]				IRQ1		
116	VSS								
117		P60	CS0#				IRQ0		
118	VCC								
119		PD7	D7[A7/D7]	MTIC5U/ POE0#	SSLC3-A	SDHI_D1-B/ QIO1-B	IRQ7	AN100	
120		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	SDHI_D0-B/ QIO0-B	IRQ6	AN101	

Table 1.7 List of Pin and Pin Functions (144-Pin LFQFP) (8/8)

Pin No.				Timer	Communication				
144-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC SDRAMC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
121		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	SDHI_CLK-B/ QSPCLK-B	IRQ5	AN102	
122		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	SDHI_CMD-B/ QSSL-B	IRQ4	AN103	
123		PD3	D3[A3/D3]	MTIOC8D/ POE8#/TOC2	RSPCKC-A	SDHI_D3-B/ QIO3-B	IRQ3	AN104	
124		PD2	D2[A2/D2]	MTIOC4D/ TIC2	CRX0/MISOC-A	SDHI_D2-B/ QIO2-B	IRQ2	AN105	
125		PD1	D1[A1/D1]	MTIOC4B/ POE0#	CTX0/MOSIC-A		IRQ1	AN106	
126		PD0	D0[A0/D0]	POE4#			IRQ0	AN107	
127		P93	A19	POE0#	CTS7#/RTS7#/ SS7#		IRQ11		
128		P92	A18	POE4#	RXD7/SMISO7/ SSCL7		IRQ10		
129		P91	A17		SCK7		IRQ9		
130	VSS								
131		P90	A16		TXD7/SMOSI7/ SSDA7		IRQ0	AN108	
132	VCC								
133		P47					IRQ15-DS	AN007	
134		P46					IRQ14-DS	AN006	
135		P45					IRQ13-DS	AN005	
136		P44					IRQ12-DS	AN004	
137		P43					IRQ11-DS	AN003	
138		P42					IRQ10-DS	AN002	
139		P41					IRQ9-DS	AN001	
140	VREFL0								
141		P40					IRQ8-DS	AN000	
142	VREFH0								
143	AVCC0								
144		P07					IRQ15	ADTRG0#	

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

1.6.4 100-Pin TFLGA

Table 1.8 List of Pin and Pin Functions (100-Pin TFLGA) (1/6)

Pin No.				Timer	Communication				
100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
A1		P05					IRQ13		
A2	AVCC1								
A3		P07					IRQ15	ADTRG0#	
A4	VREFL0								
A5		P43					IRQ11-DS	AN003	
A6		PD0	D0[A0/D0]	POE4#			IRQ0	AN107	
A7		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	SDHI_CMD-B/ QSSL-B	IRQ4	AN103	
A8		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	SCK12/SSLB1-B		IRQ8	ANEX0	
A9		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B		IRQ9	ANEX1	
A10		PE2	D10[A10/ D10]/ D2[A2/D2]	MTIOC4A/ PO23/TIC3	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B		IRQ7-DS		
B1	EMLE								
B2	AVSS0								
B3	AVCC0								
B4		P40					IRQ8-DS	AN000	
B5		P44					IRQ12-DS	AN004	
B6		PD1	D1[A1/D1]	MTIOC4B/ POE0#	CTX0/MOSIC-A		IRQ1	AN106	
B7		PD3	D3[A3/D3]	MTIOC8D/ POE8#/TOC2	RSPCKC-A	SDHI_D3-B/ QIO3-B	IRQ3	AN104	
B8		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	SDHI_D0-B/ QIO0-B	IRQ6	AN101	
B9		PD7	D7[A7/D7]	MTIC5U/ POE0#	SSLC3-A	SDHI_D1-B/ QIO1-B	IRQ7	AN100	
B10		PE3	D11[A11/ D11]/ D3[A3/D3]	MTIOC4B/ PO26/POE8#/ TOC3	CTS12#/RTS12#/ SS12#		IRQ11		
C1	VCL								
C2	AVSS1								
C3	EXCIN	PJ3	EDACK1	MTIOC3C	CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#		IRQ11		
C4	VREFH0								
C5		P42					IRQ10-DS	AN002	
C6		P47					IRQ15-DS	AN007	
C7		PD2	D2[A2/D2]	MTIOC4D/ TIC2	CRX0/MISOC-A	SDHI_D2-B/ QIO2-B	IRQ2	AN105	

Table 1.8 List of Pin and Pin Functions (100-Pin TFLGA) (2/6)

Pin No.				Timer	Communication				
100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
C8		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	SDHI_CLK-B/ QSPCLK-B	IRQ5	AN102	
C9		PE5	D13[A13/ D13]/ D5[A5/D5]	MTIOC4C/ MTIOC2B	RSPCKB-B		IRQ5		
C10		PE4	D12[A12/ D12]/ D4[A4/D4]	MTIOC4D/ MTIOC1A/ PO28	SSLB0-B		IRQ12		
D1	XCIN								
D2	XCOUT								
D3	MD/FINED								
D4	VBATT								
D5		P45					IRQ13-DS	AN005	
D6		P46					IRQ14-DS	AN006	
D7		PE6	D14[A14/ D14]/ D6[A6/D6]	MTIOC6C/ TIC1	MOSIB-B	SDHI_CD/ SDHI_D0-B/ QIO0-B	IRQ6		
D8		PE7	D15[A15/ D15]/ D7[A7/D7]	MTIOC6A/ TOC1	MISOB-B	SDHI_WP/ SDHI_D1-B/ QIO1-B	IRQ7		
D9		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	SCK5/SSLA2-B/ SSL02-B/SCK12	SDHI_CD	IRQ11		
D10		PA0	A0/BC0#	MTIOC4A/ MTIOC6D/ TIOCA0/ CACREF/ PO16	SSLA1-B/ SSL01-B		IRQ0		
E1	XTAL	P37							
E2	VSS								
E3	RES#								
E4	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE10#	SCK6/SCK0		IRQ4		TS0
E5		P41					IRQ9-DS	AN001	
E6		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B/ SSL03-B/RXD12/ SMISO12/ SSCL12/RXDX12	SDHI_WP	IRQ10		
E7		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	CTS5#/RTS5#/ SS5#/MOSIA-B/ MOSI0-B/CTS12#/ RTS12#/SS12#		IRQ14		
E8		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ SSL00-B/TXD12/ SMOSI12/ SSDA12/TXDX12/ SIOX12		IRQ5-DS		

Table 1.8 List of Pin and Pin Functions (100-Pin TFLGA) (3/6)

Pin No.				Timer	Communication				
100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
E9		PA5	A5	MTIOC6B/ TIOCB1/PO21	RSPCKA-B/ RSPCK0-B		IRQ5		
E10		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	RXD5/SMISO5/ SSCL5		IRQ6-DS		
F1	EXTAL	P36							
F2	VCC								
F3	UPSEL	P35					NMI		
F4		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCOUT/ RTCIC2/ POE0#/ POE10#	TXD6/TXD0/ SMOSI6/SMOSI0/ SSDA6/SSDA0/ CTX0/ USB0_VBUSEN		IRQ2-DS		TAMPI2
F5		P12		MTIC5U/ TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]/ SCLHS0[FM+/HS]		IRQ2		
F6		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/ TMO0/PO27/ POE11#	SCK6/PMC0-DS		IRQ3		
F7		PB2	A10	TIOCC3/ TCLKC/PO26	CTS6#/RTS6#/ SS6#		IRQ2		
F8		PB0	A8	MTIC5W/ TIOCA3/PO24	RXD6/SMISO6/ SSCL6		IRQ12		
F9		PA7	A7	TIOCB2/PO23	MISOA-B/ MISO0-B		IRQ7		
F10	VSS								
G1		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/RXD0/ SMISO6/SMISO0/ SSCL6/SSCL0/ CRX0		IRQ3-DS		TS1
G2	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A		IRQ1-DS		TAMPI1
G3	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS		TAMPI0
G4	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB-A		IRQ7		TS2
G5		P53*1	BCLK		SSIRXD0/ PMC0-DS		IRQ3		TS12
G6		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A		IRQ2		

Table 1.8 List of Pin and Pin Functions (100-Pin TFLGA) (4/6)

Pin No.				Timer	Communication				
100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
G7		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	SCK9/SCK11/ SCK011		IRQ13		
G8		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#/ SS011#/CTS011#/ RTS011#/DE011		IRQ4		
G9		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	TXD6/SMOSI6/ SSDA6		IRQ4-DS		
G10	VCC								
H1	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ MOSIB-A		IRQ6		TS3
H2		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD	IRQ5	ADTRG0#	TS4/ CLKOUT
H3		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#	
H4		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/ TMCI2/PO13	RXD1/SCK3/ SMISO1/SSCL1/ CRX1-DS		IRQ5		TS10
H5		P55	D0[A0/D0]/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	CRX1/MISOC-B		IRQ10		
H6		P54	ALE/ D1[A1/D1]/ EDACK0	MTIOC4B/ TMCI1	CTS2#/RTS2#/ SS2#/CTX1/ MOSIC-B		IRQ4		
H7	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/TOC0/ PO31/ CACREF	TXD8/SMOSI8/ SSDA8/SMOSI10/ SSDA10/TXD10/ MISOA-A/ SSITXD0/ SMOSI010/ SSDA010/ TXD010/MISO0-A		IRQ14		
H8		PC6	D2[A2/D2]/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/TIC0/ PO30	RXD8/SMISO8/ SSCL8/SMISO10/ SSCL10/RXD10/ MOSIA-A/ SSILRCK0/ SMISO010/ SSCL010/ RXD010/MOSI0-A		IRQ13		TS13

Table 1.8 List of Pin and Pin Functions (100-Pin TFLGA) (5/6)

Pin No.				Timer	Communication				
100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
H9		PB6	A14	MTIOC3D/ TIOCA5/PO30	RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11/ SMISO011/ SSCL011/RXD011		IRQ6		
H10		PB7	A15	MTIOC3B/ TIOCB5/PO31	TXD9/SMOSI9/ SSDA9/SMOSI11/ SSDA11/TXD11/ SMOSI011/ SSDA011/TXD011		IRQ15		
J1		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP	IRQ12		TS5
J2		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/ SSILRCK0	SDHI_CLK-C	IRQ9		TS8
J3		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/ TMO1/PO15/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/ SSITXD0	SDHI_D3-C	IRQ7	ADTRG1#	
J4		P13		MTIOC0B/ TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]/ SDAHS0[FM+/HS]		IRQ3	ADTRG1#	
J5	VSS_USB								
J6	VCC_USB								
J7		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A		IRQ0		
J8		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/SSLA0-A/ AUDIO_CLK/ SS010#/CTS010#/ RTS010#/DE010/ SSL00-A	SDHI_D1-A/ QIO1-A	IRQ12		TSCAP
J9		PC0	A16	MTIOC3C/ TCLKC/PO17	CTS5#/RTS5#/ SS5#/SSLA1-A/ RXD011/ SMISO011/ SSCL011/ SSL01-A		IRQ14		TS16
J10		PC1	A17	MTIOC3A/ TCLKD/PO18	SCK5/SSLA2-A/ TXD011/ SMOSI011/ SSDA011/ TXDA011/ SSL02-A		IRQ12		TS15
K1		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/ RTS0#/SMOSI3/ SS0#/SSDA3/ SSIBCK0	SDHI_D1-C	IRQ3		TS6

Table 1.8 List of Pin and Pin Functions (100-Pin TFLGA) (6/6)

Pin No.				Timer	Communication				
100-Pin TFLGA	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
K2		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_CLK	SDHI_D0-C	IRQ15		TS7
K3		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID/ SSIRXD0	SDHI_CMD-C	IRQ8		TS9
K4		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/ TMRI2/PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA		IRQ4		TS11
K5		PH2		TMRI0	USB0_DM		IRQ1		
K6		PH1		TMO0	USB0_DP		IRQ0		
K7		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A		IRQ1		
K8		PC5	D3[A3/D3]/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	SCK8/SCK10/ RSPCKA-A/ SSIBCK0/ SCK010/ RSPCK0-A		IRQ5		TS14
K9		PC3	A19	MTIOC4D/ TCLKB/PO24	TXD5/SMOSI5/ SSDA5/PMC0-DS	SDHI_D0-A/ QIO0-A	IRQ11		
K10		PC2	A18	MTIOC4B/ TCLKA/PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ TXDB011/ SSL03-A	SDHI_D3-A	IRQ10		

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

1.6.5 100-Pin LFQFP

Table 1.9 List of Pin and Pin Functions (100-Pin LFQFP) (1/6)

Pin No.				Timer	Communication				
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
1	AVCC1								
2	EMLE								
3	AVSS1								
4	EXCIN	PJ3	EDACK1	MTIOC3C	CTS6#/RTS6#/ CTS0#/RTS0#/ SS6#/SS0#		IRQ11		
5	VCL								
6	VBATT								
7	MD/FINED								
8	XCIN								
9	XCOUT								
10	RES#								
11	XTAL	P37							
12	VSS								
13	EXTAL	P36							
14	VCC								
15	UPSEL	P35					NMI		
16	TRST#	P34		MTIOC0A/ TMCI3/PO12/ POE10#	SCK6/SCK0		IRQ4		TS0
17		P33	EDREQ1	MTIOC0D/ TIOCD0/ TMRI3/PO11/ POE4#/ POE11#	RXD6/RXD0/ SMISO6/ SMISO0/SSCL6/ SSCL0/CRX0		IRQ3-DS		TS1
18		P32		MTIOC0C/ TIOCC0/ TMO3/PO10/ RTCOUT/ RTCIC2/ POE0#/ POE10#	TXD6/TXD0/ SMOSI6/ SMOSI0/SSDA6/ SSDA0/CTX0/ USB0_VBUSEN		IRQ2-DS		TAMPI2
19	TMS	P31		MTIOC4D/ TMCI2/PO9/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A		IRQ1-DS		TAMPI1
20	TDI	P30		MTIOC4B/ TMRI3/PO8/ RTCIC0/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS		TAMPI0
21	TCK	P27	CS7#	MTIOC2B/ TMCI3/PO7	SCK1/RSPCKB-A		IRQ7		TS2
22	TDO	P26	CS6#	MTIOC2A/ TMO1/PO6	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ MOSIB-A		IRQ6		TS3
23		P25	CS5#/ EDACK1	MTIOC4C/ MTCLKB/ TIOCA4/PO5	RXD3/SMISO3/ SSCL3	SDHI_CD	IRQ5	ADTRG0#	TS4/ CLKOUT

Table 1.9 List of Pin and Pin Functions (100-Pin LFQFP) (2/6)

Pin No.				Timer	Communication				
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
24		P24	CS4#/ EDREQ1	MTIOC4A/ MTCLKA/ TIOCB4/ TMRI1/PO4	SCK3/ USB0_VBUSEN	SDHI_WP	IRQ12		TS5
25		P23	EDACK0	MTIOC3D/ MTCLKD/ TIOCD3/PO3	TXD3/CTS0#/ RTS0#/SMOSI3/ SS0#/SSDA3/ SSIBCK0	SDHI_D1-C	IRQ3		TS6
26		P22	EDREQ0	MTIOC3B/ MTCLKC/ TIOCC3/ TMO0/PO2	SCK0/ USB0_OVRCURB/ AUDIO_CLK	SDHI_D0-C	IRQ15		TS7
27		P21		MTIOC1B/ MTIOC4A/ TIOCA3/ TMCI0/PO1	RXD0/SMISO0/ SSCL0/SCL1/ USB0_EXICEN/ SSILRCK0	SDHI_CLK-C	IRQ9		TS8
28		P20		MTIOC1A/ TIOCB3/ TMRI0/PO0	TXD0/SMOSI0/ SSDA0/SDA1/ USB0_ID/ SSIRXD0	SDHI_CMD-C	IRQ8		TS9
29		P17		MTIOC3A/ MTIOC3B/ MTIOC4B/ TIOCB0/ TCLKD/ TMO1/PO15/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/ SSITXD0	SDHI_D3-C	IRQ7	ADTRG1#	
30		P16		MTIOC3C/ MTIOC3D/ TIOCB1/ TCLKC/ TMO2/PO14/ RTCOUT	TXD1/RXD3/ SMOSI1/ SMISO3/SSDA1/ SSCL3/SCL2-DS/ USB0_VBUS/ USB0_VBUSEN/ USB0_OVRCURB		IRQ6	ADTRG0#	
31		P15		MTIOC0B/ MTCLKB/ TIOCB2/ TCLKB/ TMCI2/PO13	RXD1/SCK3/ SMISO1/SSCL1/ CRX1-DS		IRQ5		TS10
32		P14		MTIOC3A/ MTCLKA/ TIOCB5/ TCLKA/ TMRI2/PO15	CTS1#/RTS1#/ SS1#/CTX1/ USB0_OVRCURA		IRQ4		TS11
33		P13		MTIOC0B/ TIOCA5/ TMO3/PO13	TXD2/SMOSI2/ SSDA2/ SDA0[FM+]/ SDAHS0[FM+/ HS]		IRQ3	ADTRG1#	
34		P12		MTIC5U/ TMCI1	RXD2/SMISO2/ SSCL2/ SCL0[FM+]/ SCLHS0[FM+/ HS]		IRQ2		
35	VCC_USB								
36		PH2		TMRI0	USB0_DM		IRQ1		

Table 1.9 List of Pin and Pin Functions (100-Pin LFQFP) (3/6)

Pin No.				Timer	Communication				
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
37		PH1		TMO0	USB0_DP		IRQ0		
38	VSS_USB								
39		P55	D0[A0/D0]/ WAIT#/ EDREQ0	MTIOC4D/ TMO3	CRX1/MISOC-B		IRQ10		
40		P54	ALE/ D1[A1/D1]/ EDACK0	MTIOC4B/ TMCI1	CTS2#/RTS2#/ SS2#/CTX1/ MOSIC-B		IRQ4		
41		P53*1	BCLK		SSIRXD0/ PMC0-DS		IRQ3		TS12
42		P52	RD#		RXD2/SMISO2/ SSCL2/SSLB3-A		IRQ2		
43		P51	WR1#/ BC1#/ WAIT#		SCK2/SSLB2-A		IRQ1		
44		P50	WR0#/WR#		TXD2/SMOSI2/ SSDA2/SSLB1-A		IRQ0		
45	UB	PC7	A23/CS0#	MTIOC3A/ MTCLKB/ TMO2/TOC0/ PO31/ CACREF	TXD8/SMOSI8/ SSDA8/ SMOSI10/ SSDA10/TXD10/ MISOA-A/ SSITXD0/ SMOSI010/ SSDA010/ TXD010/ MISO0-A		IRQ14		
46		PC6	D2[A2/D2]/ A22/CS1#	MTIOC3C/ MTCLKA/ TMCI2/TIC0/ PO30	RXD8/SMISO8/ SSCL8/ SMISO10/ SSCL10/RXD10/ MOSIA-A/ SSILRCK0/ SMISO010/ SSCL010/ RXD010/ MOSI0-A		IRQ13		TS13
47		PC5	D3[A3/D3]/ A21/CS2#/ WAIT#	MTIOC3B/ MTCLKD/ TMRI2/PO29	SCK8/SCK10/ RSPCKA-A/ SSIBCK0/ SCK010/ RSPCK0-A		IRQ5		TS14
48		PC4	A20/CS3#	MTIOC3D/ MTCLKC/ TMCI1/PO25/ POE0#	SCK5/CTS8#/ RTS8#/SS8#/ SS10#/CTS10#/ RTS10#/ SSLA0-A/ AUDIO_CLK/ SS010#/ CTS010#/ RTS010#/DE010/ SSL00-A	SDHI_D1-A/ QIO1-A	IRQ12		TSCAP
49		PC3	A19	MTIOC4D/ TCLKB/PO24	TXD5/SMOSI5/ SSDA5/ PMC0-DS	SDHI_D0-A/ QIO0-A	IRQ11		

Table 1.9 List of Pin and Pin Functions (100-Pin LFQFP) (4/6)

Pin No.				Timer	Communication				
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
50		PC2	A18	MTIOC4B/ TCLKA/PO21	RXD5/SMISO5/ SSCL5/SSLA3-A/ TXDB011/ SSL03-A	SDHI_D3-A	IRQ10		
51		PC1	A17	MTIOC3A/ TCLKD/PO18	SCK5/SSLA2-A/ TXD011/ SMOSI011/ SSDA011/ TXDA011/ SSL02-A		IRQ12		TS15
52		PC0	A16	MTIOC3C/ TCLKC/PO17	CTS5#/RTS5#/ SS5#/SSLA1-A/ RXD011/ SMISO011/ SSCL011/ SSL01-A		IRQ14		TS16
53		PB7	A15	MTIOC3B/ TIOCB5/PO31	TXD9/SMOSI9/ SSDA9/ SMOSI11/ SSDA11/TXD11/ SMOSI011/ SSDA011/ TXD011		IRQ15		
54		PB6	A14	MTIOC3D/ TIOCA5/PO30	RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11/ SMISO011/ SSCL011/ RXD011		IRQ6		
55		PB5	A13	MTIOC2A/ MTIOC1B/ TIOCB4/ TMRI1/PO29/ POE4#	SCK9/SCK11/ SCK011		IRQ13		
56		PB4	A12	TIOCA4/PO28	CTS9#/RTS9#/ SS9#/SS11#/ CTS11#/RTS11#/ SS011#/ CTS011#/ RTS011#/DE011		IRQ4		
57		PB3	A11	MTIOC0A/ MTIOC4A/ TIOCD3/ TCLKD/ TMO0/PO27/ POE11#	SCK6/PMC0-DS		IRQ3		
58		PB2	A10	TIOCC3/ TCLKC/PO26	CTS6#/RTS6#/ SS6#		IRQ2		
59		PB1	A9	MTIOC0C/ MTIOC4C/ TIOCB3/ TMCI0/PO25	TXD6/SMOSI6/ SSDA6		IRQ4-DS		
60	VCC								
61		PB0	A8	MTIC5W/ TIOCA3/PO24	RXD6/SMISO6/ SSCL6		IRQ12		
62	VSS								

Table 1.9 List of Pin and Pin Functions (100-Pin LFQFP) (5/6)

Pin No.				Timer	Communication				
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
63		PA7	A7	TIOCB2/PO23	MISOA-B/ MISO0-B		IRQ7		
64		PA6	A6	MTIC5V/ MTCLKB/ TIOCA2/ TMCI3/PO22/ POE10#	CTS5#/RTS5#/ SS5#/MOSIA-B/ MOSI0-B/ CTS12#/RTS12#/ SS12#		IRQ14		
65		PA5	A5	MTIOC6B/ TIOCB1/PO21	RSPCKA-B/ RSPCK0-B		IRQ5		
66		PA4	A4	MTIC5U/ MTCLKA/ TIOCA1/ TMRI0/PO20	TXD5/SMOSI5/ SSDA5/SSLA0-B/ SSL00-B/TXD12/ SMOSI12/ SSDA12/ TXDX12/SIOX12		IRQ5-DS		
67		PA3	A3	MTIOC0D/ MTCLKD/ TIOCD0/ TCLKB/PO19	RXD5/SMISO5/ SSCL5		IRQ6-DS		
68		PA2	A2	MTIOC7A/ PO18	RXD5/SMISO5/ SSCL5/SSLA3-B/ SSL03-B/RXD12/ SMISO12/ SSCL12/RXDX12	SDHI_WP	IRQ10		
69		PA1	A1	MTIOC0B/ MTCLKC/ MTIOC7B/ TIOCB0/PO17	SCK5/SSLA2-B/ SSL02-B/SCK12	SDHI_CD	IRQ11		
70		PA0	A0/BC0#	MTIOC4A/ MTIOC6D/ TIOCA0/ CACREF/ PO16	SSLA1-B/ SSL01-B		IRQ0		
71		PE7	D15[A15/ D15]/ D7[A7/D7]	MTIOC6A/ TOC1	MISOB-B	SDHI_WP/ SDHI_D1-B/ QIO1-B	IRQ7		
72		PE6	D14[A14/ D14]/ D6[A6/D6]	MTIOC6C/ TIC1	MOSIB-B	SDHI_CD/ SDHI_D0-B/ QIO0-B	IRQ6		
73		PE5	D13[A13/ D13]/ D5[A5/D5]	MTIOC4C/ MTIOC2B	RSPCKB-B		IRQ5		
74		PE4	D12[A12/ D12]/ D4[A4/D4]	MTIOC4D/ MTIOC1A/ PO28	SSLB0-B		IRQ12		
75		PE3	D11[A11/ D11]/ D3[A3/D3]	MTIOC4B/ PO26/POE8#/ TOC3	CTS12#/RTS12#/ SS12#		IRQ11		
76		PE2	D10[A10/ D10]/ D2[A2/D2]	MTIOC4A/ PO23/TIC3	RXD12/ SMISO12/ SSCL12/ RXDX12/ SSLB3-B		IRQ7-DS		
77		PE1	D9[A9/D9]/ D1[A1/D1]	MTIOC4C/ MTIOC3B/ PO18	TXD12/SMOSI12/ SSDA12/ TXDX12/SIOX12/ SSLB2-B		IRQ9	ANEX1	

Table 1.9 List of Pin and Pin Functions (100-Pin LFQFP) (6/6)

Pin No.				Timer	Communication				
100-Pin LFQFP	Power Supply Clock System Control	I/O Port	Bus EXDMAC	(MTU, TPU, TMR, PPG, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, CAN, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, CLKOUT, Tamper detection)
78		PE0	D8[A8/D8]/ D0[A0/D0]	MTIOC3D	SCK12/SSLB1-B		IRQ8	ANEX0	
79		PD7	D7[A7/D7]	MTIC5U/ POE0#	SSLC3-A	SDHI_D1-B/ QIO1-B	IRQ7	AN100	
80		PD6	D6[A6/D6]	MTIC5V/ MTIOC8A/ POE4#	SSLC2-A	SDHI_D0-B/ QIO0-B	IRQ6	AN101	
81		PD5	D5[A5/D5]	MTIC5W/ MTIOC8C/ POE10#	SSLC1-A	SDHI_CLK-B/ QSPCLK-B	IRQ5	AN102	
82		PD4	D4[A4/D4]	MTIOC8B/ POE11#	SSLC0-A	SDHI_CMD-B/ QSSL-B	IRQ4	AN103	
83		PD3	D3[A3/D3]	MTIOC8D/ POE8#/TOC2	RSPCKC-A	SDHI_D3-B/ QIO3-B	IRQ3	AN104	
84		PD2	D2[A2/D2]	MTIOC4D/ TIC2	CRX0/MISOC-A	SDHI_D2-B/ QIO2-B	IRQ2	AN105	
85		PD1	D1[A1/D1]	MTIOC4B/ POE0#	CTX0/MOSIC-A		IRQ1	AN106	
86		PD0	D0[A0/D0]	POE4#			IRQ0	AN107	
87		P47					IRQ15-DS	AN007	
88		P46					IRQ14-DS	AN006	
89		P45					IRQ13-DS	AN005	
90		P44					IRQ12-DS	AN004	
91		P43					IRQ11-DS	AN003	
92		P42					IRQ10-DS	AN002	
93		P41					IRQ9-DS	AN001	
94	VREFL0								
95		P40					IRQ8-DS	AN000	
96	VREFH0								
97	AVCC0								
98		P07					IRQ15	ADTRG0#	
99	AVSS0								
100		P05					IRQ13		

Note 1. P53 is multiplexed with the BCLK pin function, so cannot be used as an I/O port pin when the external bus is enabled.

1.6.6 64-Pin TFBGA

Table 1.10 List of Pin and Pin Functions (64-Pin TFBGA) (1/3)

Pin No.			Timer	Communication				
64-Pin TFBGA	Power Supply Clock System Control	I/O Port	(MTU, TPU, TMR, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, Tamper detection)
A1	AVCC1							
A2	AVSS0							
A3	VREFH0							
A4	VREFL0							
A5		PD2	MTIOC4D/TIC2		SDHI_D2-B/ QIO2-B	IRQ2	AN105	
A6		PD7	MTIC5U/POE0#		SDHI_D1-B/ QIO1-B	IRQ7	AN100	
A7		PE0	MTIOC3D	SCK12/SSLB1-B		IRQ8	ANEX0	
A8		PE2	MTIOC4A/TIC3	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B		IRQ7-DS		
B1	EMLE							
B2	AVSS1							
B3	AVCC0							
B4		P42				IRQ10-DS	AN002	
B5		PD3	MTIOC8D/POE8#/ TOC2		SDHI_D3-B/ QIO3-B	IRQ3	AN104	
B6		PD6	MTIC5V/MTIOC8A/ POE4#		SDHI_D0-B/ QIO0-B	IRQ6	AN101	
B7		PE1	MTIOC4C/ MTIOC3B	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B		IRQ9	ANEX1	
B8		PE6	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/ SDHI_D0-B/ QIO0-B	IRQ6		
C1	VCL							
C2	VBATT							
C3	MD/FINED							
C4		P41				IRQ9-DS	AN001	
C5		PD4	MTIOC8B/POE11#		SDHI_CMD-B/ QSSL-B	IRQ4	AN103	
C6		PD5	MTIC5W/ MTIOC8C/POE10#		SDHI_CLK-B/ QSPCLK-B	IRQ5	AN102	
C7		PA1	MTIOC0B/ MTCLKC/ MTIOC7B/TIOCB0	SCK5/SSLA2-B/ SSL02-B/SCK12	SDHI_CD	IRQ11		
C8		PE7	MTIOC6A/TOC1	MISOB-B	SDHI_WP/ SDHI_D1-B/ QIO1-B	IRQ7		
D1	XCIN							
D2	XCOUT							
D3	RES#							
D4		P40				IRQ8-DS	AN000	
D5		P43				IRQ11-DS	AN003	
D6		PA6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/ POE10#	CTS5#/RTS5#/ SS5#/MOSIA-B/ MOSI0-B/CTS12#/ RTS12#/SS12#		IRQ14		

Table 1.10 List of Pin and Pin Functions (64-Pin TFBGA) (2/3)

Pin No.			Timer	Communication				
64-Pin TFBGA	Power Supply Clock System Control	I/O Port	(MTU, TPU, TMR, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, Tamper detection)
D7		PA2	MTIOC7A	RXD5/SMISO5/ SSCL5/SSLA3-B/ SSL03-B/RXD12/ SMISO12/SSCL12/ RXDX12	SDHI_WP	IRQ10		
D8		PA4	MTIC5U/MTCLKA/ TIOCA1/TMRI0	TXD5/SMOSI5/ SSDA5/SSLA0-B/ SSL00-B/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12		IRQ5-DS		
E1	XTAL	P37						
E2	VSS							
E3	TRST#	P34	MTIOC0A/TMCI3/ POE10#			IRQ4		TS0
E4		P13	MTIOC0B/TIOCA5/ TMO3	TXD2/SMOSI2/ SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]		IRQ3	ADTRG1#	
E5	BSCANP							
E6		PA7	TIOCB2	MISOA-B/MISO0-B		IRQ7		
E7	VCC							
E8	VSS							
F1	EXTAL	P36						
F2	VCC							
F3	UPSEL	P35				NMI		
F4		P12	TMCI1/MTIC5U	RXD2/SMISO2/ SSCL2/SCL0[FM+]/ SCLHS0[FM+/HS]		IRQ2		
F5		P53		SSIRXD0/PMC0-DS		IRQ3		TS12
F6		PB7	MTIOC3B/TIOCB5	TXD9/SMOSI9/ SSDA9/SMOSI11/ SSDA11/TXD11/ SMOSI011/ SSDA011/TXD011		IRQ15		
F7		PB6	MTIOC3D/TIOCA5	RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11/ SMISO011/ SSCL011/RXD011		IRQ6		
F8		PB5	MTIOC2A/ MTIOC1B/TIOCB4/ TMRI1/POE4#	SCK9/SCK11/ SCK011		IRQ13		
G1	TCK	P27	MTIOC2B/TMCI3	SCK1/RSPCKB-A		IRQ7		TS2
G2	TMS	P31	MTIOC4D/TMCI2/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A		IRQ1-DS		TAMPI1
G3	TDI	P30	MTIOC4B/TMRI3/ RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS		TAMPI0
G4	VCC_USB							
G5	VSS_USB							
G6	UB	PC7	MTIOC3A/ MTCLKB/TMO2/ TOC0/CACREF	TXD8/SMOSI8/ SSDA8/SMOSI10/ SSDA10/TXD10/ MISOA-A/SSITXD0/ SMOSI010/ SSDA010/TXD010/ MISO0-A		IRQ14		

Table 1.10 List of Pin and Pin Functions (64-Pin TFBGA) (3/3)

Pin No.			Timer	Communication				
64-Pin TFBGA	Power Supply Clock System Control	I/O Port	(MTU, TPU, TMR, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, Tamper detection)
G7		PC5	MTIOC3B/ MTCLKD/TMRI2	SCK8/SCK10/ RSPCKA-A/ SSIBCK0/SCK010/ RSPCK0-A		IRQ5		TS14
G8		PC0	MTIOC3C/TCLKC	CTS5#/RTS5#/ SS5#/SSLA1-A/ RXD011/SMISO011/ SSCL011/SSL01-A		IRQ14		TS16
H1	TDO	P26	MTIOC2A/TMO1	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ MOSIB-A		IRQ6		TS3
H2		P17	MTIOC3A/ MTIOC3B/ MTIOC4B/TIOCB0/ TCLKD/TMO1/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/SSITXD0	SDHI_D3-C	IRQ7	ADTRG1#	
H3		P16	MTIOC3C/ MTIOC3D/TIOCB1/ TCLKC/TMO2/ RTCOUT	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ SCL2-DS/ USB0_VBUS		IRQ6	ADTRG0#	
H4		PH2	TMRI0	USB0_DM		IRQ1		
H5		PH1	TMO0	USB0_DP		IRQ0		
H6		PC6	MTIOC3C/ MTCLKA/TMCI2/ TIC0	RXD8/SMISO8/ SSCL8/SMISO10/ SSCL10/RXD10/ MOSIA-A/ SMISO010/ SSCL010/RXD010/ MOSI0-A/SSILRCK0		IRQ13		TS13
H7		PC4	MTIOC3D/ MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/ RTS8#/SS8#/SS10#/ CTS10#/RTS10#/ SSLA0-A/ AUDIO_CLK/ SS010#/CTS010#/ RTS010#/DE010/ SSL00-A	SDHI_D1-A/ QIO1-A	IRQ12		TSCAP
H8		PC1	MTIOC3A/TCLKD	SCK5/SSLA2-A/ TXD011/SMOSI011/ SSDA011/TXDA011/ SSL02-A		IRQ12		TS15

1.6.7 64-Pin LFQFP

Table 1.11 List of Pin and Pin Functions (64-Pin LFQFP) (1/3)

Pin No.			Timer	Communication				
64-Pin LFQFP	Power Supply Clock System Control	I/O Port	(MTU, TPU, TMR, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, Tamper detection)
1	AVCC1							
2	EMLE							
3	AVSS1							
4	VCL							
5	VBATT							
6	MD/FINED							
7	XCIN							
8	XCOUT							
9	RES#							
10	XTAL	P37						
11	VSS							
12	EXTAL	P36						
13	VCC							
14	UPSEL	P35				NMI		
15	TRST#	P34	MTIOC0A/TMCI3/ POE10#			IRQ4		TS0
16	TDI	P30	MTIOC4B/TMRI3/ RTCIC0/POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS		TAMPI0
17	TMS	P31	MTIOC4D/TMCI2/ RTCIC1	CTS1#/RTS1#/ SS1#/SSLB0-A		IRQ1-DS		TAMPI1
18	TDO	P26	MTIOC2A/TMO1	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ MOSIB-A		IRQ6		TS3
19	TCK	P27	MTIOC2B/TMCI3	SCK1/RSPCKB-A		IRQ7		TS2
20		P17	MTIOC3A/ MTIOC3B/ MTIOC4B/TIOCB0/ TCLKD/TMO1/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/SSITXD0	SDHI_D3-C	IRQ7	ADTRG1#	
21		P16	MTIOC3C/ MTIOC3D/TIOCB1/ TCLKC/TMO2/ RTCOUT	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ SCL2-DS/ USB0_VBUS		IRQ6	ADTRG0#	
22		P13	MTIOC0B/TIOCA5/ TMO3	TXD2/SMOSI2/ SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]		IRQ3	ADTRG1#	
23		P12	TMCI1/MTIC5U	RXD2/SMISO2/ SSCL2/SCL0[FM+]/ SCLHS0[FM+/HS]		IRQ2		
24	VCC_USB							
25		PH2	TMRI0	USB0_DM		IRQ1		
26		PH1	TMO0	USB0_DP		IRQ0		
27	VSS_USB							
28		P53		SSIRXD0/PMC0-DS		IRQ3		TS12

Table 1.11 List of Pin and Pin Functions (64-Pin LFQFP) (2/3)

Pin No.	Power Supply Clock System Control	I/O Port	Timer	Communication		Interrupt	A/D	Others
64-Pin LFQFP			(MTU, TPU, TMR, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, USB, SSIE, REMC)	(QSPIX, SDHI)			(CTSU, Tamper detection)
29	UB	PC7	MTIOC3A/ MTCLKB/TMO2/ TOC0/CACREF	TXD8/SMOSI8/ SSDA8/SMOSI10/ SSDA10/TXD10/ MISOA-A/SSITXD0/ SMOSI010/ SSDA010/TXD010/ MISO0-A		IRQ14		
30		PC6	MTIOC3C/ MTCLKA/TMCI2/ TIC0	RXD8/SMISO8/ SSCL8/SMISO10/ SSCL10/RXD10/ MOSIA-A/ SMISO010/ SSCL010/RXD010/ MOSI0-A/SSILRCK0		IRQ13		TS13
31		PC5	MTIOC3B/ MTCLKD/TMRI2	SCK8/SCK10/ RSPCKA-A/ SSIBCK0/SCK010/ RSPCK0-A		IRQ5		TS14
32		PC4	MTIOC3D/ MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/ RTS8#/SS8#/SS10#/ CTS10#/RTS10#/ SSLA0-A/ AUDIO_CLK/ SS010#/CTS010#/ RTS010#/DE010/ SSL00-A	SDHI_D1-A/ QIO1-A	IRQ12		TSCAP
33		PC1	MTIOC3A/TCLKD	SCK5/SSLA2-A/ TXD011/SMOSI011/ SSDA011/TXDA011/ SSL02-A		IRQ12		TS15
34		PC0	MTIOC3C/TCLKC	CTS5#/RTS5#/ SS5#/SSLA1-A/ RXD011/SMISO011/ SSCL011/SSL01-A		IRQ14		TS16
35		PB7	MTIOC3B/TIOCB5	TXD9/SMOSI9/ SSDA9/SMOSI11/ SSDA11/TXD11/ SMOSI011/ SSDA011/TXD011		IRQ15		
36		PB6	MTIOC3D/TIOCA5	RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11/ SMISO011/ SSCL011/RXD011		IRQ6		
37		PB5	MTIOC2A/ MTIOC1B/TIOCB4/ TMRI1/POE4#	SCK9/SCK11/ SCK011		IRQ13		
38	VCC							
39	VSS							
40		PA7	TIOCB2	MISOA-B/MISO0-B		IRQ7		
41		PA6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/ POE10#	CTS5#/RTS5#/ SS5#/MOSIA-B/ MOSI0-B/CTS12#/ RTS12#/SS12#		IRQ14		

Table 1.11 List of Pin and Pin Functions (64-Pin LFQFP) (3/3)

Pin No.			Timer	Communication				
64-Pin LFQFP	Power Supply Clock System Control	I/O Port	(MTU, TPU, TMR, RTC, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, USB, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU, Tamper detection)
42		PA4	MTIC5U/MTCLKA/ TIOCA1/TMRI0	TXD5/SMOSI5/ SSDA5/SSLA0-B/ SSL00-B/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12		IRQ5-DS		
43		PA2	MTIOC7A	RXD5/SMISO5/ SSCL5/SSLA3-B/ SSL03-B/RXD12/ SMISO12/SSCL12/ RXDX12	SDHI_WP	IRQ10		
44		PA1	MTIOC0B/ MTCLKC/ MTIOC7B/TIOCB0	SCK5/SSLA2-B/ SSL02-B/SCK12	SDHI_CD	IRQ11		
45		PE7	MTIOC6A/TOC1	MISOB-B	SDHI_WP/ SDHI_D1-B/ QIO1-B	IRQ7		
46		PE6	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/ SDHI_D0-B/ QIO0-B	IRQ6		
47		PE2	MTIOC4A/TIC3	RXD12/SMISO12/ SSCL12/RXDX12/ SSLB3-B		IRQ7-DS		
48		PE1	MTIOC4C/ MTIOC3B	TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/SSLB2-B		IRQ9	ANEX1	
49		PE0	MTIOC3D	SCK12/SSLB1-B		IRQ8	ANEX0	
50		PD7	MTIC5U/POE0#		SDHI_D1-B/ QIO1-B	IRQ7	AN100	
51		PD6	MTIC5V/MTIOC8A/ POE4#		SDHI_D0-B/ QIO0-B	IRQ6	AN101	
52		PD5	MTIC5W/ MTIOC8C/POE10#		SDHI_CLK-B/ QSPCLK-B	IRQ5	AN102	
53		PD4	MTIOC8B/POE11#		SDHI_CMD-B/ QSSL-B	IRQ4	AN103	
54		PD3	MTIOC8D/POE8#/ TOC2		SDHI_D3-B/ QIO3-B	IRQ3	AN104	
55		PD2	MTIOC4D/TIC2		SDHI_D2-B/ QIO2-B	IRQ2	AN105	
56		P43				IRQ11-DS	AN003	
57		P42				IRQ10-DS	AN002	
58		P41				IRQ9-DS	AN001	
59	VREFL0							
60		P40				IRQ8-DS	AN000	
61	VREFH0							
62	AVCC0							
63	AVSS0							
64		P05				IRQ13		

1.6.8 48-Pin HWQFN

Table 1.12 List of Pin and Pin Functions (48-Pin HWQFN) (1/3)

Pin No.			Timer	Communication				
48-Pin HWQFN	Power Supply Clock System Control	I/O Port	(MTU, TPU, TMR, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU)
1	EMLE							
2	MD/FINED							
3	RES#							
4	XTAL	P37						
5	VSS							
6	EXTAL	P36						
7	VCC							
8	UPSEL	P35				NMI		
9	TRST#	P34	MTIOC0A/TMCI3/ POE10#			IRQ4		TS0
10	TMS	P31	MTIOC4D/TMCI2	CTS1#/RTS1#/ SS1#/SSLB0-A		IRQ1-DS		
11	TDI	P30	MTIOC4B/TMRI3/ POE8#	RXD1/SMISO1/ SSCL1/MISOB-A		IRQ0-DS		
12	TCK	P27	MTIOC2B/TMCI3	SCK1/RSPCKB-A		IRQ7		TS2
13	TDO	P26	MTIOC2A/TMO1	TXD1/CTS3#/ RTS3#/SMOSI1/ SS3#/SSDA1/ MOSIB-A		IRQ6		TS3
14		P17	MTIOC3A/ MTIOC3B/ MTIOC4B/TIOCB0/ TCLKD/TMO1/ POE8#	SCK1/TXD3/ SMOSI3/SSDA3/ SDA2-DS/SSITXD0	SDHI_D3-C	IRQ7	ADTRG1#	
15		P16	MTIOC3C/ MTIOC3D/TIOCB1/ TCLKC/TMO2	TXD1/RXD3/ SMOSI1/SMISO3/ SSDA1/SSCL3/ SCL2-DS		IRQ6	ADTRG0#	
16		P13	MTIOC0B/TIOCA5/ TMO3	TXD2/SMOSI2/ SSDA2/SDA0[FM+]/ SDAHS0[FM+/HS]		IRQ3	ADTRG1#	
17		P12	TMCI1/MTIC5U	RXD2/SMISO2/ SSCL2/SCL0[FM+]/ SCLHS0[FM+/HS]		IRQ2		
18	VCC							
19	VSS							
20		P53		SSIRXD0/PMC0-DS		IRQ3		TS12
21	UB	PC7	MTIOC3A/ MTCLKB/TMO2/ TOC0/CACREF	TXD8/SMOSI8/ SSDA8/SMOSI10/ SSDA10/TXD10/ MISOA-A/SSITXD0/ SMOSI010/ SSDA010/TXD010/ MISO0-A		IRQ14		
22		PC6	MTIOC3C/ MTCLKA/TMCI2/ TIC0	RXD8/SMISO8/ SSCL8/SMISO10/ SSCL10/RXD10/ MOSIA-A/ SSILRCK0/ SMISO010/ SSCL010/RXD010/ MOSI0-A		IRQ13		TS13

Table 1.12 List of Pin and Pin Functions (48-Pin HWQFN) (2/3)

Pin No.			Timer	Communication				
48-Pin HWQFN	Power Supply Clock System Control	I/O Port	(MTU, TPU, TMR, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU)
23		PC5	MTIOC3B/ MTCLKD/TMRI2	SCK8/SCK10/ RSPCKA-A/ SSIBCK0/SCK010/ RSPCK0-A		IRQ5		TS14
24		PC4	MTIOC3D/ MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/ RTS8#/SS8#/SS10#/ CTS10#/RTS10#/ SSLA0-A/ AUDIO_CLK/ SS010#/CTS010#/ RTS010#/DE010/ SSL00-A	SDHI_D1-A/ QIO1-A	IRQ12		TSCAP
25		PB7	MTIOC3B/TIOCB5	TXD9/SMOSI9/ SSDA9/SMOSI11/ SSDA11/TXD11/ SMOSI011/ SSDA011/TXD011		IRQ15		
26		PB6	MTIOC3D/TIOCA5	RXD9/SMISO9/ SSCL9/SMISO11/ SSCL11/RXD11/ SMISO011/ SSCL011/RXD011		IRQ6		
27		PB5	MTIOC2A/ MTIOC1B/TIOCB4/ TMRI1/POE4#	SCK9/SCK11/ SCK011		IRQ13		
28	VCC							
29	VSS							
30	VCL							
31		PA6	MTIC5V/MTCLKB/ TIOCA2/TMCI3/ POE10#	CTS5#/RTS5#/ SS5#/MOSIA-B/ MOSI0-B/CTS12#/ RTS12#/SS12#		IRQ14		
32		PA4	MTIC5U/MTCLKA/ TIOCA1/TMRI0	TXD5/SMOSI5/ SSDA5/SSLA0-B/ SSL00-B/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12		IRQ5-DS		
33		PA2	MTIOC7A	RXD5/SMISO5/ SSCL5/SSLA3-B/ SSL03-B/RXD12/ SMISO12/SSCL12/ RXDX12	SDHI_WP	IRQ10		
34		PA1	MTIOC0B/ MTCLKC/ MTIOC7B/TIOCB0	SCK5/SSLA2-B/ SSL02-B/SCK12	SDHI_CD	IRQ11		
35		PE7	MTIOC6A/TOC1	MISOB-B	SDHI_WP/ SDHI_D1-B/ QIO1-B	IRQ7		
36		PE6	MTIOC6C/TIC1	MOSIB-B	SDHI_CD/ SDHI_D0-B/ QIO0-B	IRQ6		
37		PD5	MTIC5W/ MTIOC8C/POE10#		SDHI_CLK-B/ QSPCLK-B	IRQ5	AN102	
38		PD4	MTIOC8B/POE11#		SDHI_CMD-B/ QSSL-B	IRQ4	AN103	
39		PD3	MTIOC8D/POE8#/ TOC2		SDHI_D3-B/ QIO3-B	IRQ3	AN104	

Table 1.12 List of Pin and Pin Functions (48-Pin HWQFN) (3/3)

Pin No.			Timer	Communication				
48-Pin HWQFN	Power Supply Clock System Control	I/O Port	(MTU, TPU, TMR, CMTW, POE, CAC)	(SCI, RSCI, RSPI, RSPIA, RIIC, RIICHS, SSIE, REMC)	(QSPIX, SDHI)	Interrupt	A/D	Others (CTSU)
40		PD2	MTIOC4D/TIC2		SDHI_D2-B/ QIO2-B	IRQ2	AN105	
41		P43				IRQ11-DS	AN003	
42		P42				IRQ10-DS	AN002	
43		P41				IRQ9-DS	AN001	
44	VREFL0							
45		P40				IRQ8-DS	AN000	
46	VREFH0							
47	AVCC0/ AVCC1							
48	AVSS0/AVSS1							

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2.1 Absolute Maximum Rating

Conditions: VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	–0.3 to +4.0	V
V_{BATT} power supply voltage		V_{BATT}	–0.3 to +4.0	V
Analog power supply voltage		AVCC0, AVCC1*1	–0.3 to +4.0	V
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3 (up to 4.0)	V
Input voltage	Ports for 5 V tolerant: P12 to P17, P20, P21, P30 to P33, P67, P73, PC0 to PC3, and PJ3	V_{in}	–0.3 to VCC + 4.0 (up to 5.8)	V
	TAMPI0 to TAMPI2, RTCIC0 to RTCIC2, EXCIN*2		–0.3 to +4.0	
	Port for 5 V tolerant: P07		–0.3 to AVCC0 + 4.0 (up to 5.8)	
	P03, P05, P40 to P47		–0.3 to AVCC0 + 0.3 (up to 4.0)	
	Other than above		–0.3 to VCC + 0.3 (up to 4.0)	
Junction temperature		T_j	–40 to +125	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Connect the AVCC0, AVCC1, and VCC_USB pins to VCC, and the AVSS0, AVSS1, and VSS_USB pins to VSS. When the A/D converter unit 0 is not to be used, connect the VREFH0 pin to VCC and the VREFL0 pin to VSS, respectively. Do not leave these pins open. Insert capacitors of high frequency characteristics between the AVCC0 and AVSS0 pins, or AVCC1 and AVSS1 pins. Place capacitors of about 0.1 µF as close as possible to every power supply pin and use the shortest and heaviest possible traces.

Note 2. The listed values apply when pins P30, P31, and P32 are set for the TAMPIn or RTCICn (n = 0 to 2) functions, and pin PJ3 is set for the EXCIN function.

2.2 Recommended Operating Conditions

Table 2.2 Recommended Operating Conditions (1)

Item		Symbol	Min.	Typ.	Max.	Unit
Power supply voltage*1		VCC	2.7	—	3.6	V
		VSS	—	0	—	
V_{BATT} power supply voltage		V_{BATT}	1.62*2	—	3.6	V
USB power supply voltage		VCC_USB	—	VCC	—	V
		VSS_USB	—	0	—	
Analog power supply voltage*1, *3		AVCC0	—	VCC	—	V
		AVSS0	—	0	—	
		AVCC1	—	VCC	—	
		AVSS1	—	0	—	
		VREFH0	2.7	—	AVCC0	
		VREFL0	—	0	—	
Input voltage	Ports for 5 V tolerant: P12 to P17, P20, P21, P30 to P33, P67, P73, PC0 to PC3, and PJ3	V_{in}	–0.3	—	VCC + 3.6 (up to 5.5)	V
	TAMPI0 to TAMPI2, RTCIC0 to RTCIC2, EXCIN*4		–0.3	—	3.9	
	SCLHS0, SDAHS0*5		–0.3	—	VCC + 0.3	
	Port for 5 V tolerant: P07		–0.3	—	AVCC0 + 3.6 (up to 5.5)	
	P03, P05, P40 to P47		–0.3	—	AVCC0 + 0.3	
	Other than above		–0.3	—	VCC + 0.3	
Operating temperature	D version	T_{opr}	–40	—	85	°C
	G version		–40	—	105	
Junction temperature	D version	T_j	–40	—	105	°C
	G version		–40	—	125	

Note 1. Comply with the following potential condition: VCC = AVCC0 = AVCC1 = VCC_USB
Note 2. The low CL crystal unit cannot be used when the V_{BATT} voltage is less than 2.0 V.
Note 3. For details, see section 50.6.11, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.
Note 4. The listed values apply when pins P30, P31, and P32 are set for the TAMPIn or RTCICn (n = 0 to 2) functions, and pin PJ3 is set for the EXCIN function.
Note 5. The listed values apply when pins P12 and P13 are respectively set for the SCLHS0 and SDAHS0 functions in Hs-mode of the RIICHS.

Table 2.3 Recommended Operating Conditions (2)

Item	Symbol	Value
Decoupling capacitance for stabilizing the internal voltage	C_{VCL}	0.22 µF ± 30%*1

Note 1. Use a multilayer ceramic capacitor with a nominal capacitance of 0.22 µF, for which the sum of the capacitance tolerance and change in the capacitance under the usage conditions will be no greater than ±30%.

2.3 DC Characteristics

Table 2.4 DC Characteristics (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	IRQ input pin*1 MTU input pin*1 POE3 input pin*1 TPU input pin*1 TMR input pin*1 CMTW input pin*1 SCI input pin*1 RSCIA input pin*1 CAN input pin*1 CAC input pin*1 ADTRG# input pin*1 QSPIX input pin*1 SSIE input pin*1 REMC input pin*1 RES#, NMI, TCK	V_{IH}	0.8 × VCC	—	—	V	
		V_{IL}	—	—	0.2 × VCC		
		ΔV_T	0.06 × VCC	—	—		
	RIIC input pin RIICHS input pin (except for SMBus)	V_{IH}	0.7 × VCC	—	—		
		V_{IL}	—	—	0.3 × VCC		
		ΔV_T	0.05 × VCC	—	—		
	TAMPIn/RTCICn pin EXCIN pin	V_{IH}	0.8 × V_{BKP}	—	—		
		V_{IL}	—	—	0.2 × V_{BKP}		
	Ports for 5 V tolerant*2	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
	Other input pins excluding ports for 5 V tolerant	V_{IH}	0.8 × VCC	—	—		
		V_{IL}	—	—	0.2 × VCC		
High level input voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IH}	0.9 × VCC	—	—	V	
	EXTAL, RSPI input pin, RSPIA input pin, EXDMAC input pin, WAIT#, SDHI input pin		0.8 × VCC	—	—		
	D0 to D15		0.7 × VCC	—	—		
	RIIC, RIICHS (SMBus)		2.1	—	—		
Low level input voltage (except for Schmitt trigger input pin)	MD pin, EMLE	V_{IL}	—	—	0.1 × VCC	V	
	EXTAL, RSPI input pin, RSPIA input pin, EXDMAC input pin, WAIT#, SDHI input pin		—	—	0.2 × VCC		
	D0 to D15		—	—	0.3 × VCC		
	RIIC, RIICHS (SMBus)		—	—	0.8		

Note 1. This does not include the pins, which are multiplexed as ports for 5 V tolerant.
Note 2. P07, P12 to P17, P20, P21, P30 to P33, P67, P73, PC0 to PC3, and PJ3 are 5 V tolerant.

Table 2.5 DC Characteristics (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	All output pins	V_{OH}	VCC – 0.5	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins (except for RIIC0 to RIIC2 pins and RIICHS0 pin)	V_{OL}	—	—	0.5	V	I_{OL} = 1.0 mA
	RIIC0 to RIIC2 output pin RIICHS0 output pin		—	—	0.4		I_{OL} = 3.0 mA
			—	—	0.6		I_{OL} = 6.0 mA
	RIIC0 output pin RIICHS0 output pin		—	—	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			—	0.4	—		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	RIICHS0 output pin		—	—	0.4		I_{OL} = 3.0 mA (ICFER.HSME = 1)
Input leakage current	RES#, MD pin, EMLE*1, BSCANP*1, NMI	| I_{in} |	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	Other than ports for 5 V tolerant	| I_{TSI} |	—	—	1.0	µA	V_{in} = 0 V V_{in} = VCC
	Ports for 5 V tolerant		—	—	5.0		V_{in} = 0 V V_{in} = 5.5 V
Input pull-up resistor	Other than P35	R_{PU}	10	—	100	kΩ	V_{in} = 0 V
Input pull-down resistor	EMLE, BSCANP	R_{PD}	10	—	100	kΩ	V_{in} = VCC
Pull-up current serving as the SCLHS0 current source	SCLHS0 pin (P12)	I_{CS}	3	—	12	mA	VCC = 3.0 to 3.6 V V_{in} = 0.3 × VCC to 0.7 × VCC
Input capacitance	All input pins (except for P12, P13, P16, P17, P20, P21, EMLE, BSCANP, USB0_DP, USB0_DM, USB1_DP and USB1_DM)	C_{in}	—	—	8	pF	Vbias = 0 V Vamp = 20 mV f = 1 MHz T_a = 25°C
	P12, P13, P16, P17, P20, P21, EMLE, BSCANP, USB0_DP, USB0_DM, USB1_DP and USB1_DM		—	—	16		
Power supply voltage in the backup domain		V_{BKP}	—	VCC	—	V	VCC ≥ $V_{DETBATT}$
			—	VBATT	—		VCC < $V_{DETBATT}$
Output voltage of the VCL pin		V_{CL}	—	1.18	—	V	

Note 1. The input leakage current value at the EMLE and BSCANP pins are only when V_{in} = 0 V.

Table 2.6 DC Characteristics (3)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item				Symbol	D version		G version		Unit	Test Conditions
					Typ.	Max.	Typ.	Max.		
Supply current*1	High-speed operating mode	Full operation*2		I_{CC}*3	—	55	—	68	mA	ICLK = 120 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 60 MHz, PCLKD = 60 MHz, FCLK = 60 MHz, BCLK = 120 MHz, BCLK pin = 60 MHz
		Normal operation	Peripheral module clocks are supplied *4		23	—	23	—		
			Peripheral module clocks are stopped *4, *5		13	—	13	—		
		Core Mark	Peripheral module clocks are stopped *4, *5		14.5	—	14.5	—		
		Sleep mode: Peripheral module clocks are supplied*4			20	38	20	51		
		All module clock stop mode (reference value)			9	26	9	39		
		Increased by BGO operation*8	Reading from the code flash memory while the data flash memory is being programmed		6	—	6	—		
			Reading from the code flash memory while the code flash memory is being programmed		7	—	7	—		
		Increased by Trusted Secure IP operation			—	15	—	15		
	Low-speed operating mode 1: Peripheral module clocks are stopped*4				1.6	—	1.6	—		All clocks 1 MHz
	Low-speed operating mode 2: Peripheral module clocks are stopped*4				1.6	—	1.6	—		All clocks 32.768 kHz
	Software standby mode				1.1	18	1.1	27		
	Deep software standby mode	Power is supplied to the standby RAM, USB resume detecting unit (USB0 only) and REMC			15.5	69	15.5	85	μA	
		Power is not supplied to the standby RAM, USB resume detecting unit (USB0 only) and REMC	Low power consumption function of the power-on reset circuit is disabled*6		11.5	42	11.5	54		
			Low power consumption function of the power-on reset circuit is enabled*7		4.9	32	4.9	47		
		Increase current by operating RTC	Drive capacity for low CL is set in RCR3.RTCDV[2:0].		1	—	1	—		
			Drive capacity for standard CL is set in RCR3.RTCDV[2:0].		2	—	2	—		
		Increase current by operating REMC	External clock (32 kHz) input		0.1	—	0.1	—		
			Drive capacity for standard CL is set in RCR3.RTCDV[2:0].		1.4	—	1.4	—		
	When the RTC is operating while VCC is not supplied (Only the RTC and sub-clock oscillator operate with the battery backup function)		Drive capacity for low CL is set in RCR3.RTCDV[2:0].		0.9	—	0.9	—		V_{BATT} = 2.0 V, VCC = 0 V
					1.6	—	1.6	—		V_{BATT} = 3.3 V, VCC = 0 V
			Drive capacity for standard CL is set in RCR3.RTCDV[2:0].		1.6	—	1.6	—		V_{BATT} = 1.62 V, VCC = 0 V
					1.7	—	1.7	—		V_{BATT} = 2.0 V, VCC = 0 V
					3.3	—	3.3	—		V_{BATT} = 3.3 V, VCC = 0 V
	Inrush current on release from deep software standby mode		Inrush current*9	I_{RUSH}	—	130	—	130	mA	
			Total inrush current*9	E_{RUSH}	—	1	—	1	μC	

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.

Note 2. Peripheral module clocks are supplied.
Note 3. I_{CC} depends on the f (ICLK) as follows (when ICLK/PCLKA : PCLKB/PCLKC/PCLKD : BCLK : BCLK pin = 2 : 1 : 2 : 1 and EXTAL = 12 MHz).
- D version
  I_{CC} max = 0.28 × f + 21.0 (full operation in high-speed operating mode)
  I_{CC} typ = 0.16 × f + 3.5 (normal operation in high-speed operating mode)
  I_{CC} typ = 0.20 × f + 1.4 (ICLK 1 MHz max) (low-speed operating mode 1)
  I_{CC} max = 0.14 × f + 21.0 (sleep mode)
- G version
  I_{CC} max = 0.31 × f + 30.0 (full operation in high-speed operating mode)
  I_{CC} typ = 0.16 × f + 3.5 (normal operation in high-speed operating mode)
  I_{CC} typ = 0.20 × f + 1.4 (ICLK 1 MHz max) (low-speed operating mode 1)
  I_{CC} max = 0.17 × f + 30.0 (sleep mode)

Note 4. Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.
Note 5. When the peripheral module clock is stopped, the settings of the clock frequency are as follows:
ICLK = 120 MHz and PCLKA = PCLKB = PCLKC = PCLKD = FCLK = BCLK = BCLK pin = 3.75 MHz (divided by 64).
Note 6. When the low power consumption function is disabled, the DEEPCUT[1:0] bits are set to 01b.
Note 7. When the low power consumption function is enabled, the DEEPCUT[1:0] bits are set to 11b.
Note 8. These are the increases during programming of the code flash memory after the code flash memory (limitations apply to the combinations of address ranges of the program area and the readable area) or the data flash memory has been programmed or erased.
Note 9. Reference value

Table 2.7 DC Characteristics (4)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	D version			G version			Unit	Test Conditions
				Min.	Typ.	Max.	Min.	Typ.	Max.		
Analog power supply current*1, *2	During 12-bit A/D conversion (unit 0)		I_{AVCC0}	—	0.8	1	—	0.8	1	mA	
	During 12-bit A/D conversion (unit 1)		I_{AVCC1}	—	0.6	1	—	0.6	1	mA	
	During 12-bit A/D conversion (unit 1) + temperature sensor			—	0.7	1.1	—	0.7	1.1		
	Waiting for A/D and temperature sensor conversion (all units)		I_{AVCC}	—	0.9	1.4	—	0.9	1.4	mA	$I_{AVCC} = I_{AVCC0} + I_{AVCC1}$
	A/D and temperature sensor are in standby mode (all units)			—	1.4	6.7	—	1.4	9.0	µA	
Reference power supply current	During 12-bit A/D conversion (unit 0)		I_{VREFH0}	—	38	60	—	38	60	µA	
	Waiting for 12-bit A/D conversion (unit 0)			—	0.07	0.5	—	0.07	0.6		
	12-bit A/D converter in module stop status (unit 0)			—	0.07	0.4	—	0.07	0.5		
USB operating current (increase per channel)		Low speed	$I_{CCUSBLS}$	—	3.7	6.5	—	3.7	6.5	mA	
		Full speed	$I_{CCUSBFS}$	—	4.2	10	—	4.2	10	mA	
CTSU operating current			I_{CTSU}	—	100	—	—	100	—	µA	
RAM retension voltage			V_{RAM}	2.7	—	—	2.7	—	—	V	
VCC rising gradient			SrVCC	8.4	—	20000	8.4	—	20000	µs/V	
VCC falling gradient*3			SfVCC	8.4	—	—	8.4	—	—	µs/V	

Note 1. The reference power supply current is included in the power supply current value for 12-bit A/D converter (unit 1).
Note 2. The analog power supply current cannot be separated into I_{AVCC0} and I_{AVCC1} in the 48-pin products because AVCC0 and AVCC1 share the same pin.
Note 3. This applies when V_{BATT} is used.

Table 2.8 Permissible Output Currents

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (average value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	2.0	mA
	All output pins*2	High drive		—	—	3.8	
	All output pins*3	High-speed interface high-drive		—	—	7.5	
Permissible output low current (max. value per pin)	All output pins*1	Normal drive	I_{OL}	—	—	4.0	mA
	All output pins*2	High drive		—	—	7.6	
	All output pins*3	High-speed interface high-drive		—	—	15	
Permissible output low current (total)	Total of all output pins		ΣI_{OL}	—	—	80	mA
Permissible output high current (average value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–2.0	mA
	All output pins*2	High drive		—	—	–3.8	
	All output pins*3	High-speed interface high-drive		—	—	–7.5	
Permissible output high current (max. value per pin)	All output pins*1	Normal drive	I_{OH}	—	—	–4.0	mA
	All output pins*2	High drive		—	—	–7.6	
	All output pins*3	High-speed interface high-drive		—	—	–15	
Permissible output high current (total)	Total of all output pins		ΣI_{OH}	—	—	–80	mA

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Note 3. This is the value when high-speed interface high-driving ability is set with a pin for which high-speed interface high-driving ability is selectable.

Table 2.9 Normal Output Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V, T_a = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high level voltage	Normal drive (P00 to P02, P12 to P14, P27, P36, P40 to P47, P50 to P52, P54 to P56, P72, P74 to P77, P80 to P83, P90 to P93, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PH1, PH2)	V_{OH}	—	3.26	—	V	I_{OH} = –0.5 mA
			—	3.22	—		I_{OH} = –1.0 mA
			—	3.13	—		I_{OH} = –2.0 mA
			—	2.94	—		I_{OH} = –4.0 mA
	High drive (P00 to P02, P03, P05, P07, P12 to P17, P20 to P27, P30 to P34, P37, P50 to P56, P60 to P67, P70 to P77, P80 to P83, P86, P87, P90 to P93, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF5, PH1, PH2, PJ3, PJ5)		—	3.28	—		I_{OH} = –0.5 mA
			—	3.25	—		I_{OH} = –1.0 mA
			—	3.20	—		I_{OH} = –2.0 mA
			—	3.10	—		I_{OH} = –4.0 mA
	Highs-peed interface high-drive (P00 to P02, P12 to P14, P17, P20 to P23, P27, P30, P31, P50 to P56, P70, P72, P73 to P77, P80 to P83, P86, P87, P90 to P93, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PH1, PH2)		—	3.29	—		I_{OH} = –0.5 mA
			—	3.28	—		I_{OH} = –1.0 mA
			—	3.25	—		I_{OH} = –2.0 mA
			—	3.20	—		I_{OH} = –4.0 mA
			—	3.18	—		I_{OH} = –5.0 mA
Output low level voltage	Normal drive (P00 to P02, P12 to P14, P27, P36, P40 to P47, P50 to P52, P54 to P56, P72, P74 to P77, P80 to P83, P90 to P93, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PH1, PH2)	V_{OL}	—	0.04	—		I_{OL} = 0.5 mA
			—	0.09	—		I_{OL} = 1.0 mA
			—	0.18	—		I_{OL} = 2.0 mA
			—	0.39	—		I_{OL} = 4.0 mA
	High drive (P00 to P02, P03, P05, P07, P12 to P17, P20 to P27, P30 to P34, P37, P50 to P56, P60 to P67, P70 to P77, P80 to P83, P86, P87, P90 to P93, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PF5, PH1, PH2, PJ3, PJ5)		—	0.02	—		I_{OL} = 0.5 mA
			—	0.04	—		I_{OL} = 1.0 mA
			—	0.09	—		I_{OL} = 2.0 mA
			—	0.18	—		I_{OL} = 4.0 mA
	Highs-peed interface high-drive (P00 to P02, P12 to P14, P17, P20 to P23, P27, P30, P31, P50 to P56, P70, P72, P73 to P77, P80 to P83, P86, P87, P90 to P93, PA0 to PA7, PB0 to PB7, PC0 to PC7, PD0 to PD7, PE0 to PE7, PH1, PH2)		—	0.01	—		I_{OL} = 0.5 mA
			—	0.02	—		I_{OL} = 1.0 mA
			—	0.04	—		I_{OL} = 2.0 mA
			—	0.09	—		I_{OL} = 4.0 mA
			—	0.11	—		I_{OL} = 5.0 mA
			—	0.23	—		I_{OL} = 10.0 mA
			—	0.36	—		I_{OL} = 15.0 mA

Table 2.10 Thermal Resistance Value (Reference)

Item	Package	Symbol	Max.	Unit	Test Conditions
Thermal resistance	144-pin LFQFP (PLQP0144KA-B)	θ_{ja}	48.4	°C/W	JESD51-2 and JESD51-7 compliant
	100-pin LFQFP (PLQP0100KB-B)		51.7		
	64-pin LFQFP (PLQP0064KB-C)		51.2		
	48-pin HWQFN (PWQN0048KC-A)		19.1*1		
	145-pin TFLGA (PTLG0145JC-A)		30.9		JESD51-2 and JESD51-9 compliant
	145-pin TFLGA (PTLG0145KB-A)		30.6		
	100-pin TFLGA (PTLG0100JB-A)		30.9		
	64-pin TFBGA (PTBG0064KB-A)		32.0		
	144-pin LFQFP (PLQP0144KA-B)	Ψ_{jt}	1.2	°C/W	JESD51-2 and JESD51-7 compliant
	100-pin LFQFP (PLQP0100KB-B)		1.2		
	64-pin LFQFP (PLQP0064KB-C)		1.2		
	48-pin HWQFN (PWQN0048KC-A)		0.1*1		
	145-pin TFLGA (PTLG0145JC-A)		0.4		JESD51-2 and JESD51-9 compliant
	145-pin TFLGA (PTLG0145KB-A)		0.4		
	100-pin TFLGA (PTLG0100JB-A)		0.4		
	64-pin TFBGA (PTBG0064KB-A)		0.4		

Note: The values are reference values when the 4-layer board is used. Thermal resistance depends on the number of layers or size of the board. For details, refer to the JEDEC standards.

Note 1. This value applies when the exposed die pad for this purpose is connected to VSS.

2.4 AC Characteristics

Table 2.11 Operating Frequency (High-Speed Operating Mode)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	—	—	120	MHz
	Peripheral module clock (PCLKA)			—	—	120	
	Peripheral module clock (PCLKB)			—	—	60	
	Peripheral module clock (PCLKC)			—	—	60	
	Peripheral module clock (PCLKD)			—	—	60	
	Flash-IF clock (FCLK)			—*1	—	60	
	External bus clock (BCLK)	Package of 144 pins or more		—	—	120	
		100-pin package		—	—	60	
	BCLK pin output	Package of 144 pins or more		—	—	60	
		100-pin package		—	—	30	
	SDRAM clock (SDCLK)	Package of 144 pins or more		—	—	60	
	SDCLK pin output	Package of 144 pins or more		—	—	60	

Note 1. The FCLK must run at a frequency of at least 4 MHz when changing the flash memory contents.

Table 2.12 Operating Frequency (Low-Speed Operating Mode 1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	—	—	1	MHz
	Peripheral module clock (PCLKA)			—	—	1	
	Peripheral module clock (PCLKB)			—	—	1	
	Peripheral module clock (PCLKC)*1			—	—	1	
	Peripheral module clock (PCLKD)*1			—	—	1	
	Flash-IF clock (FCLK)			—	—	1	
	External bus clock (BCLK)	Package of 144 pins or more		—	—	1	
		100-pin package		—	—	1	
	BCLK pin output	Package of 144 pins or more		—	—	1	
		100-pin package		—	—	1	
	SDRAM clock (SDCLK)	Package of 144 pins or more		—	—	1	
	SDCLK pin output	Package of 144 pins or more		—	—	1	

Note 1. When the 12-bit A/D converter is used, the frequency must be set to at least 1 MHz.

Table 2.13 Operating Frequency (Low-Speed Operating Mode 2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit
Operating frequency	System clock (ICLK)		f	32	—	264	kHz
	Peripheral module clock (PCLKA)			—	—	264	
	Peripheral module clock (PCLKB)			—	—	264	
	Peripheral module clock (PCLKC)*1			—	—	264	
	Peripheral module clock (PCLKD)*1			—	—	264	
	Flash-IF clock (FCLK)			32	—	264	
	External bus clock (BCLK)	Package of 144 pins or more		—	—	264	
		100-pin package		—	—	264	
	BCLK pin output	Package of 144 pins or more		—	—	264	
		100-pin package		—	—	264	
	SDRAM clock (SDCLK)	Package of 144 pins or more		—	—	264	
	SDCLK pin output	Package of 144 pins or more		—	—	264	

Note 1. The 12-bit A/D converter cannot be used.

2.4.1 Reset Timing

Table 2.14 Reset Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	Power-on	t_{RESWP}	1	—	—	ms	Figure 2.1
	Deep software standby mode	t_{RESWD}	0.6	—	—	ms	Figure 2.2
	Software standby mode, low-speed operating mode 2	t_{RESWS}	0.3	—	—	ms	
	Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory	t_{RESWF}	200	—	—	µs	
	Other than above	t_{RESW}	200	—	—	µs	
Waiting time after release from the RES# pin reset		t_{RESWT}	54	—	55	t_{Lcyc}	Figure 2.1
Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset)		t_{RESW2}	100	—	108	t_{Lcyc}	

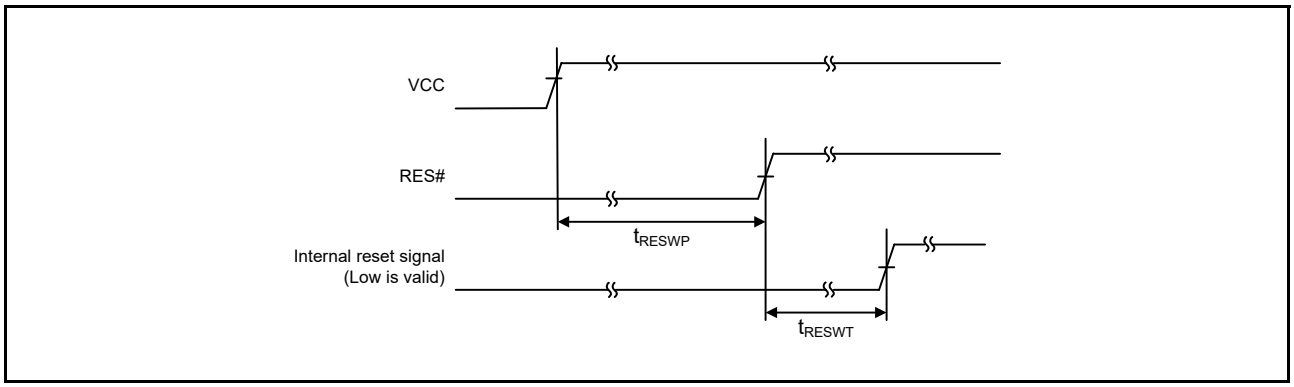


Figure 2.1 Reset Input Timing at Power-On

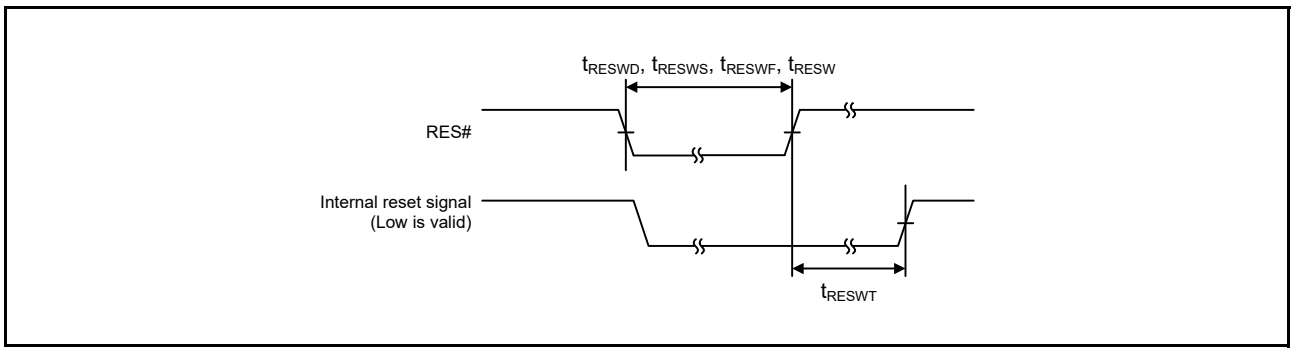


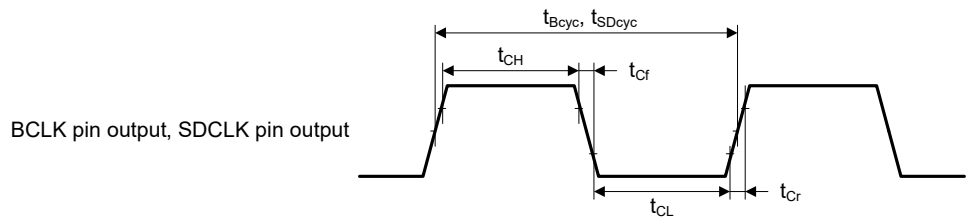
Figure 2.2 Reset Input Timing

2.4.2 Clock Timing

Table 2.15 BCLK Pin Output, SDCLK Pin Output Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BCLK pin output cycle time	Package of 144 pins or more	t_{Bcyc}	16.6	—	—	ns	Figure 2.3
	100-pin package		33.2	—	—		
BCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
BCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
BCLK pin output rising time		t_{Cr}	—	—	5	ns	
BCLK pin output falling time		t_{Cf}	—	—	5	ns	
SDCLK pin output cycle time	Package of 144 pins or more	t_{Bcyc}	16.6	—	—	ns	
SDCLK pin output high pulse width		t_{CH}	3.3	—	—	ns	
SDCLK pin output low pulse width		t_{CL}	3.3	—	—	ns	
SDCLK pin output rising time		t_{Cr}	—	—	5	ns	
SDCLK pin output falling time		t_{Cf}	—	—	5	ns	



Test conditions: V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, C = 30 pF

Figure 2.3 BCLK Pin and SDCLK Pin Output Timing

Table 2.16 EXTAL Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	f_{EXMAIN} ≤ 24MHz			f_{EXMAIN} > 24MHz			Unit	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
EXTAL external clock input cycle time	t_{EXcyc}	41.66	—	—	33.33	—	—	ns	Figure 2.4
EXTAL external clock input frequency	f_{EXMAIN}	—	—	24	—	—	30	MHz	
EXTAL external clock input high pulse width	t_{EXH}	15.83	—	—	13.33	—	—	ns	
EXTAL external clock input low pulse width	t_{EXL}	15.83	—	—	13.33	—	—	ns	
EXTAL external clock rising time	t_{EXr}	—	—	5	—	—	5	ns	
EXTAL external clock falling time	t_{EXf}	—	—	5	—	—	5	ns	

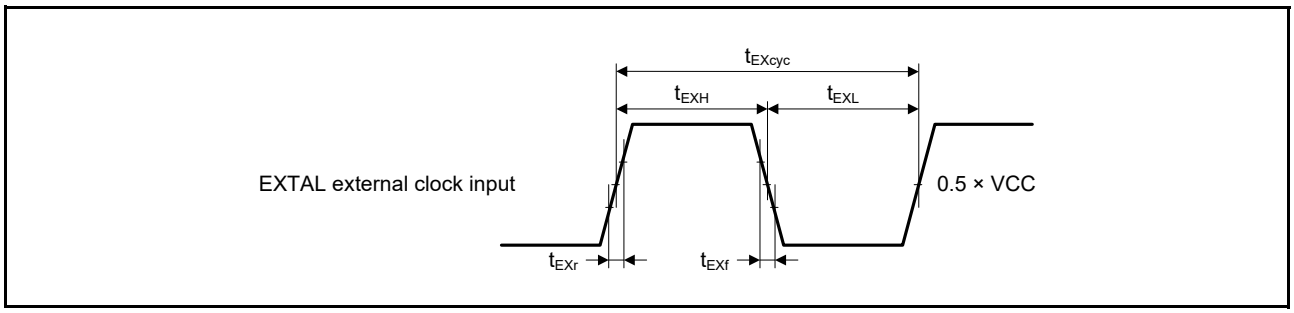


Figure 2.4 EXTAL External Clock Input Timing

Table 2.17 Main Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Main clock oscillation frequency	f_{MAIN}	8	—	24	MHz	
Main clock oscillator stabilization time (crystal)	$t_{MAINOSC}$	—	—	—*1	ms	Figure 2.5
Main clock oscillation stabilization waiting time (crystal)	$t_{MAINOSCWT}$	—	—	—*2	ms	

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization waiting time in accord with the formula below.
$t_{MAINOSCWT}$ = [(MSTS[7:0] bits × 32) + 10] / f_{LOCO}

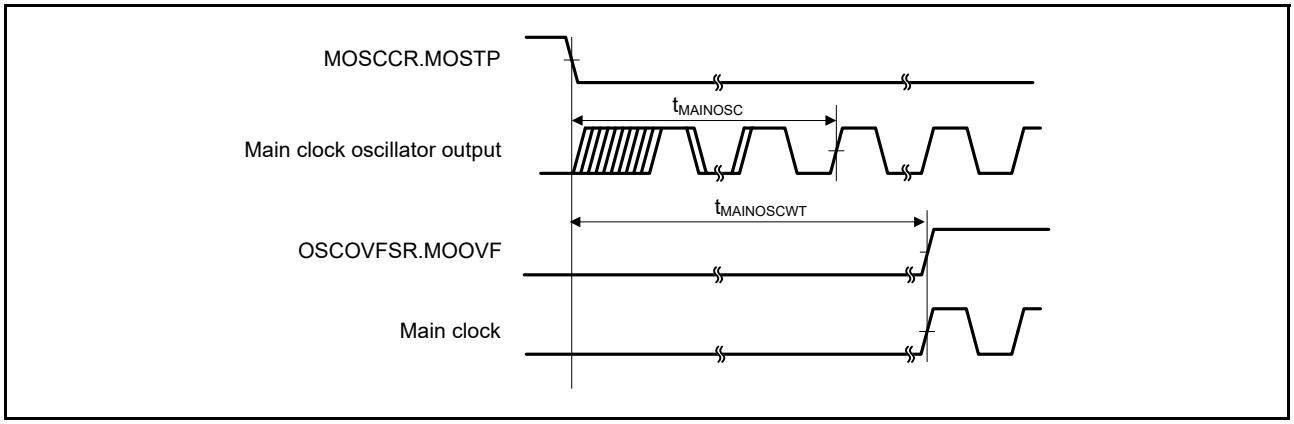


Figure 2.5 Main Clock Oscillation Start Timing

Table 2.18 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
LOCO clock cycle time	t_{Lcyc}	3.78	4.16	4.63	µs	
LOCO clock oscillation frequency	f_{LOCO}	216 (–10%)	240	264 (+10%)	kHz	
LOCO clock oscillation stabilization waiting time	t_{LOCOWT}	—	—	44	µs	Figure 2.6
IWDT-dedicated low-speed clock cycle time	t_{ILcyc}	7.57	8.33	9.26	µs	
IWDT-dedicated low-speed clock oscillation frequency	f_{ILOCO}	108 (–10%)	120	132 (+10%)	kHz	
IWDT-dedicated low-speed clock oscillation stabilization waiting time	$t_{ILOCOWT}$	—	142	190	µs	Figure 2.7

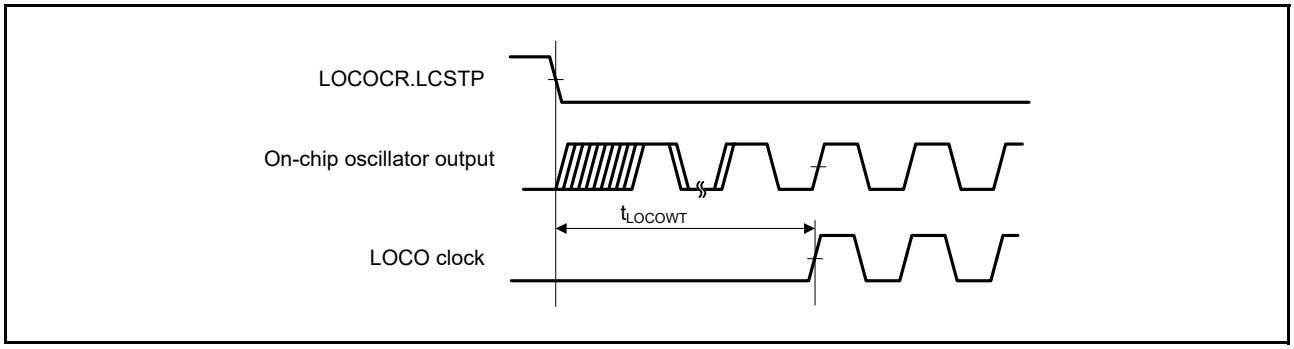


Figure 2.6 LOCO Clock Oscillation Start Timing

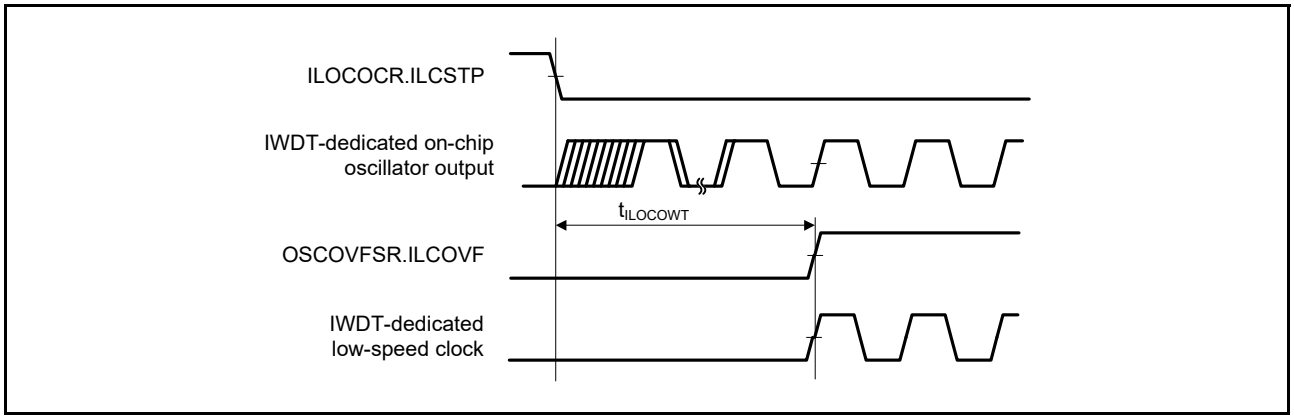


Figure 2.7 IWDT-dedicated Low-Speed Clock Oscillation Start Timing

Table 2.19 HOCO Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
HOCO clock oscillation frequency	FLL not in use	f_{HOCO}	15.616 (–2.40%)	16	16.384 (+2.40%)	MHz	–20°C ≤ T_a
			17.568 (–2.40%)	18	18.432 (+2.40%)		
			19.520 (–2.40%)	20	20.480 (+2.40%)		
			15.520 (–3.00%)	16	16.480 (+3.00%)		T_a < –20°C
			17.460 (–3.00%)	18	18.540 (+3.00%)		
			19.400 (–3.00%)	20	20.600 (+3.00%)		
	FLL in use	f_{HOCO}	15.960 (–0.25%)	16	16.040 (+0.25%)	MHz	Sub-clock frequency precision: ±50 ppm
			17.955 (–0.25%)	18	18.045 (+0.25%)		
			19.950 (–0.25%)	20	20.050 (+0.25%)		
HOCO clock oscillation stabilization waiting time		t_{HOCOWT}	—	105	149	μs	Figure 2.8
HOCO clock power supply stabilization time		t_{HOCOP}	—	—	150	μs	Figure 2.9
FLL stabilization waiting time		t_{FLLWT}	—	—	1.8	ms	

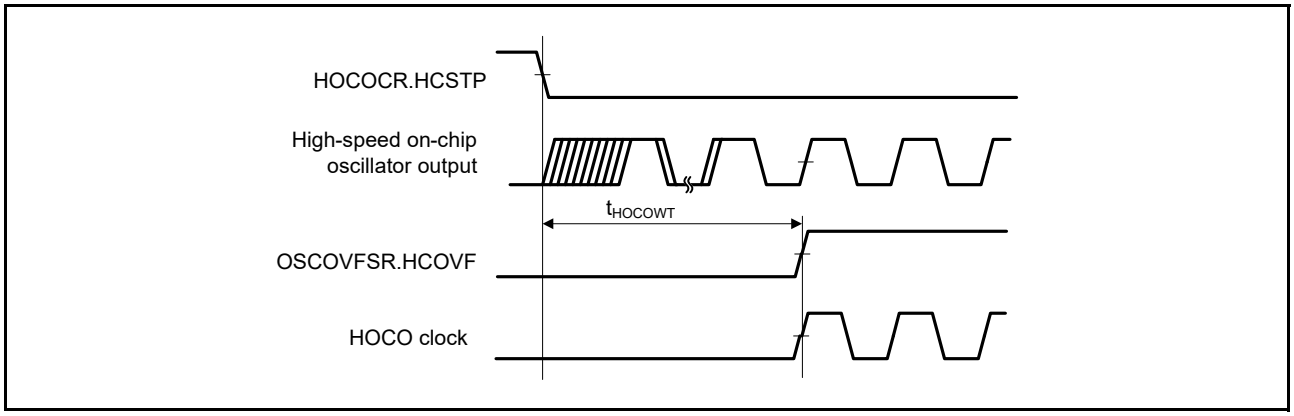


Figure 2.8 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCOCR.HCSTP Bit)

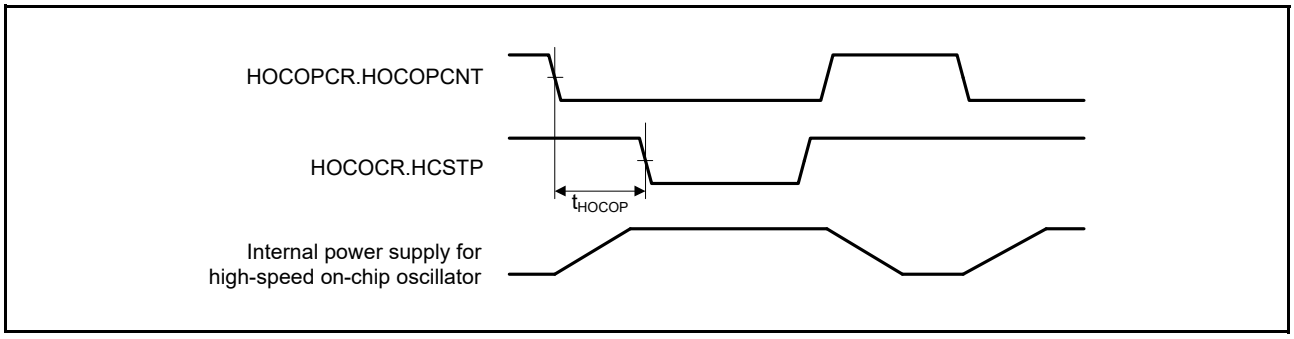


Figure 2.9 High-Speed On-Chip Oscillator Power Supply Control Timing

Table 2.20 PLL Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
PLL clock oscillation frequency	f_{PLL}	120	—	240	MHz	
PLL clock oscillation stabilization waiting time	t_{PLLWT}	—	259	320	µs	Figure 2.10

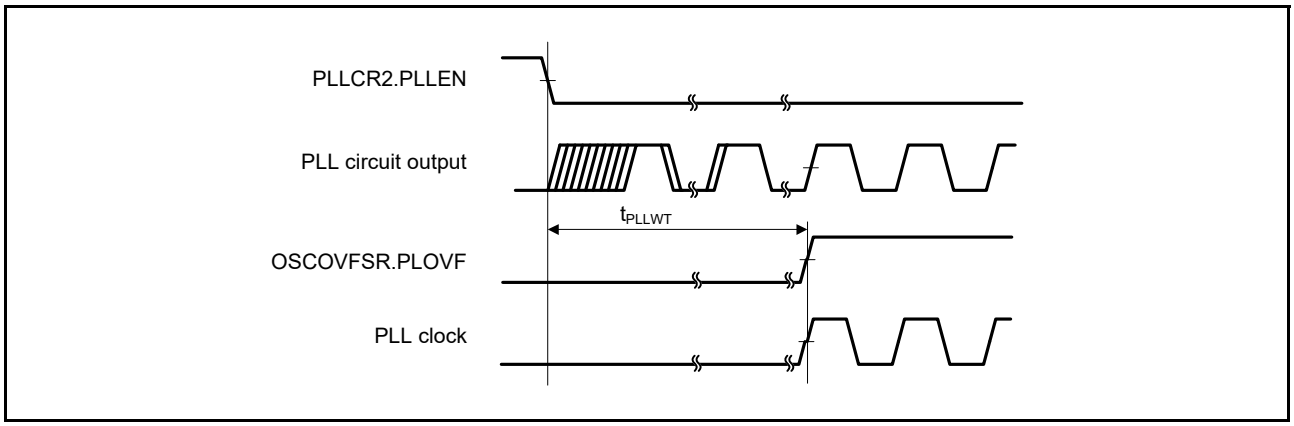


Figure 2.10 PLL Clock Oscillation Start Timing

Table 2.21 Sub-Clock Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
When a low C_L crystal resonator is in use: V_{BATT} = 2.0 to 3.6 V,
When a standard C_L crystal resonator is in use: V_{BATT} = 1.62 to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Sub-clock oscillation frequency	f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time	t_{SUBOSC}	—	—	*1	s	Figure 2.11
Sub-clock oscillation stabilization waiting time	$t_{SUBOSCWT}$	—	—	*2	s	

Note 1. When using a sub-clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the SOSCWTCR.SSTS[7:0] bits determines the sub-clock oscillation stabilization waiting time in accord with the formula below.
$t_{SUBOSCWT}$ = [(SSTS[7:0] bits × 16384) + 10] / f_{LOCO}

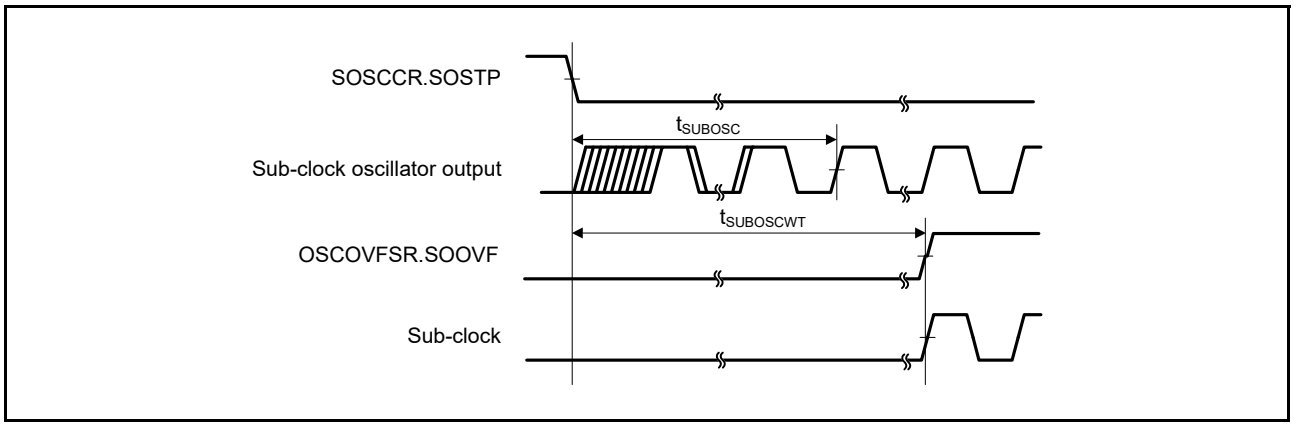


Figure 2.11 Sub-Clock Oscillation Start Timing

Table 2.22 CLKOUT Pin Output Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$,
High-drive output is selected by the drive capacity control register

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CLKOUT pin output cycle time	t_{Ccyc}	25	—	—	ns	Figure 2.12 t_{Ccyc} = 25 ns
CLKOUT pin output high pulse width*1	t_{CH}	5	—	—	ns	
CLKOUT pin output low pulse width*1	t_{CL}	5	—	—	ns	
CLKOUT pin output rising time	t_{Cr}	—	—	5	ns	
CLKOUT pin output falling time	t_{Cf}	—	—	5	ns	

Note 1. If the main clock oscillator is selected by the CLKOUT output source select bit (CKOCR.CKOSEL[2:0]) and the external clock input is selected by the main clock oscillator switching bit (MOFCR.MOSEL), the pulse width depends on the input clock wave form.

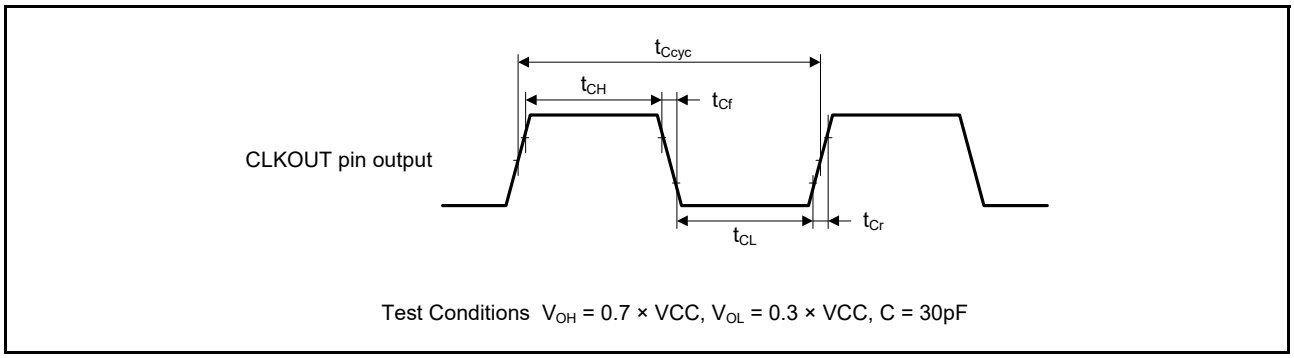


Figure 2.12 CLKOUT Pin Output Timing

2.4.3 Timing of Recovery from Low Power Consumption Modes

Table 2.23 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.		Unit	Test Conditions
						$t_{SBYOSCWT}$*2	t_{SBYSEQ}*3		
Recovery time from software standby mode *1	Crystal resonator connected to main clock oscillator	Main clock oscillator operating	t_{SBYMC}	—	—	{(MSTS[7:0] bit × 32) + 76} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{MAIN}	μs	Figure 2.13
		Main clock oscillator and PLL circuit operating	t_{SBYPC}			{(MSTS[7:0] bit × 32) + 138} / 0.216	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	External clock input to main clock oscillator	Main clock oscillator operating	t_{SBYEX}			352	100 + 7 / f_{ICLK} + 2n / f_{EXMAIN}		
		Main clock oscillator and PLL circuit operating	t_{SBYPE}			639	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	Sub-clock oscillator operating		t_{SBYSC}			{(SSTS[7:0] bit × 16384) + 13} / 0.216 + 10 / f_{FCLK}	100 + 4 / f_{ICLK} + 2n / f_{SUE}		
	High-speed on-chip oscillator operating	High-speed on-chip oscillator operating	t_{SBYHO}			454	100 + 7 / f_{ICLK} + 2n / f_{HOCO}		
		High-speed on-chip oscillator operating and PLL circuit operating	t_{SBYPH}			741	100 + 7 / f_{ICLK} + 2n / f_{PLL}		
	Low-speed on-chip oscillator operating*4		t_{SBYLO}			338	100 + 7 / f_{ICLK} + 2n / f_{LOCO}		

Note 1. The time for recovery from software standby mode is determined by the value obtained by adding the oscillation stabilization waiting time ($t_{SBYOSCWT}$) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).
Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time $t_{SBYOSCWT}$ is selected.
Note 3. For n, the greatest value is selected from among the internal clock division settings.
Note 4. This condition applies when f_{ICLK}:f_{FCLK} = 1:1, 2:1, or 4:1.

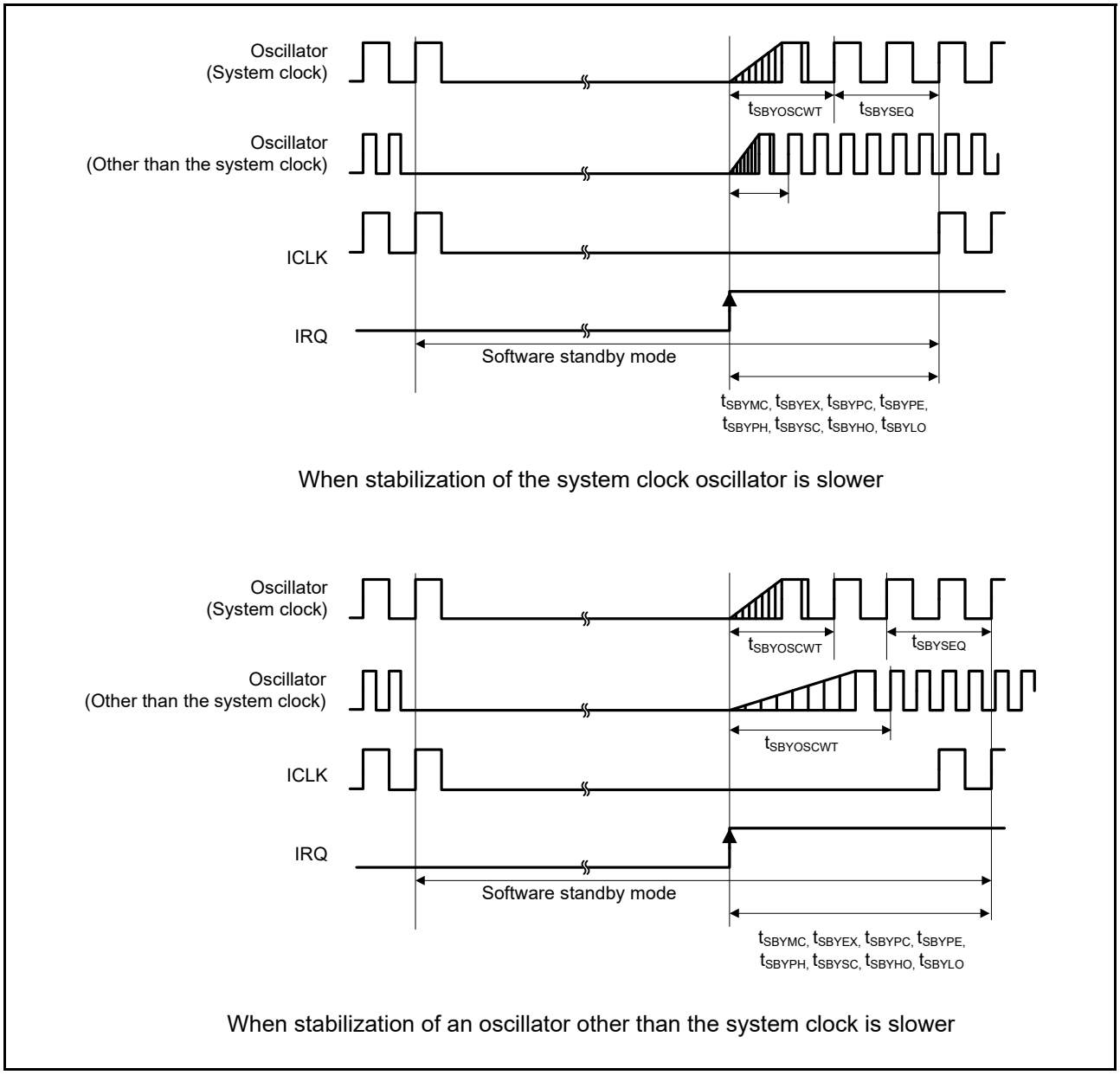


Figure 2.13 Software Standby Mode Recovery Timing

Table 2.24 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep software standby mode	t_{DSBY}	—	—	0.9	ms	Figure 2.14
Waiting time after recovery from deep software standby mode	t_{DSBYWT}	23	—	24	t_{Lcyc}	

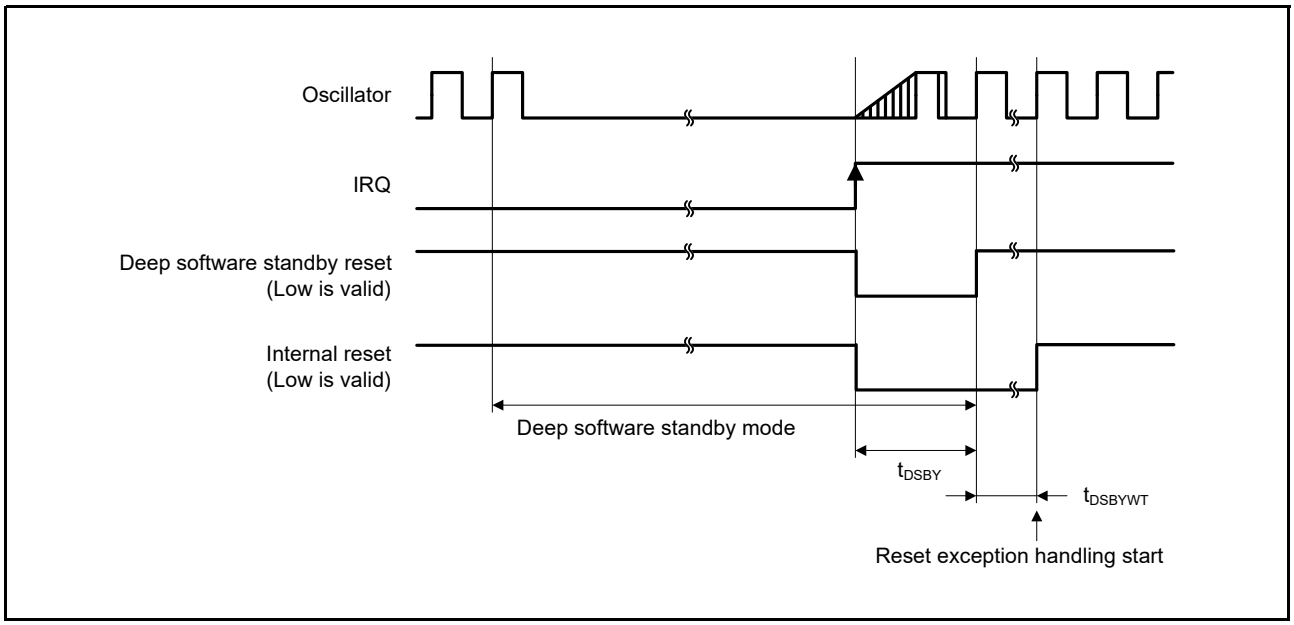


Figure 2.14 Deep Software Standby Mode Recovery Timing

2.4.4 Control Signal Timing

Table 2.25 Control Signal Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item	Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions*1
NMI pulse width	t_{NMIW}	200	—	—	ns	t_{PBcyc} × 2 ≤ 200 ns, Figure 2.15
		t_{PBcyc} × 2	—	—		t_{PBcyc} × 2 > 200 ns, Figure 2.15
IRQ pulse width	t_{IRQW}	200	—	—	ns	t_{PBcyc} × 2 ≤ 200 ns, Figure 2.16
		t_{PBcyc} × 2	—	—		t_{PBcyc} × 2 > 200 ns, Figure 2.16

Note 1. t_{PBcyc}: PCLKB cycle

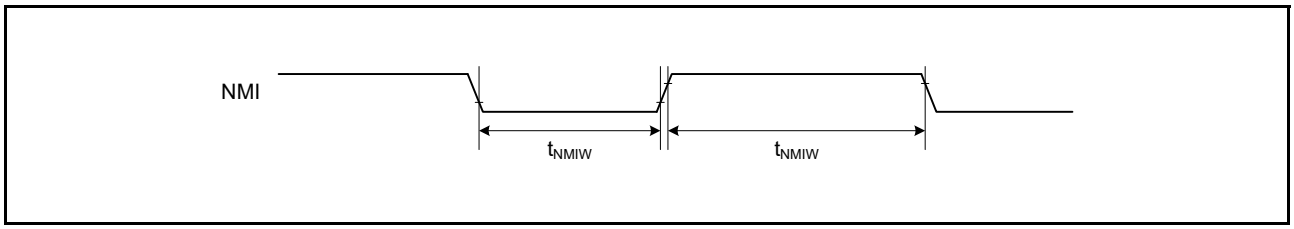


Figure 2.15 NMI Interrupt Input Timing

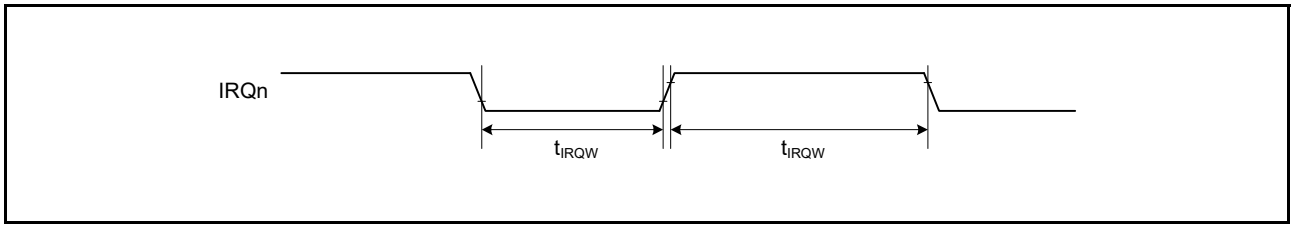


Figure 2.16 IRQ Interrupt Input Timing

2.4.5 Bus Timing

Table 2.26 Bus Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address delay time	t_{AD}	—	12.5	ns	Figure 2.17 to Figure 2.22
Byte control delay time	t_{BCD}	—	12.5	ns	
CS# delay time	t_{CSD}	—	12.5	ns	
ALE delay time	t_{ALED}	—	12.5	ns	
RD# delay time	t_{RSD}	—	12.5	ns	
Read data setup time	t_{RDS}	12.5	—	ns	
Read data hold time	t_{RDH}	0	—	ns	
WR# delay time	t_{WRD}	—	12.5	ns	
Write data delay time	t_{WDD}	—	12.5	ns	
Write data hold time	t_{WDH}	0	—	ns	
WAIT# setup time	t_{WTS}	12.5	—	ns	Figure 2.23
WAIT# hold time	t_{WTH}	0	—	ns	
Address delay time 2 (SDRAM)	t_{AD2}	1	12.5	ns	Figure 2.24 to Figure 2.30
CS# delay time 2 (SDRAM)	t_{CSD2}	1	12.5	ns	
DQM delay time (SDRAM)	t_{DQMD}	1	12.5	ns	
CKE delay time (SDRAM)	t_{CKED}	1	12.5	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	10	—	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	0	—	ns	
Write data delay time 2 (SDRAM)	t_{WDD2}	—	12.5	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	1	—	ns	
WE# delay time (SDRAM)	t_{WED}	1	12.5	ns	
RAS# delay time (SDRAM)	t_{RASD}	1	12.5	ns	
CAS# delay time (SDRAM)	t_{CASD}	1	12.5	ns	

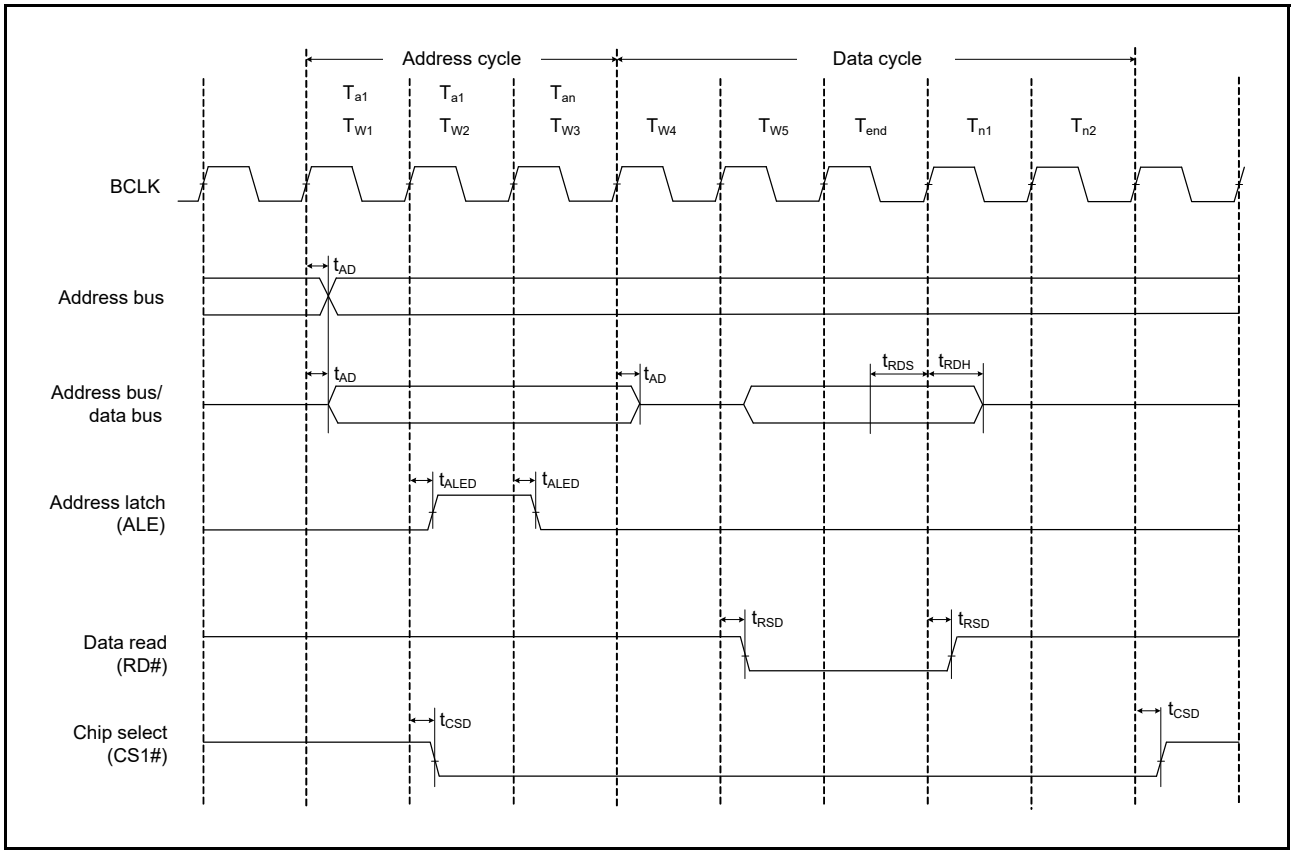


Figure 2.17 Address/Data Multiplexed Bus Read Access Timing

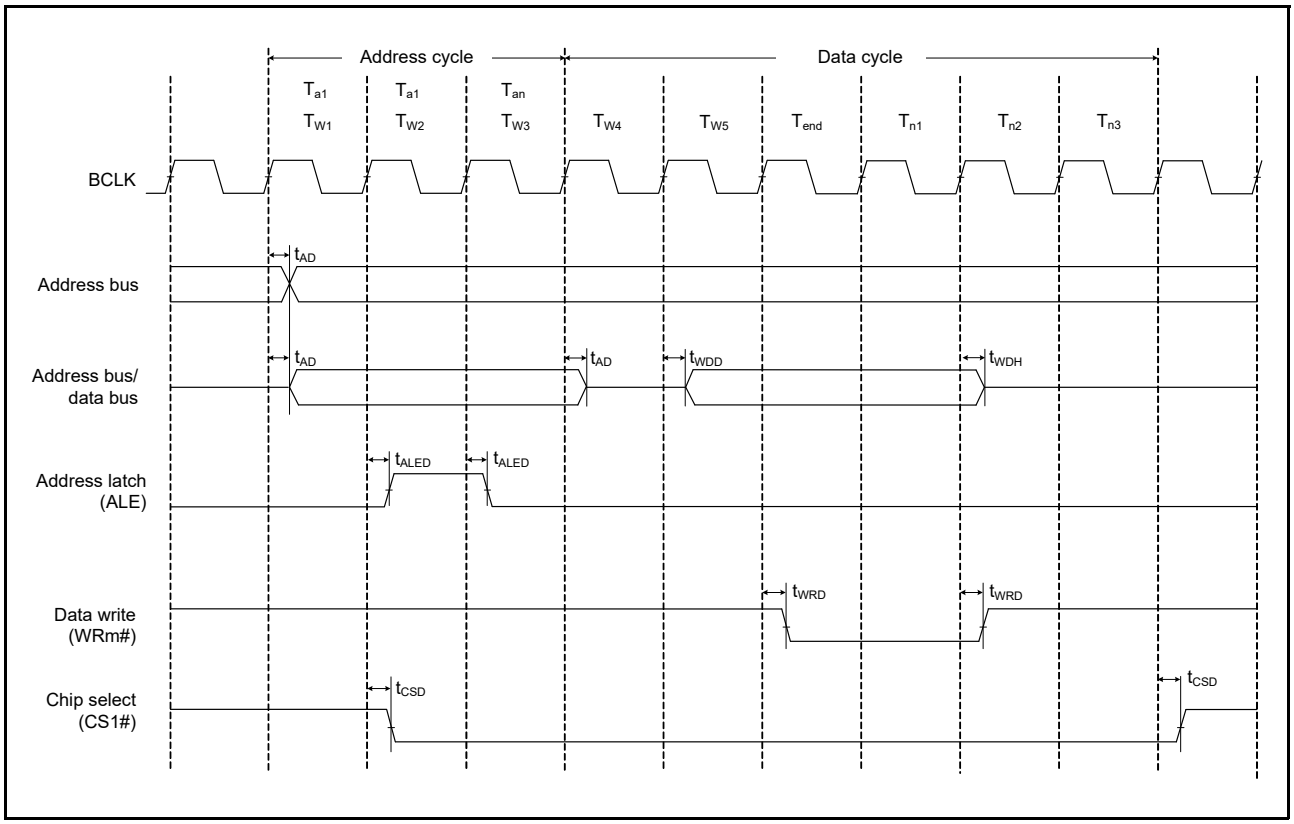


Figure 2.18 Address/Data Multiplexed Bus Write Access Timing

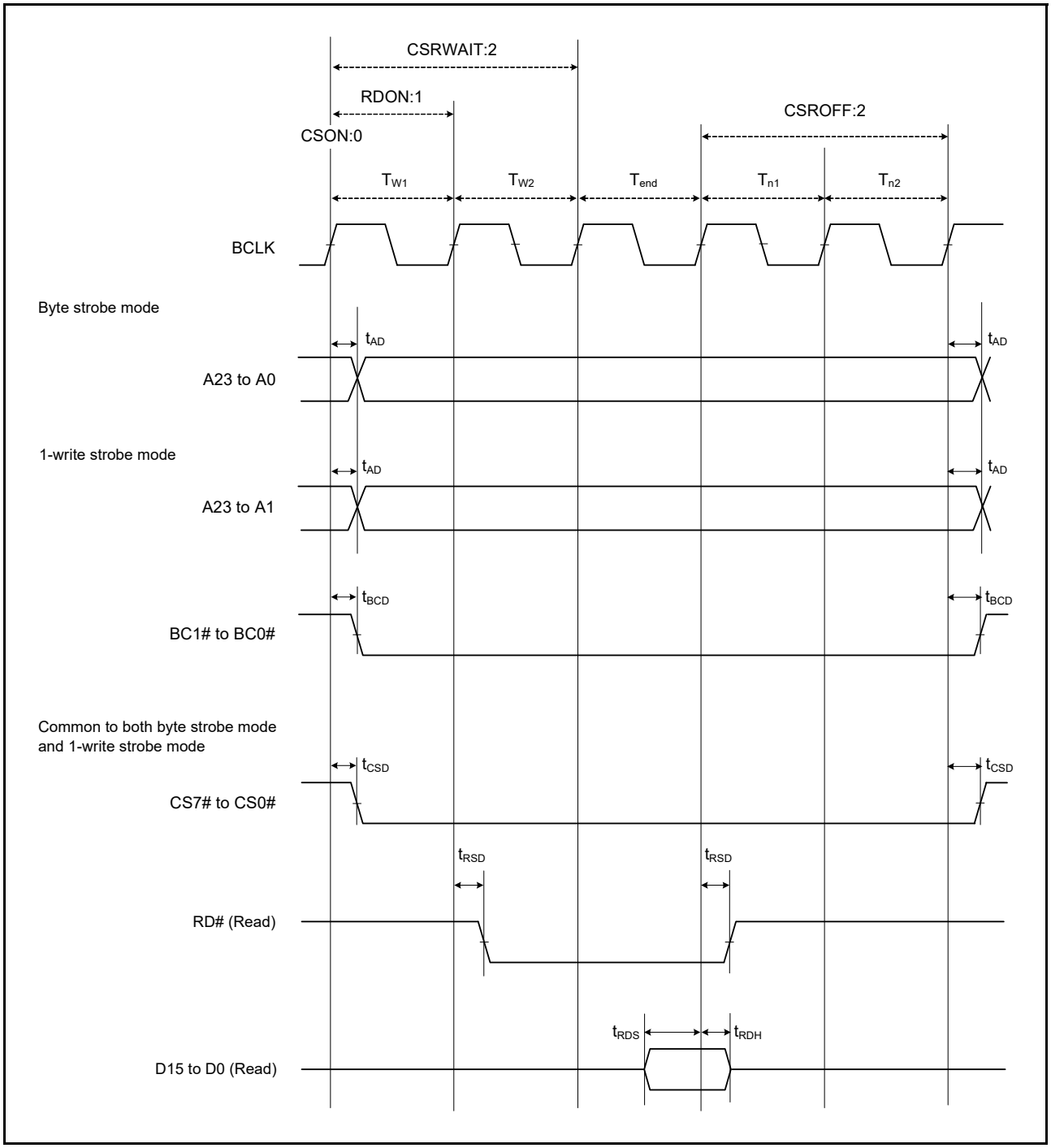
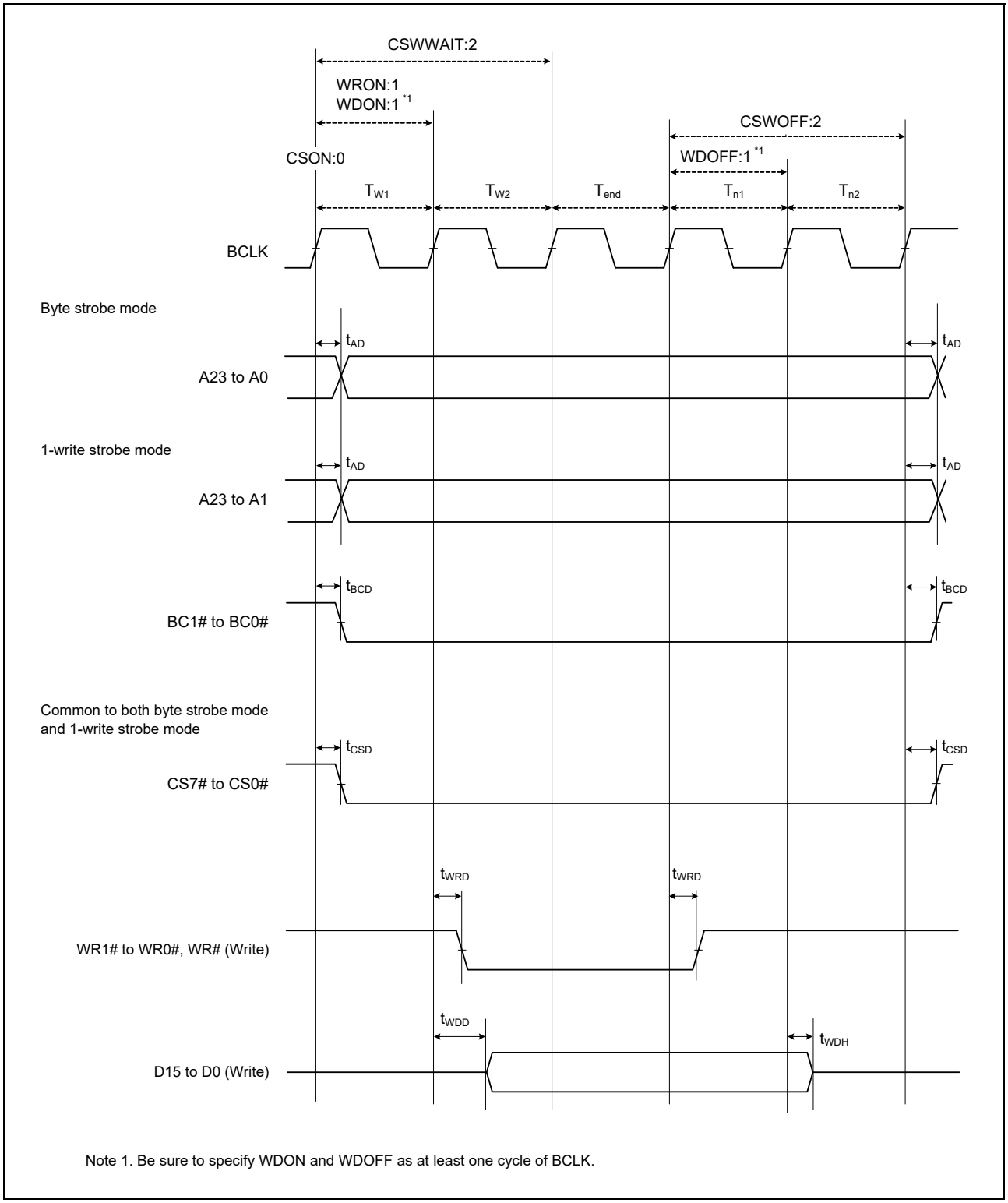


Figure 2.19 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)



Note 1. Be sure to specify WDON and WDOFF as at least one cycle of BCLK.

Figure 2.20 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

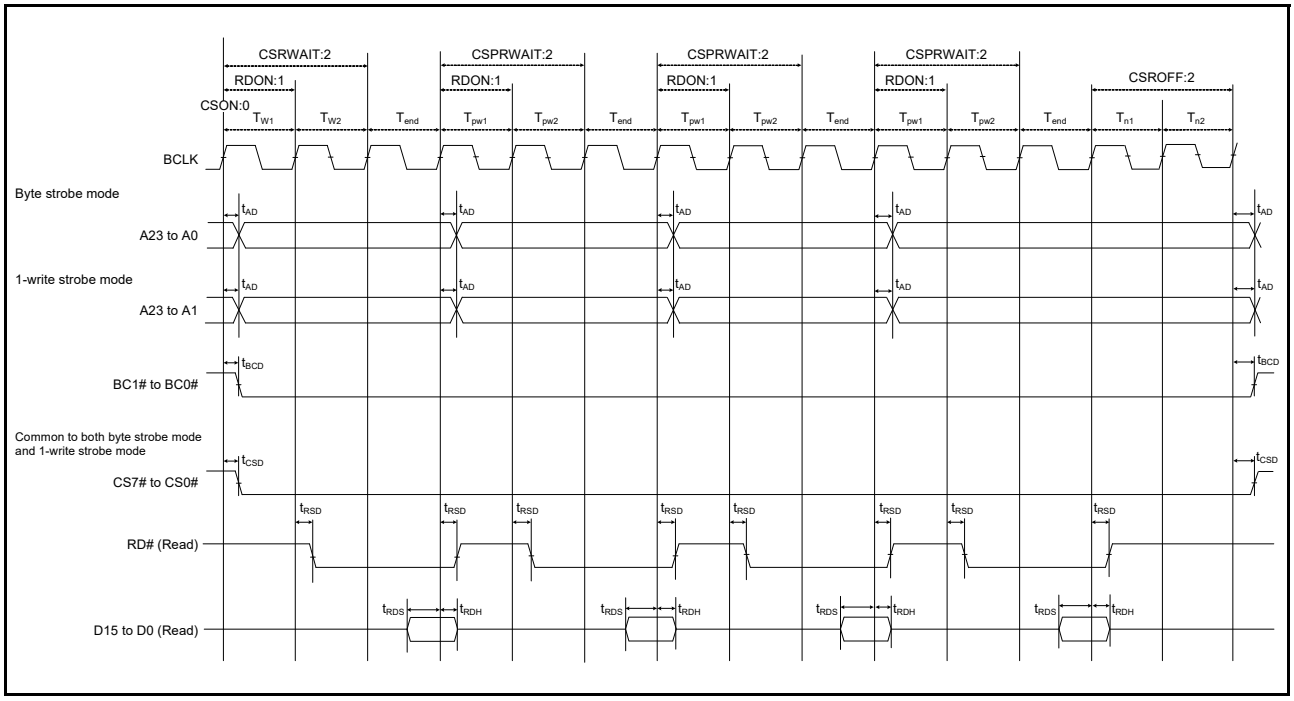


Figure 2.21 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

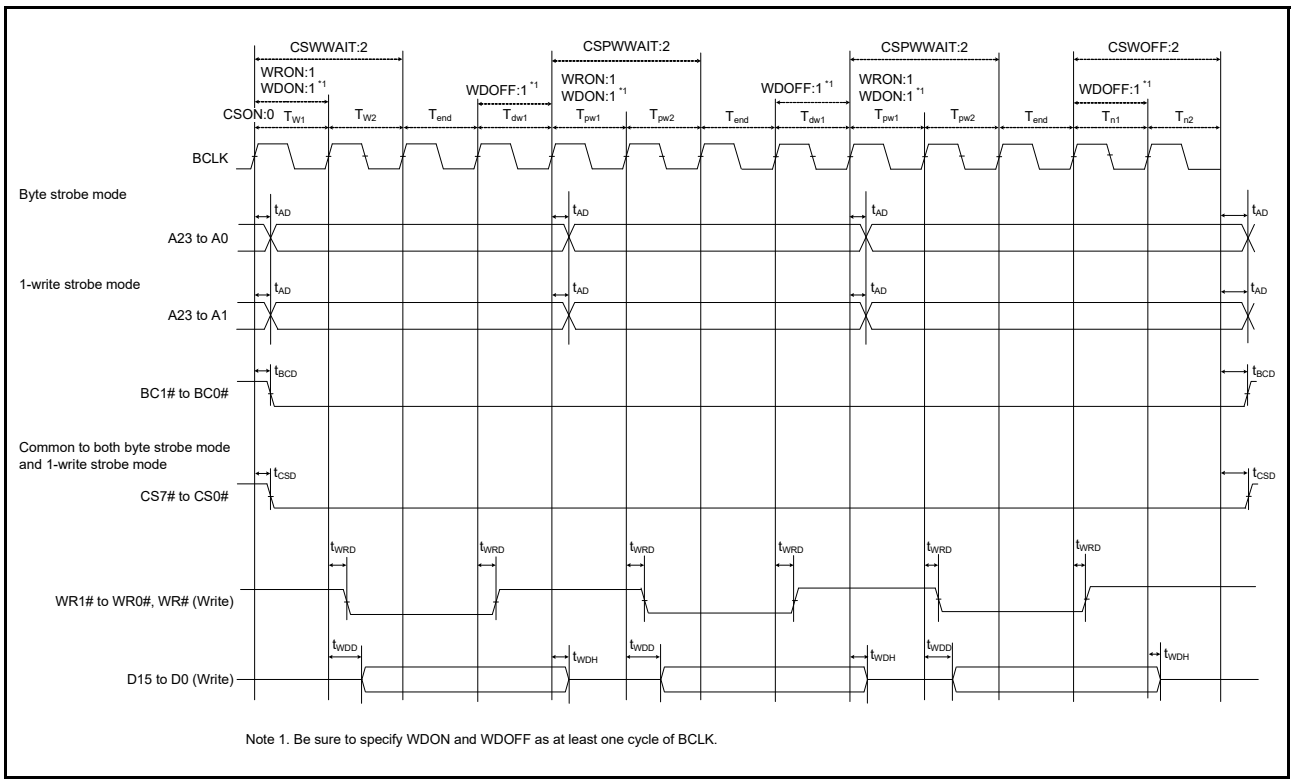


Figure 2.22 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

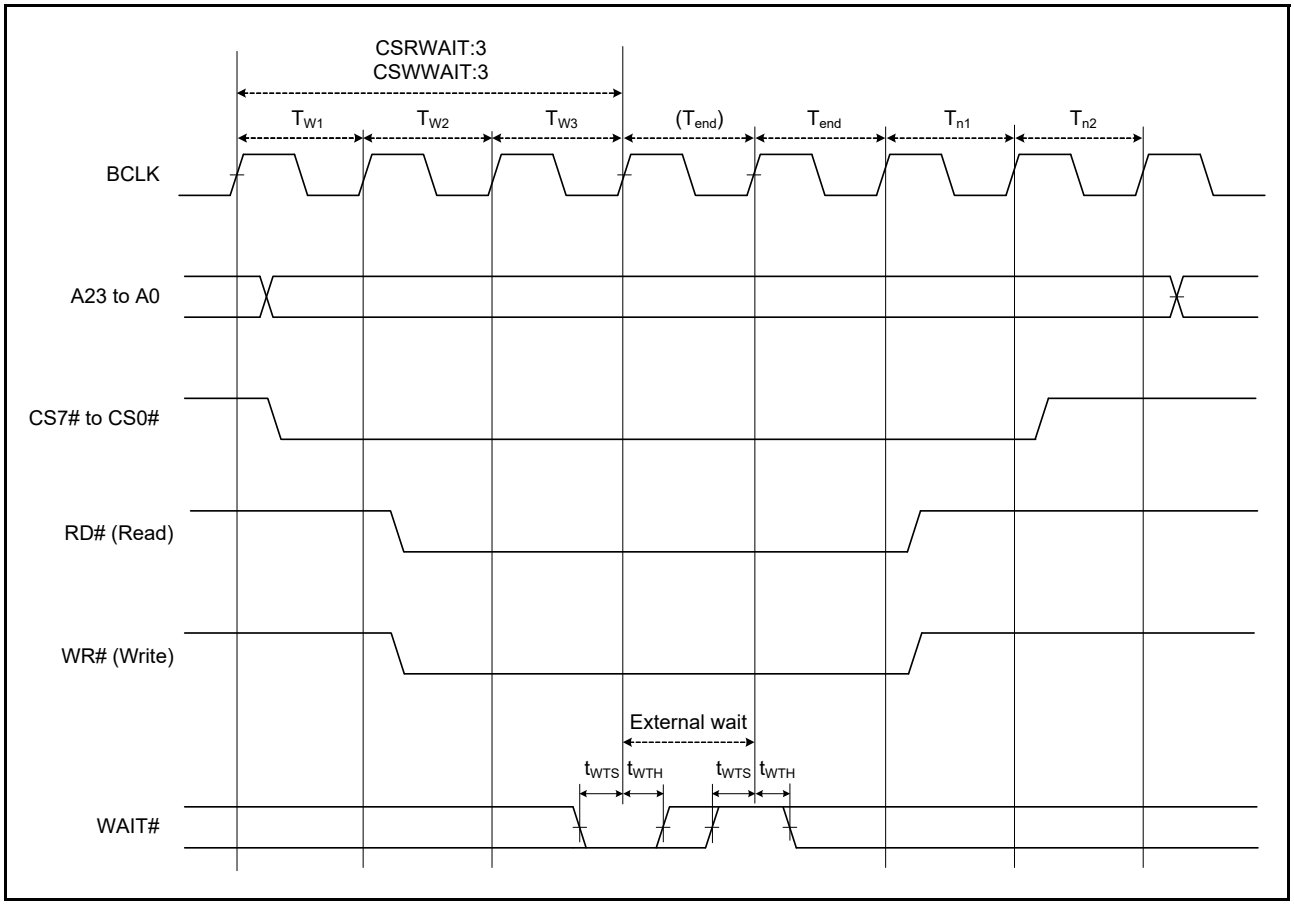
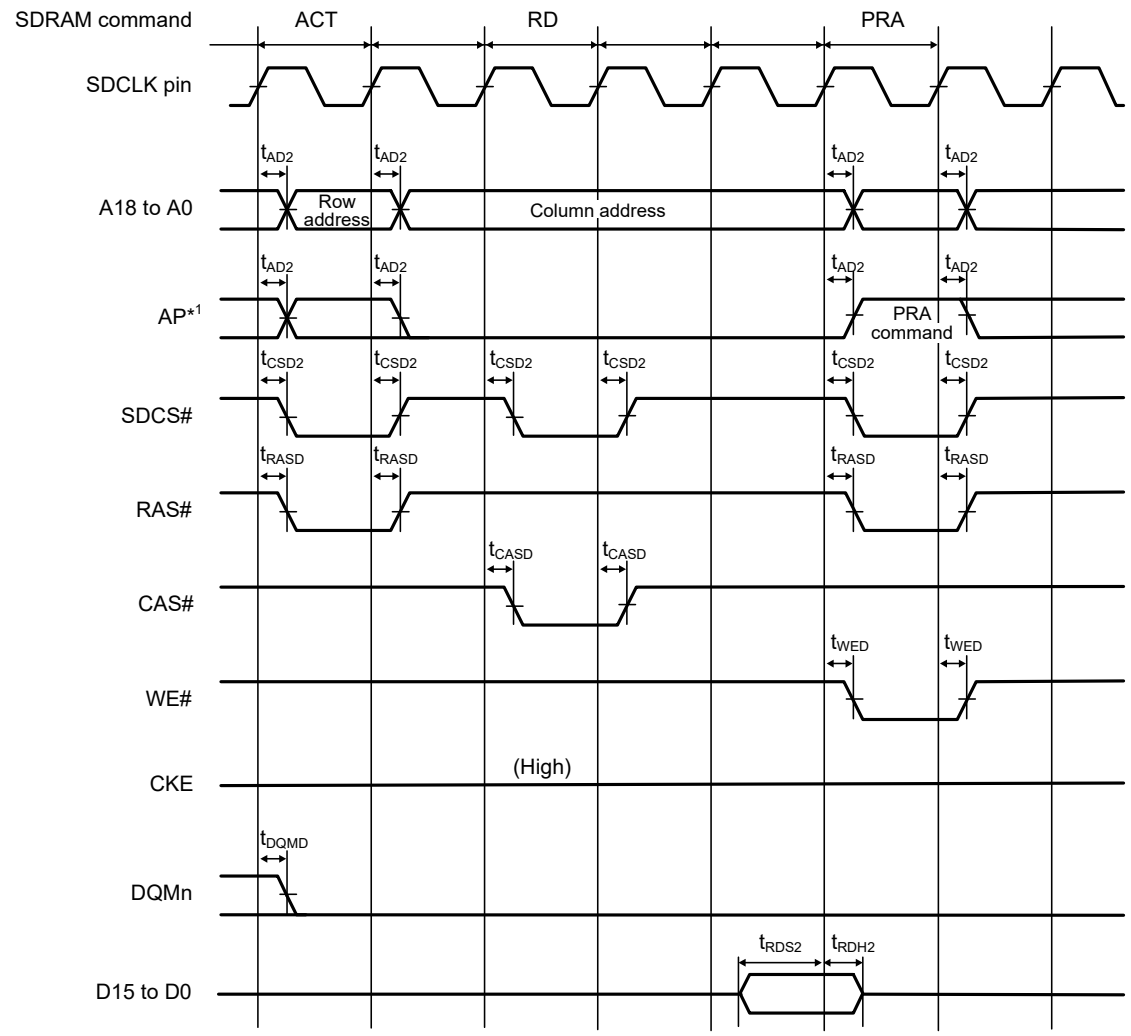
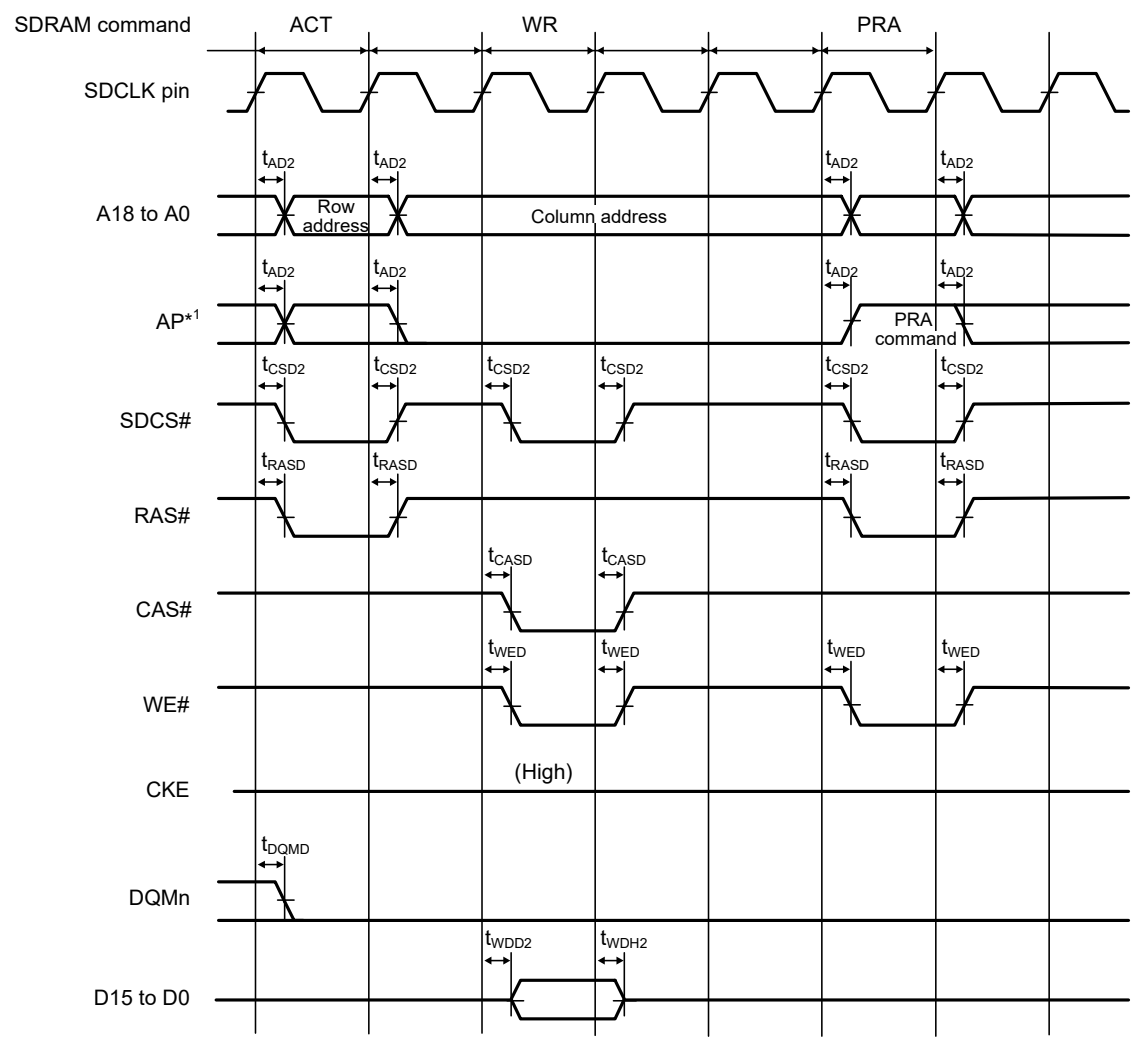


Figure 2.23 External Bus Timing/External Wait Control



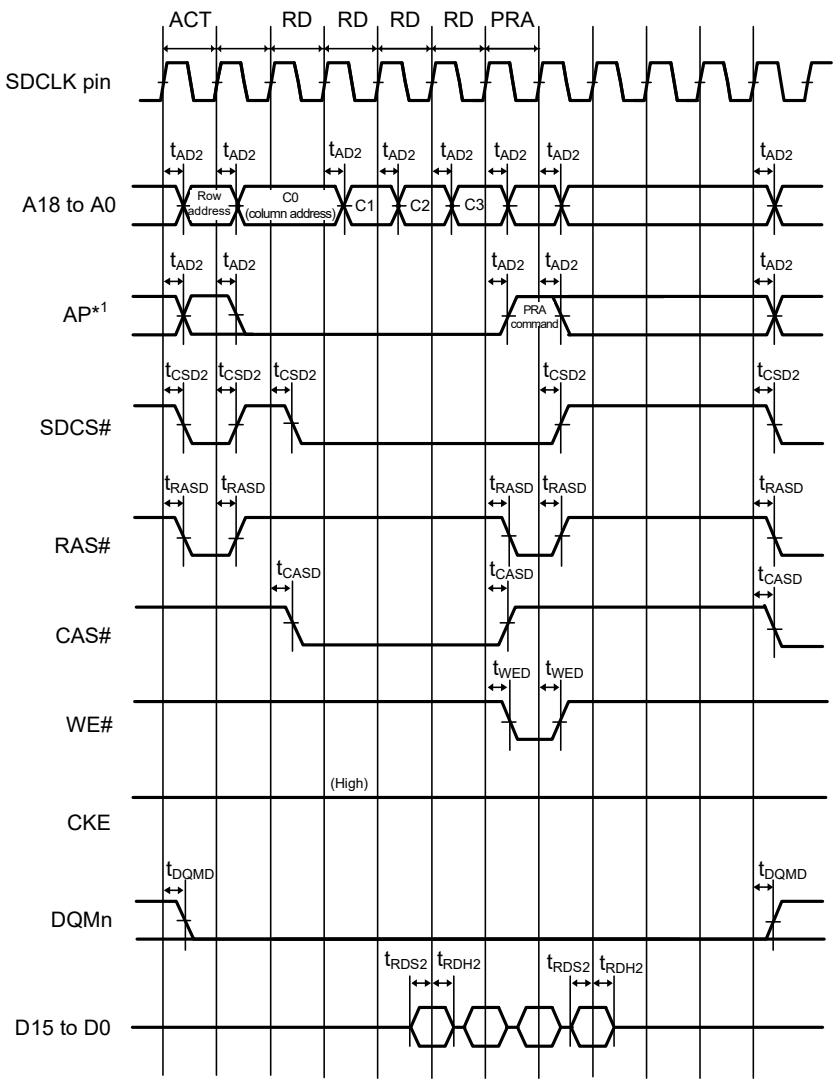
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.24 SDRAM Space Single Read Bus Timing



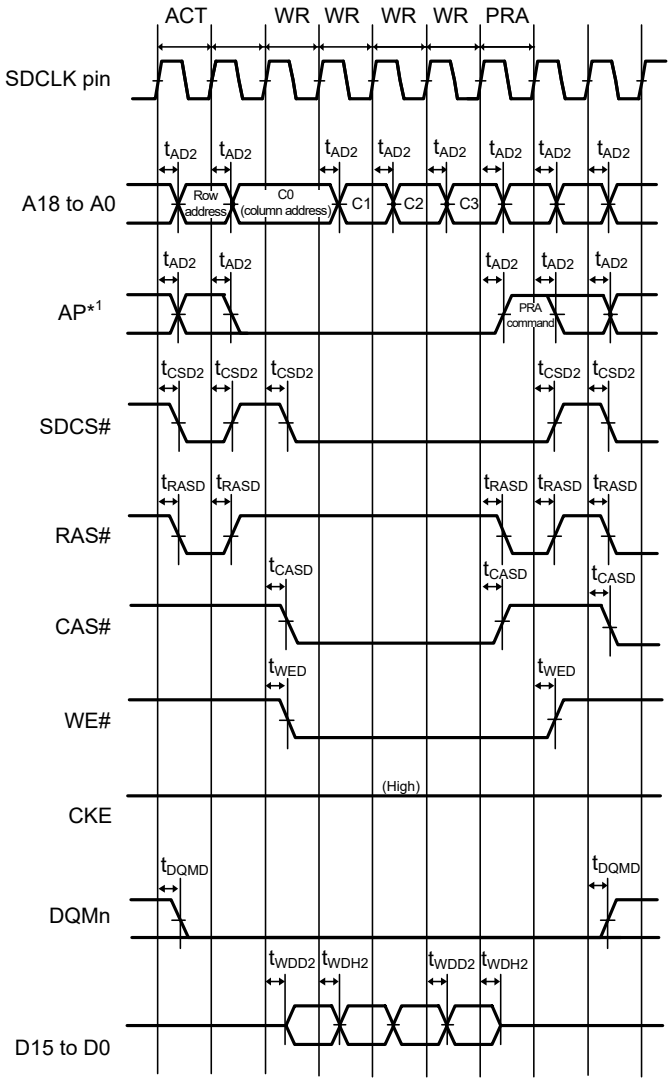
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.25 SDRAM Space Single Write Bus Timing



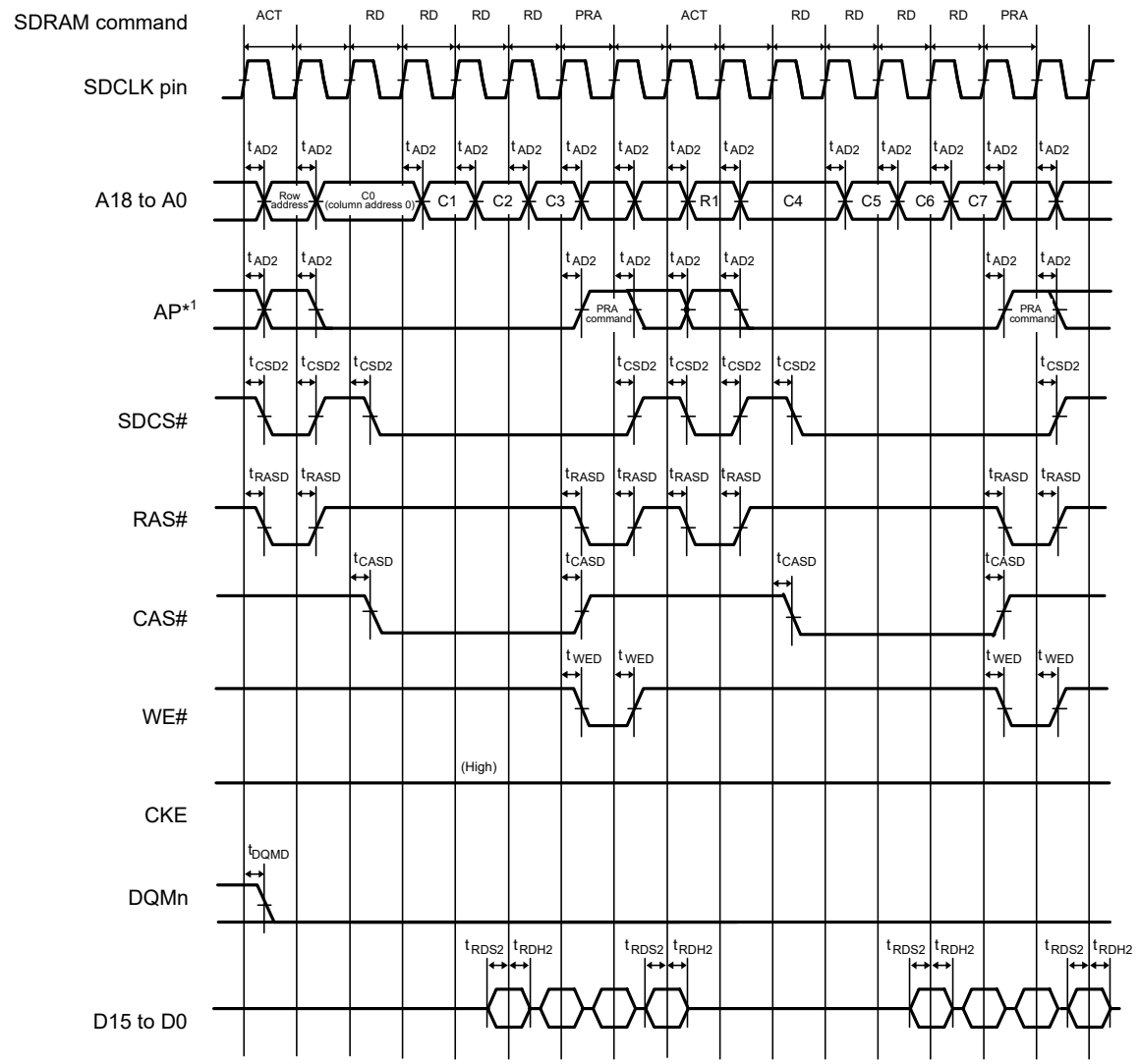
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.26 SDRAM Space Multiple Read Bus Timing



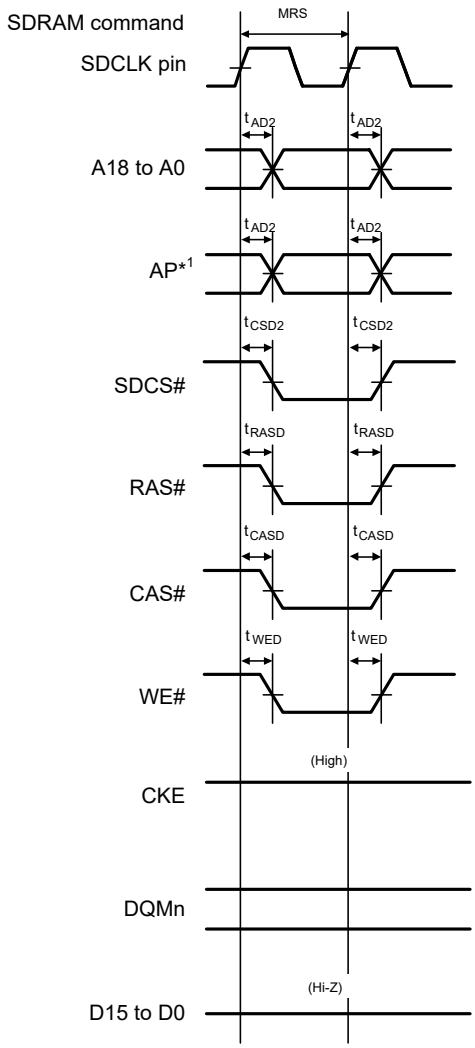
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.27 SDRAM Space Multiple Write Bus Timing



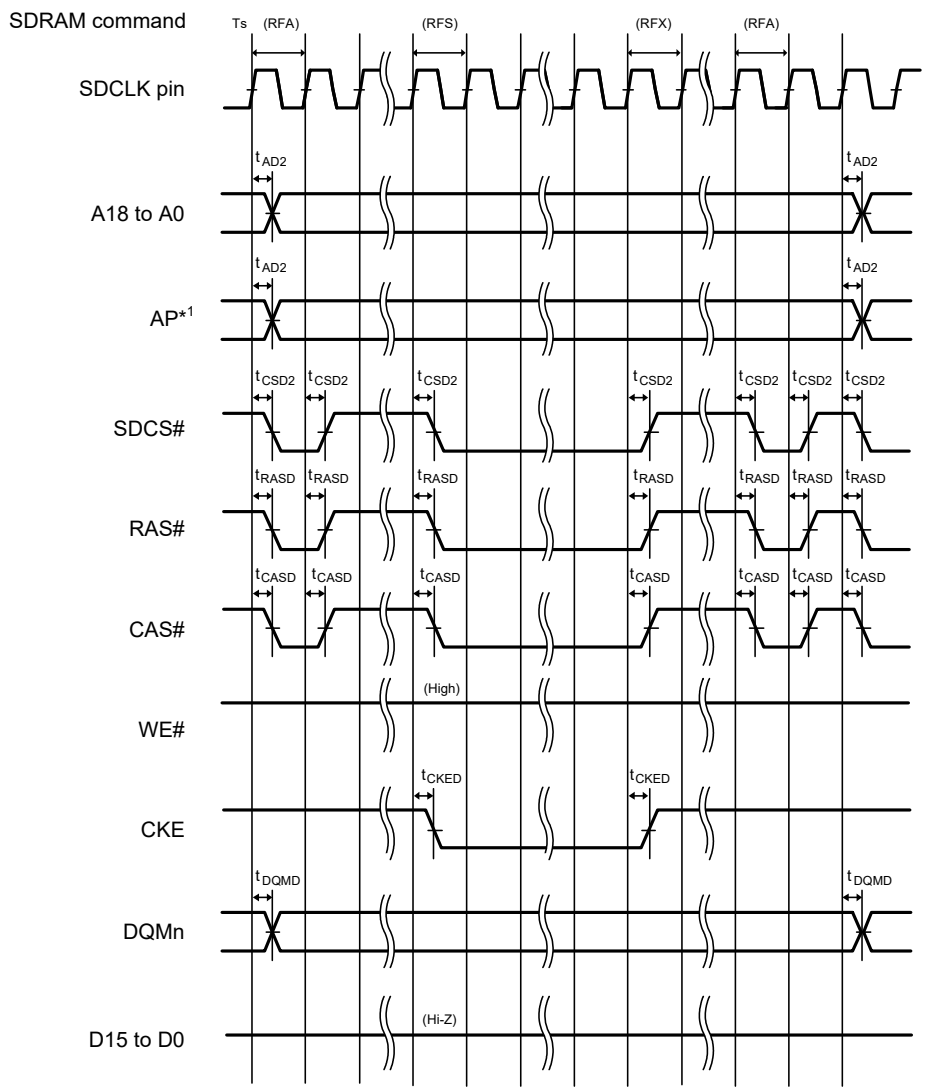
Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.28 SDRAM Space Multiple Read Line Stride Bus Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.29 SDRAM Space Mode Register Set Bus Timing



Note 1. Address pins for output of the precharge-setting command (Precharge-sel) for SDRAM.

Figure 2.30 SDRAM Space Self-Refresh Bus Timing

2.4.6 EXDMAC Timing

Table 2.27 EXDMAC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = PCLKA = 8 to 120 MHz, PCLKB = BCLK = SDCLK = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
EXDMAC	EDREQ setup time	t_{EDRQS}	13	—	ns	Figure 2.31
	EDREQ hold time	t_{EDRQH}	2	—	ns	
	EDACK delay time	t_{EDACD}	—	13	ns	Figure 2.32, Figure 2.33

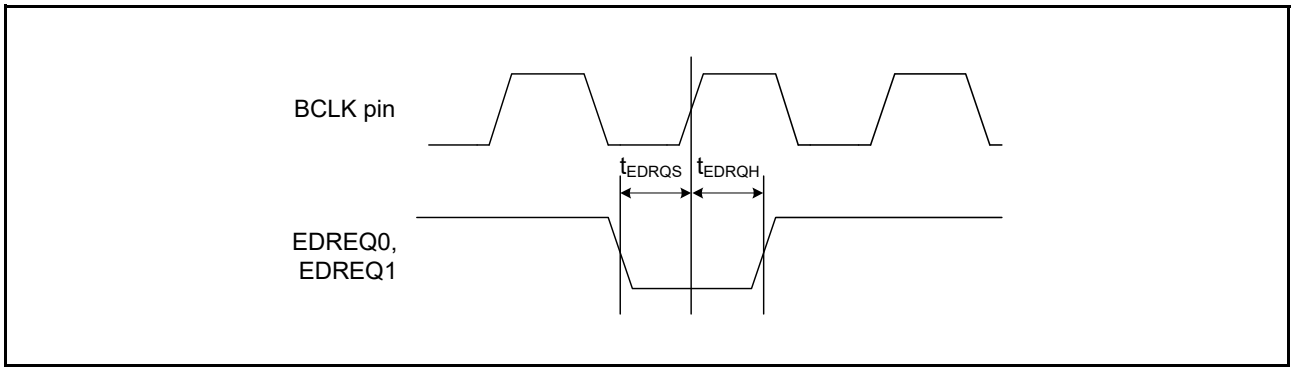


Figure 2.31 EDREQ0 and EDREQ1 Input Timing

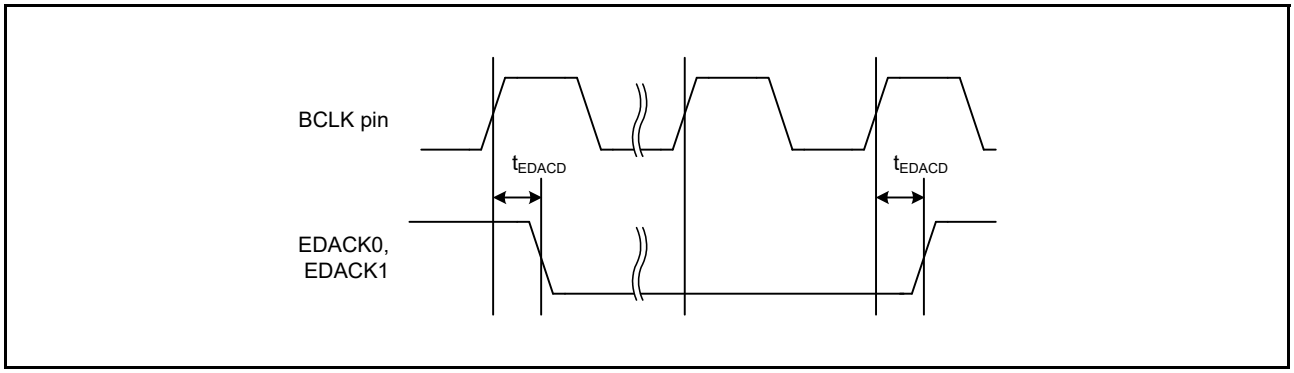


Figure 2.32 EDACK0 and EDACK1 Single-Address Transfer Timing (for a CS Area)

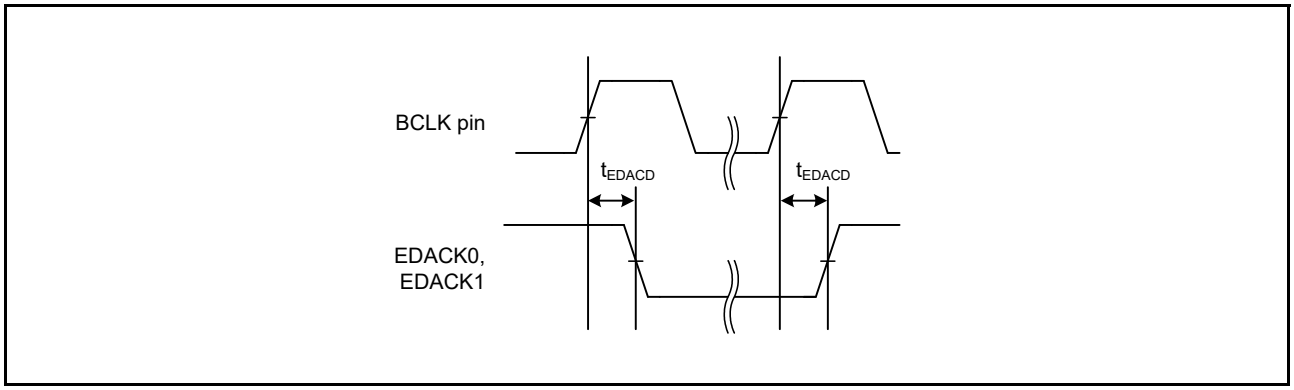


Figure 2.33 EDACK0 and EDACK1 Single-Address Transfer Timing (for SDRAM)

2.4.7 Timing of On-Chip Peripheral Modules

2.4.7.1 I/O Port

Table 2.28 I/O Port Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{PBcyc}	Figure 2.34

Note 1. t_{PBcyc}: PCLKB cycle

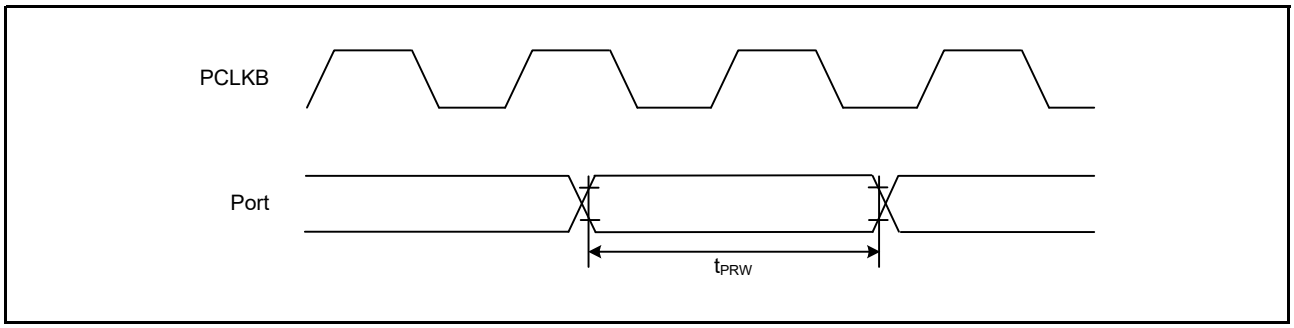


Figure 2.34 I/O Port Input Timing

2.4.7.2 TPU

Table 2.29 TPU Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TPU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{PBcyc}	Figure 2.35
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{PBcyc}	Figure 2.36
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

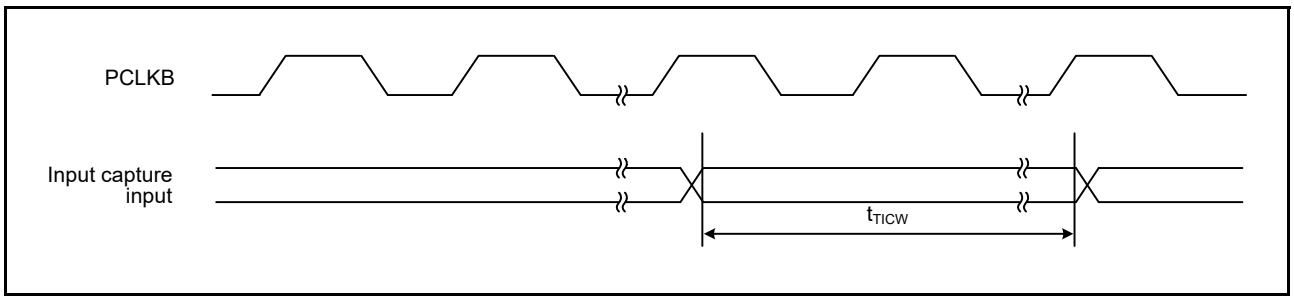


Figure 2.35 TPU Input Capture Input Timing

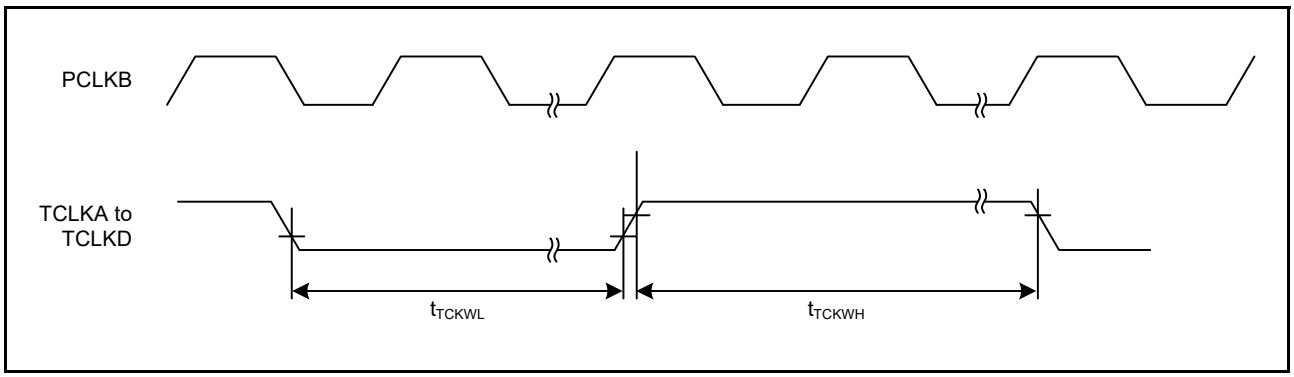


Figure 2.36 TPU Clock Input Timing

2.4.7.3 TMR

Table 2.30 TMR Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{PBcyc}	Figure 2.37
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

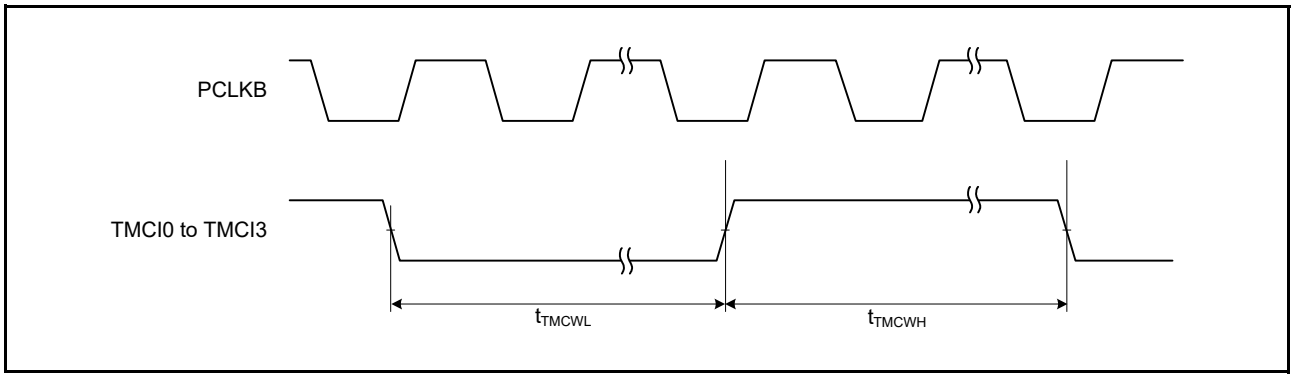


Figure 2.37 TMR Clock Input Timing

2.4.7.4 CMTW

Table 2.31 CMTW Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
CMTW	Input capture input pulse width	Single-edge setting	$t_{CMTWTICW}$	1.5	—	t_{PBcyc}	Figure 2.38
		Both-edge setting		2.5	—		

Note 1. t_{PBcyc}: PCLKB cycle

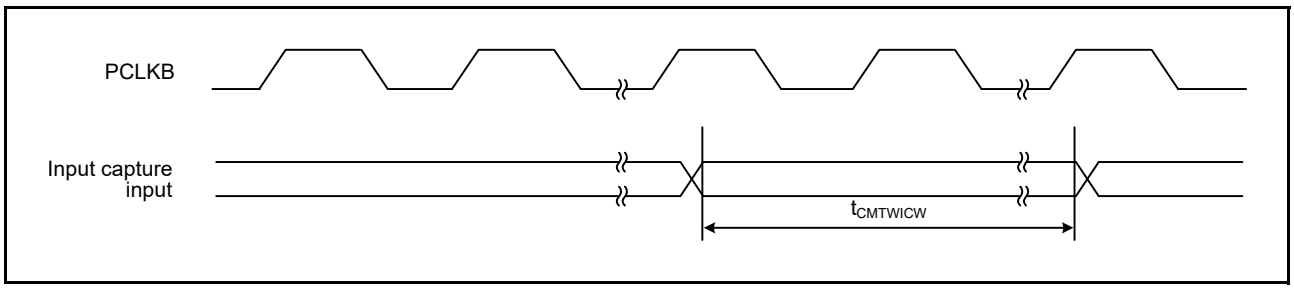


Figure 2.38 CMTW Input Capture Input Timing

2.4.7.5 MTU

Table 2.32 MTU Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
MTU	Input capture input pulse width	Single-edge setting	t_{MTICW}	1.5	—	t_{PAcyc}	Figure 2.39
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{MTCKWH}, t_{MTCKWL}	1.5	—	t_{PAcyc}	Figure 2.40
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{PAcyc}: PCLKA cycle

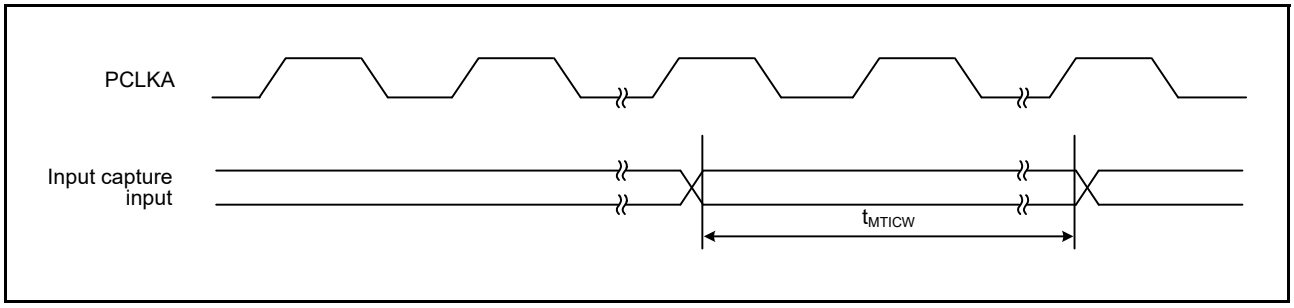


Figure 2.39 MTU Input Capture Input Timing

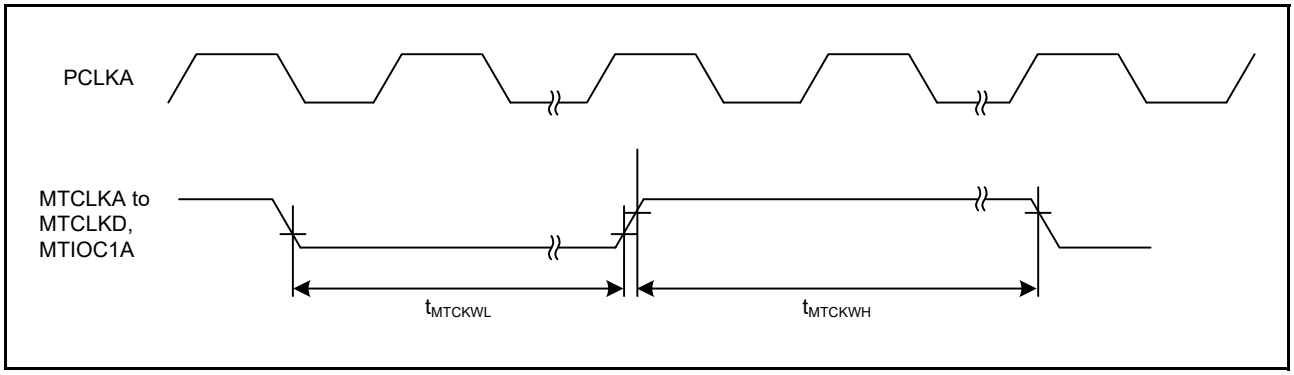


Figure 2.40 MTU Clock Input Timing

2.4.7.6 POE3

Table 2.33 POE3 Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Typ.	Max.	Unit*1	Test Conditions
POE	POEn# input pulse width (n = 0, 4, 8, 10, 11)		t_{POEW}	1.5	—	—	t_{PBcyc}	Figure 2.41
	Output disable time	Transition of the POEn# signal level	t_{POEDI}	—	—	5 PCLKB + 0.24	µs	Figure 2.42 When detecting falling edges (ICSRm.POEnM[3:0] = 0000b (m = 1 to 5; n = 0, 4, 8, 10, 11))
		Simultaneous conduction of output pins	t_{POEDO}	—	—	3 PCLKB + 0.2	µs	Figure 2.43
		Register setting	t_{POEDS}	—	—	1 PCLKB + 0.2	µs	Figure 2.44 Time for access to the register is not included.
		Oscillation stop detection	t_{POEDOS}	—	—	21	µs	Figure 2.45

Note 1. t_{PBcyc}: PCLKB cycle

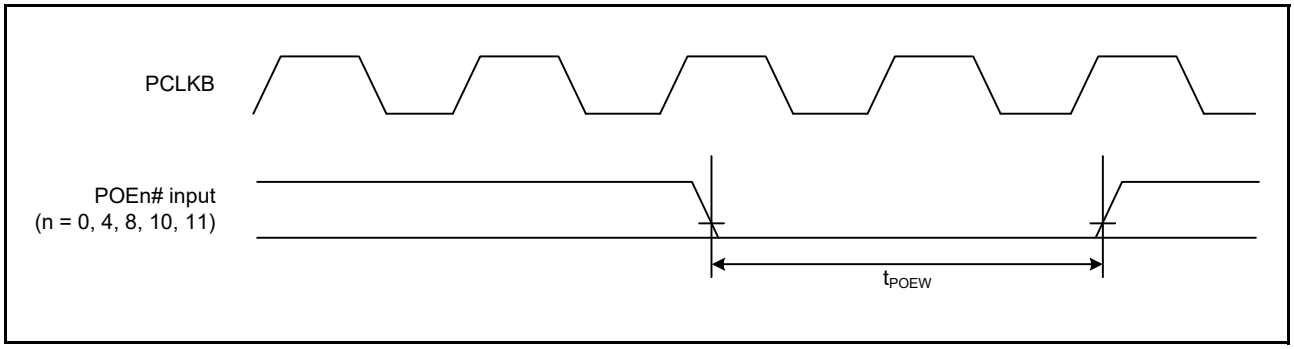


Figure 2.41 POE# Pin Input Timing

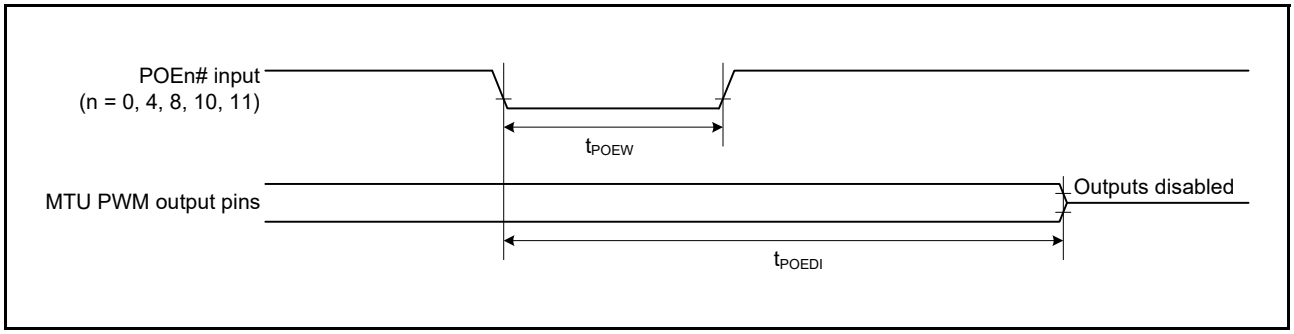
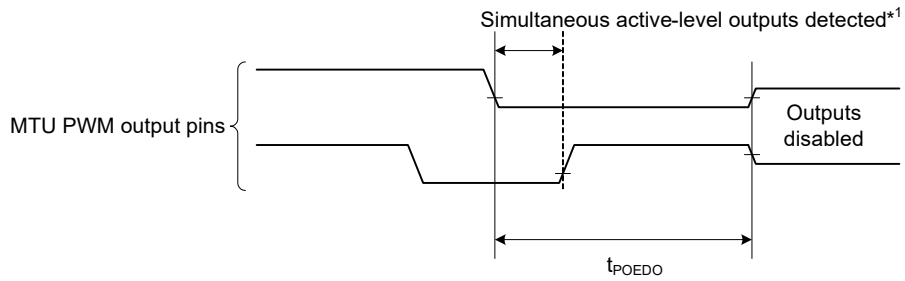


Figure 2.42 Output Disable Time for POE in Response to Transition of the POEn# Signal Level



Note 1. When the active level is set to low.

Figure 2.43 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

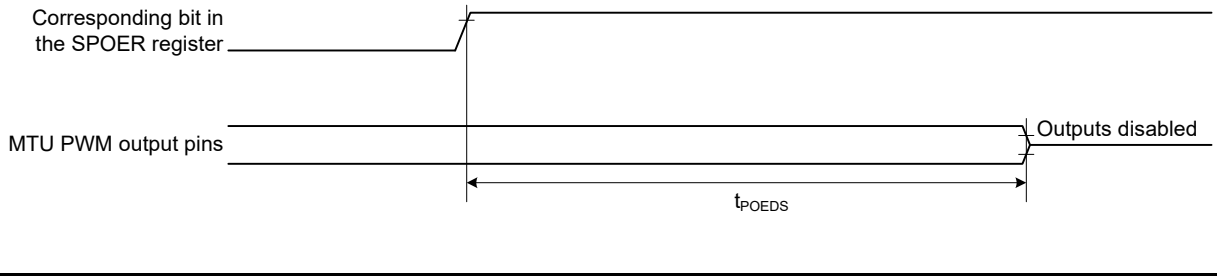


Figure 2.44 Output Disable Time for POE in Response to the Register Setting

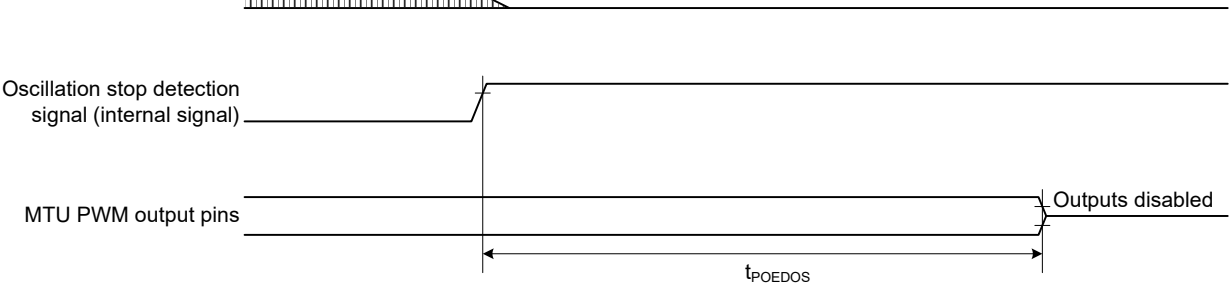


Figure 2.45 Output Disable Time for POE in Response to the Oscillation Stop Detection

2.4.7.7 A/D Converter Trigger

Table 2.34 A/D Converter Trigger Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit*1	Test Conditions
A/D converter	A/D converter trigger input pulse width	t_{TRGW}	1.5	—	t_{PBcyc}	Figure 2.46

Note 1. t_{PBcyc}: PCLKB cycle

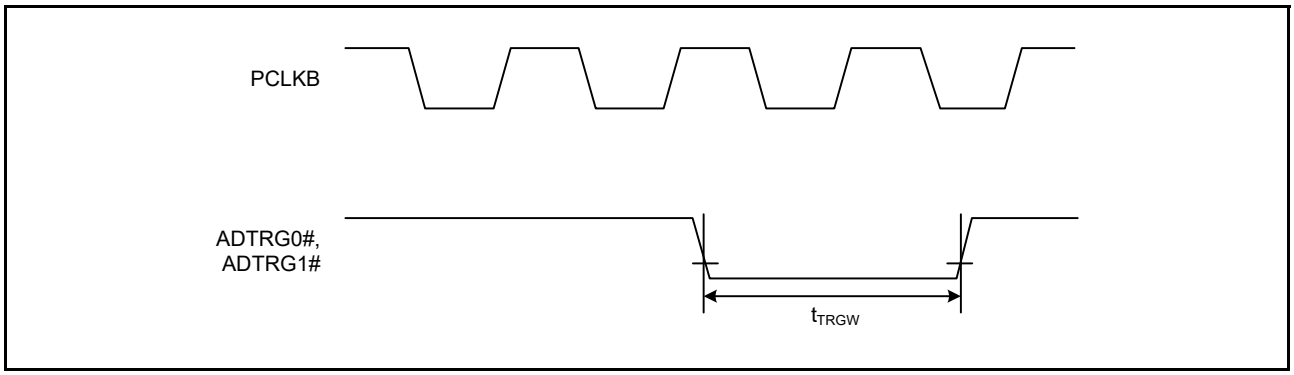


Figure 2.46 A/D Converter Trigger Input Timing

2.4.7.8 CAC

Table 2.35 CAC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item*1, *2			Symbol	Min.*1, *2	Max.	Unit	Test Conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le t_{CAC}$	t_{CACREF}	4.5 t_{CAC} + 3 t_{PBcyc}	—	ns	
		$t_{PBcyc} > t_{CAC}$		5 t_{CAC} + 6.5 t_{PBcyc}	—		

Note 1. t_{PBcyc}: PCLKB cycle
Note 2. t_{CAC}: CAC count clock source cycle

2.4.7.9 SCI

Table 2.36 SCIk, SCIh, and SCIm Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
SCIk, SCIh	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PBcyc}	Figure 2.47
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous (SCIk)	t_{Scyc}	6	—	t_{PBcyc}	
		Asynchronous (SCIh)		8	—		
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay time	Clock synchronous	t_{TXD}	—	28	ns	Figure 2.48
	Receive data setup time	Clock synchronous	t_{RXS}	15	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	
SCIm	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PAcyc}	Figure 2.47
		Clock synchronous		6	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	—	t_{PAcyc}	
		Clock synchronous		4	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Transmit data delay time	Master	t_{TXD}	—	15	ns	Figure 2.48
		Slave		—	28		
	Receive data setup time	Clock synchronous	t_{RXS}	20	—	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	—	ns	

Note 1. t_{PBcyc}: PCLKB cycle; t_{PAcyc}: PCLKA cycle

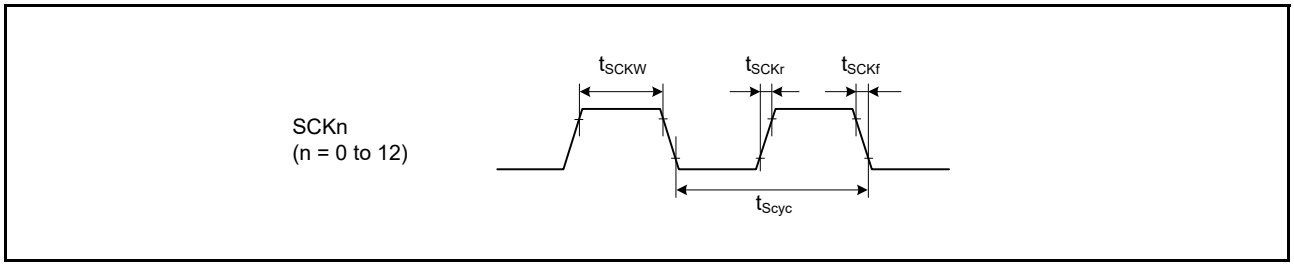


Figure 2.47 SCK Clock Input Timing

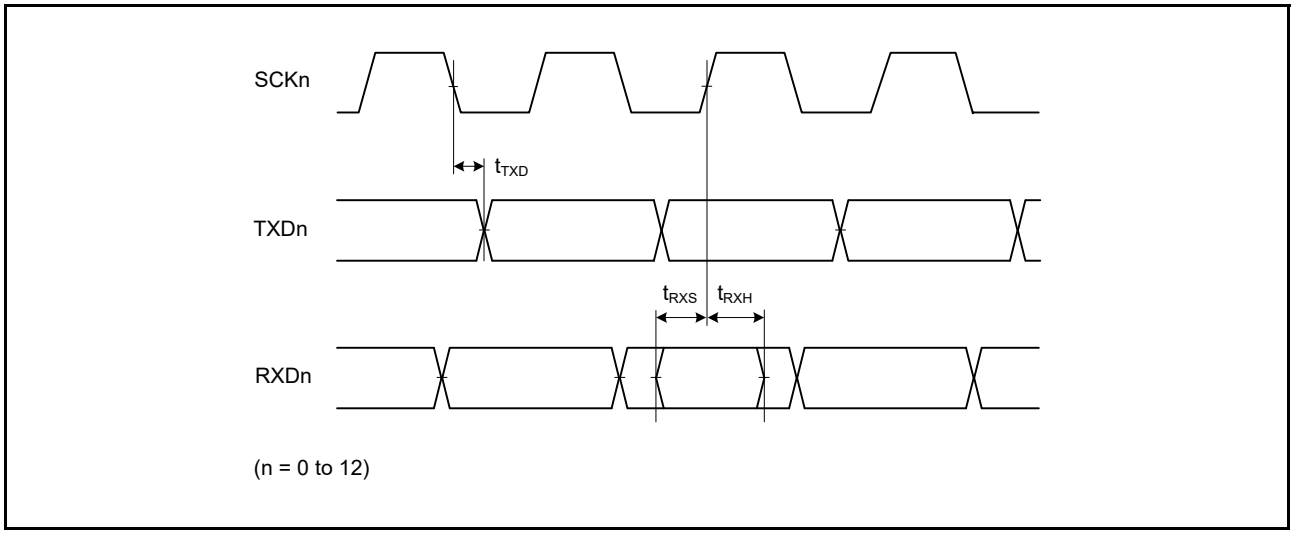


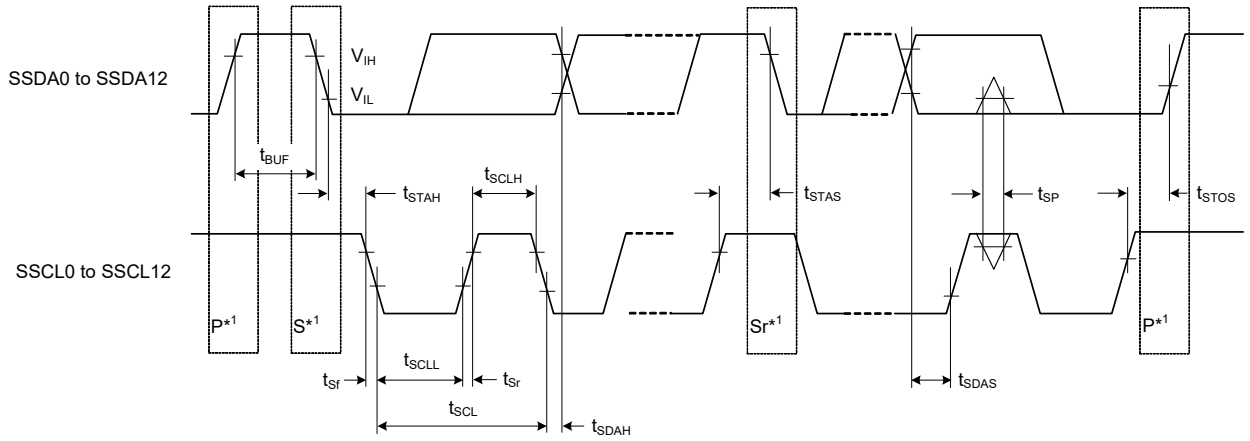
Figure 2.48 SCI Input/Output Timing: Clock Synchronous Mode

Table 2.37 Simple IIC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SSCL, SSDA input rise time	t_{Sr}	—	1000	ns	Figure 2.49
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast-mode)	SSCL, SSDA input rise time	t_{Sr}	—	300	ns	
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b*1	—	400	pF	

Note: t_{Pcyc} refers to the period of PCLKA in SCI10 and SCI11, and of PCLKB in SCI0 to SCI9, and SCI12.
Note 1. Cb is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC
V_{OL} = 0.6 V, I_{OL} = 6 mA

Figure 2.49 Simple IIC Bus Interface Input/Output Timing

Table 2.38 Simple SPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4	—	t_{Pcyc}	Figure 2.50
	SCK clock cycle input (slave)		6	—		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time	t_{SU}	33.3	—	ns	Figure 2.51 to Figure 2.54
	Data input hold time	t_H	33.3	—	ns	
	SS input setup time	t_{LEAD}	1	—	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	—	t_{SPcyc}	
	Data output delay time	t_{OD}	—	33.3	ns	
	Data output hold time	t_{OH}	–10	—	ns	
	Data rise/fall time	t_{Dr}, t_{Df}	—	16.6	ns	
	SS input rise/fall time	t_{SSLr}, t_{SSLf}	—	16.6	ns	
	Slave access time	t_{SA}	—	5	t_{Pcyc}	Figure 2.53, Figure 2.54
	Slave output release time	t_{REL}	—	5	t_{Pcyc}	

Note: t_{Pcyc} refers to the period of PCLKA in SCI10 and SCI11, and of PCLKB in SCI0 to SCI9, and SCI12.

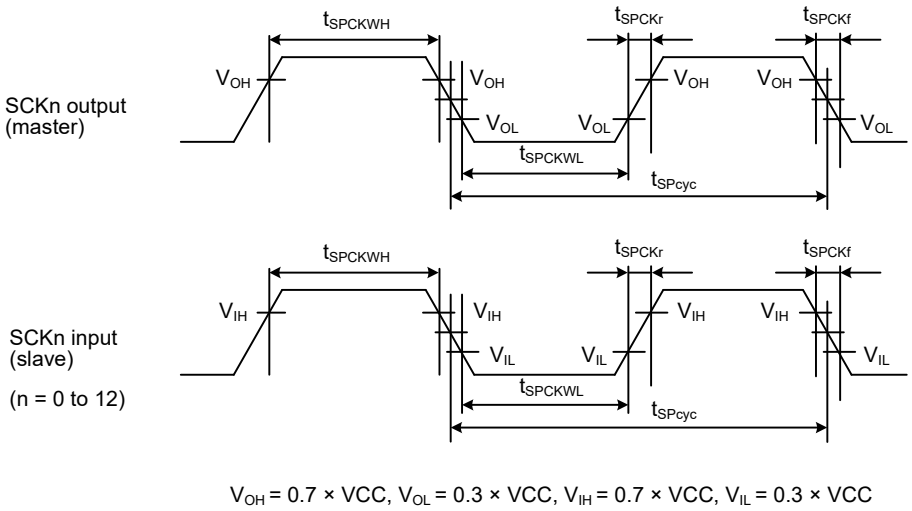


Figure 2.50 Simple SPI Clock Timing

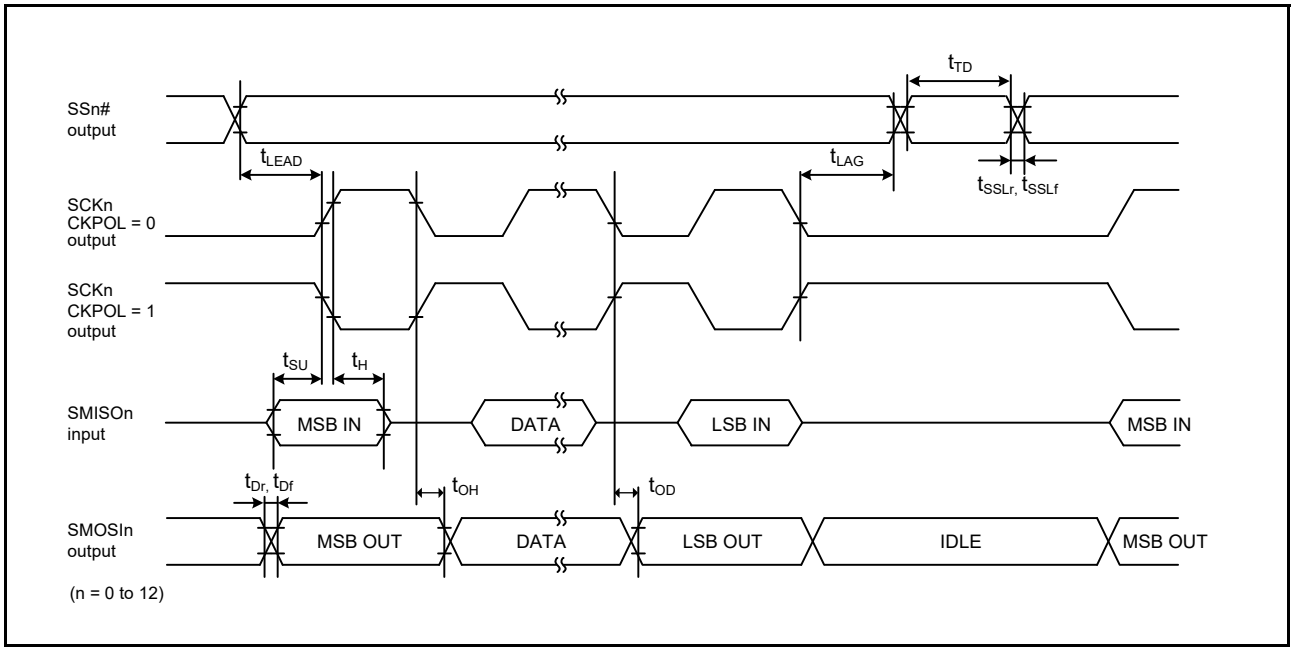


Figure 2.51 Simple SPI Timing (Master, CKPH = 1)

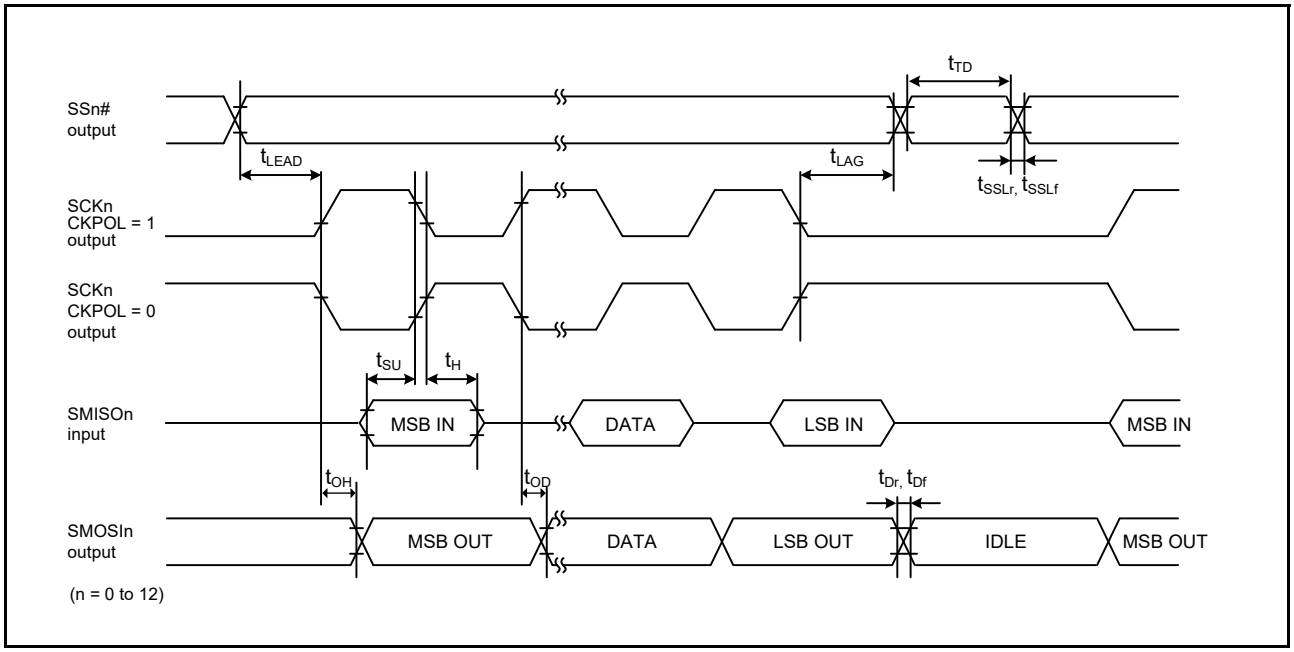


Figure 2.52 Simple SPI Timing (Master, CKPH = 0)

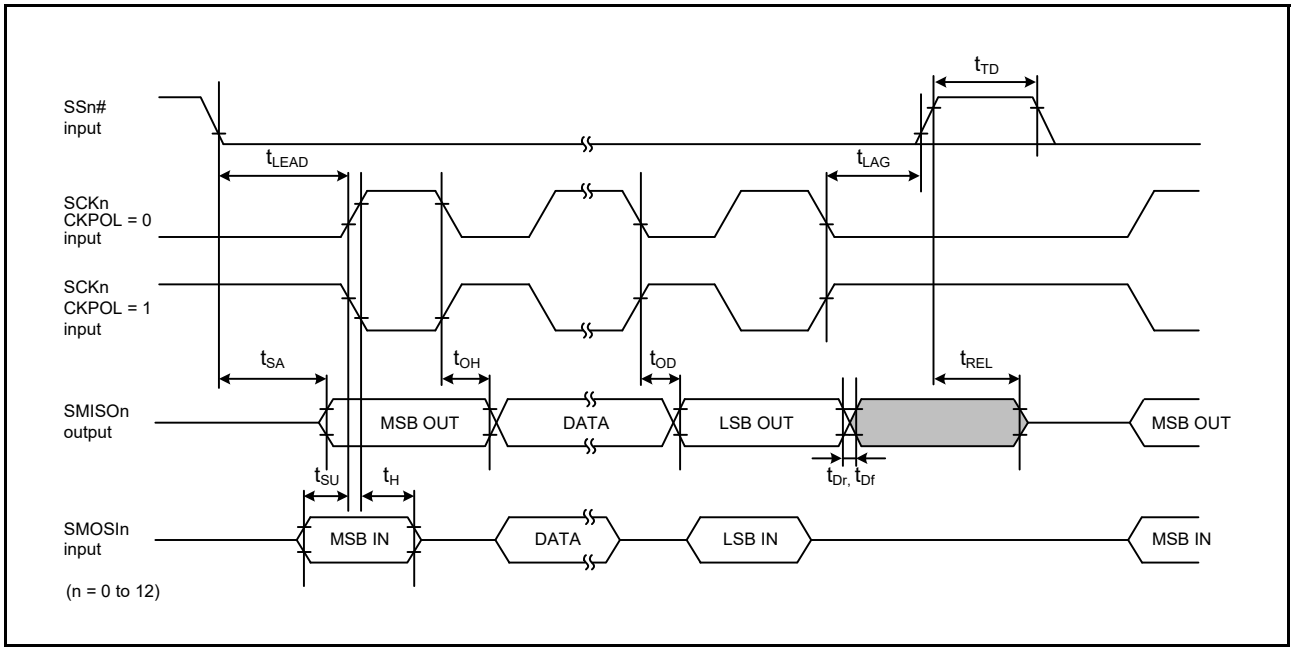


Figure 2.53 Simple SPI Timing (Slave, CKPH = 1)

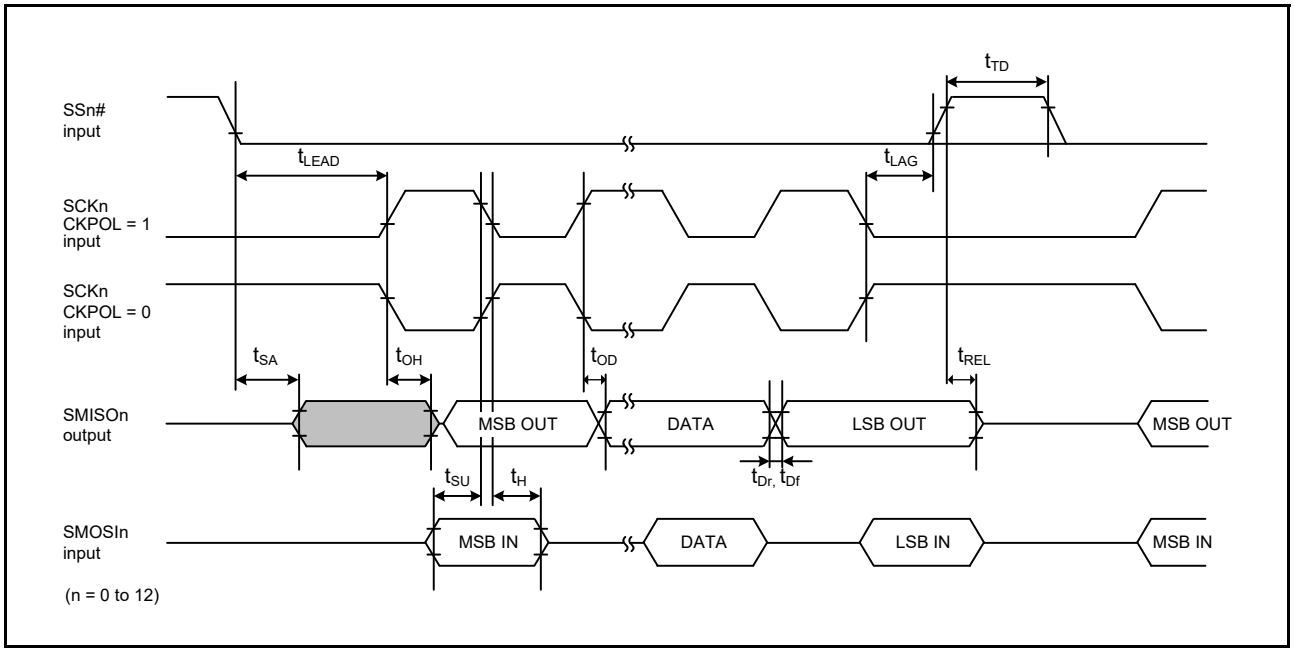


Figure 2.54 Simple SPI Timing (Slave, CKPH = 0)

2.4.7.10 RSCI

Table 2.39 RSCI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-speed interface high-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
RSCI	Input clock cycle	Asynchronous	t_{Scyc}	4	—	t_{PAcyc}	Figure 2.55
		Clock synchronous		2	—		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	—	5	ns	
	Input clock fall time		t_{SCKf}	—	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	—	t_{PAcyc}	
		Clock synchronous		2	—		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	—	5	ns	
	Output clock fall time		t_{SCKf}	—	5	ns	
	Receive data setup time	Master	t_{RXS}	0.5	—	ns	Figure 2.56
		Slave		2.5	—		
	Receive data hold time	Master	t_{RXH}	11	—	ns	
		Slave		2.5	—		
	Transmit data delay time	Master	t_{TXD}	—	4	ns	
		Slave		—	15		

Note 1. t_{PAcyc}: PCLKA cycle; t_{Scyc}: SCK cycle

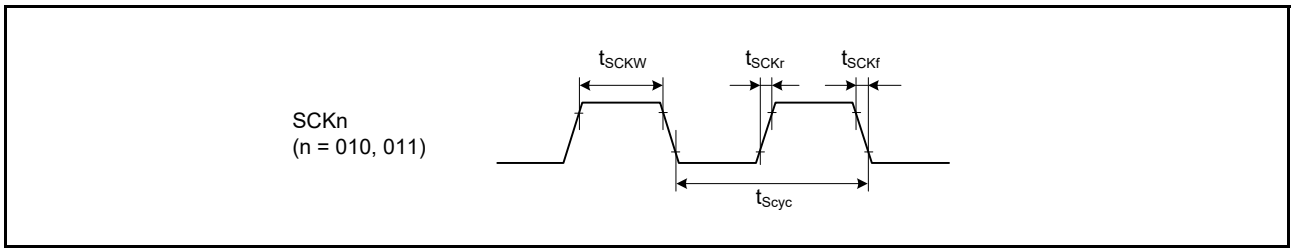


Figure 2.55 SCK Clock Input Timing

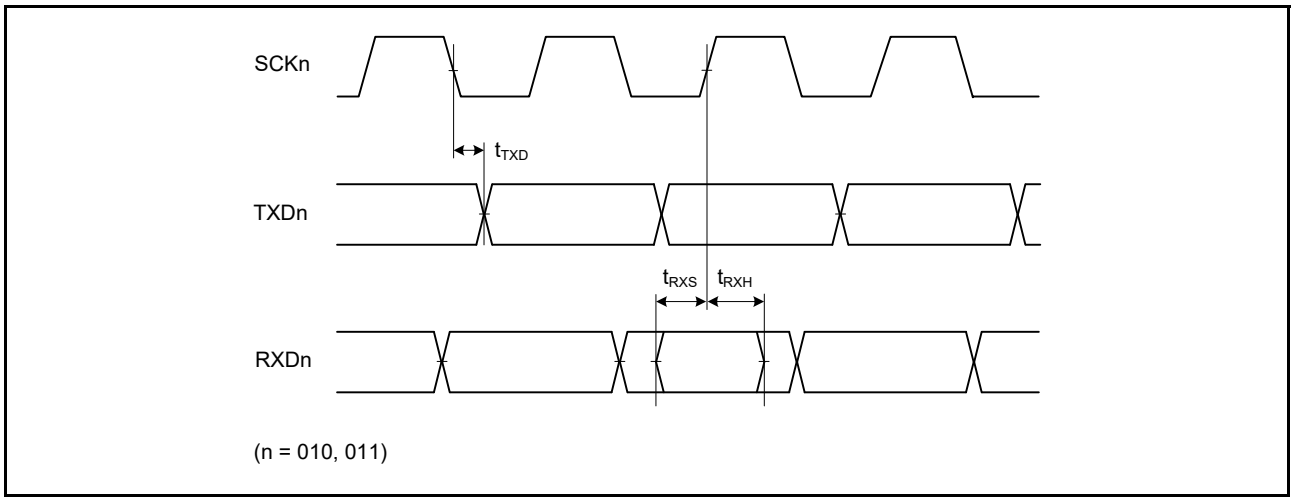


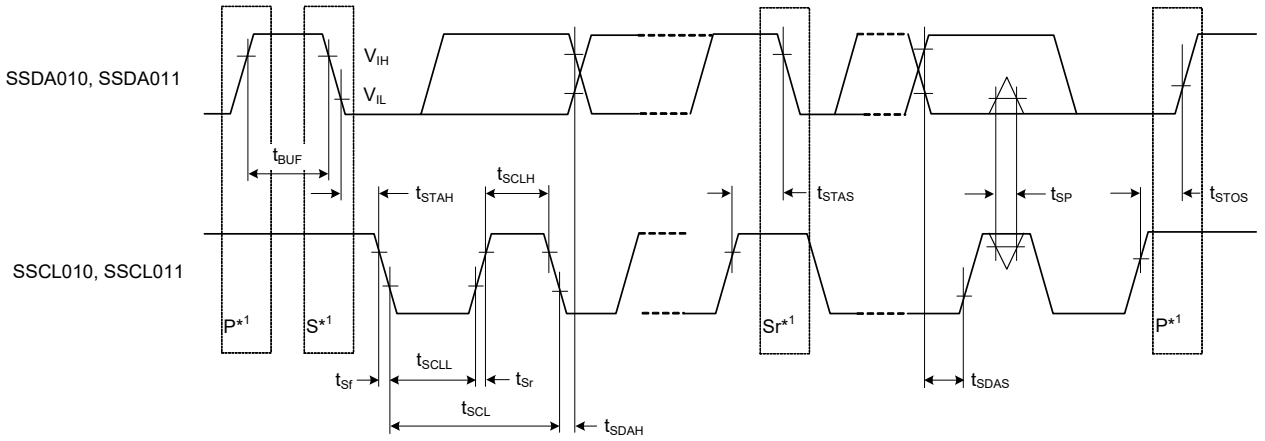
Figure 2.56 RSCI Input/Output Timing: Clock Synchronous Mode

Table 2.40 Simple IIC Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
High-speed interface high-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
Simple IIC (Standard-mode)	SSCL, SSDA input rise time	t_{Sr}	—	1000	ns	Figure 2.57
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{PAcyc}	ns	
	Data input setup time	t_{SDAS}	250	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b*1	—	400	pF	
Simple IIC (Fast-mode)	SSCL, SSDA input rise time	t_{Sr}	—	300	ns	
	SSCL, SSDA input fall time	t_{Sf}	—	300	ns	
	SSCL, SSDA input spike pulse removal time	t_{SP}	0	4 × t_{PAcyc}	ns	
	Data input setup time	t_{SDAS}	100	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b*1	—	400	pF	

Note: t_{PAcyc}: PCLKA cycle
Note 1. Cb is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC
V_{OL} = 0.6 V, I_{OL} = 6 mA

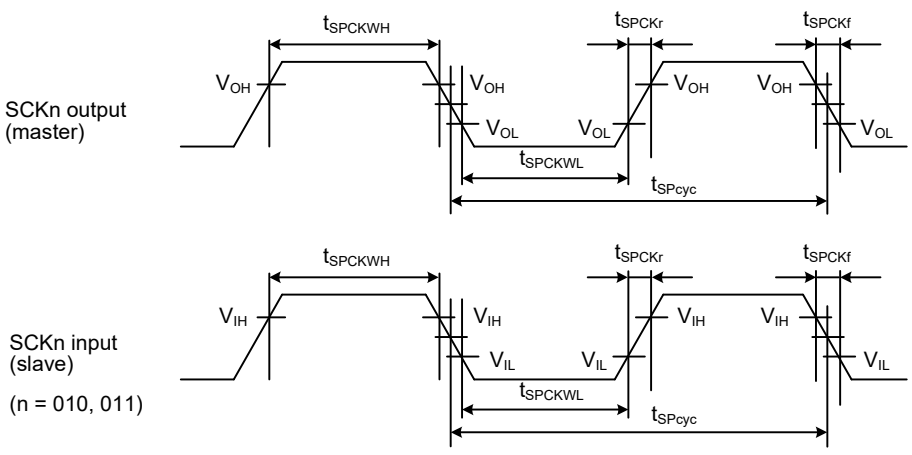
Figure 2.57 Simple IIC Bus Interface Input/Output Timing

Table 2.41 Simple SPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-speed interface high-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	2	—	t_{PAcyc}	Figure 2.58
	SCK clock cycle input (slave)			2	—		
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Input		—	1	μs	
	Data input setup time	Master	t_{SU}	0.5	—	ns	Figure 2.59 to Figure 2.62
		Slave		2.5	—		
	Data input hold time	Master	t_H	11	—	ns	
		Slave		2.5	—		
	Data output delay time	Master	t_{OD}	—	4	ns	
		Slave		—	15		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Data rise/fall time	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	—	
	Slave access time		t_{SA}	—	5	t_{PAcyc}	Figure 2.61, Figure 2.62
	Slave output release time		t_{REL}	—	5	t_{PAcyc}	
	SS input setup time		t_{LEAD}	1	—	t_{SPcyc}	Figure 2.59 to Figure 2.62
	SS input hold time		t_{LAG}	1	—	t_{SPcyc}	
	SS input rise/fall time		t_{SSLr}, t_{SSLf}	—	1	μs	

Note 1. t_{PAcyc}: PCLKA cycle



V_{OH} = 0.7 × VCC, V_{OL} = 0.3 × VCC, V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC

Figure 2.58 Simple SPI Clock Timing

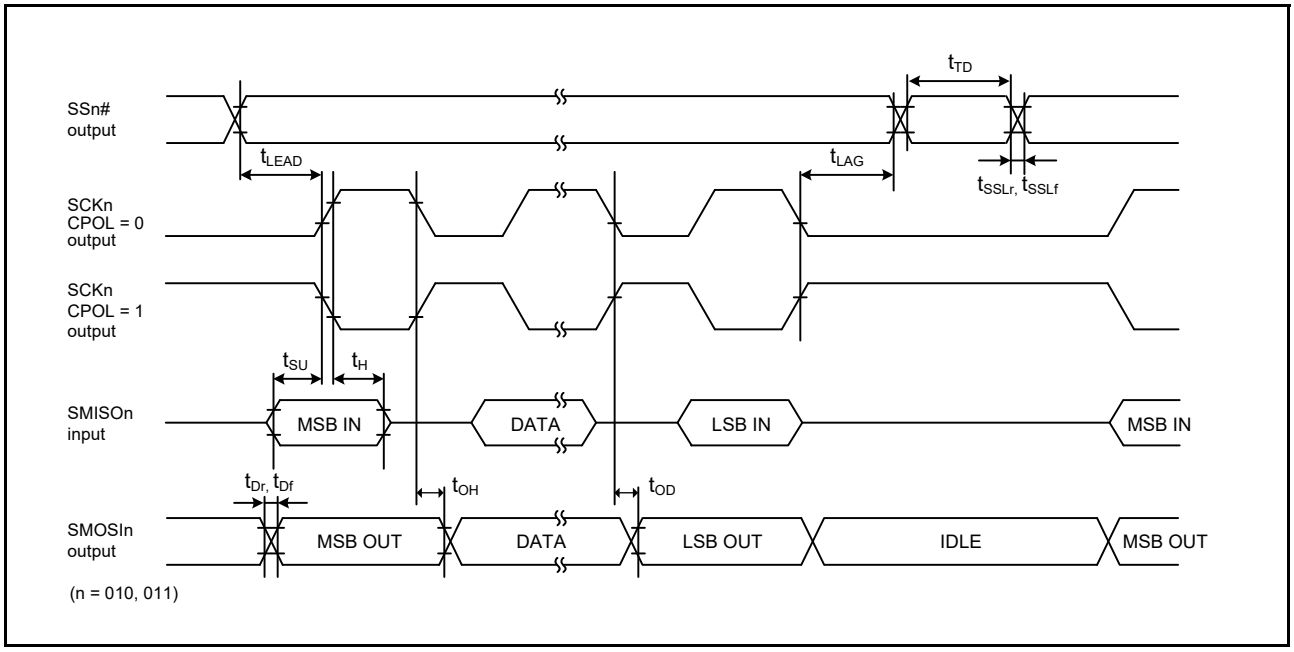


Figure 2.59 Simple SPI Timing (Master, CPHA = 0)

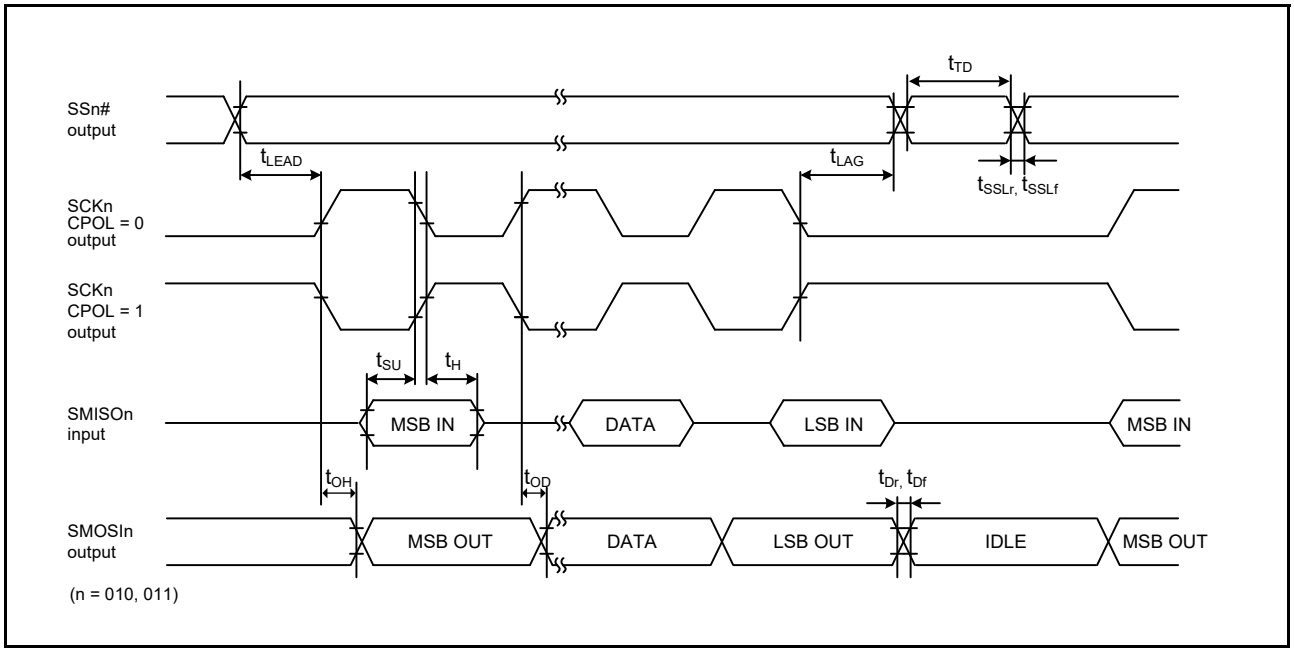


Figure 2.60 Simple SPI Timing (Master, CPHA = 1)

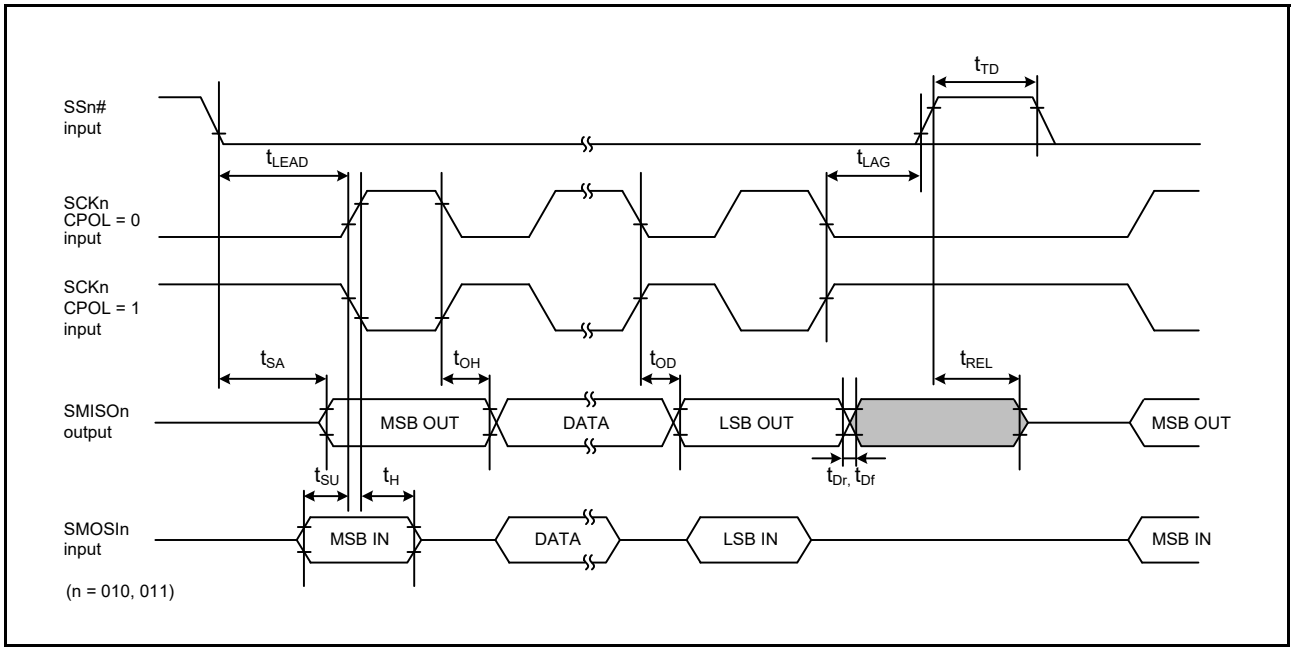


Figure 2.61 Simple SPI Timing (Slave, CPHA = 0)

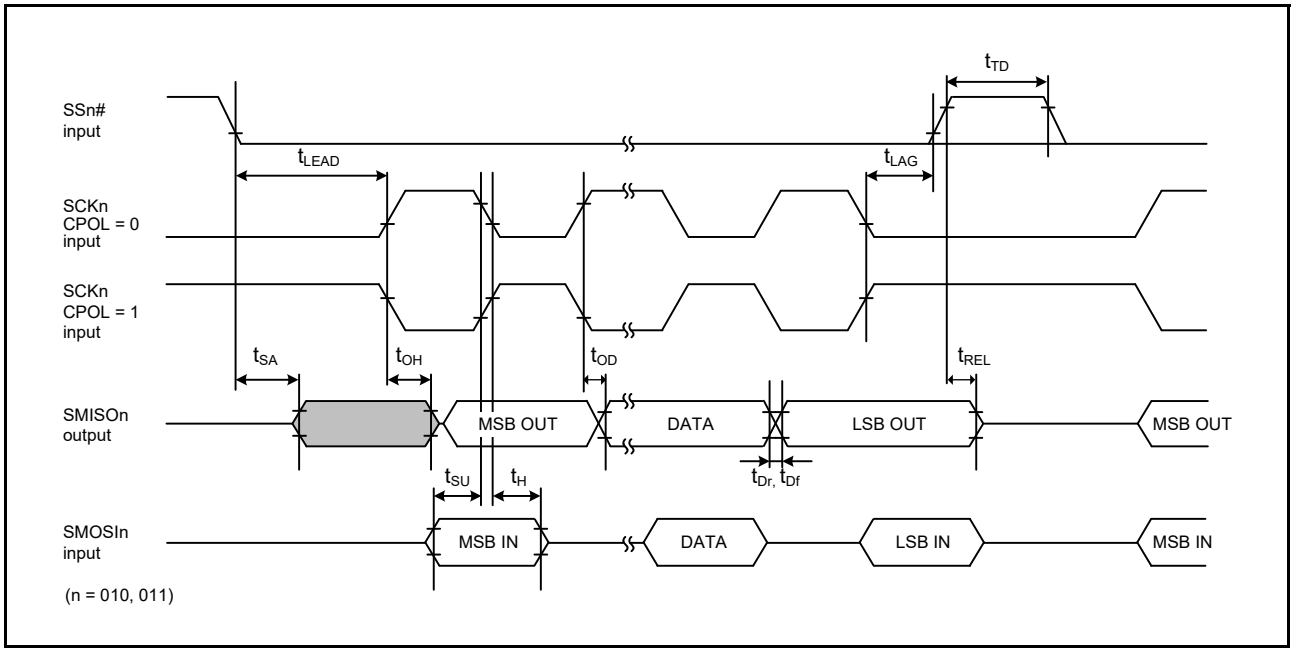


Figure 2.62 Simple SPI Timing (Slave, CPHA = 1)

2.4.7.11 SSIE

Table 2.42 Expansion Serial Sound Interface Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item			Symbol	Min.	Max.	Unit	Test Conditions
AUDIO_CLK	Cycle		t_{EXcyc}	20	—	ns	Figure 2.63
	High/low level		t_{EXL}/t_{EXH}	0.4	0.6	t_{EXcyc}	
SSIBCK0	Cycle	Master	t_O	80	—	ns	Figure 2.64
		Slave	t_I	80	—	ns	
	Output clock high level	Master	t_{HC}	0.35	—	t_O	
	Output clock low level		t_{LC}	0.35	—	t_O	
	Input clock high level	Slave	t_{HC}	0.35	—	t_I	
	Input clock low level		t_{LC}	0.35	—	t_I	
	Output clock rise time	Master	t_{RC}	—	0.15	t_O	
	Output clock fall time		t_{FC}	—	0.15	t_O	
	Input clock rise time	Slave	t_{RC}	—	0.15	t_I	
	Input clock fall time		t_{FC}	—	0.15	t_I	
SSILRCK0,SSITXD0, SSIRXD0	Input setup time	Master	t_{SR}	12	—	ns	Figure 2.65, Figure 2.66
		Slave		12	—		
	Input hold time	Master	t_{HR}	8	—	ns	
		Slave		15	—		
	Output delay time	Master	t_{DTR}	–10	5	ns	
		Slave		0	20		
	Output delay time from when an SSILRCK0 signal is changed	Slave	t_{DTRW}	—	20	ns	Figure 2.67

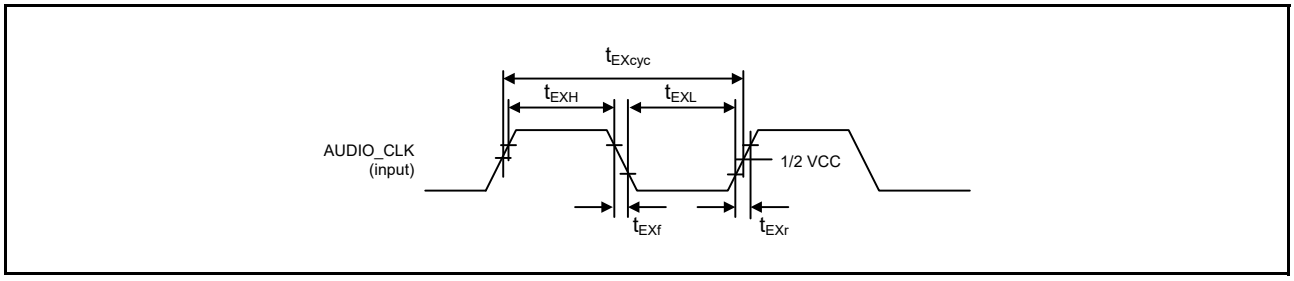


Figure 2.63 Clock Input Timing

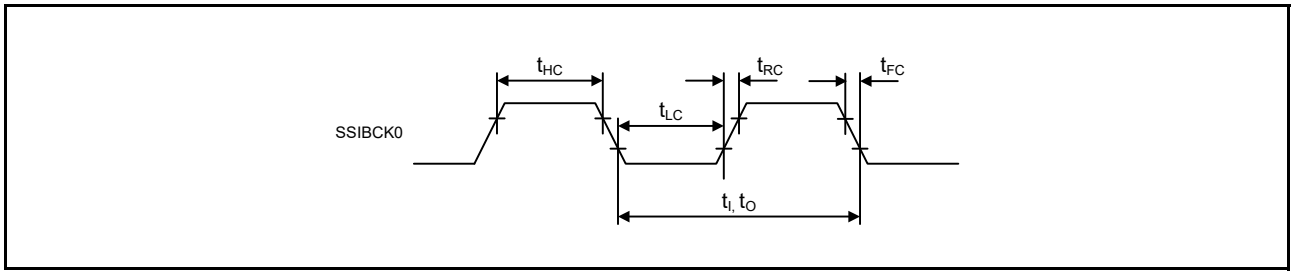


Figure 2.64 SSIE Clock Input/Output Timing

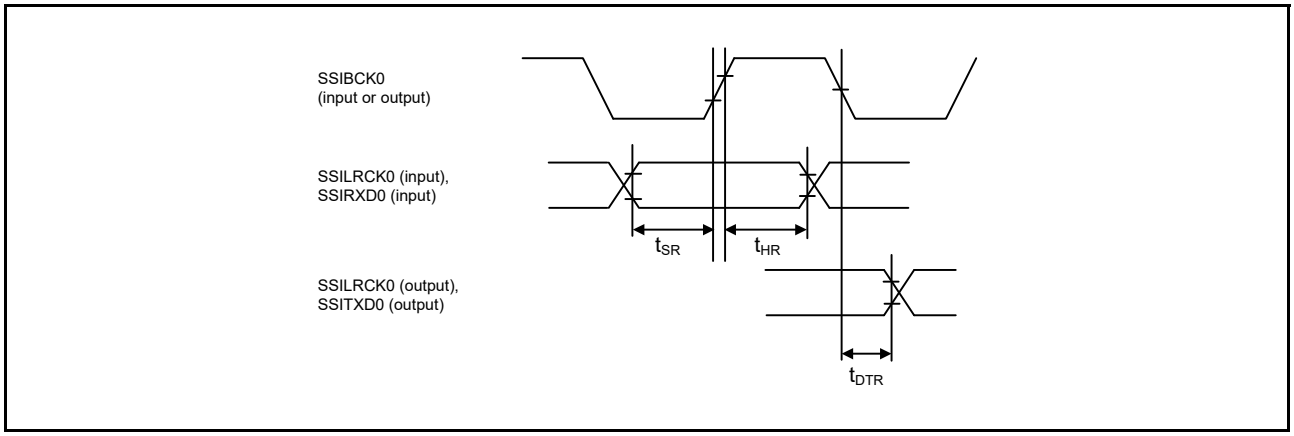


Figure 2.65 Transmission and Reception Timing for the SSIE Data When the SSICR.BCKP Bit is 0

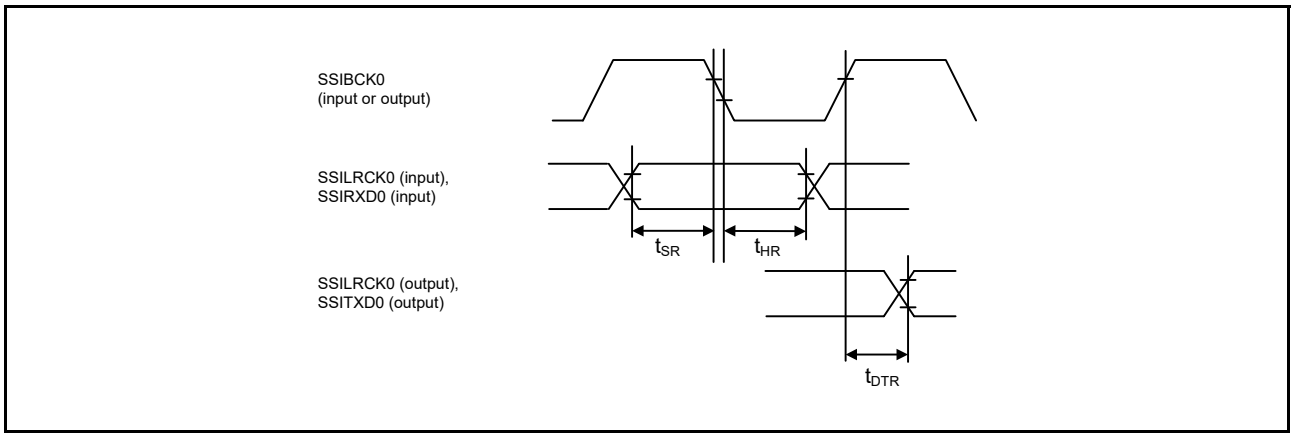


Figure 2.66 Transmission and Reception Timing for the SSIE Data When the SSICR.BCKP Bit is 1

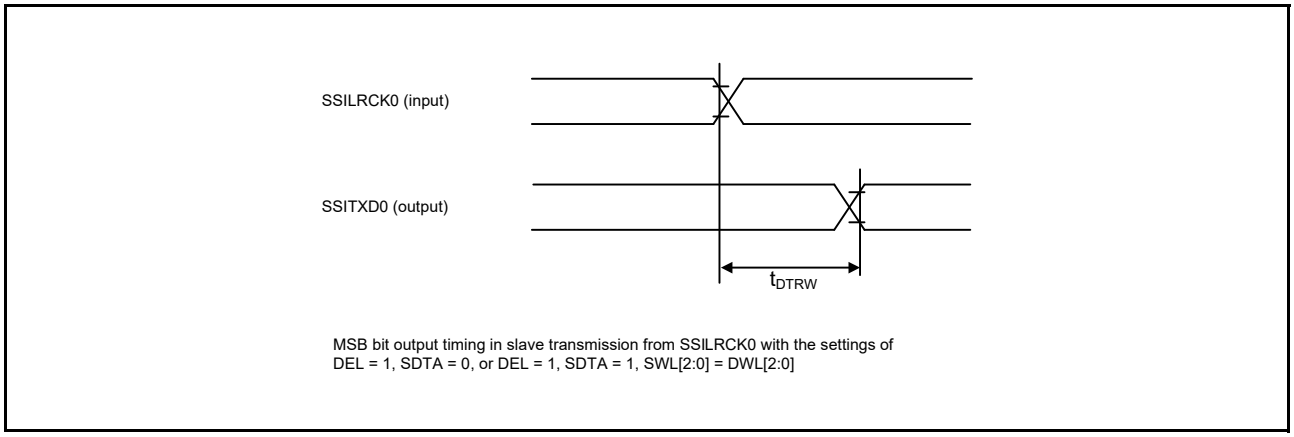


Figure 2.67 Output Delay of the SSIE Data from When an SSILRCK0 Signal is Changed

2.4.7.12 RSPI

Table 2.43 RSPI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item				Symbol	Min.*1	Max.*1	Unit*1	Test Conditions*2
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	—	t_{PAcyc}	Figure 2.68
		Slave			4	—		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2 – 3	—	ns	
		Slave			0.4	0.6	t_{SPcyc}	
	RSPCK clock low pulse width	Master		t_{SPCKWL}	(t_{SPcyc} – t_{SPCKr} – t_{SPCKf}) / 2 – 3	—	ns	
		Slave			0.4	0.6	t_{SPcyc}	
	RSPCK clock rise/fall time	Output		t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Input			—	1	μs	
	Data input setup time	Master		t_{SU}	6	—	ns	Figure 2.69 to Figure 2.74
		Slave			8.3	—		
	Data input hold time	Master	PCLKA division ratio set to 1/2	t_{HF}	0	—	ns	
			PCLKA division ratio set to a value other than 1/2	t_H	t_{PAcyc}	—	ns	
		Slave			8.3	—		
	SSL setup time	Master		t_{LEAD}	1	8	t_{SPcyc}	
		Slave			4	—	t_{PAcyc}	
	SSL hold time	Master		t_{LAG}	1	8	t_{SPcyc}	
		Slave			4	—	t_{PAcyc}	
	Data output delay time	Master		t_{OD}	—	6.3	ns	
		Slave			—	28		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	t_{SPcyc} + 2 × t_{PAcyc}	8 × t_{SPcyc} + 2 × t_{PAcyc}	ns	
		Slave			4 × t_{PAcyc}	—		
	MOSI and MISO rise/fall time	Output		t_{Dr}, t_{Df}	—	5	ns	
		Input			—	1	μs	
	SSL rise/fall time	Output		t_{SSLr}, t_{SSLf}	—	5	ns	
		Input			—	1	μs	
	Slave access time			t_{SA}	—	28	ns	Figure 2.73, Figure 2.74
	Slave output release time			t_{REL}	—	28	ns	

Note 1. t_{PAcyc}: PCLKA cycle
Note 2. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All RSPI AC timings are measured in combination with the pins in the same group.

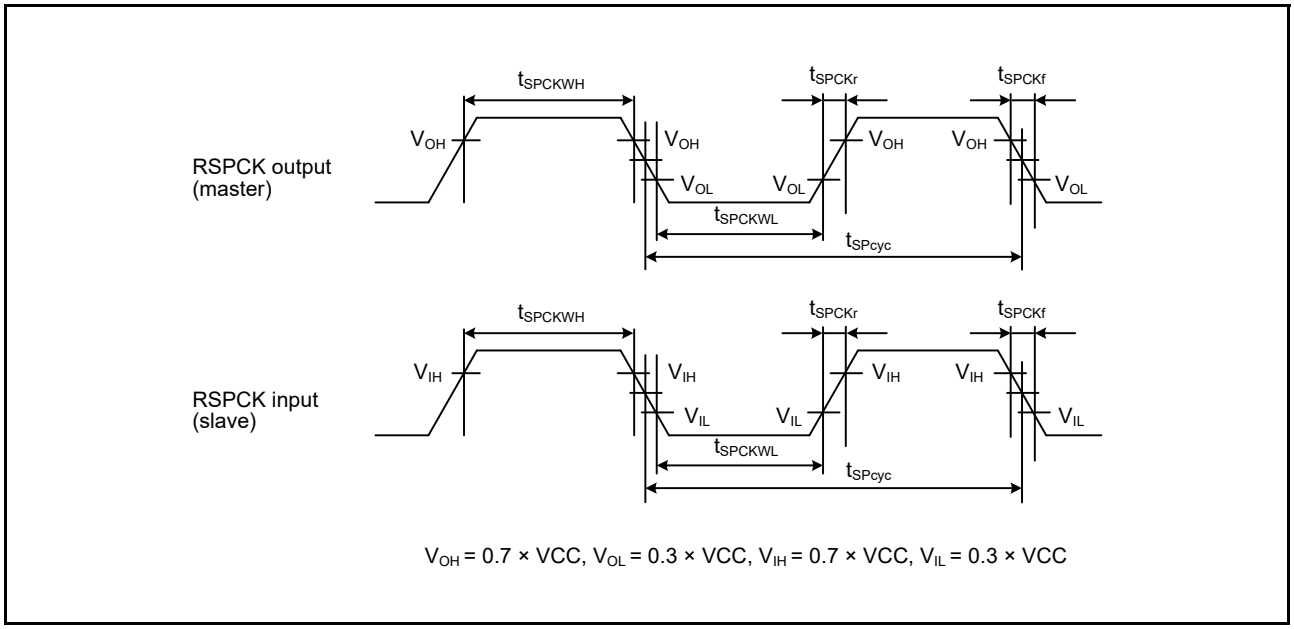


Figure 2.68 RSPI Clock Timing

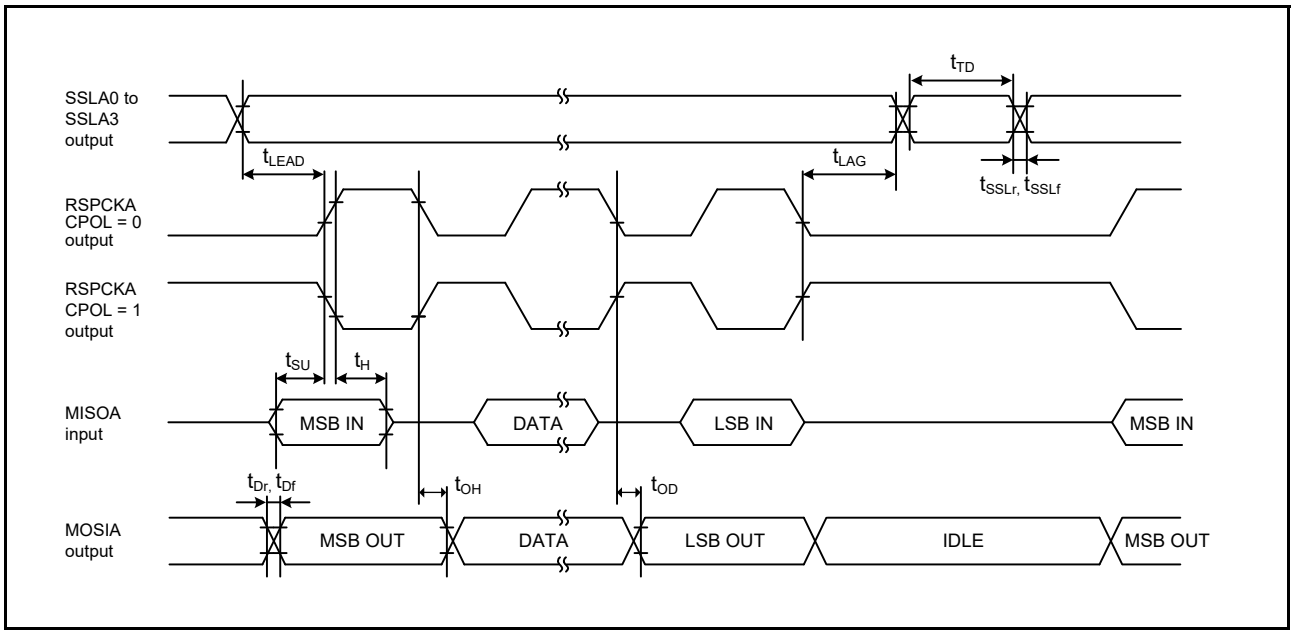


Figure 2.69 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

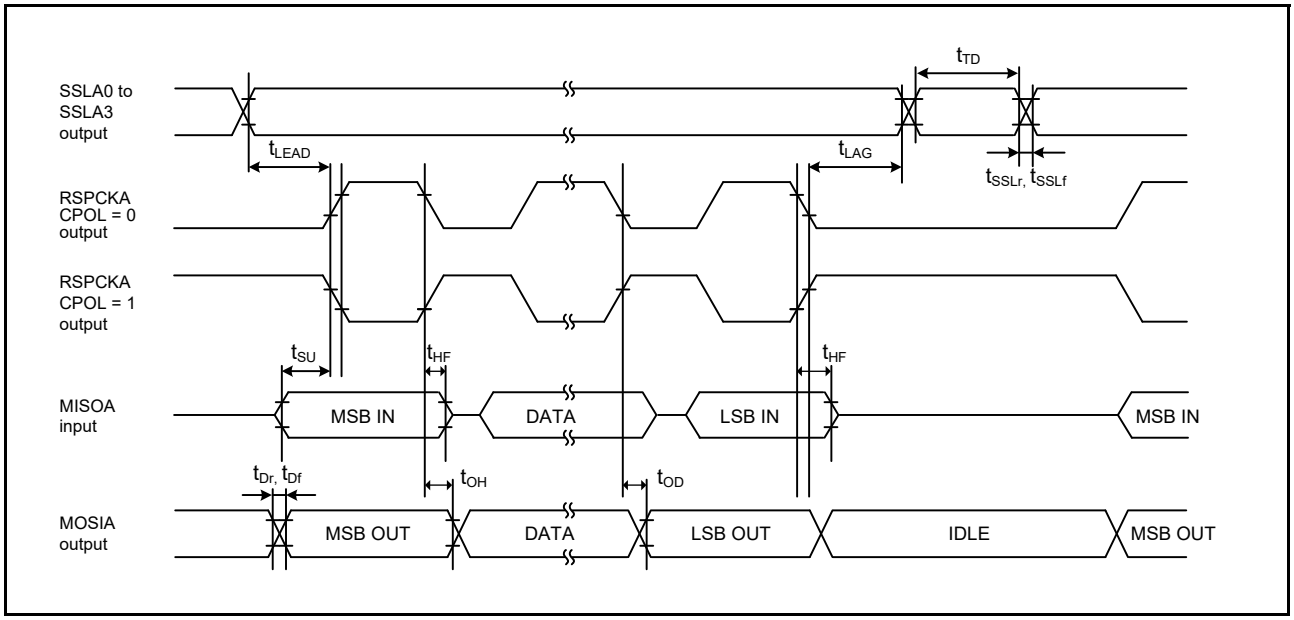


Figure 2.70 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)

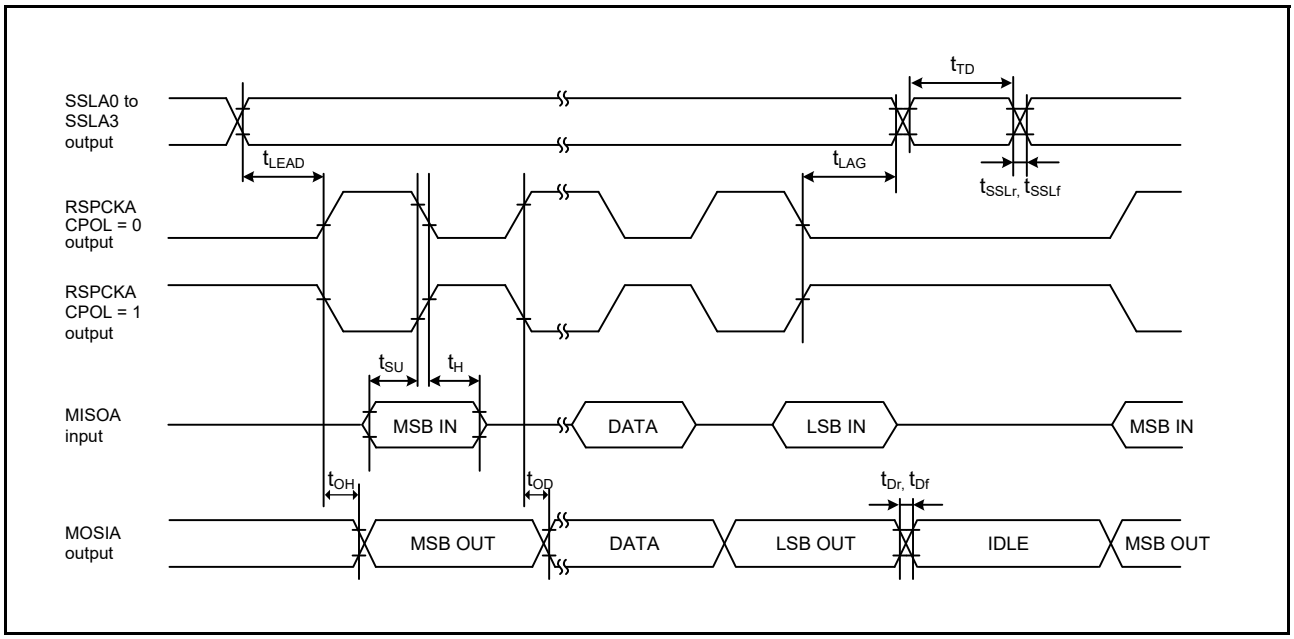


Figure 2.71 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2)

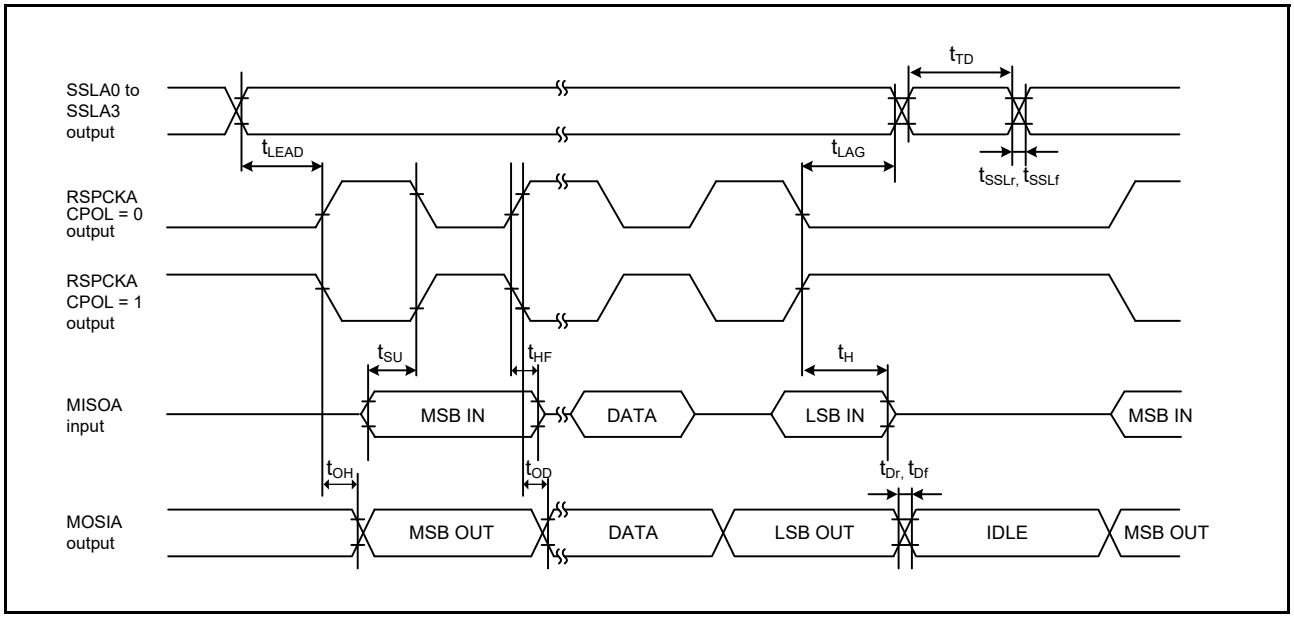


Figure 2.72 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)

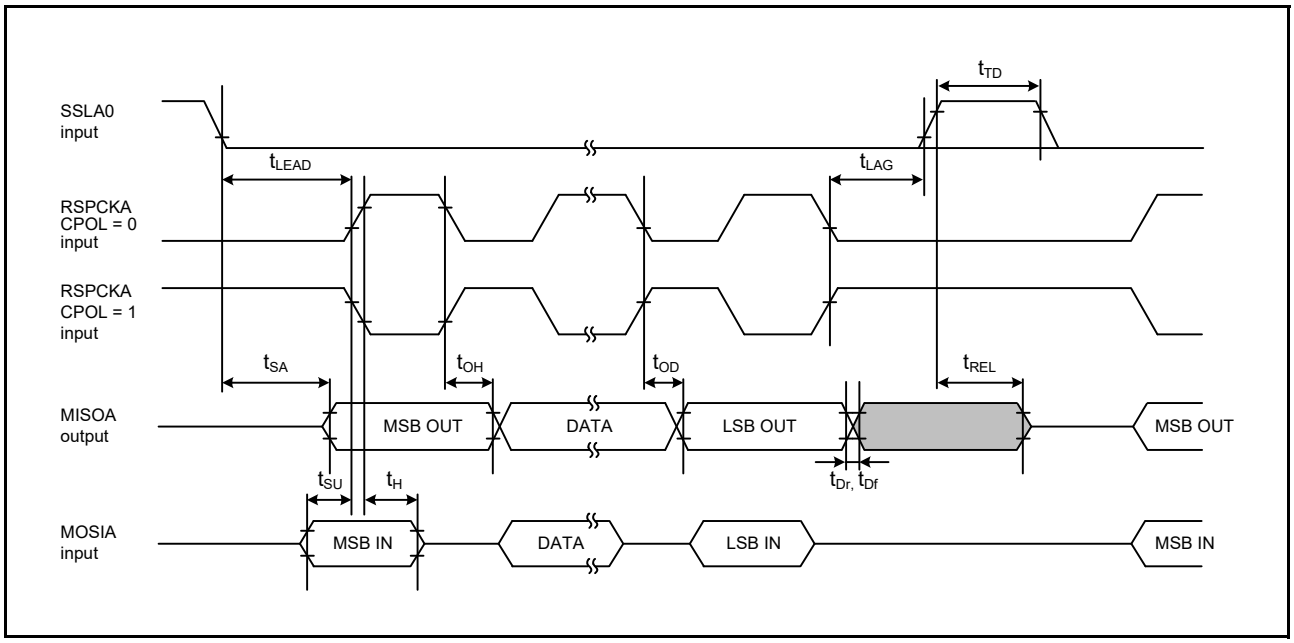


Figure 2.73 RSPI Timing (Slave, CPHA = 0)

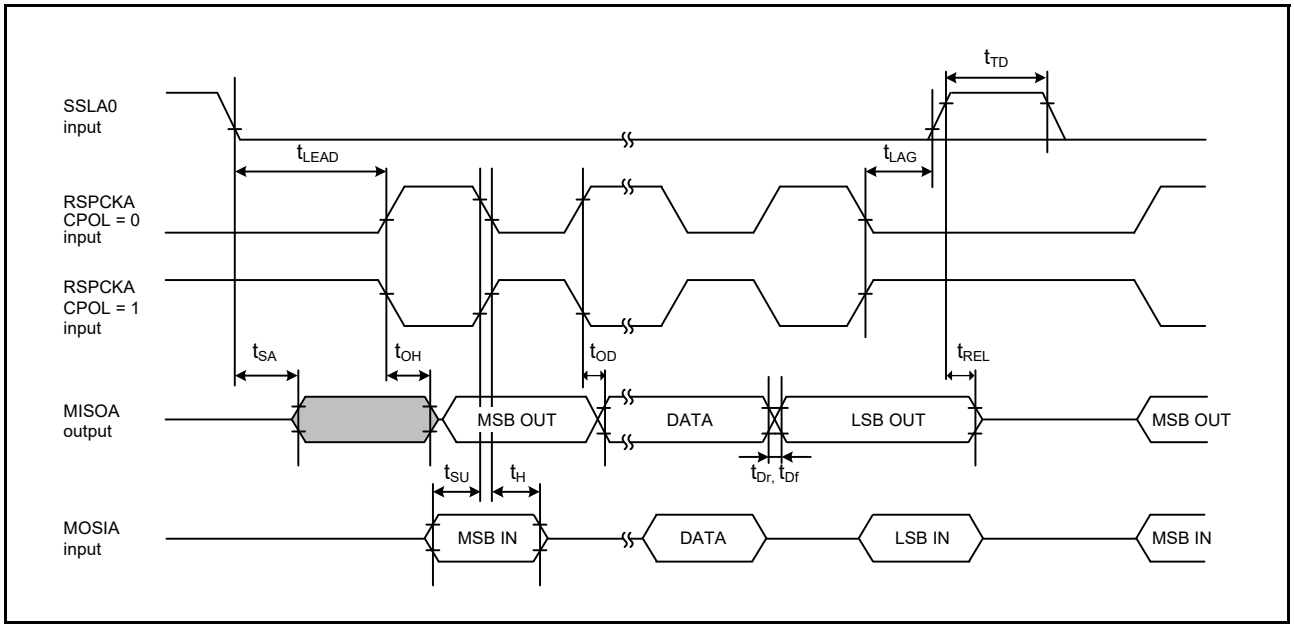


Figure 2.74 RSPI Timing (Slave, CPHA = 1)

2.4.7.13 RSPIA

Table 2.44 RSPIA Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-speed interface high-drive output is selected by the drive capacity control register.

Item			Symbol	Min.*1	Max.*1	Unit*1	Test Conditions*2
RSPI	RSPCK clock cycle	Master	t_{SPcyc}	2	—	t_{PAcyc}	Figure 2.75
		Slave		2	—		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$	—	ns	
		Slave		0.4	0.6	t_{SPcyc}	
	RSPCK clock rise/fall time	Output	t_{SPCKr}, t_{SPCKf}	—	5	ns	
		Input		—	1	µs	
	Data input setup time	Master	t_{SU}	0	—	ns	Figure 2.76 to Figure 2.82
		Slave		2.5	—		
	Data input hold time	Master	t_H	5.7	—	ns	
		Slave		2.5	—		
	SSL setup time	Master	t_{LEAD}	1	8	t_{SPcyc}	
		Slave		6	—	t_{PAcyc}	
	SSL hold time	Master	t_{LAG}	1	8	t_{SPcyc}	
		Slave		6	—	t_{PAcyc}	
	Data output delay time	Master	t_{OD}	—	4	ns	
		Slave		—	14		
	Data output hold time	Master	t_{OH}	0	—	ns	
		Slave		0	—		
	Successive transmission delay time	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{PAcyc}$	$8 \times t_{SPcyc} + 2 \times t_{PAcyc}$	ns	
		Slave		t_{SPcyc}	—		
	MOSI and MISO rise/fall time	Output	t_{Dr}, t_{Df}	—	5	ns	
		Input		—	1	µs	
	SSL rise/fall time	Output	t_{SSLr}, t_{SSLf}	—	5	ns	
		Input		—	1	µs	
	Slave access time		t_{SA}	—	20	ns	Figure 2.79, Figure 2.80
	Slave output release time		t_{REL}	—	20	ns	
	TI SSP SS input setup time	Slave	t_{TISS}	4.5	—	ns	Figure 2.81, Figure 2.82
	TI SSP SS input hold time	Slave	t_{TISH}	2.5	—	ns	
	TI SSP next-access delay time	Slave	t_{TIND}	$2 \times t_{PAcyc}$ + SLNDL × t_{PAcyc}	—	ns	
	TI SSP SS output delay time	Master	t_{TISSOD}	—	7	ns	Figure 2.78

Note 1. t_{PAcyc}: PCLKA cycle
Note 2. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All RSPIA AC timings are measured in combination with the pins in the same group.

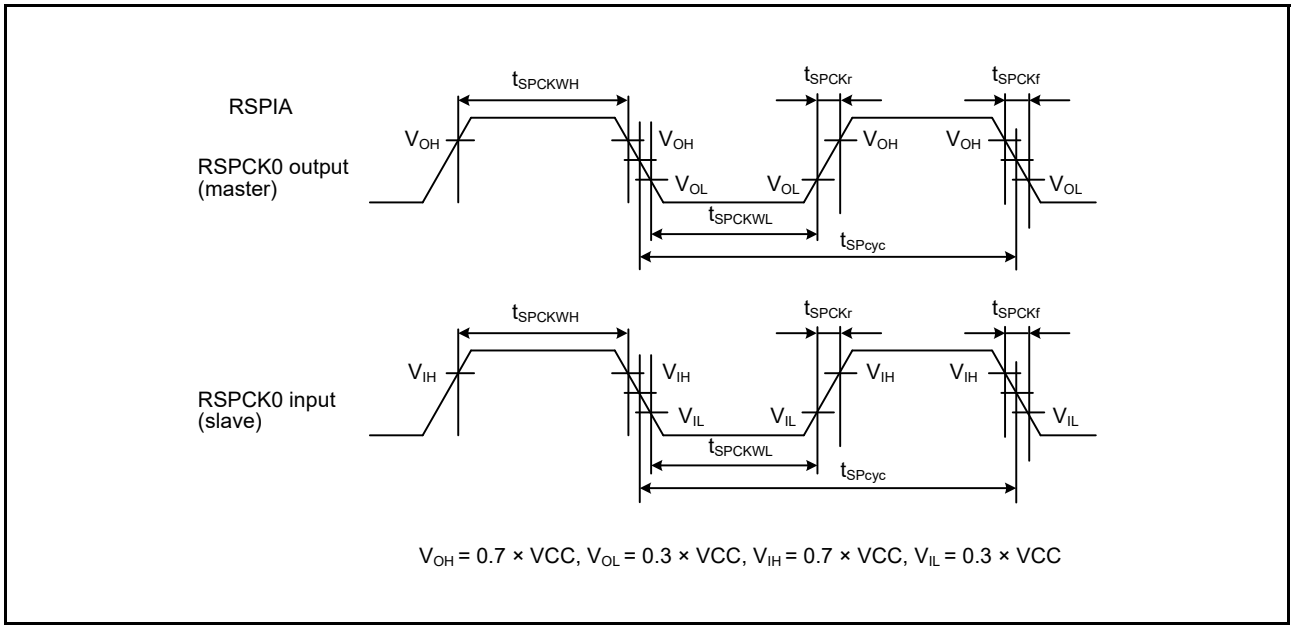


Figure 2.75 RSPIA Clock Timing

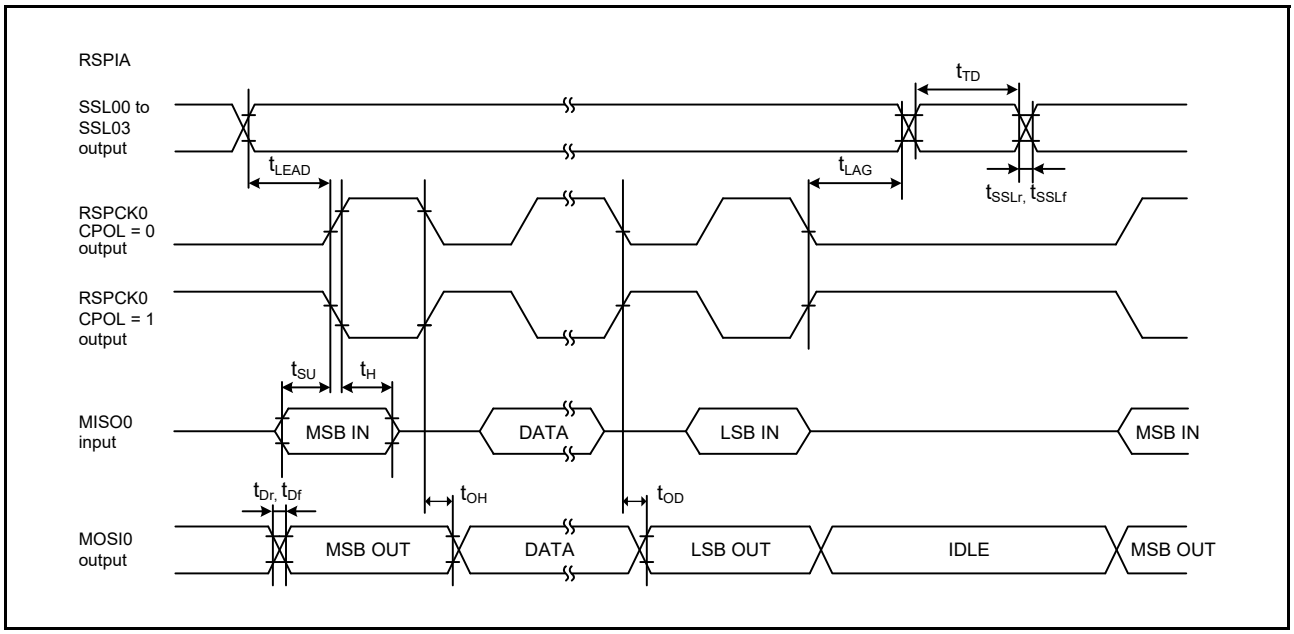


Figure 2.76 RSPIA Timing (Master, Motorola SPI, CPHA = 0)

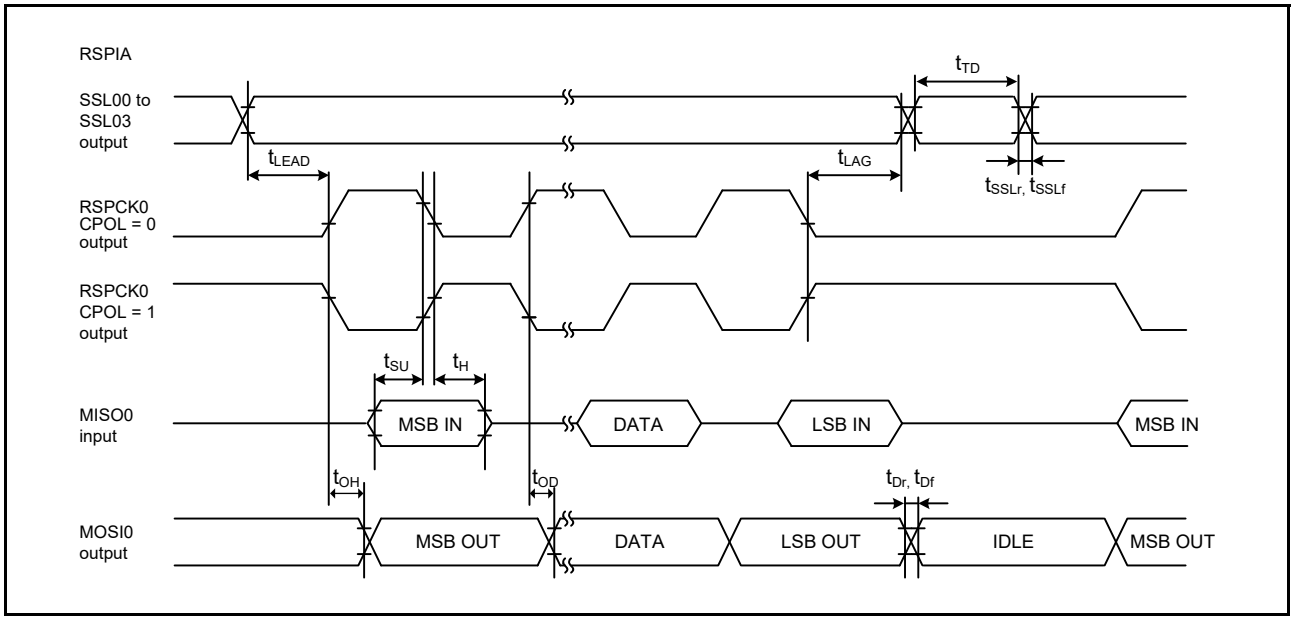


Figure 2.77 RSPIA Timing (Master, Motorola SPI, CPHA = 1)

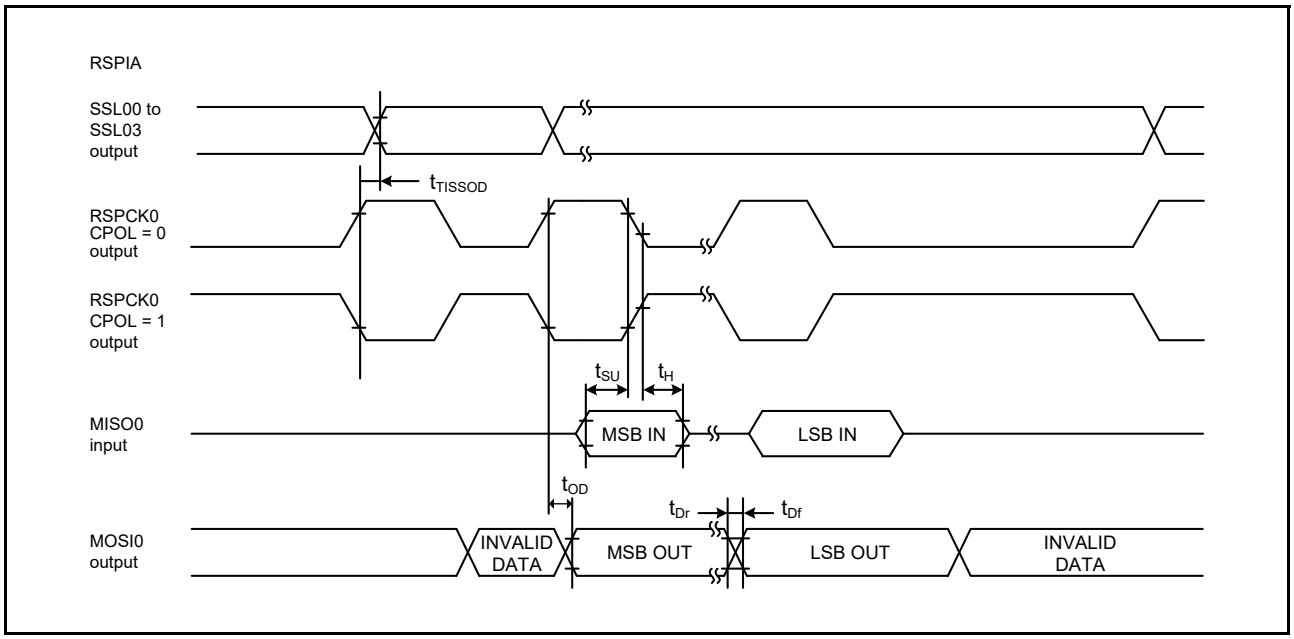


Figure 2.78 RSPIA Timing (Master, TI SSP)

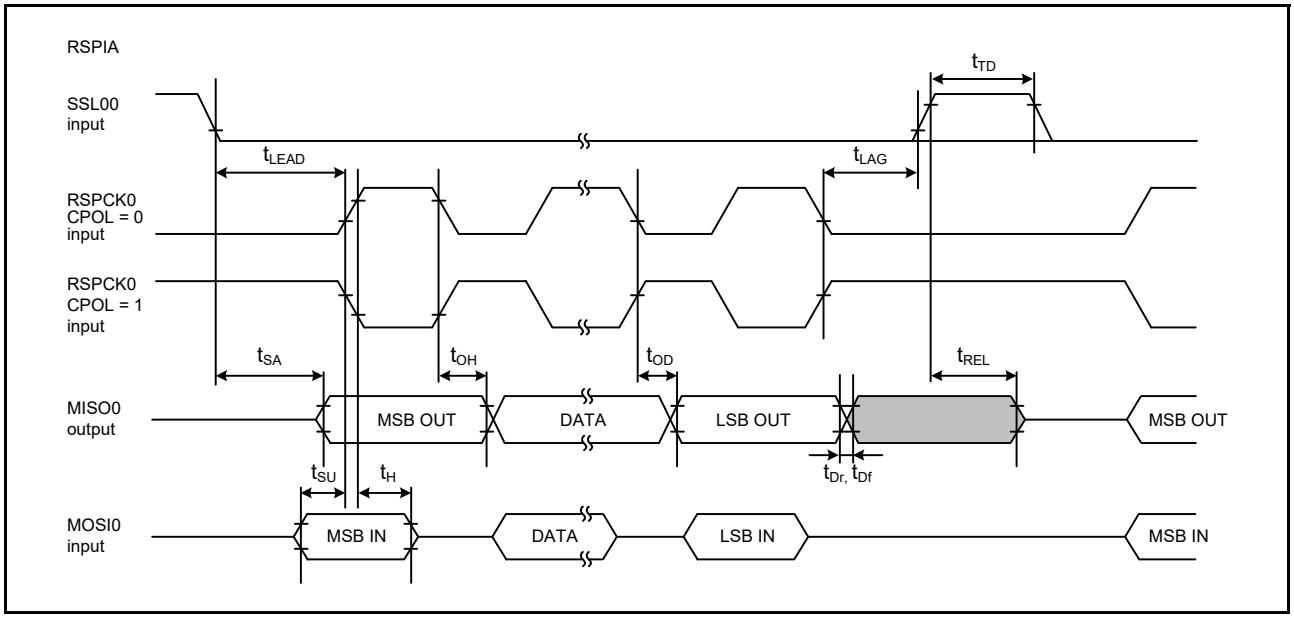


Figure 2.79 RSPIA Timing (Slave, Motorola SPI, CPHA = 0)

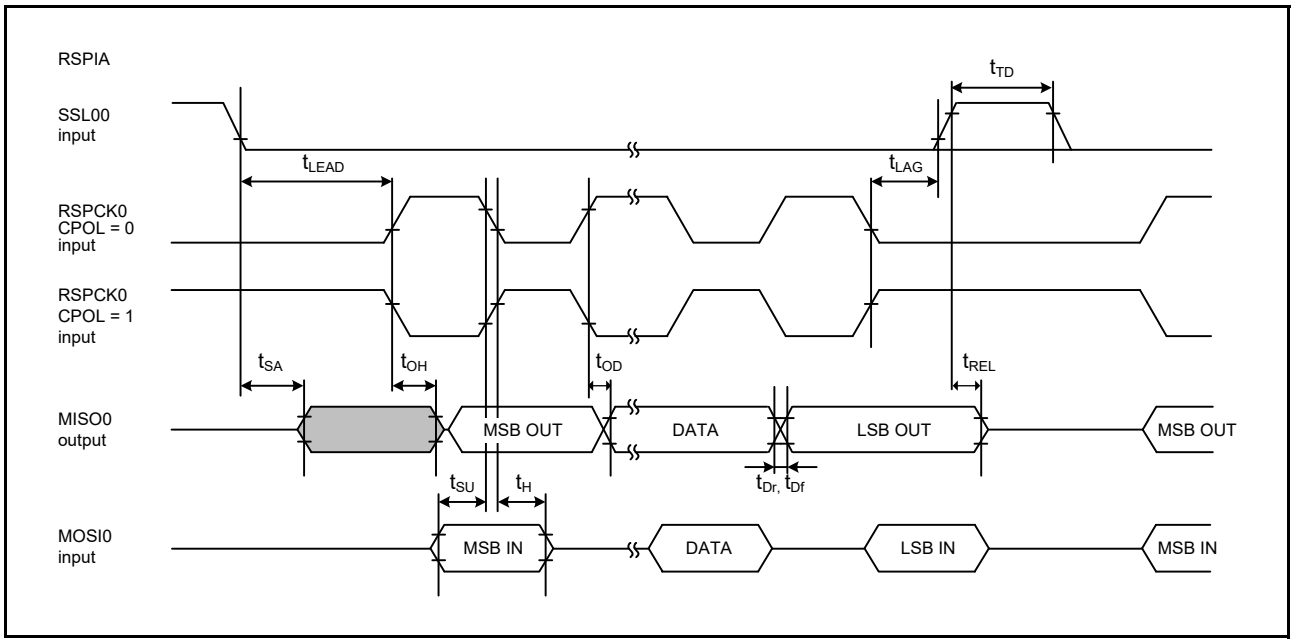


Figure 2.80 RSPIA Timing (Slave, Motorola SPI, CPHA = 1)

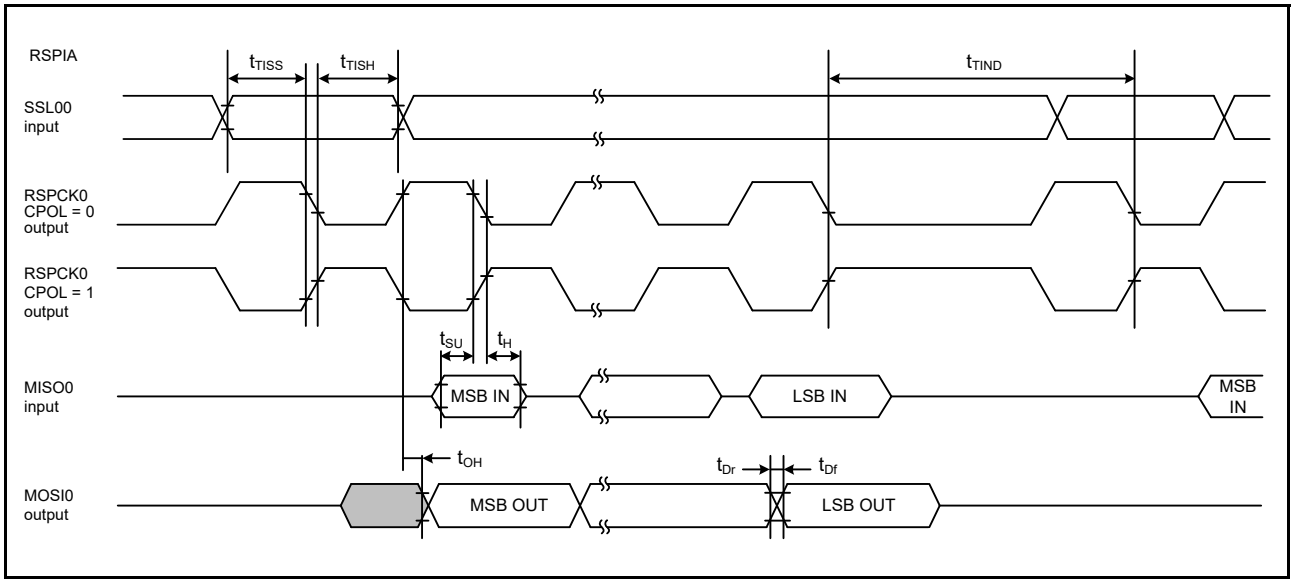


Figure 2.81 RSPIA Timing (Slave, TI SSP, Transmit with Delay between Frames)

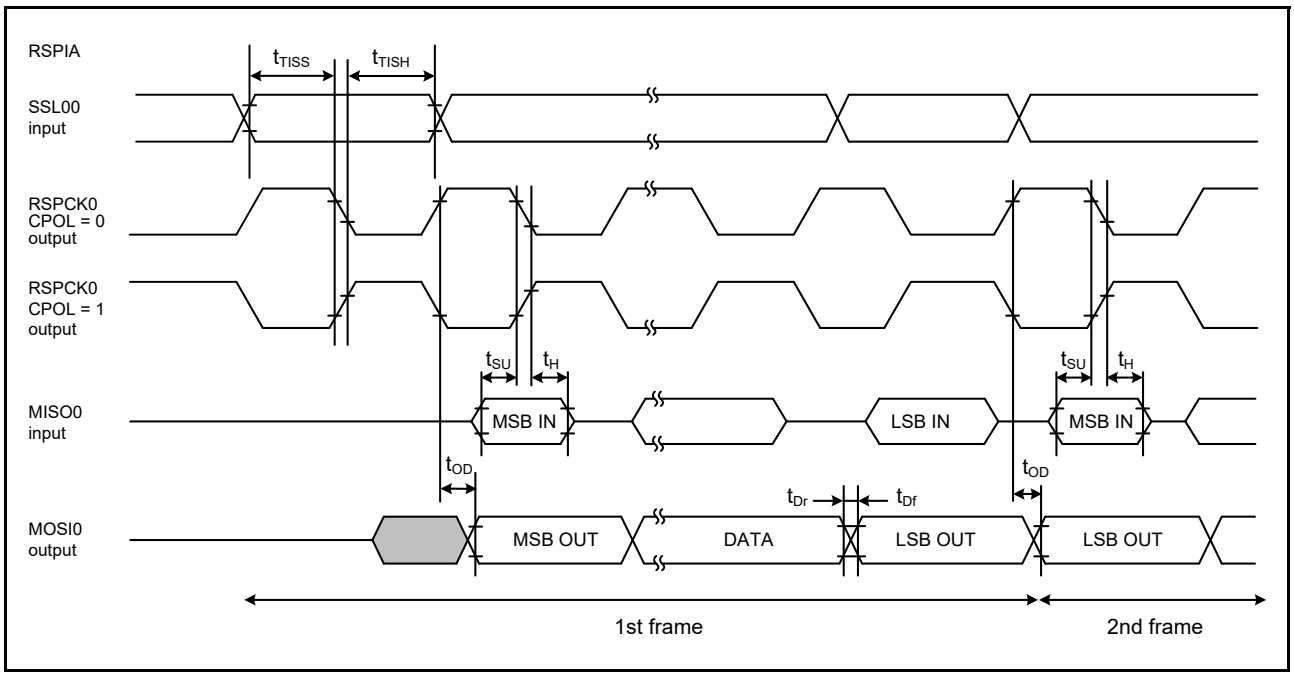


Figure 2.82 RSPIA Timing (Slave, TI SSP, Transmit with No Delay between Frames)

2.4.7.14 QSPIX

Table 2.45 QSPIX Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
ICLK = 8 to 120 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-speed interface high-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions
QSPIX	QSPCLK clock cycle	t_{QScyc}	2	48	t_{Icyc}*1	Figure 2.83
	QSPCLK clock high pulse width	t_{QSWH}	t_{QScyc} × 0.4	—	ns	
	QSPCLK clock low pulse width	t_{QSWL}	t_{QScyc} × 0.4	—	ns	
	Data input setup time	t_{Su}	8	—	ns	Figure 2.84
	Data input hold time	t_{IH}	0	—	ns	
	QSSL setup time	t_{LEAD}	(N + 0.5) × t_{QScyc} – 5*2	(N + 0.5) × t_{QScyc} + 100*2	ns	
	QSSL hold time	t_{LAG}	(N + 0.5) × t_{QScyc} – 5*3	(N + 0.5) × t_{QScyc} + 100*3	ns	
	Data output delay time	t_{OD}	—	4	ns	
	Data output hold time	t_{OH}	–3.3	—	ns	
	Successive transmission delay time	t_{TD}	1	16	t_{QScyc}	

Note 1. t_{Icyc}: ICLK cycle
Note 2. N: Value of the SPSSCR.SSSU bit (0 or 1)
Note 3. N: Value of the SPSSCR.SSHLD bit (0 or 1)

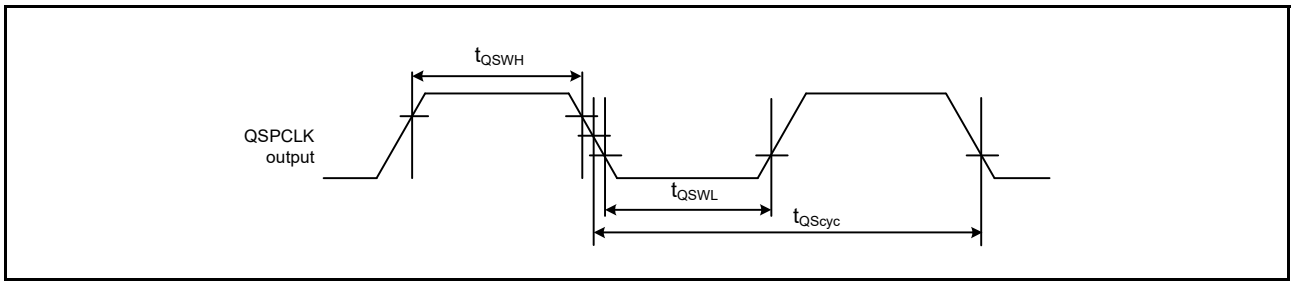


Figure 2.83 QSPIX Clock Timing

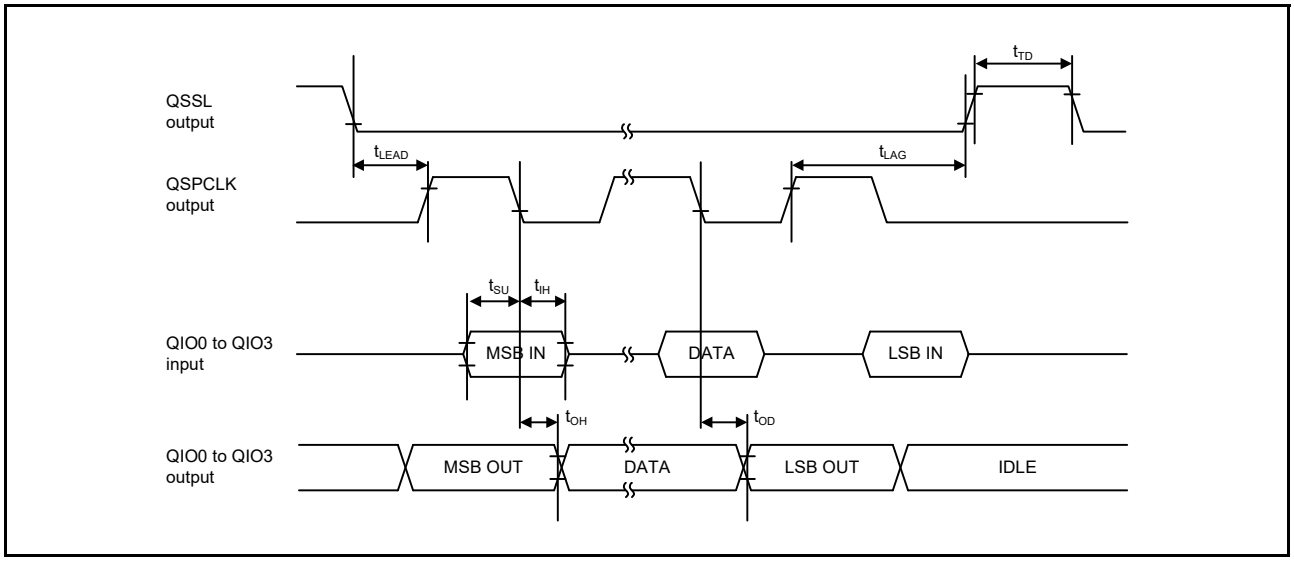


Figure 2.84 Transmit/Receive Timing

2.4.7.15 RIIC

Table 2.46 RIIC Timing (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIIC (Standard-mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 1300	—	ns	Figure 2.85
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	1000	ns	
	SCL, SDA input fall time	t_{Sf}	—	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	
RIIC (Fast-mode) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 600	—	ns	
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. C_b is the total capacitance of the bus lines.

Table 2.47 RIIC Timing (2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6(12) × t_{IICcyc} + 240	—	ns	Figure 2.85
	SCL input high pulse width	t_{SCLH}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL input low pulse width	t_{SCLL}	3(6) × t_{IICcyc} + 120	—	ns	
	SCL, SDA input rise time	t_{Sr}	—	120	ns	
	SCL, SDA input fall time	t_{Sf}	—	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDA input bus free time	t_{BUF}	3(6) × t_{IICcyc} + 120	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 120	—	ns	
	Repeated START condition input setup time	t_{STAS}	120	—	ns	
	STOP condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 20	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b*2	—	550	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycle
Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.
Note 2. C_b is the total capacitance of the bus lines.

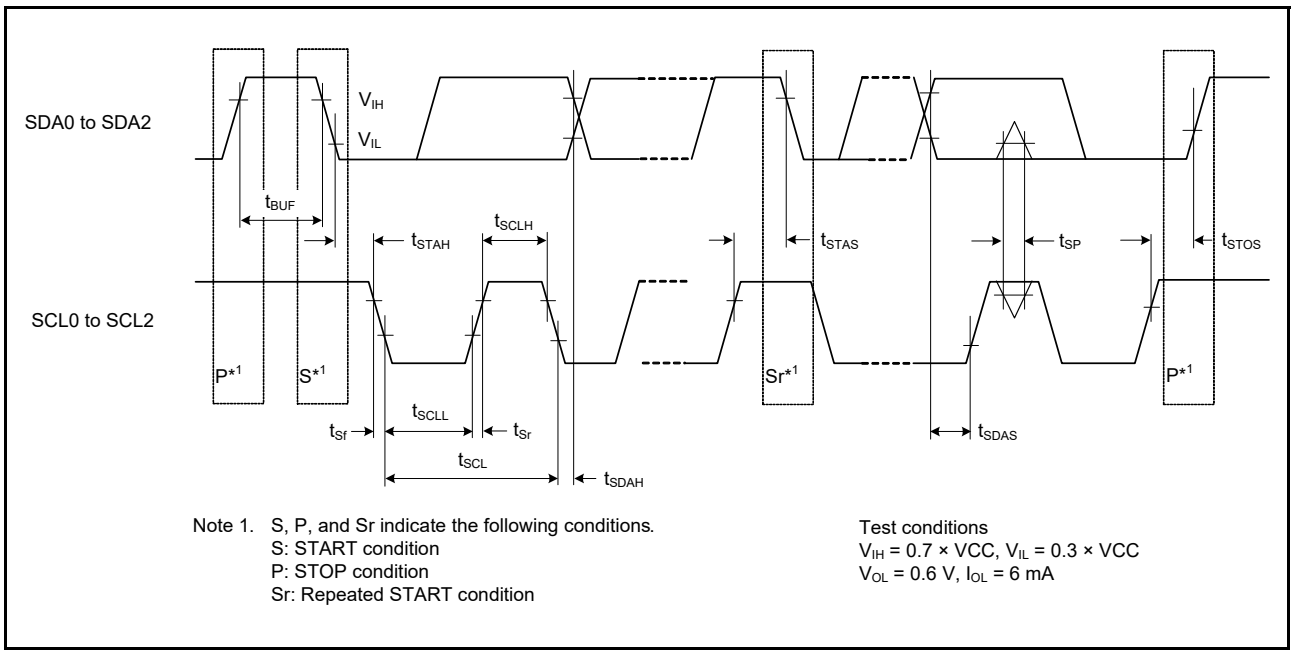


Figure 2.85 RIIC Bus Interface Input/Output Timing

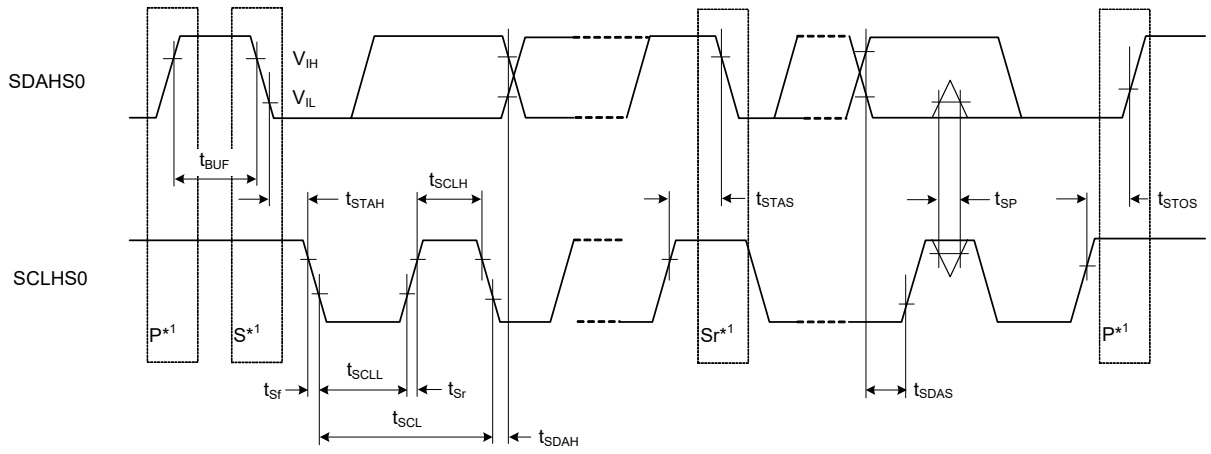
2.4.7.16 RIICHS

Table 2.48 RIICHS Timing (1)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
RIICHS (Standard-mode, SMBus) ICFER.FMPE = 0	SCLHS input cycle time	t_{SCL}	10(18) × t_{IICcyc} + 1300	—	ns	Figure 2.86
	SCLHS input high pulse width	t_{SCLH}	5(9) × t_{IICcyc} + 300	—	ns	
	SCLHS input low pulse width	t_{SCLL}	5(9) × t_{IICcyc} + 300	—	ns	
	SCLHS, SDAHS input rise time	t_{Sr}	—	1000	ns	
	SCLHS, SDAHS input fall time	t_{Sf}	—	300	ns	
	SCLHS, SDAHS input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDAHS input bus free time	t_{BUF}	5(9) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	1000	—	ns	
	STOP condition input setup time	t_{STOS}	1000	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCLHS, SDAHS capacitive load	C_b*2	—	400	pF	
RIICHS (Fast-mode) ICFER.FMPE = 0	SCLHS input cycle time	t_{SCL}	10(18) × t_{IICcyc} + 600	—	ns	
	SCLHS input high pulse width	t_{SCLH}	5(9) × t_{IICcyc} + 300	—	ns	
	SCLHS input low pulse width	t_{SCLL}	5(9) × t_{IICcyc} + 300	—	ns	
	SCLHS, SDAHS input rise time	t_{Sr}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCLHS, SDAHS input fall time	t_{Sf}	20 × (External pull-up voltage/5.5V)	300	ns	
	SCLHS, SDAHS input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDAHS input bus free time	t_{BUF}	5(9) × t_{IICcyc} + 300	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition input setup time	t_{STAS}	300	—	ns	
	STOP condition input setup time	t_{STOS}	300	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCLHS, SDAHS capacitive load	C_b*2	—	400	pF	
RIICHS (Fast-mode+) ICFER.FMPE = 1	SCLHS input cycle time	t_{SCL}	10(18) × t_{IICcyc} + 240	—	ns	
	SCLHS input high pulse width	t_{SCLH}	5(9) × t_{IICcyc} + 120	—	ns	
	SCLHS input low pulse width	t_{SCLL}	5(9) × t_{IICcyc} + 120	—	ns	
	SCLHS, SDAHS input rise time	t_{Sr}	—	120	ns	
	SCLHS, SDAHS input fall time	t_{Sf}	—	120	ns	
	SCLHS, SDAHS input spike pulse removal time	t_{SP}	0	1(4) × t_{IICcyc}	ns	
	SDAHS input bus free time	t_{BUF}	5(9) × t_{IICcyc} + 120	—	ns	
	START condition input hold time	t_{STAH}	t_{IICcyc} + 120	—	ns	
	Repeated START condition input setup time	t_{STAS}	120	—	ns	
	STOP condition input setup time	t_{STOS}	120	—	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 20	—	ns	
	Data input hold time	t_{SDAH}	0	—	ns	
	SCLHS, SDAHS capacitive load	C_b*2	—	550	pF	

Note: t_{IICcyc}: RIICHS internal reference clock (IICφ) cycle
Note 1. The value within parentheses is applicable when the value of the ICICR.NF[3:0] bits is 0011b while the digital filter is enabled by the setting ICICR.NFE = 1.
Note 2. C_b is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions.
S: START condition
P: STOP condition
Sr: Repeated START condition

Test conditions
V_{IH} = 0.7 × VCC, V_{IL} = 0.3 × VCC
V_{OL} = 0.6 V, I_{OL} = 6 mA

Figure 2.86 RIICHS Bus Interface Input/Output Timing

Table 2.49 RIICHS Timing (2) (1/2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item			Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions
RIICHS (Hs-mode) ICFER.HSME = 1	SCLHS input cycle time		t_{SCL}	10(12) × t_{IICcyc} + 80	—	—	ns	Figure 2.87
	SCLHS input high pulse width		t_{SCLH}	5(6) × t_{IICcyc}	—	—	ns	
	SCLHS input low pulse width		t_{SCLL}	5(6) × t_{IICcyc}	—	—	ns	
	SCLHS input rise time	C_b = 400pF	t_{SrCL}	—	—	80	ns	
		C_b = 100pF		—	—	40		
	SDAHS input rise time	C_b = 400pF	t_{SrDA}	—	—	160	ns	
		C_b = 100pF		—	—	80		
	SCLHS input fall time	C_b = 400pF	t_{SfCL}	—	—	80	ns	
		C_b = 100pF		—	—	40		
	SDAHS input fall time	C_b = 400pF	t_{SfDA}	—	—	160	ns	
		C_b = 100pF		—	—	80		
	SCLHS, SDAHS input spike pulse removal time		t_{SP}	0	—	1(1) × t_{IICcyc}	ns	Figure 2.86
	SDAHS input bus free time		t_{BUF}	5(6) × t_{IICcyc} + 40	—	—	ns	
	START condition input hold time		t_{STAH}	t_{IICcyc} + 40	—	—	ns	Figure 2.87
	Repeated START condition input setup time		t_{STAS}	40	—	—	ns	
	STOP condition input setup time		t_{STOS}	40	—	—	ns	
	Data input setup time		t_{SDAS}	10	—	—	ns	
	Data input hold time	C_b = 400pF	t_{SDAH}	0	—	150	ns	
		C_b = 100pF		0	—	70		
	SCLHS, SDAHS capacitive load		C_b*2	—	—	400	pF	

Table 2.49 RIICHS Timing (2) (2/2)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item			Symbol	Min.*1	Typ.	Max.	Unit	Test Conditions
RIICHS (Hs-mode) ICFER.HSME = 1	SCLHS output minimum high pulse width	C_b = 400pF	$t_{SCLH(min)}$	—	120	233	ns	Figure 2.87
		C_b = 100pF		—	60	150		
	SCLHS output minimum low pulse width	C_b = 400pF	$t_{SCLL(min)}$	—	—	320	ns	
		C_b = 100pF		—	—	160		

Note: t_{IICcyc}: RIICHS internal reference clock (IICφ) cycle

Note 1. The value within parentheses is applicable when the value of the ICICR.NF[3:0] bits is 0011b while the digital filter is enabled by the setting ICICR.NFE = 1. Note that, in Hs-mode, the lower-order 2 bits of the NF[3:0] bits are ignored and the number of stages in the digital filter is single.

Note 2. C_b is the total capacitance of the bus lines.

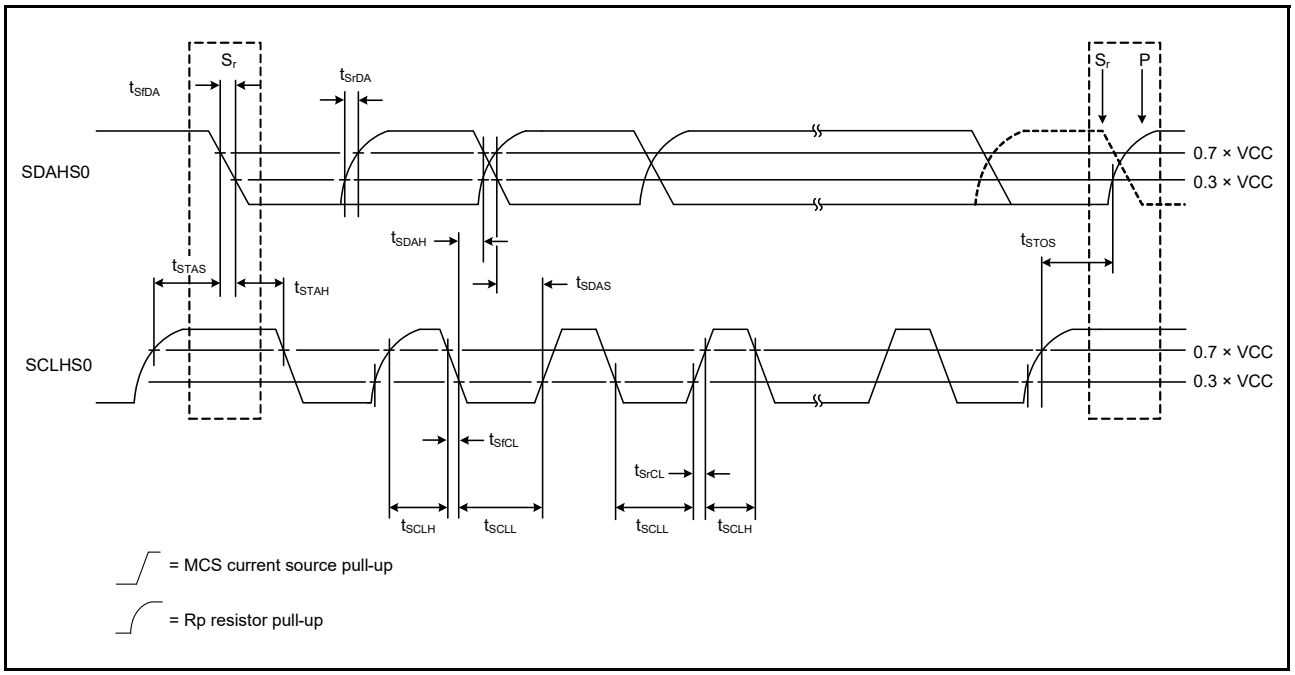


Figure 2.87 RIICHS Bus Interface Input/Output Timing (Hs-mode)

2.4.7.17 SDHI

Table 2.50 SDHI Timing

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item		Symbol	Min.	Max.	Unit	Test Conditions*1
SDHI	SDHI_CLK pin output cycle time	$t_{PP(SD)}$	20	—	ns	Figure 2.88
	SDHI_CLK pin output high pulse width	$t_{WH(SD)}$	0.4 × $t_{PP(SD)}$	—	ns	
	SDHI_CLK pin output low pulse width	$t_{WL(SD)}$	0.4 × $t_{PP(SD)}$	—	ns	
	SDHI_CLK pin output rise time	$t_{TLH(SD)}$	—	3	ns	
	SDHI_CLK pin output fall time	$t_{THL(SD)}$	—	3	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ODLY(SD)}$	–6.5	4	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ISU(SD)}$	6	—	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{IH(SD)}$	2	—	ns	

Note 1. When a letter “-A”, “-B”, etc. to indicate group membership is appended to the pin name, each pin is recommended to use in combination with the pins in the same group. All SDHI AC timings are measured in combination with the pins in the same group.

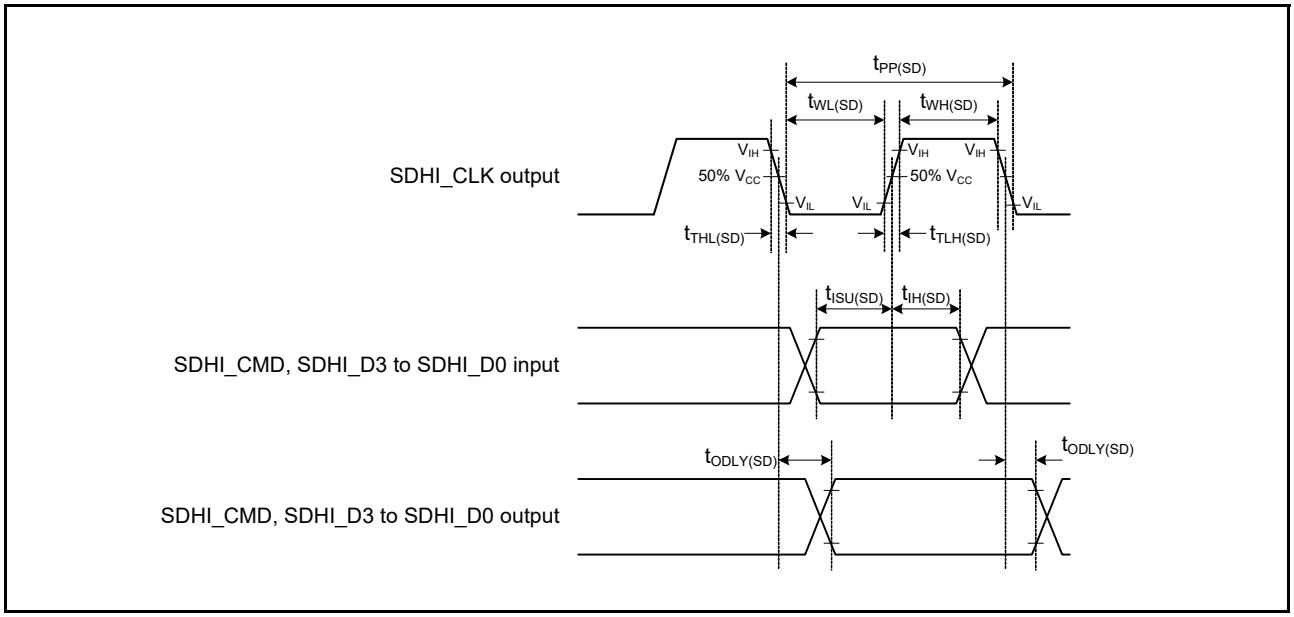


Figure 2.88 SD Host Interface Input/Output Signal Timing

2.5 USB Characteristics

Table 2.51 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
UCLK = 48 MHz,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V	
	Input low level voltage	V_{IL}	—	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| DP – DM |
	Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low level voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.89
	Rise time	t_{LR}	75	—	300	ns	
	Fall time	t_{LF}	75	—	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	—	125	%	t_{LR}/ t_{LF}
Pull-down characteristics	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	kΩ	

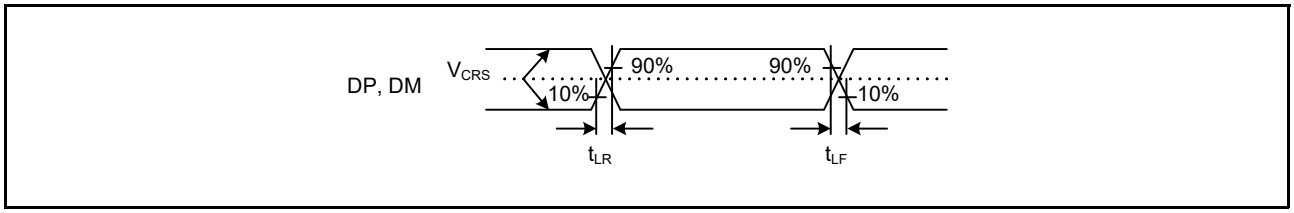


Figure 2.89 DP and DM Output Timing (Low Speed)

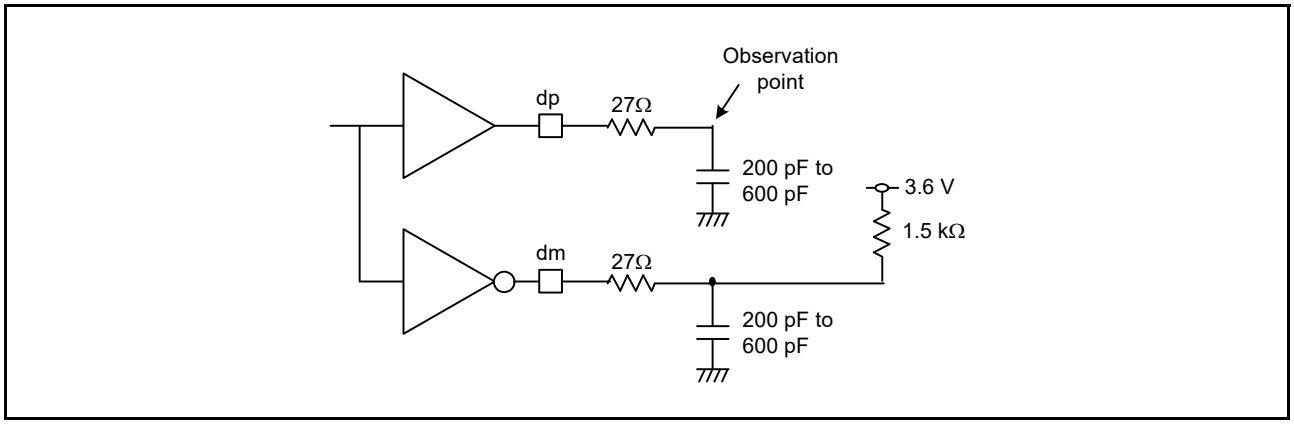


Figure 2.90 Test Circuit (Low Speed)

Table 2.52 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 3.0 to 3.6 V, 3.0 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
UCLK = 48 MHz,
PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, $T_a = T_{opr}$

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input characteristics	Input high level voltage	V_{IH}	2.0	—	—	V	
	Input low level voltage	V_{IL}	—	—	0.8	V	
	Differential input sensitivity	V_{DI}	0.2	—	—	V	| DP – DM |
	Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output characteristics	Output high level voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 µA
	Output low level voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	—	2.0	V	Figure 2.91
	Rise time	t_{FR}	4	—	20	ns	
	Fall time	t_{FF}	4	—	20	ns	
	Rise/fall time ratio	t_{FR} / t_{FF}	90	—	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	—	44	Ω	Rs = 27 Ω included
Pull-up and pull-down characteristics	DP pull-up resistance (when the function controller function is selected)	R_{pu}	0.900	—	1.575	kΩ	Idle state
			1.425	—	3.090		At transmission and reception
	DP/DM pull-down resistance (when the host controller function is selected)	R_{pd}	14.25	—	24.80	kΩ	

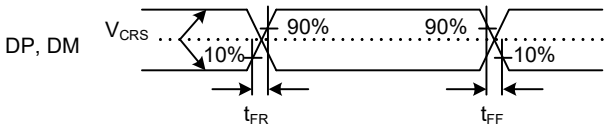


Figure 2.91 DP and DM Output Timing (Full-Speed)

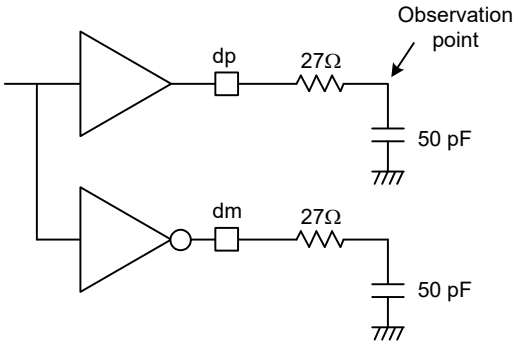


Figure 2.92 Test Circuit (Full-Speed)

2.6 A/D Conversion Characteristics

Table 2.53 12-Bit A/D (Unit 0) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKC = 1 MHz to 60 MHz, $T_a = T_{opr}$,
Source impedance = 1.0 kΩ

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	8	—	12	Bit	
Analog input capacitance	—	—	30	pF	
Conversion time*1 (Operation at PCLKC = 60 MHz)	0.48 (0.267)*2	—	—	µs	Sampling in 16 states
Offset error	—	±1.0	±2.5	LSB	
Full-scale error	—	±1.0	±2.5	LSB	
Quantization error	—	±0.5	—	LSB	
Absolute accuracy	—	±2.5	±4.5	LSB	
DNL differential nonlinearity error	—	±0.5	±1.5	LSB	
INL integral nonlinearity error	—	±1.0	±2.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

Table 2.54 12-Bit A/D (Unit 1) Conversion Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKD = 1 MHz to 60 MHz, $T_a = T_{opr}$,
Source impedance = 1.0 kΩ

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	8	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 60 MHz)	0.88 (0.633)*2	—	—	µs	Sampling in 38 states (ADSAM.SAM = 1)
Conversion time*1 (Operation at PCLKD = 30 MHz)	1 (0.500)*2	—	—	µs	Sampling in 15 states (ADSAM.SAM = 1)
Analog input capacitance	—	—	30	pF	
Offset error	—	±2.0	±3.5	LSB	
Full-scale error	—	±2.0	±3.5	LSB	
Quantization error	—	±0.5	—	LSB	
Absolute accuracy	—	±4.0	±6.0	LSB	
DNL differential nonlinearity error (Operation at PCLKD = 60 MHz)	—	±1.5	±4.0	LSB	
DNL differential nonlinearity error (Operation at PCLKD = 30 MHz)	—	±1.5	±2.5	LSB	
INL integral nonlinearity error (Operation at PCLKD = 60 MHz)	—	±2.0	±4.0	LSB	
INL integral nonlinearity error (Operation at PCLKD = 30 MHz)	—	±2.0	±3.5	LSB	

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.
Note 1. The conversion time includes the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.
Note 2. The value in parentheses indicates the sampling time.

Table 2.55 A/D Internal Reference Voltage Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
PCLKB = PCLKD = 60 MHz, $T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
A/D internal reference voltage	1.13	1.18	1.23	V	

2.7 Temperature Sensor Characteristics

Table 2.56 Temperature Sensor Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	±1	—	°C	
Temperature slope	—	4	—	mV/°C	
Output voltage	—	1.21	—	V	T_a = 25°C
Temperature sensor start time	—	—	30	µs	
Sampling time*1	4.15	—	—	µs	

Note 1. Set the S12AD1.ADSSTRT register such that the sampling time of the 12-bit A/D converter satisfies this specification.

2.8 CTSU Characteristics

Table 2.57 CTSU Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	
TS pin capacitive load	C_{base}	—	—	50	pF	
Total sum of the high-level output current*1	ΣI_{OH}	—	—	–40*2	mA	The mutual capacitance method is in use.

Note 1. Total sum of I_{OH} of the pins other than TSCAP, and TS0 to TS16
Note 2. In the mutual capacitance method, when the amount of current output from the I/O pins other than those of the CTSU is relatively large, the VCC voltage largely drops, affecting measurement by the CTSU. Accordingly, the total sum of I_{OH} of the other pins should be no more than the listed value when the CTSU is in use.

2.9 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 2.58 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	Low power consumption function disabled*1	V_{POR}	2.5	2.6	2.7	V	Figure 2.93
		Low power consumption function enabled*2		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.94
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.95
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.96
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	—	4.6	—	ms	Figure 2.93
	LVD0 reset time		t_{LVD0}	—	0.70	—		Figure 2.94
	LVD1 reset time		t_{LVD1}	—	0.57	—		Figure 2.95
	LVD2 reset time		t_{LVD2}	—	0.57	—		Figure 2.96
Minimum VCC down time			t_{VOFF}	200	—	—	µs	Figure 2.93, Figure 2.94
Response delay time			t_{det}	—	—	200	µs	Figure 2.93 to Figure 2.96
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	—	—	10	µs	Figure 2.95, Figure 2.96
Hysteresis width (LVD1 and LVD2)			V_{LVH}	—	70	—	mV	

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for the POR/ LVD.
Note 1. The low power consumption function is disabled and DEEPCUT[1:0] = 00b or 01b.
Note 2. The low power consumption function is enabled and DEEPCUT[1:0] = 11b.

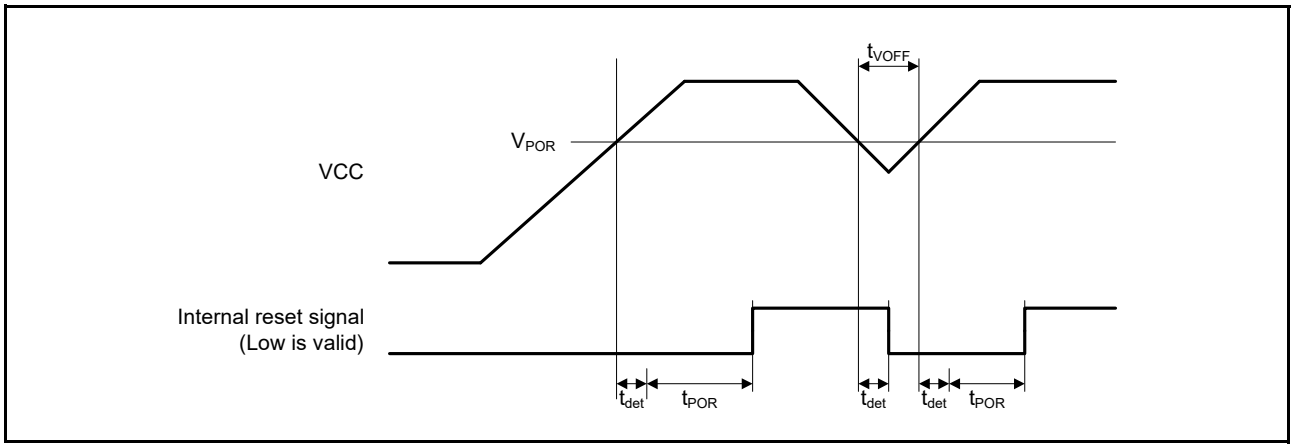


Figure 2.93 Power-on Reset Timing

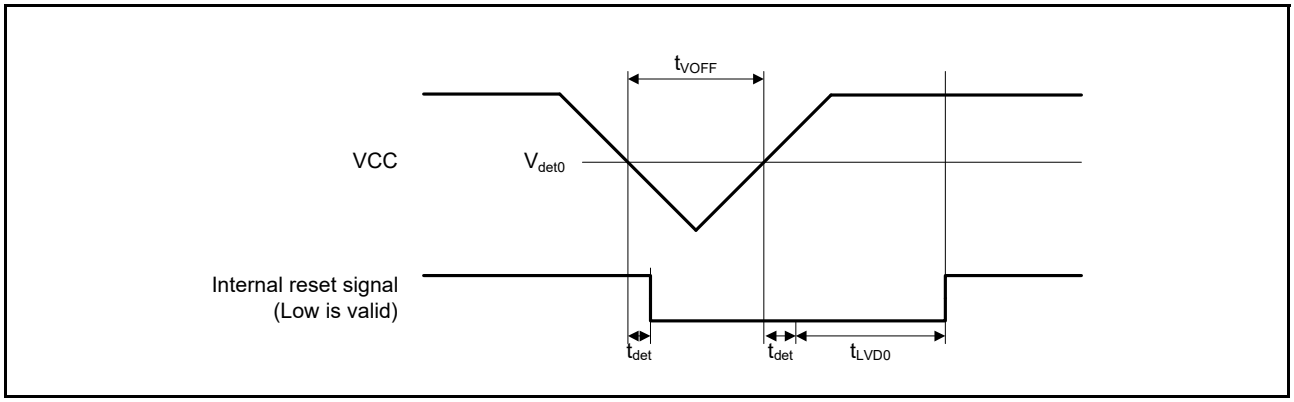


Figure 2.94 Voltage Detection Circuit Timing (V_{det0})

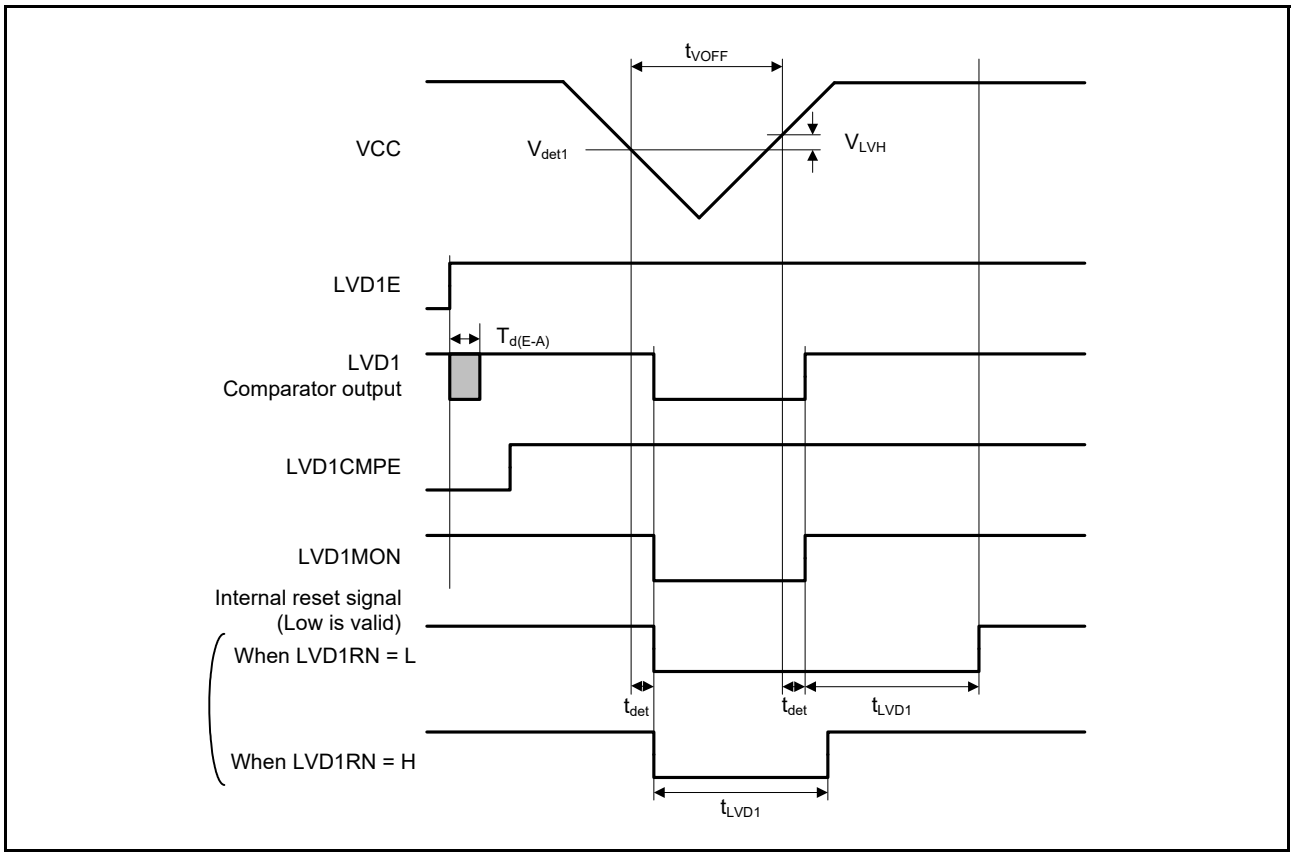


Figure 2.95 Voltage Detection Circuit Timing (V_{det1})

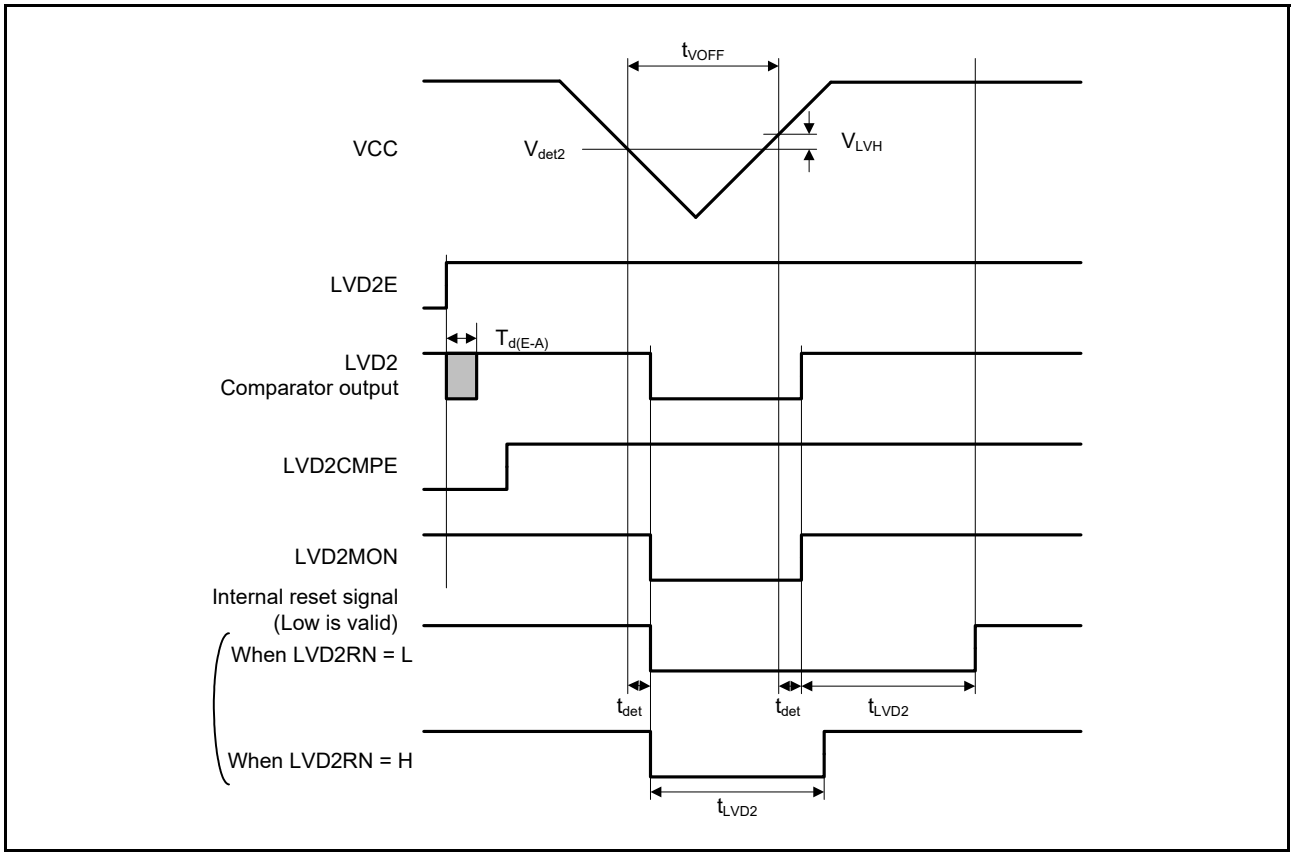


Figure 2.96 Voltage Detection Circuit Timing (V_{det2})

2.10 Oscillation Stop Detection Timing

Table 2.59 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 2.97

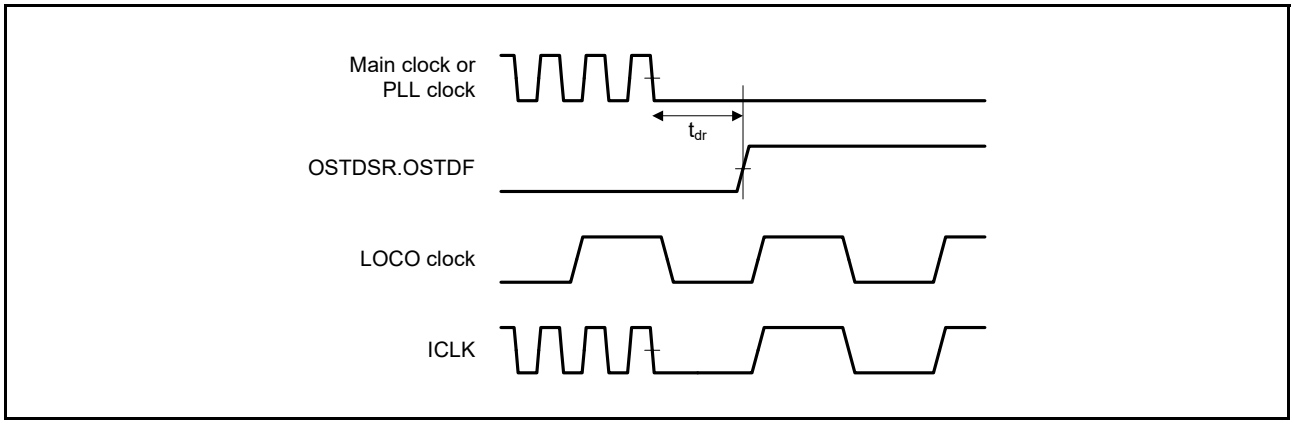


Figure 2.97 Oscillation Stop Detection Timing

2.11 Battery Backup Function Characteristics

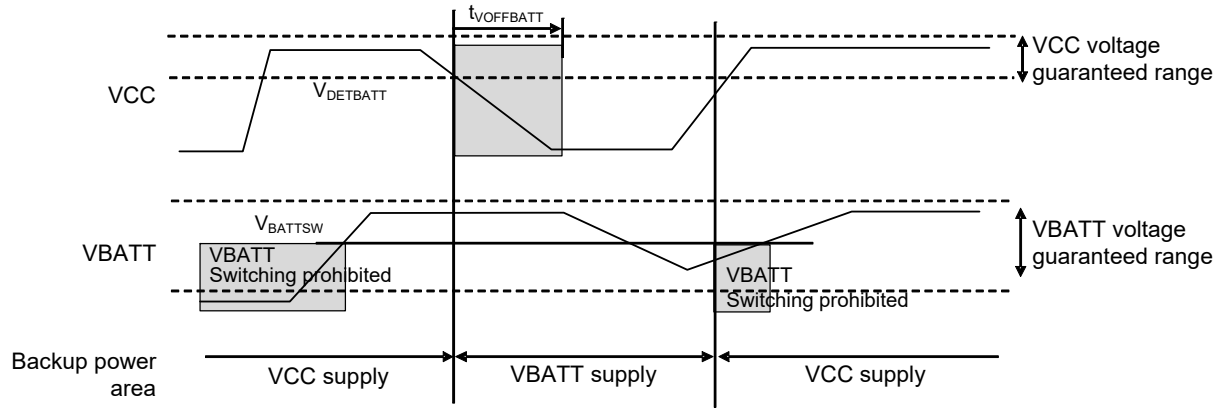
Table 2.60 Battery Backup Function Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
V_{BATT} = 1.62 to 3.6 V, $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 2.98
Lower-limit V_{BATT} voltage for power supply switching due to VCC voltage drop	V_{BATTSW}	2.00	—	—	V	
VCC-off period for starting power supply switching*1	$t_{VOFFBATT}$	200	—	—	µs	
Backup domain power-down detection level	$V_{PDR(BKP)}$	1.45	1.5	1.55	V	Figure 2.99
Time delay in assertion of the reset signal for the backup domain*2	$t_{p(PDRL)}$	—	—	2000	µs	
Time delay in negation of the reset signal for the backup domain	$t_{p(PDRH)}$	—	—	1000	µs	
Temper input pulse width	$t_{w(TAMPI)}$	200	—	—	ns	Figure 2.100

Note 1. The VCC-off period for switching power supply indicates the period from VCC falling below the minimum value of the battery backup switching threshold voltage ($V_{DETBATT}$) until the source of supply is switched to VBATT. When the VCC recovers within this period, the source may not be switched to VBATT and supply from VCC is continued.

Note 2. When the V_{BKP} recovers within this period, the backup domain reset signal may not be generated.



Note. The VBATT voltage when the supplied power source switches from VCC to VBATT should not be lower than V_{BATTSW}, the lower-limit VBATT voltage for switching between power supplies due to a drop in the VCC voltage.

Figure 2.98 Battery Backup Function Characteristics

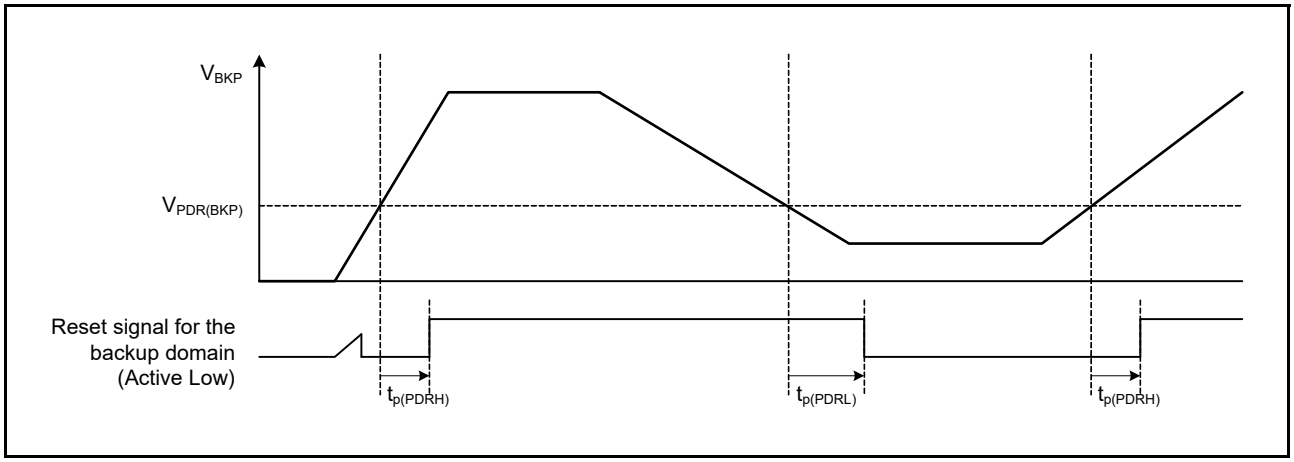


Figure 2.99 Backup Domain Reset Characteristics

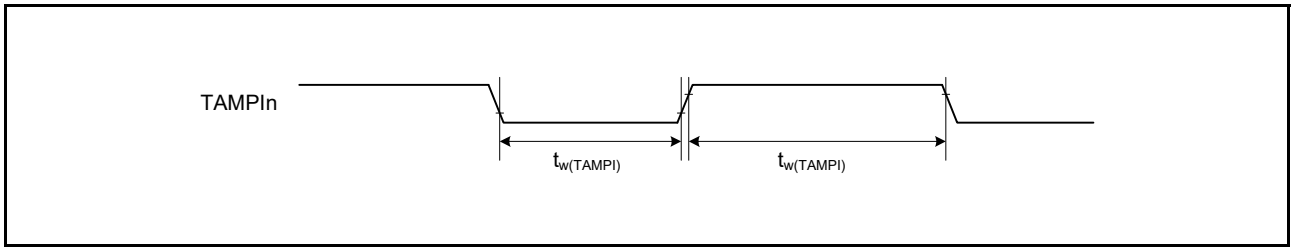


Figure 2.100 TAMPIn Input Timing

2.12 Flash Memory Characteristics

Table 2.61 Code Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			FCLK = 15 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time N_{PEC} ≤ 100 times	128 bytes	t_{P128}	—	0.75	13.2	—	0.38	6.6	—	0.34	6	ms	
	8 Kbytes	t_{P8K}	—	49	176	—	25	88	—	22	80	ms	
	32 Kbytes	t_{P32K}	—	194	704	—	97	352	—	88	320	ms	
Programming time N_{PEC} > 100 times	128 bytes	t_{P128}	—	0.91	15.8	—	0.46	8	—	0.41	7.2	ms	
	8 Kbytes	t_{P8K}	—	60	212	—	30	106	—	27	96	ms	
	32 Kbytes	t_{P32K}	—	234	848	—	117	424	—	106	384	ms	
Erasure time N_{PEC} ≤ 100 times	8 Kbytes	t_{E8K}	—	78	216	—	48	132	—	43	120	ms	
	32 Kbytes	t_{E32K}	—	283	864	—	173	528	—	157	480	ms	
Erasure time N_{PEC} > 100 times	8 Kbytes	t_{E8K}	—	94	260	—	58	158	—	52	144	ms	
	32 Kbytes	t_{E32K}	—	341	1040	—	208	632	—	189	576	ms	
Reprogramming/erasure cycle*1		N_{PEC}	10000 *2	—	—	10000 *2	—	—	10000 *2	—	—	Times	
Suspend delay time during programming		t_{SPD}	—	—	264	—	—	132	—	—	120	µs	
First suspend delay time during erasing (in suspend priority mode)		t_{SESD1}	—	—	216	—	—	132	—	—	120	µs	
Second suspend delay time during erasure (in suspend priority mode)		t_{SESD2}	—	—	1.7	—	—	1.7	—	—	1.7	ms	
Suspend delay time during erasure (in erasure priority mode)		t_{SEED}	—	—	1.7	—	—	1.7	—	—	1.7	ms	
Forced stop command		t_{FD}	—	—	32	—	—	22	—	—	20	µs	
Data hold time*3, *4		t_{DRP}	20	—	—	20	—	—	20	—	—	Year	T_a ≤ 85°C
			10	—	—	10	—	—	10	—	—		T_a ≤ 105°C

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 128-byte program is performed 64 times for different addresses in 8-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

Table 2.62 Data Flash Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item		Symbol	FCLK = 4 MHz			FCLK = 15 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test Conditions
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Programming time	4 bytes	t_{DP4}	—	0.36	3.8	—	0.18	1.9	—	0.16	1.7	ms	
Erasure time	64 bytes	t_{DP64}	—	3.1	18	—	1.9	11	—	1.7	10	ms	
	128 bytes	t_{DP128}	—	4.7	27	—	2.9	16	—	2.6	15	ms	
	256 bytes	t_{DP256}	—	8.9	50	—	5.4	31	—	4.9	28	ms	
Blank check time	4 bytes	t_{DBC4}	—	—	84	—	—	33	—	—	30	µs	
	64 bytes	t_{DBC64}	—	—	280	—	—	110	—	—	100	µs	
	2 Kbytes	t_{DBC2K}	—	—	6160	—	—	2420	—	—	2200	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	100000 *2	—	—	100000 *2	—	—	100000 *2	—	—	Times	
Suspend delay time during programming		t_{DSPD}	—	—	264	—	—	132	—	—	120	µs	
First suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	216	—	—	132	—	—	120	µs	
	128 bytes	—	—	—	216	—	—	132	—	—	120	µs	
	256 bytes	—	—	—	216	—	—	132	—	—	120	µs	
Second suspend delay time during erasure (in suspend priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs	
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs	
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs	
Suspend delay time during erasing (in erasure priority mode)	64 bytes	—	—	—	300	—	—	300	—	—	300	µs	
	128 bytes	—	—	—	390	—	—	390	—	—	390	µs	
	256 bytes	—	—	—	570	—	—	570	—	—	570	µs	
Forced stop command		t_{FD}	—	—	32	—	—	22	—	—	20	µs	
Data hold time*3, *4		t_{DDRP}	20	—	—	20	—	—	20	—	—	Year	$T_a \leq 85°C$
			10	—	—	10	—	—	10	—	—		$T_a \leq 105°C$

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 4-byte program is performed 512 times for different addresses in 2-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.

Note 4. These values are based on the results of reliability testing.

Table 2.63 Option Setting Memory Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
Temperature range for programming/erasure: $T_a = T_{opr}$

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Program/erase cycles*1	N_{PEC}	1000*2	—	—	Cycles	
Data retention*3, *4	t_{DRP}	20	—	—	Year	$T_a \leq 85°C$
		10	—	—		$T_a \leq 105°C$

Note 1. Definition of program/erase cycle:
The program/erase cycle is the number of program for the same address.
Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.
Note 3. This shows the characteristic when the flash memory writer or self-programming library from Renesas Electronics is in use, and the number of times programming and erasure proceed does not exceed the specified value.
Note 4. These values are based on the results of reliability testing.

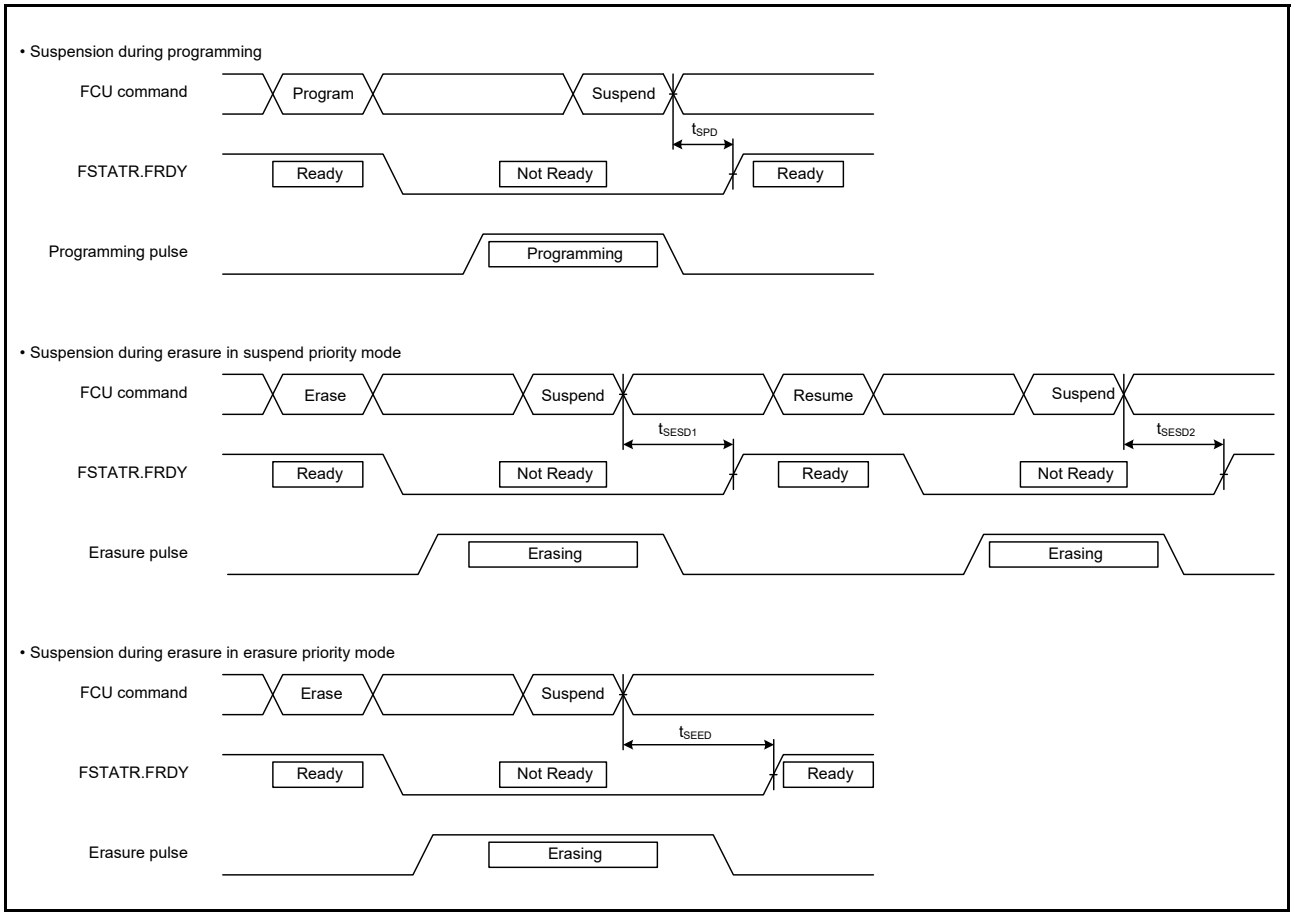


Figure 2.101 Flash Memory Programming/Erasure Suspension Timing

2.13 Boundary Scan

Table 2.64 Boundary Scan Characteristics

Conditions: VCC = AVCC0 = AVCC1 = VCC_USB = V_{BATT} = 2.7 to 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = AVSS1 = VREFL0 = VSS_USB = 0 V,
$T_a = T_{opr}$,
Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
High-drive output is selected by the drive capacity control register.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
TCK clock cycle time	t_{TCKcyc}	100	—	—	ns	Figure 2.102
TCK clock high pulse width	t_{TCKH}	45	—	—	ns	
TCK clock low pulse width	t_{TCKL}	45	—	—	ns	
TCK clock rise time	t_{TCKr}	—	—	5	ns	
TCK clock fall time	t_{TCKf}	—	—	5	ns	
TRST# pulse width	t_{TRSTW}	20	—	—	t_{TCKcyc}	Figure 2.103
TMS setup time	t_{TMSS}	20	—	—	ns	Figure 2.104
TMS hold time	t_{TMSH}	20	—	—	ns	
TDI setup time	t_{TDIS}	20	—	—	ns	
TDI hold time	t_{TDIH}	20	—	—	ns	
TDO data delay time	t_{TDOD}	—	—	40	ns	

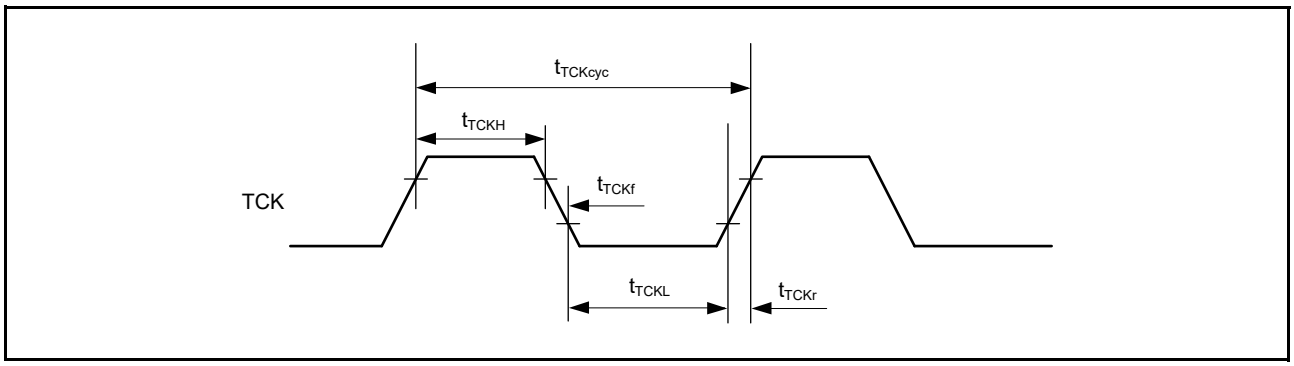


Figure 2.102 Boundary Scan TCK Timing

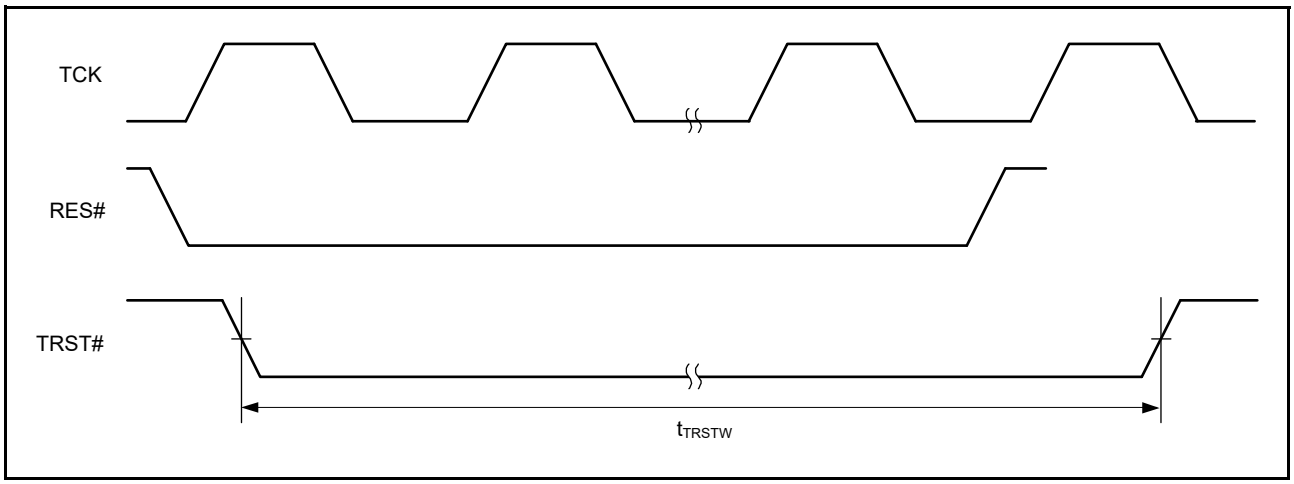


Figure 2.103 Boundary Scan TRST# Timing

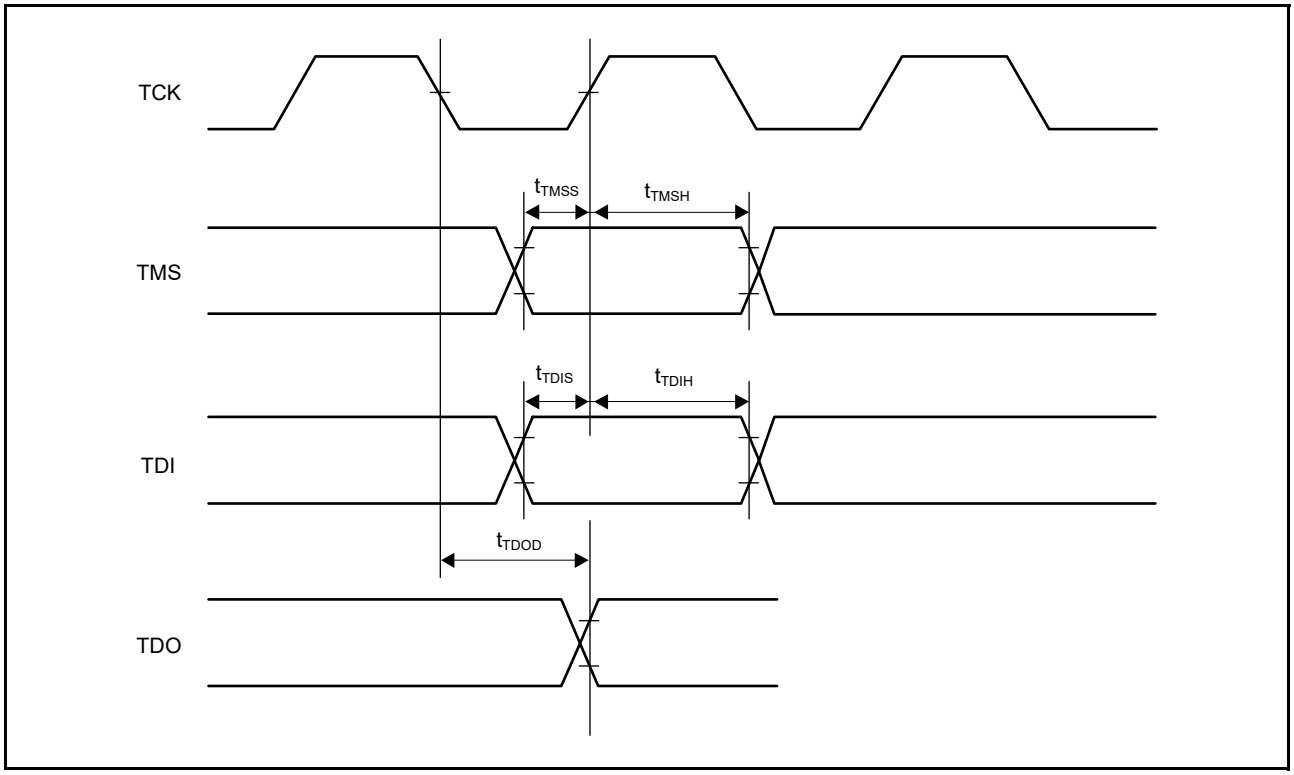
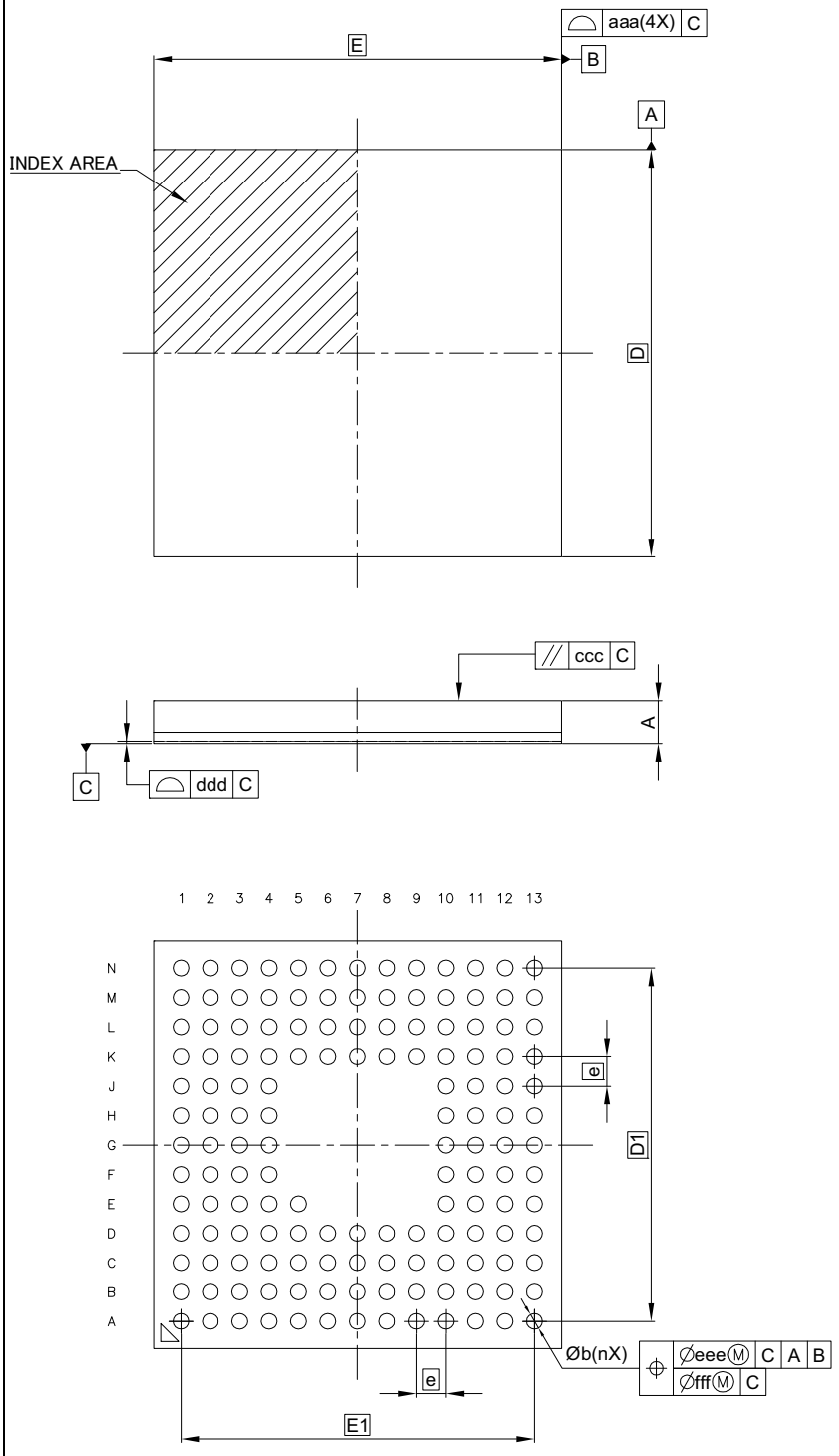


Figure 2.104 Boundary Scan Input/Output Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

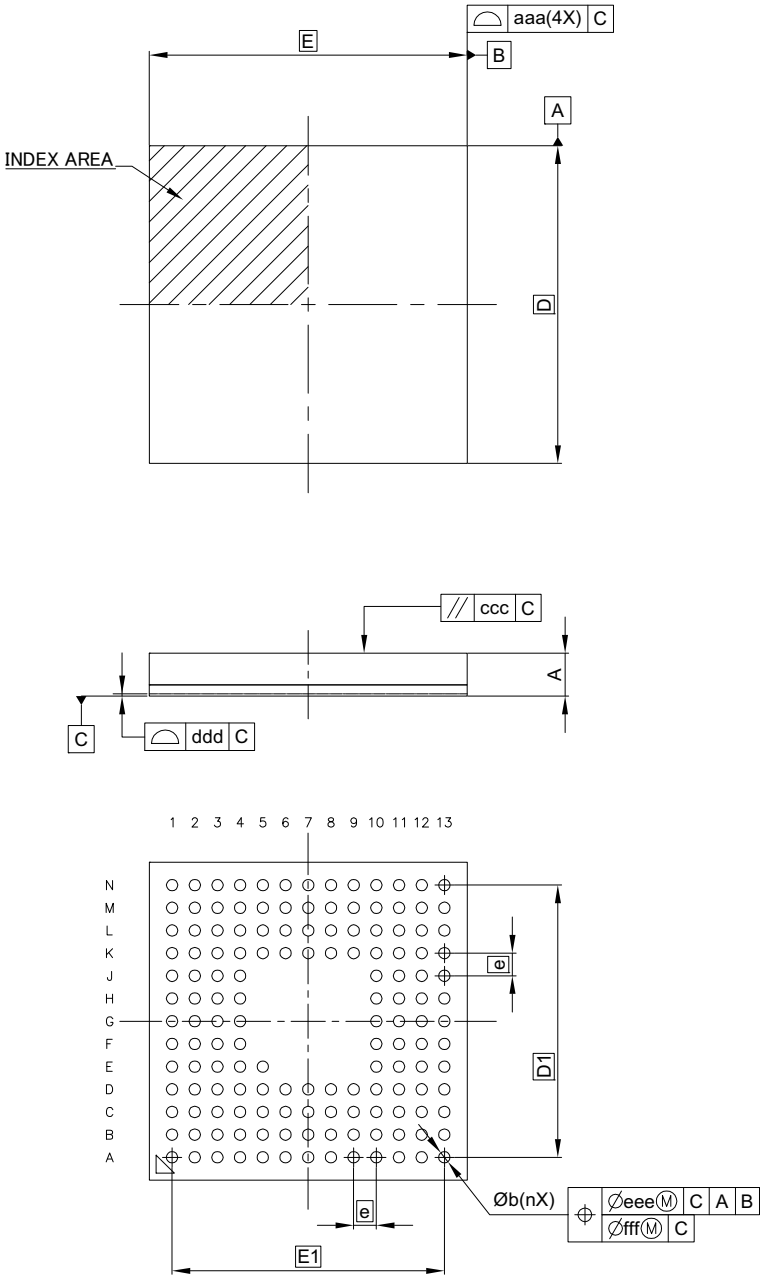
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-TFLGA145-9×9-0.65	PTLG0145JC-A	0.16



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	9.00	—
E	—	9.00	—
D1	—	7.80	—
E1	—	7.80	—
A	—	—	1.01
b	—	0.35	—
e	—	0.65	—
aaa	—	—	0.10
ccc	—	—	0.10
ddd	—	—	0.10
eee	—	—	0.08
fff	—	—	0.08
n	—	145	—

Figure A 145-Pin TFLGA (PTLG0145JC-A)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-TFLGA145-7×7-0.5	PTLG0145KB-A	0.09

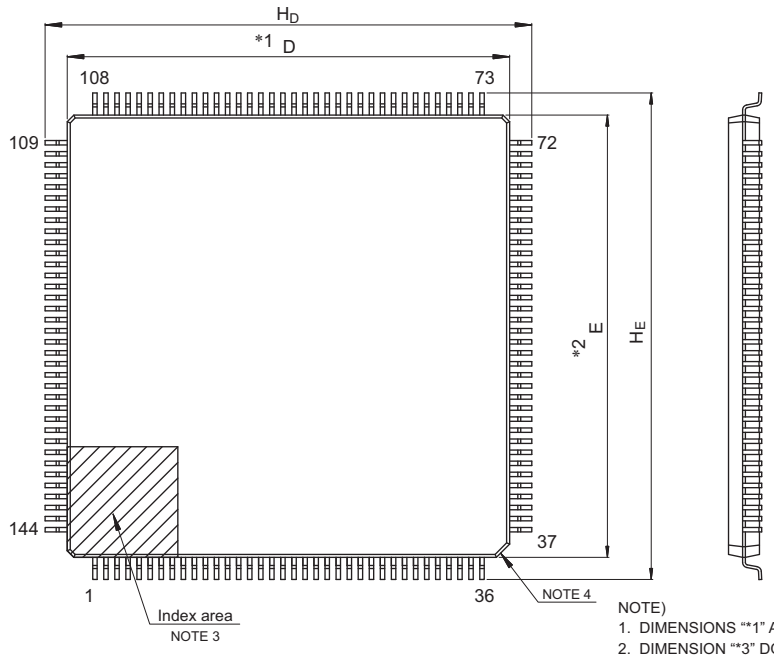


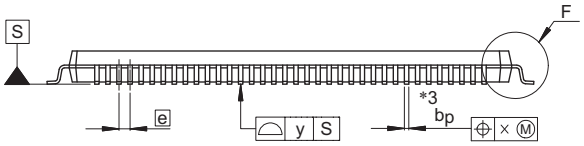
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	7.00	—
E	—	7.00	—
D1	—	6.00	—
E1	—	6.00	—
A	—	—	1.01
b	—	0.25	—
e	—	0.50	—
aaa	—	—	0.10
ccc	—	—	0.10
ddd	—	—	0.08
eee	—	—	0.08
fff	—	—	0.05
n	—	145	—

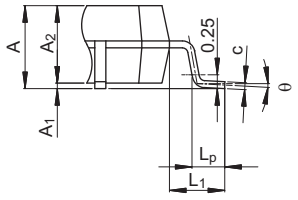
Figure B 145-Pin TFLGA (PTLG0145KB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP144-20x20-0.50	PLQP0144KA-B	—	1.2

Unit: mm







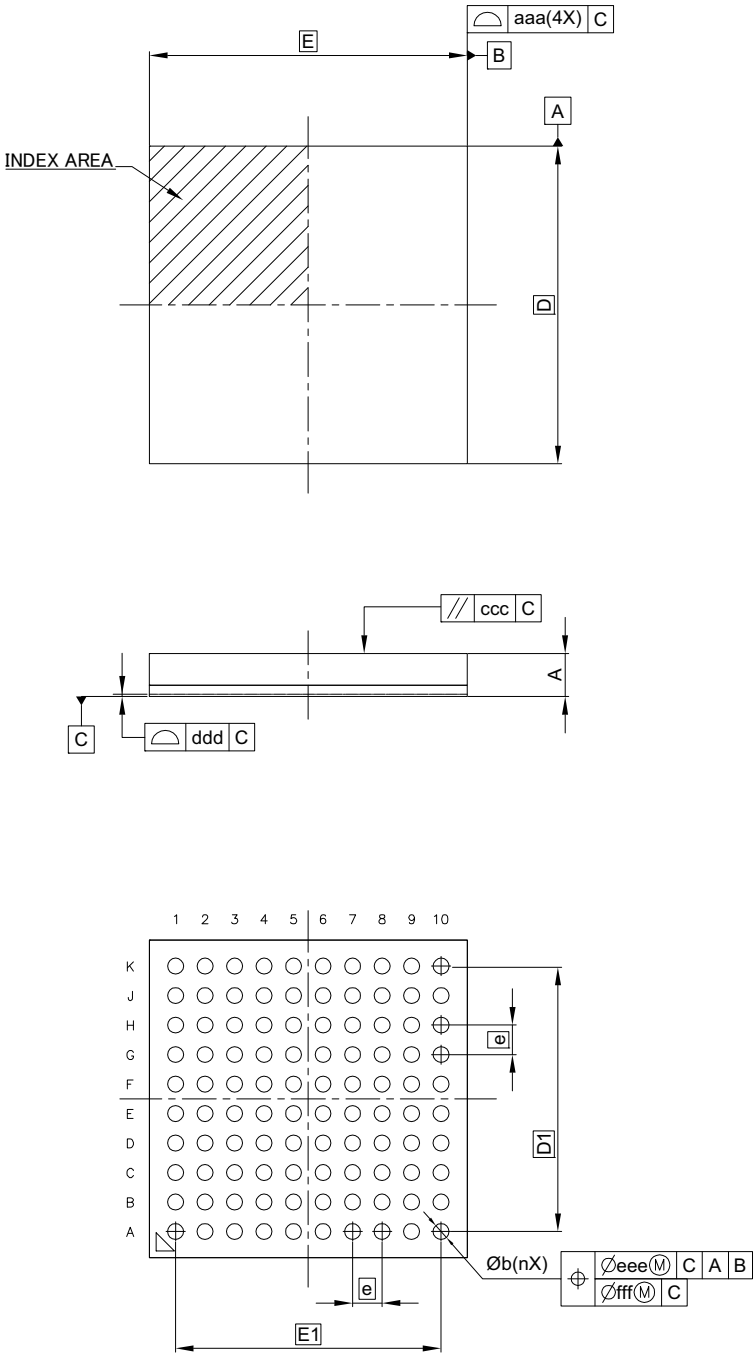
Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure C 144-Pin LFQFP (PLQP0144KA-B)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-TFLGA100-7×7-0.65	PTLG0100JB-A	0.09

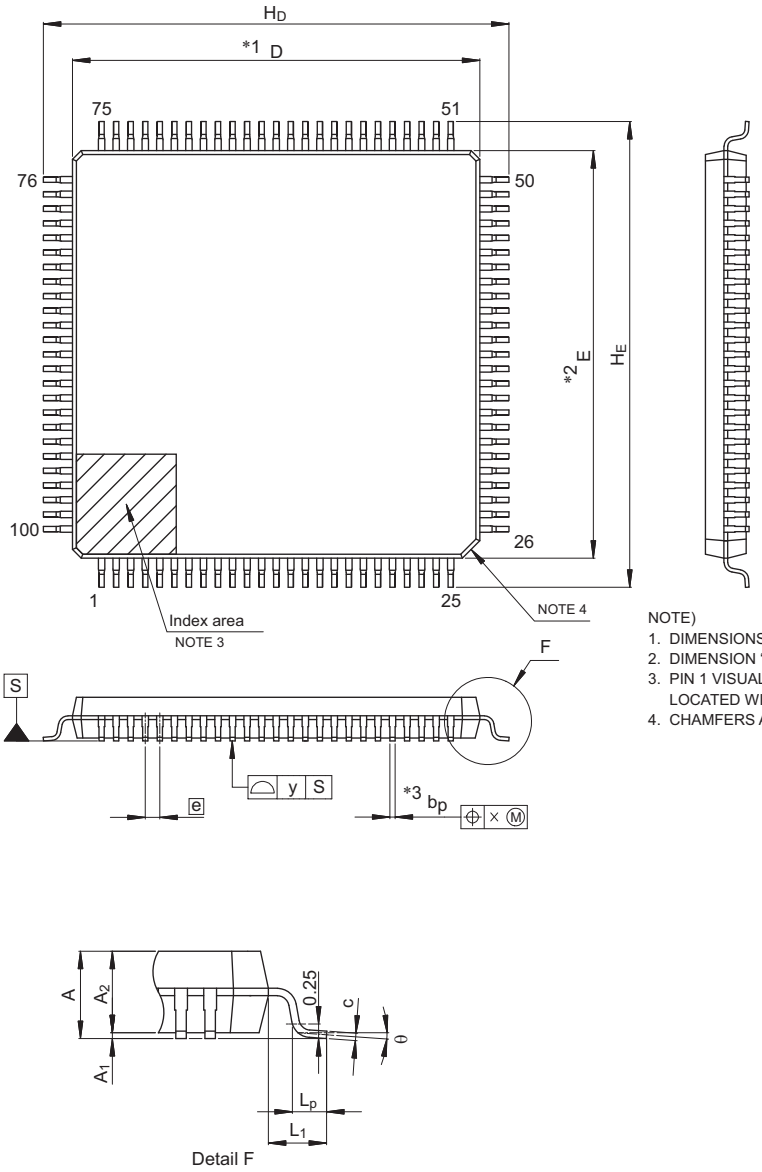


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	7.00	—
E	—	7.00	—
D1	—	5.85	—
E1	—	5.85	—
A	—	—	1.01
b	—	0.35	—
e	—	0.65	—
aaa	—	—	0.10
ccc	—	—	0.10
ddd	—	—	0.08
eee	—	—	0.08
fff	—	—	0.08
n	—	100	—

Figure D 100-Pin TFLGA (PTLG0100JB-A)

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm

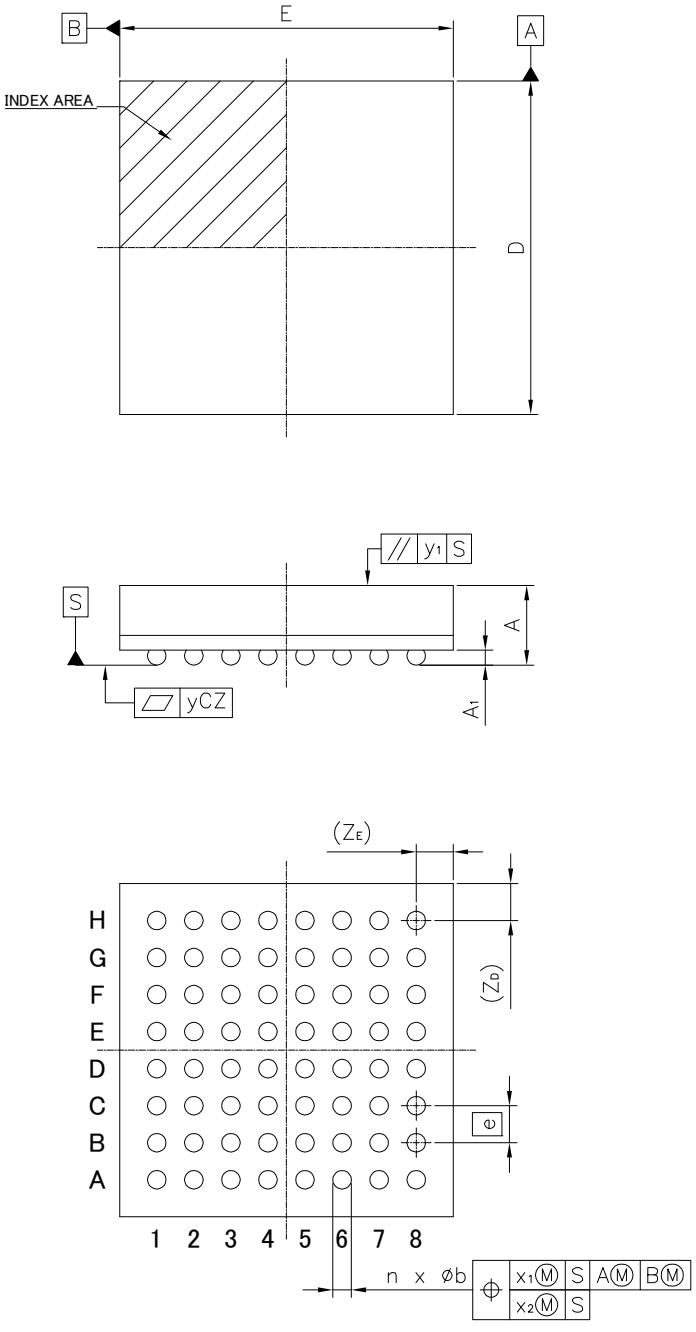


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure E 100-Pin LFQFP (PLQP0100KB-B)

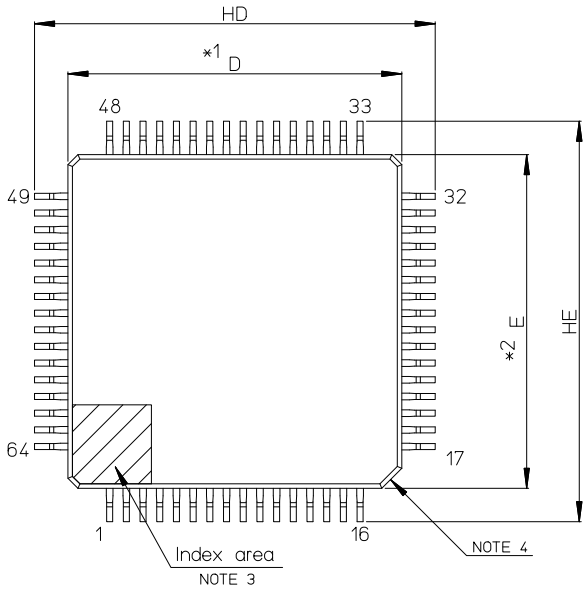
JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-TFBGA64-4.5×4.5-0.50	PTBG0064KB-A	0.04

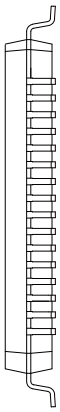


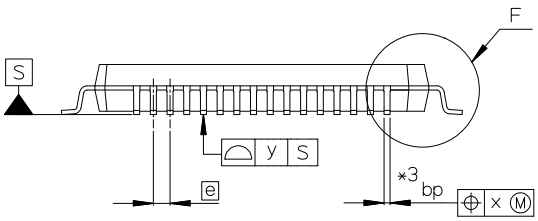
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	4.42	4.50	4.58
E	4.42	4.50	4.58
A	—	—	1.20
A_1	0.15	0.20	0.25
e	—	0.50	—
b	0.20	0.25	0.30
x_1	—	—	0.15
x_2	—	—	0.05
y	—	—	0.08
y_1	—	—	0.20
n	—	64	—
Z_D	—	0.50	—
Z_E	—	0.50	—

Figure F 64-Pin TFBGA (PTBG0064KB-A)

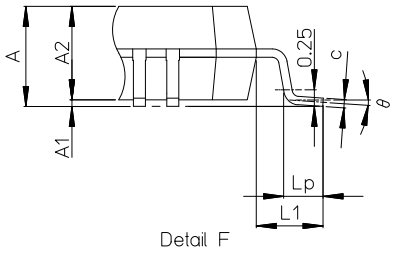
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	——	0.3g







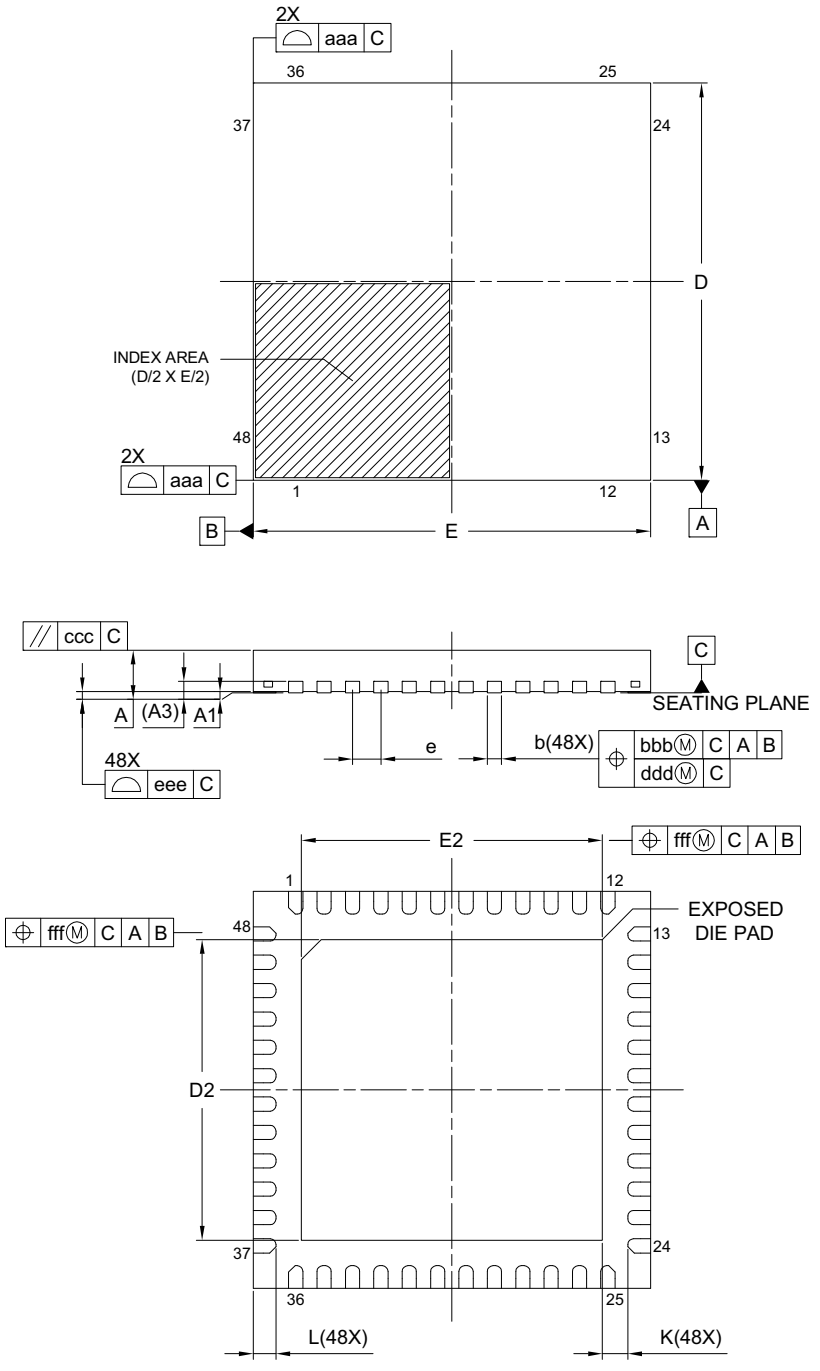
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL; SIZE MAY VARY.



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A2	——	1.4	——
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	——	——	1.7
A1	0.05	——	0.15
bp	0.15	0.20	0.27
c	0.09	——	0.20
θ	0°	3.5°	8°
e	——	0.5	——
x	——	——	0.08
y	——	——	0.08
Lp	0.45	0.6	0.75
L1	——	1.0	——

Figure G 64-Pin LFQFP (PLQP0064KB-C)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Figure H 48-Pin HWQFN (PWQN0048KC-A)

REVISION HISTORY	RX671 Group Datasheet

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Mar 31, 2021	—	First edition, issued	
1.10	Apr 15, 2022	Features		
		1	Coremark value, changed	
		1	Useful functions for IEC60730 compliance, changed	
		1. Overview		
		8	Table 1.1 Outline of Specifications (7/10), changed	
		11	Table 1.1 Outline of Specifications (10/10), changed	
		14 to 16	Table 1.3 List of Products, changed	
		17	Figure 1.1 How to Read the Product Part Number, changed	
		18	Figure 1.2 Block Diagram, changed	
		23	Table 1.4 Pin Functions (5/8), changed	
		24	Table 1.4 Pin Functions (6/8), changed	
		26	Table 1.4 Pin Functions, Note changed	
		2. Electrical Characteristics		
		87	Table 2.9 Normal Output Characteristics, added	
		88	Table 2.10 Thermal Resistance Value (Reference), changed	
		Appendix 1. Package Dimensions		
		168	Figure A 145-Pin TFLGA (PTLG0145JC-A), added	
		169	Figure B 145-Pin TFLGA (PTLG0145KB-A), added	
		171	Figure D 100-Pin TFLGA (PTLG0100JB-A), added	
		173	Figure F 64-Pin TFBGA (PTBG0064KB-A), added	
		175	Figure H 48-Pin HWQFN (PWQN0048KC-A), added	
1.20	Sep 30, 2024	1. Overview		
		9	Table 1.1 Outline of Specifications Note2, deleted	
		16	Table 1.3 List of Products Note, added	
		17	Figure 1.1 How to Read the Product Part Number, changed	
		2. Electrical Characteristics		
		81	Table 2.3 Recommended Operating Conditions (2) Note1, changed	TN-RX*-A0273A/E
		84	Table 2.6 DC Characteristics (3), changed	
		130	Figure 2.57 Simple IIC Bus Interface Input/Output Timing, changed	
		147	Table 2.46 RIIC Timing (1), changed	
		148	Table 2.47 RIIC Timing (2), changed	
		148	Figure 2.85 RIIC Bus Interface Input/Output Timing, changed	
		149	Table 2.48 RIICHS Timing (1), changed	
		150	Figure 2.86 RIICHS Bus Interface Input/Output Timing, changed	
		150, 151	Table 2.49 RIICHS Timing (2), changed	TN-RX*-A0266A/E
		165	Table 2.63 Option Setting Memory Characteristics, added	TN-RX*-A0276B/E

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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